

[54] **SOLID STATE INSTRUMENT SYSTEM FOR DIGITAL COUNTING AND CONTINUOUSLY INDICATING COUNT RESULTS**

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235/92 R, 235/92 FQ, 235/92 TF**

[51] Int. Cl. **G01p 3/12**

[58] Field of Search..... **235/92 EA, 92 TF,
235/92 FQ, 92 PL; 73/499, 507; 324/166;
340/336, 324 R**

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[57] **ABSTRACT**

A digital solid state engine RPM sensing and indicating system for multi-engine aircraft, the RPM indications made simultaneously in the form of side-by-side bar graphs and side-by-side numeric displays for each engine showing RPM as a percentage of rated RPM, the displays being formed by light-emitting diodes and the system arranged such that the bar graphs indicate changes at each 5 percent of noted RPM below 70 percent and at 1 percent above 70 percent. Special current limiting and cooling features are provided to handle the current requirements of the diodes and power supply.

9 Claims, 10 Drawing Figures

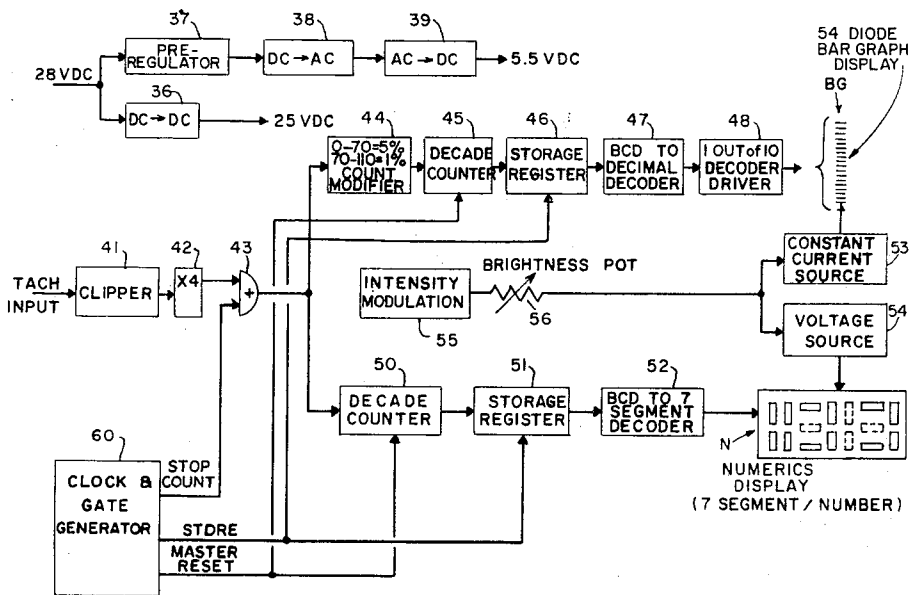


Fig. 2.

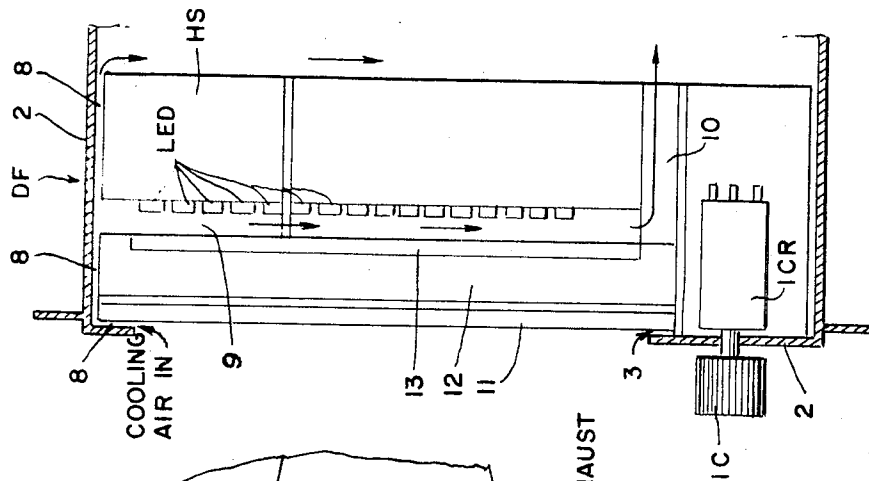
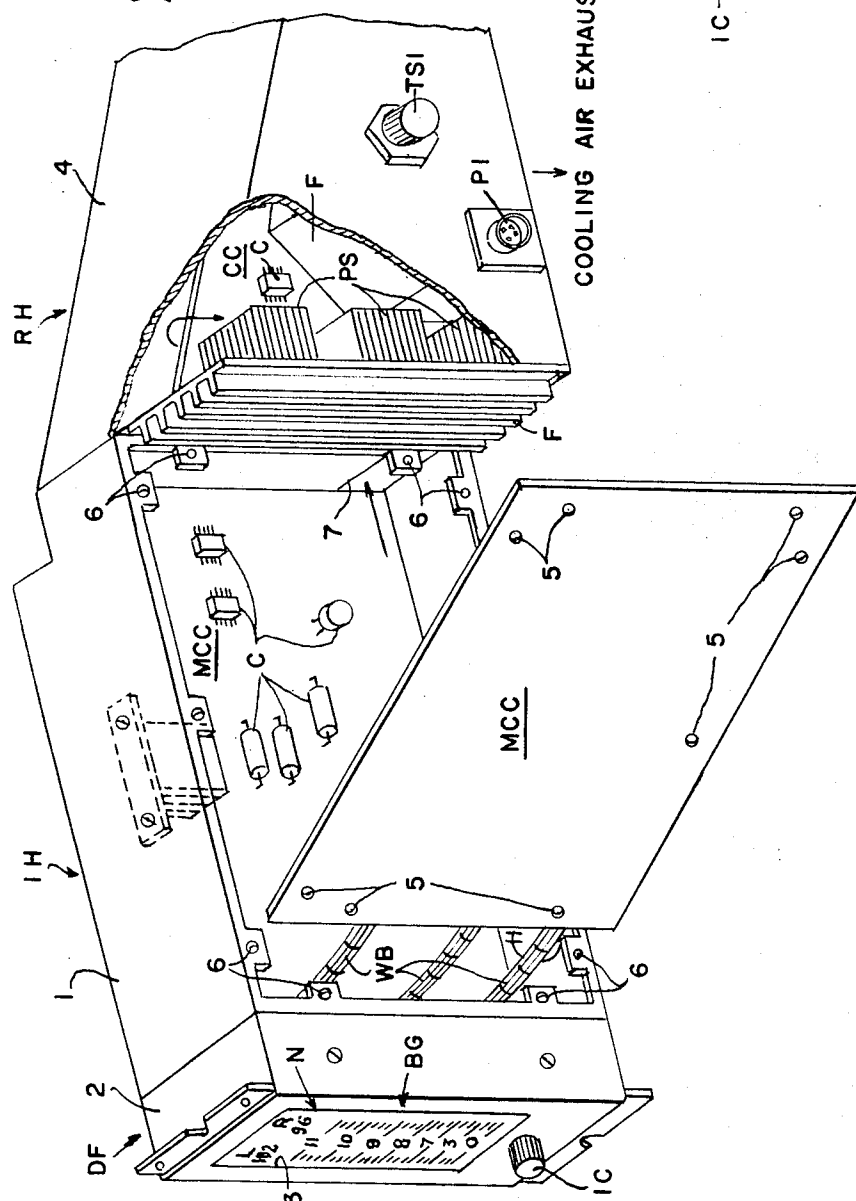


Fig. 1.



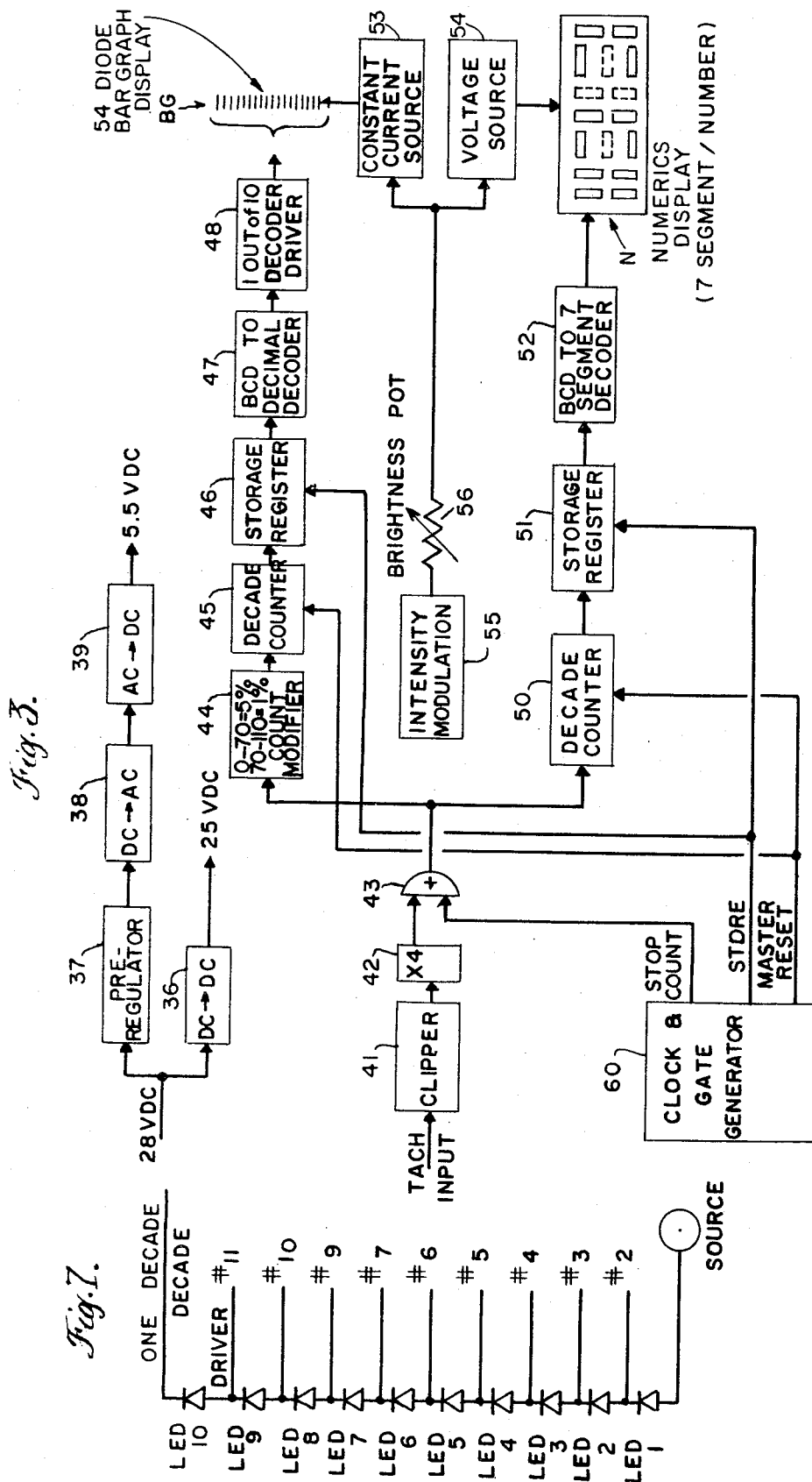


Fig. 4A.

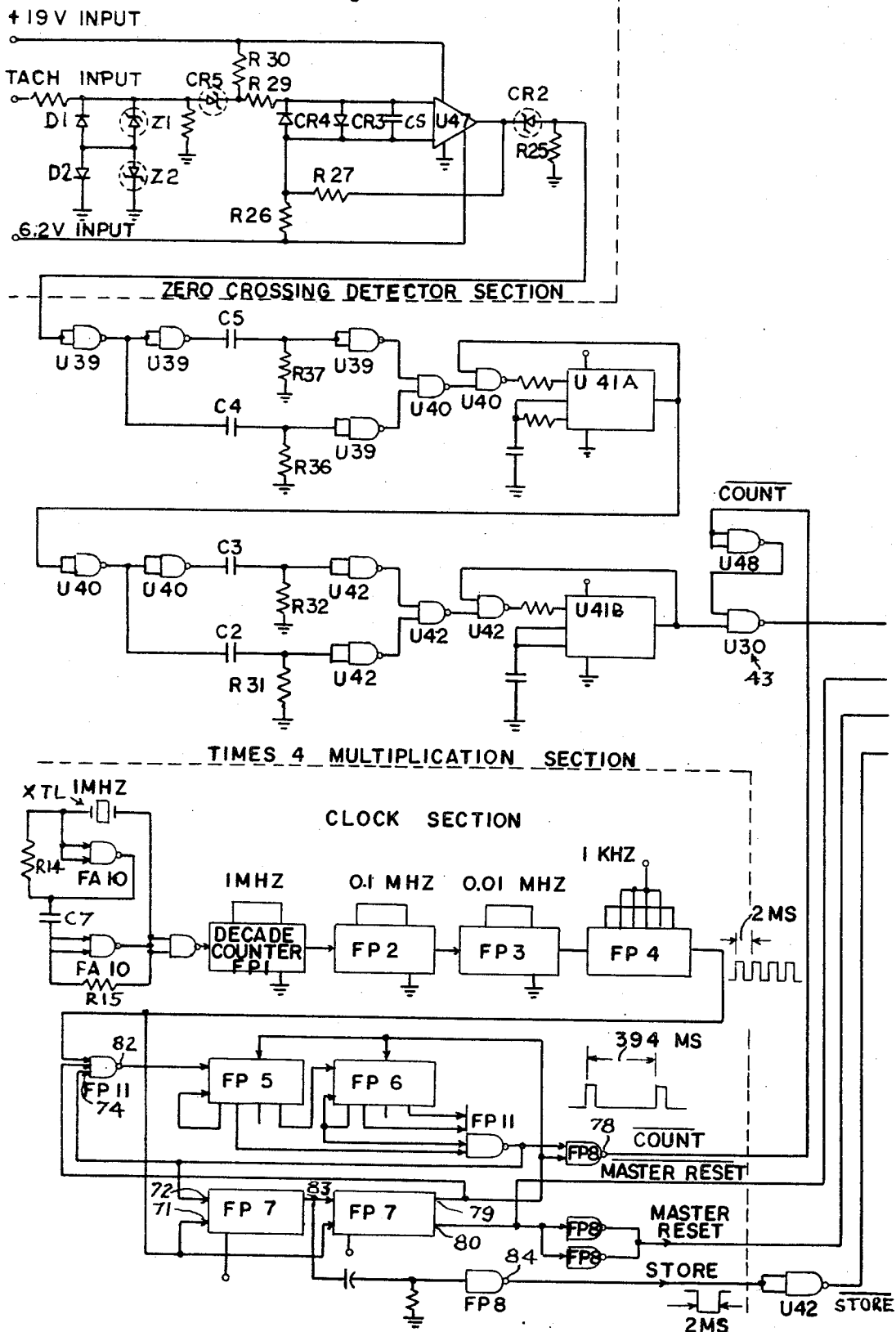
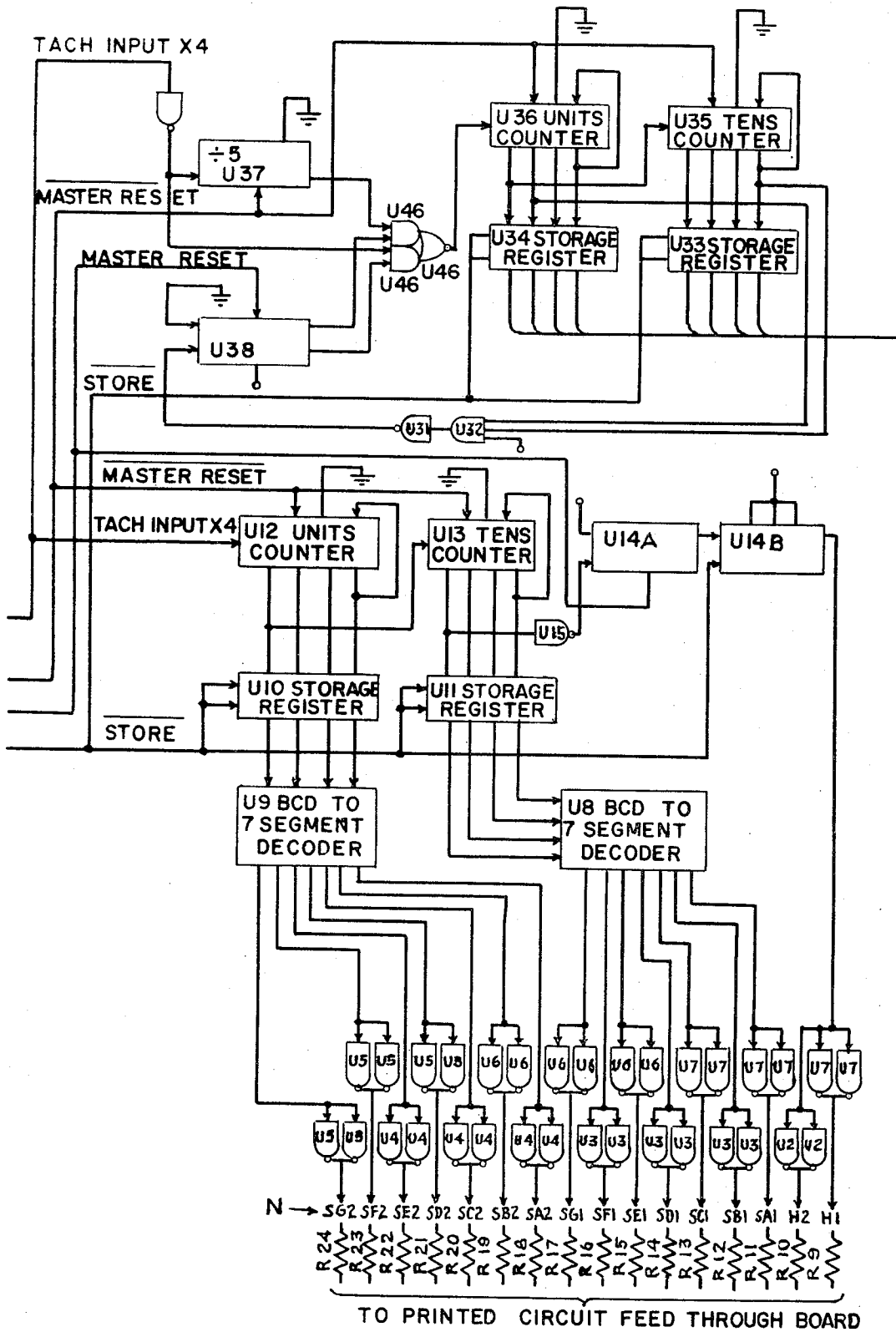


Fig. 4B.



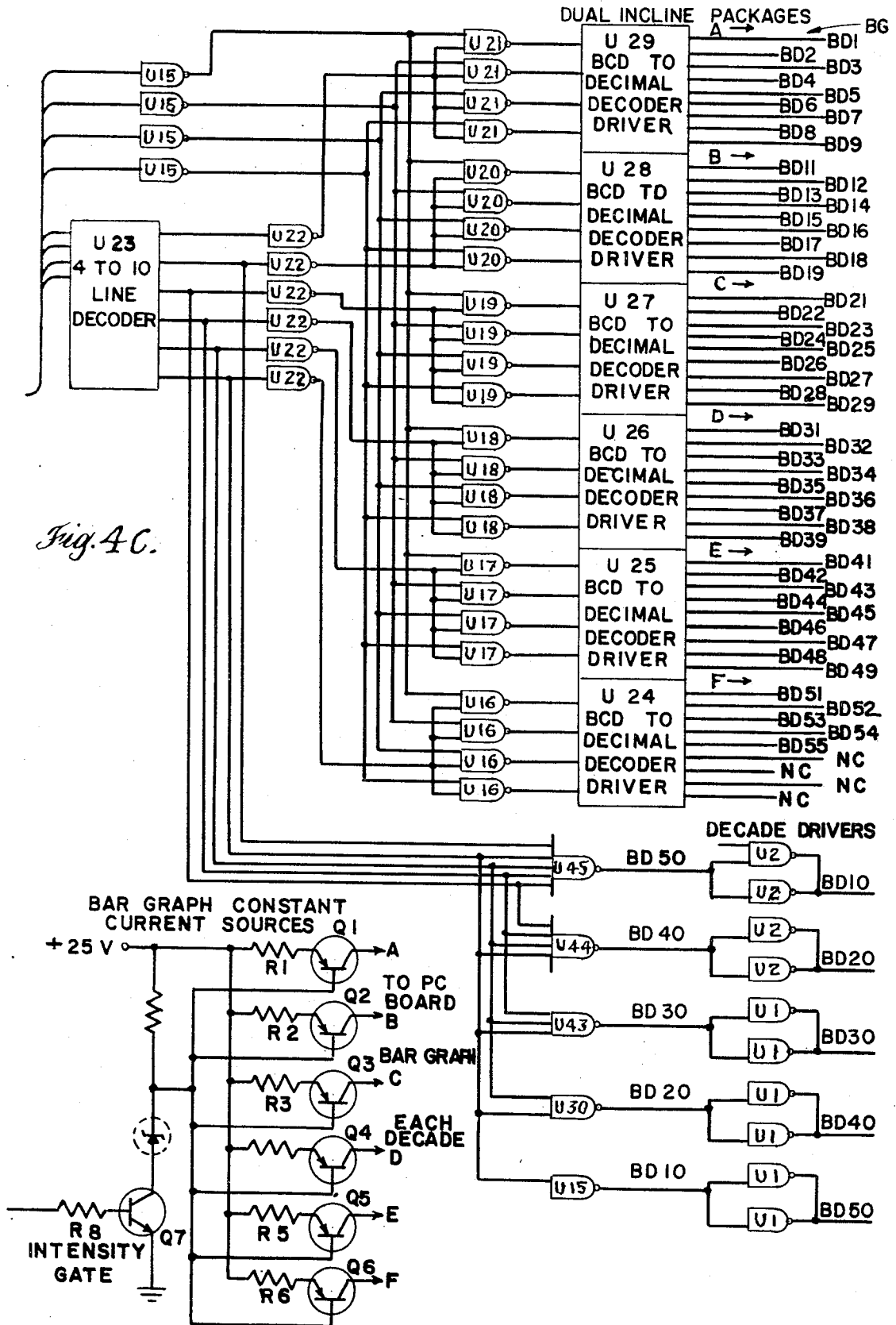


Fig. 5.

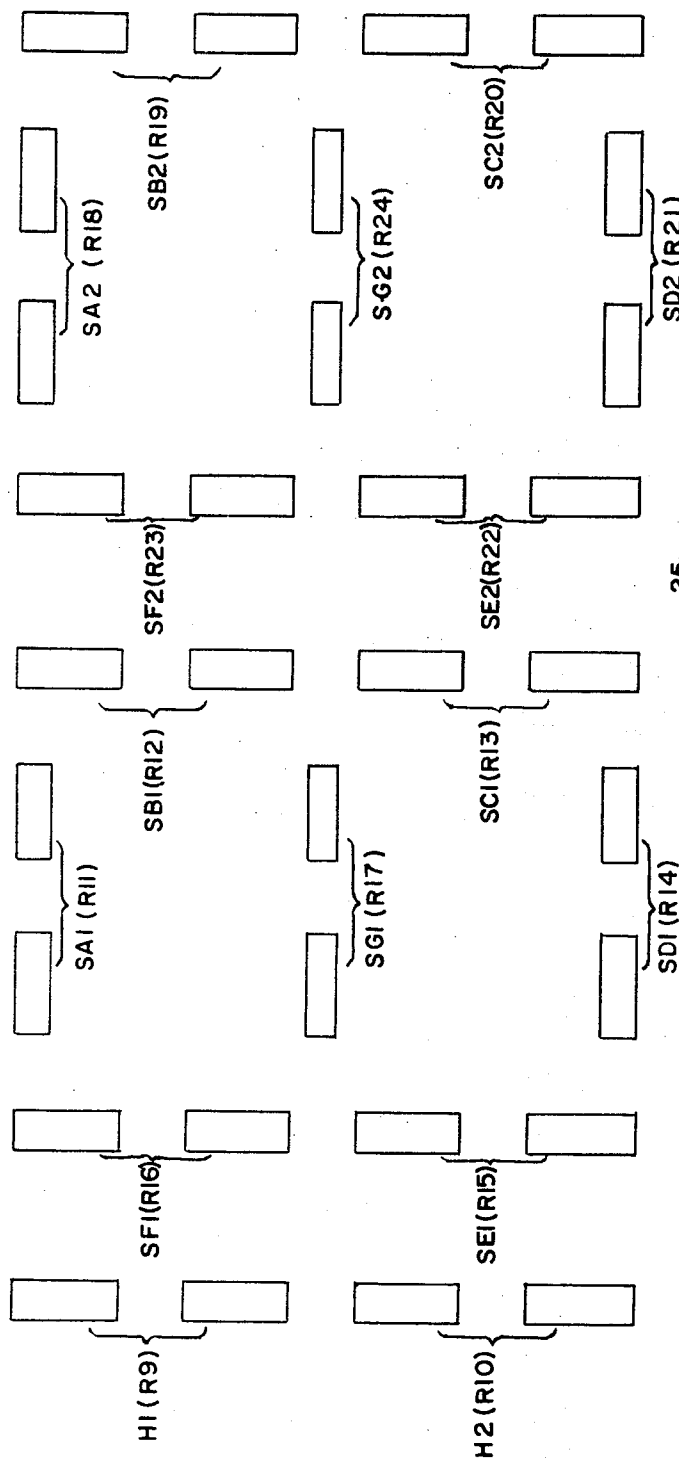


Fig. 8.

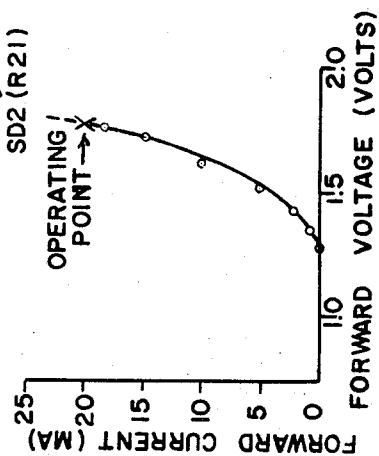
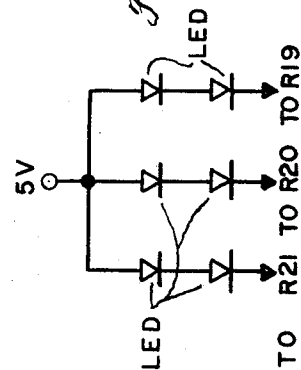


Fig. 6.



SOLID STATE INSTRUMENT SYSTEM FOR DIGITAL COUNTING AND CONTINUOUSLY INDICATING COUNT RESULTS

STATEMENT OF GOVERNMENT INTEREST

The invention described herein may be manufactured and used by or for the Government of the United States of America for governmental purposes without the payment of any royalties thereon or therefor.

BACKGROUND OF THE INVENTION

This invention generally relates to the field of electronic counting with visual indication of count results for high frequency events. More specifically the invention involves an improved digital solid state airborne engine RPM sensing and indicating system for multi-engine aircraft.

Solid state digital pulse counting and indicating systems are generally known, as is the general use of light-emitting diodes in illuminated display systems. However it appears that these known arrangements or principles have not been applied to the specific problems involved in airborne instruments for counting and displaying information concerning high speed aircraft engine RPMs. Current airborne instruments for counting and indicating engine RPM still seem to be basically of the electromechanical type which appear undesirably high in weight and power consumption, expensive, and which also could be significantly improved in reliability and effectiveness. The steady increases in aircraft power and speed, together with increasing number and complexity of aircraft instruments and indicators indicate a strong need for improvements in the undesirable aspects of present instruments for the sake of safety and for greater combat efficiency in military aircraft where weight, space, and effectiveness are most important considerations.

SUMMARY OF THE INVENTION

The shortcomings of prior art aircraft instruments in this field have been avoided, and the hereinafter-mentioned objects of the invention have been achieved by an improved electronic solid state instrument system, embodying features of this invention, for digitally counting events and continuously clearly visually indicating the counted results, the system comprising in combination, pulse generating means for receiving information corresponding to a given series of events and generating a series of independent electrical input pulses proportional in number to the number of events; clock means for measuring predetermined time intervals; electrical counting means cooperating with said pulse generating means; storage register means cooperating with said counting means; decoder means cooperating with said storage register means and said plurality of diode elements; control means cooperating with said clock means, said counting means, and said storage register means; a plurality of light-emitting diode elements cooperating with said decoder means and arranged in a visual display arrangement comprising a first group of said diode elements aligned serially to form a bar graph presentation of counted events per unit time, and a second group of said diode elements arranged to form a numeric presentation of counted events per unit time adjacent said bar graph presentation; power supply means cooperating and operatively connected with said plurality of diode elements to con-

tinuously apply to one electrode of each diode element a series of independent electrical power pulses each sufficient to activate said diode element into a light-emitting condition which appears as steady illumination to a human eye, said control means enabling said counting means to count input pulses from said pulse generating means for a predetermined interval, said control means then enabling said storage register means to receive and store the counted pulse information and to apply the same to said coding means for activation of selected diode elements to visually present counted elements, said control means then enabling reset of the counting means to zero and reenabling the counting of input pulses for another interval, said decoding means connected and arranged to selectively apply ground potential to the other electrodes of the selected diode elements to activate them to the light-emitting state.

STATEMENT OF THE OBJECT OF INVENTION

It is an object of the invention to provide a novel improved instrument system which overcomes the deficiencies of the prior art systems in terms of improved reliability, reduced size, weight, power consumption, and cost, together with improved visibility, accuracy, and a desirable redundancy of indicated information.

It is a further object to provide such an improved system which also is simple in construction, economical and easy to fabricate, operate, maintain, and service yet rugged and effective over long operating periods.

Other objects and advantages will become apparent from a consideration of the following specification and the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a partial perspective view of a basic two-engine aircraft tachometer unit embodying principles of the invention with certain parts broken away and others shown partially disassembled for a clearer disclosure of the main unit features and components.

FIG. 2 is a partial vertical cross-sectional view through the front display face portion of the unit of FIG. 1 showing the general construction and arrangement of the visual display formed by the light-emitting diodes.

FIG. 3 is a general schematic or functional block diagram of an aircraft engine RPM counting and indicating instrument system embodying features of the invention.

FIGS. 4A, 4B, and 4C are a more detailed schematic diagram of the system of the invention showing the arrangement for sensing and displaying RPM information from one engine.

FIG. 5 is a general showing of the arrangement of light-emitting diode elements on their heat sink support to form one of the numeric RPM displays used in the system of the invention.

FIG. 6 is an illustrative showing of a preferred way in which the light-emitting diode elements of the numeric RPM display are electrically connected between the power supply means and the encoder means drive or switching arrangement for the display.

FIG. 7 is a showing similar to that of FIG. 6 illustrating a preferred way in which the light-emitting diode elements for one decade of the linear bar graph display are electrically connected between the power supply

means and the encoder means drive or switching arrangement for this display.

FIG. 8 is a graphical presentation showing the typical relationship of forward current to forward voltage for the light-emitting diode elements preferably utilized in the system of the invention.

DESCRIPTION OF THE PREFERRED EMBODIMENT

As shown in FIG. 1 the tachometer or instrument system of the invention comprises a display face assembly DF cooperating with an intermediate housing IH and a rear housing RH. The housings generally contain the power supply and circuitry components needed to activate the information display of the display face assembly. The information display for a two-engine aircraft consists of a vertical bar graph presentation BG for each engine and a corresponding numeric readout or presentation N appearing in a window 3 in housing 2 of the display face assembly.

Engine RPM of the left and right engines is presented in increments of 5 percent (from 0 to 70 percent of rated RPM) and 1 percent (from 70 to 110 percent of rated RPM) on the bar graph presentations or displays. Each bar graph display comprises 54 light-emitting diodes, indicated as LED in the drawings. Each diode is preferably sized at about 0.020 by 0.030 inches and will be described in greater detail hereinafter. Each numeric display is made up of two seven-segment numeric indicators and a single two-segment numeric indicator as shown in FIGS. 3 and 5. The seven-segment numeric indicators are configured in a window frame format as shown from 14 light-emitting diodes (0.35 by 0.015 inches each) with two diode elements per segment. The numeric display reads out percent of rated engine RPM in 1 percent steps over the full range of the system to provide the pilot or viewer with a precision RPM reading at any desired time.

The diode elements of the bar graph display are configured in decades with each decade having its own constant current source and decade enable line (FIG. 4C and FIG. 7). The constant current sources provide uniform light intensity from all diode elements of this display.

The numeric display indicates the same data or information shown in the cooperating bar graph to provide redundancy and reliability. Generally, referring to FIG. 2, after the tachometer input signal is clipped, limited and multiplied by a factor of four, it is counted by the same type of decade counter as the bar graph display signal. At the end of each count period a store gate occurs and new count data is transferred to storage registers. From the storage registers the information is processed by BCD to seven-segment decoders which double as drivers to the light-emitting diode elements.

Intensity of the light-emitting diode displays is controlled by modulating the "on" currents of the diode elements by a variable pulse width generator. This variable duty cycle control gates the diode elements on and off at a non-flicker rate, the variable duty cycle gating appearing to the human eye as an intensity variation on the diode element emitted light. Since the diode elements are very rapidly driven to upper ranges of forward current on each power pulse, the various diode elements light emission need not be matched over the forward current operating curve but only at the predetermined upper range of this current. The diode ele-

ments are matched as to light emission only at this upper current range which simplifies their manufacture and lowers their cost. In addition, the "on" state is selected to involve that value or range of forward current where the light-emitting diode element efficiency is optimum.

Generally describing light-emitting diodes and their functioning, the direct conversion of electrical energy to light energy, or electroluminescence, is reasonably well known, having been first observed in semiconductors in about 1923 during work with silicon carbide detectors. The flow of current through the silicon carbide produced light without the crystal becoming incandescent, the color of the emitted light depending on the material and experimental conditions. This technology remained rather inactive until the 1950s when workers in the field applied theories developed for p-n junctions in transistors developed a theoretical explanation and renewed interest in the electroluminescent properties of semiconductors. Early light-emitting diodes radiated infrared and visible red color and more recently brightness and efficiency have improved to the point where they can be used to alert operating personnel even in well-lighted environments. The light emission is produced by injection and recombination of electrons and holes in the crystal material. As these excess carriers recombine, they give up energy in the form of photons.

Suitable efficient light-emitting diodes for use in systems embodying the present invention are fabricated from gallium aluminum arsenide using a solution growth technique. This method permits the formation of carefully controlled p-n junctions by slowly cooling a solution of Ga, Al, and GaAs, where the Ga is in excess, and n- or p- type dopants (Te or Zn). Epitaxial layers of GaAlAs are deposited on a GaAs substrate as the solution cools from about 1,000° C to about 880° C. Later, the substrate crystal is removed and the GaAlAs p-n junction that remains is provided with contacts using vapor-deposited metallurgy techniques. Through careful control of dopants and material concentrations, the emission wavelength of the diodes may be varied from about 6,000 Angstroms (visible) to 9,000 Angstroms (near IR).

Light-emitting diodes require reasonably high forward current densities before useful emission can occur. This current is generally greater than 10 amperes/cm². For a typical GaAlAs diode crystal of square 0.015 × 0.015 inch configuration, and assuming 20 milliamperes are required for a nominal value of 400 ft-lamberts, the current density J is about 14 amperes/cm². A forward voltage versus forward current curve for a typical GaAlAs light-emitting diode is shown in FIG. 8.

A summary of GaAlAs light-emitting diode characteristics is presented in Table I.

TABLE I
GaAlAs Light-emitting Diode Data

	Min.	Max.	Units
Power Dissipation Derate Linearly from 25°C 2.5 mW per °C		150	milli-watts
Forward Current, Continuous		100	milli-amperes
Peak Forward Current 1 us Pulse, 300 pulses per second		3	amperes
Operating Temperature	-55	100	°C
Reverse Voltage at I = 10 u A	3		volts

Electro-Optical Operating Characteristics (25°C Unless Otherwise Specified)

	Min.	Typical	Max.	Units
External Radiated Power If = 50 mA		3		Milli-watts
Peak Emission Wavelength	6000		9000	Angstroms
Emission Line Half Width		375		Angstroms
Forward Voltage Drop at IF = 100 mA		1.8		volts
Forward Dynamic Resistance at IF = 100 mA		20		ohms
Reverse Current at VR = 3V		1.0		Micro-amperes
Capacitance at Vf = 0		100		pico-farads
Capacitance at Vf = 0.8V		150		pico-farads
Capacitance at VR = 3v		70		pico-farads
Light Turn-on Time		25		nanoseconds
Light Turn-off Time		25		nanoseconds

Thermal Characteristics

	Min.	Typical	Max.	Units
Wavelength Temperature Coefficient (Case Temperature)		1.3		Angstroms per °C
Forward Voltage Temperature		-1.5		milli-volts per °C
Coefficient Vf/T Output Attenuation Temperature Coefficient %/T		0.43		% per °C Ref at 20°C

More specifically the preferred diodes for use in the system of the invention are GaAlAs elements approximately 35 × 15 mils in size. A host crystal, serving as a substrate, of GaAs approximately 18 mils thick is the starting material. On top of this substrate a layer of N-type GaAlAs of approximately 2 mils thickness is grown. In turn, another layer of P-type GaAlAs is grown over the N-layer. Both the substrate and the P-layer are opaque while the N-layer is transparent with respect to the red light which is emitted when current is passed through the final p-n junction. The substrate is then lapped off leaving a p-n wafer approximately 4 mils thick. A layer of metal is then deposited on both sides of this wafer. The p-side is uniformly coated with gold/zinc, while the n-side is coated with gold/germanium/nickel through a mask which defines the N contacts. The whole wafer is then heated and the semiconductor-metal contacts are formed by the resulting alloying process. The metallized wafer is then cut up into discrete diode elements by a string saw. An etching process is then carried out to remove crystal damage caused by the sawing operation. Each diode element has a solid metal layer on the bottom or p-side and a metal contact on the n-side which will accommodate interconnecting wires. Each diode element is then bonded with a conductive epoxy compound to an anodized aluminum block. This block, which is machined to size is then anodized to provide an aluminum oxide insulation, and acts as a heat sink for the diode elements. The base of block is designed to maintain the diode element array at 40° C temperature when the ambient air is 25° C. The block is prepared with a black dye to eliminate reflective surfaces. One mil gold wires are used as flying leads to make the diode-diode and diode-terminal connections. In operation the display becomes

visible, or illuminated as a result of the light generated within the p-n junction and passing through the top transparent n-layer. As seen in FIG. 8 the current-voltage characteristics of the light-emitting diodes used are similar to ordinary semiconductor diodes in shape. As voltage increases to about 1.8 volts the current change is somewhat gradual. However, at this point the current begins increasing very rapidly without appreciable voltage increase and will stress the diode/wire interface. As will become apparent in the following description a constant current source or series resistor in conjunction with a constant voltage source must be used to light or activate these diode elements. In the preferred system of the invention the constant current approach is used for the bar graph display and the series resistor is used for the numeric display.

As shown in FIGS. 1 and 2, the display face assembly DF contains the light-emitting diode elements LED plus filter and other elements for visual enhancement of the overall display. Directly inside an opening 3 in the front of aluminum housing 2 of display face assembly DF is a cover glass 11 which has an HEA non-glare coating on both sides. Against this glass element is a plexiglas edge lighting insert element 12 which is provided with a plurality of incandescent lamps (not shown) to provide conventional illumination to engraved legends on red filter element 13. This filter element 13, visible from the front of the instrument is a clear circular polarized filter and a red filter sandwiched together. This filter over the black background of the heat sink member HS on which the light-emitting diodes LED are mounted provides maximum visual enhancement of the display. The diode element array on heat sink member HS is directly behind filter member 13. Diode elements LED are encapsulated beneath a layer of clear epoxy material to protect the diode elements, their leads, and interconnections. In addition the clear epoxy coating more effectively optically couples the diode element to the ambient air, giving an apparent brightness improvement of more than two over the unencapsulated condition.

The intermediate housing portion IH of the instrument comprises an aluminum framework member 1 to which is secured, by suitable conventional means, the display face assembly DF, its diode element heat sink member HS, two main printed circuit cards MCC, power converters and other elements (not shown).

The instrument has been designed for easy maintenance, the display face assembly DF, diode element array and heat sink HS being removable from the front, and the electronic circuit cards designed to swing out from the sides from operative positions in member 1, with conductor bundles WB acting as hinged connections, to lie flat on a work bench. Two rectangular cover plates having an inside coating of a glass-epoxy compound are secured by suitable means to the sides of framework member 1 to enclose printed circuit cards MCC in the intermediate housing. The glass-epoxy compound provides electrical insulation to prevent the printed circuit card conductors from shorting out against the housing. A durable conformal coating is applied to the component side of the circuit cards MCC to provide a good mechanical support between the components, wiring and the cards. Printed circuit cards are identical except for intensity control transistor Q7 for the bar graph.

Rear housing RH is enclosed by wall member 4 and contains electrical power supply units PS, printed circuit clock card CC and a fan for cooling air mounted in casing F. Wall member 4 also supports power supply connection PI and tachometer signal input connection TSI.

As shown by the arrows in FIGS. 1 and 2 the cooling fan in casing F brings in cooling air through the spaces 8 between glass panel 11 and front wall 2 of the display face assembly DF, moves the cooling air over the diode element array and heat sink HS, rearwardly through the intermediate housing IH and out through opening 7 into rear housing RH where it is passed over the power supply units PS for the light-emitting diodes and exhausted out the bottom of housing RH as shown through an exhaust opening not shown.

Clock card CC and power supply units PS can be reached for test and service by removing housing element 4. Power supply units are mounted on a wall portion of rear housing RH which wall portion is provided on its exterior surface with cooling fins FI for additional cooling effect.

Manually adjustable knob IC on the front of the display face assembly and the cooperating intensity control potentiometer ICR provide the means for selecting and adjusting the intensity of light produced by the light-emitting array.

Referring again to the general schematic showing of FIG. 3 it will be seen that the tachometer input is received by a clipper circuit 41 the output of which is connected through a multiplication-by-four circuit 42 to gate 43. The output of gate 43 is connected both to count modifier circuit 44 and to decade counter 50. The output of count modifier circuit 44 is connected to decade counter 45 which is in turn connected to storage register 46. Storage register 46 is connected to the input of BCD-to-decimal decoder 47 which is in turn connected to 1-out-of-10 decoder driver 48 which activates the selected light-emitting diode elements of bar graph display BG.

The output of decade counter 50 is connected to storage register 51 which is connected to BCD-to-seven-segment decoder 52 which activates the selected light-emitting diodes of numeric display N.

Intensity modulation unit 55 generates a series of independent power control pulses which are applied to the light-emitting diodes of the bar graph display BG via constant current source unit 53, and to the light-emitting diodes of the numeric display N via constant voltage (+ fixed resistance) source 54. Brightness pot 56 varies the bias applied to the output of a sawtooth oscillator circuit (not shown) to control the duration of the power control pulses and vary the apparent intensity of illumination for both displays BG and N.

Clock and gate generator circuit 60 is operatively connected in conventional fashion to gate 43 to control counting of tachometer input pulses for a precisely measured predetermined interval. Clock and gate generator circuit 60 is also operatively connected conventionally to storage registers 46 and 51 to enable them to store the count results of the decade counters 45 and 50, respectively, and further operatively connected to decade counters 45 and 50 to reset them to zero after count results have been stored in the storage registers 46 and 51.

Normal aircraft power at 28 volts DC is converted to more precisely controlled 25 volts DC and 5.5 volts DC

used for the logic circuits and activation of the light-emitting diodes in a suitable arrangement of conventional units 36, 37, 38 and 39.

The tachometer input signal is a sine wave signal received from the aircraft engine tachometer and has a frequency proportional to engine RPM. In the preferred embodiment disclosed 100 percent of rated RPM equals 70 Hz. The input signal is clipped and limited by clipper circuit 41 and then multiplied by a factor of four in circuit unit 42 to provide 280 discrete pulses when the engine RPM = 100 percent rated. This signal passes gate 43 when enabled by a count signal from the clock and gate generator circuit 60 and is applied to two channels one including units 50, 51, and 52 associated with the numerics display N and the other including units 44, 45, 46, 47, and 48 associated with the bar graph display BG. Count modifier unit 44 is operated alternatively as a divide-by-five counter or a one-for-one straight-through counter. When the counted input pulses indicate an RPM of less than 70 percent rated RPM this circuit passes one pulse for each five it receives. When counted pulses exceed 70 percent rated RPM this circuit passes each pulse it receives. During the predetermined interval that gate 43 is enabled by the count signal from the clock and gate generating means 60 to pass tachometer input pulses the decade counters 45 and 50 are making the count of these pulses. At the end of this interval the enabling count signal to gate 43 is terminated, and the transmission of input pulses therethrough ceases. The clock and gate generator 60 next transmits a "store" signal to the storage registers 46 and 51 to enable them to receive and store the count results from the counters 45 and 50. The stored count result information in the storage registers 46 and 51 is simultaneously decoded by the respective decoder units and utilized to selectively cause energization of appropriate light-emitting diodes in each of the displays BG and N to indicate visually the stored count results. Following storage of count results and visual indication thereof, the clock and gate generator circuit provides a "reset" signal to each counter 45 and 50 to return the count to zero and again provides the "count" signal to enable gate 43 to again pass tachometer input pulses to the counters for a succeeding interval and repetition of the counting and storage-display cycle.

FIGS. 4A, 4B, and 4C together represent a more detailed schematic diagram of the instrument system corresponding to the more general schematic showing of FIG. 3.

The clock gate generator circuit is located on one surface of the clock and in the rear housing RH. The basic oscillator is made up of crystal XTL, quadruple two-input NAND gate FP10, resistors R14 and R15, and capacitor C7. The 1 MHz signal is divided down to 50 KHz by decade counters FP1, FP2, FP3, and dual D-type edge-triggered flip-flop FP4 to provide better temperature stability than would be achieved by using a 500 KHz crystal. The initial state of the signals in the clock gate generator circuit are as follows: pin 70 of dual four-input NAND gate FP11 is positive awaiting the 197 clock pulse count, pin 79 of shift register FP7 is positive, having been shifted through FP7 (both sides) from pin 70. The 2 ms clock pulses are applied to four-bit binary counters FP5 and FP6 and counted BCD to 197 at which time the voltage on pin 70 drops to zero level. This inhibits further counting by counters

FP5 and FP6 by dropping the voltage on pin 74 of triple three-input NAND gate FP11 to zero level. Pin 78 of quadruple two-input NAND stop count gate FP8 now becomes positive and counting of the input pulses from the tachometer signal ceases. The next clock pulse to pin 71 of FP7 shifts the zero level voltage on pin 72 of FP7 to pin 83 of FP7. This signal from pin 83 of FP7 is differentiated by the action of capacitor C55 and resistance R56 and a 2 ms store command signal is sent to storage registers U33, U34, U10 and U11 from pin 84 of quadruple two-input NAND gate FP8. The next clock pulse to pin 71 of FP7 transfers the zero voltage level to pin 80 of FP7 and the Master Reset line, resetting counters U35, U36, U37, U38, U12 and U13 and transfers a positive level reset signal from pin 80 of FP7 to four-bit binary counters FP5 and FP6. When counters FP5 and FP6 are reset pin 70 of FP11 becomes positive enabling pin 82 of FP11 to start carrying the clock count pulses and the timing process begins again. The 197 count of 2 ms pulses provides the 394 ms count time, or predetermined interval, for sampling and counting the input tachometer signal pulses.

Both main circuit cards MCC in intermediate housing 1H are identical except that the intensity gating transistor Q7, resistors R7 and R8 are on one card only, as shown in FIG. 4C, the light-emitting diodes of the systems for both aircraft engines being controlled from this one intensity gating circuit. Referring again to FIGS. 4A, 4B, and 4C which show the schematic diagram for this one current card and corresponding one engine, the tachometer input signal at the upper left-hand portion of FIG. 4A is limited to approximately 18 volts per pulse by Zener diodes Z1 and Z2. Parallel diodes D1 and D2 provide good forward conduction paths which the Zener diodes do not possess. Zener diode CR5 and resistor R30 are a Zener biasing network to raise the baseline of the input signal 6.2 volts above ground to allow the use of integrated circuit comparator U47. Comparator U47 normally requires a negative voltage but since none is available, the ground pin and baseline signal were run up to 6.2 volts, the positive supply to 18 volts DC and the negative pin to ground. After processing of the signal by comparator U47 the baseline of the output is Zenered down to ground reference once more by Zener diode CR2 and resistor R25. Comparator U47 receives the input signal, a clipped sine wave limited at the input to the comparator to about the +6.2 volts reference by diodes CR3 and CR4. Small capacitor CS provides noise quieting. Comparator U47 produces a square wave output signal, the transition edges are coincident with the points at which the input signal passes through the 6.2 volt reference level. The resulting output signal, after being brought down to ground level by diode CR2 and resistor R25, is a square wave from ground to about 3 volts and the same frequency as the input signal. The output signal then is transmitted to the "times 4" multiplication section. A key portion of this section is an integrated circuit unit containing two "one-shot" or monostable multivibrator units U41A and U41B. The multiplication process commences when the square wave output from comparator U47 enters quadruple two-input NAND gate formed by units U39 where complementary inverse and true signals are formed. Resistors R36 and R37 plus capacitors C4 and C5 differentiate each signal providing positive and negative spikes for each transition of the original square wave.

The positive spikes are "anded" at the input terminals of quadruple two-input NAND gate formed by unit U40 and are applied to the input of the first "one-shot" or monostable multivibrator unit U41A. The two positive spikes trigger the "one-shot" multivibrator twice to form two output pulses of about 3 ms each. The input data signal now has two digital pulses where one was provided or has been multiplied by a factor of two. The resulting output goes through an identical circuit arrangement comprising units U40, U42 and U41B for a total multiplication factor of 4. The data pulses are no longer equally spaced but appear as pulse pairs. However since it is the number of pulses that is significant rather than their placement no significant accuracy problems arise.

Referring to the logic for the bar graph display at the upper portion of FIG. 4B and on FIG. 4C, the data signal passes from unit 41B via gate 43 to decade divide-by-five integrated circuit counter. Eight input NAND gate U32, storage registers U33 and U34 (quadruple bistable latch units), decade counters U35, U36, and U37, and dual D-type edge-triggered flip-flop U38 all function as a nonlinear counting arrangement for the input signal pulses. Counter U37 passes every fifth input signal pulse until the U35 and U36 counters reach a count of 14 (70 divided by five). At this point the coded count is used to clock U38. The output of U38 directs either the divide-by-five line of data or the straight one-for-one 1 percent step data to the counters U35 and U36. At the conclusion of each sample period, or predetermined counting interval, a Master Reset pulse from the clock and gate generating section resets all counters to zero and flip-flop U38 back to the divide-by-five position. Prior to this resetting action, however, a storage command has been sent from the clock and gate generator section to storage registers U33 and U34 and the count is stored, holding or activating the light-emitting diode elements necessary to visually indicate the stored count until the next data input to the storage registers.

From the storage registers U33 and U34 the coded (BCD) count information signal goes to the decoder/drive section for the bar graph display which consists of inverters U15 and U22, quadruple two-input NAND gates U16, U17, U18, U19, U20, U21, and U30, BCD-to-decimal decoder U23, BCD-to-decimal decoder-drivers (with open collector outputs) U24, U25, U26, U27, U28, U29, quadruple two-input NAND gate U30, triple three-input NAND gate U43, dual four-input NAND gate U44, eight-input NAND gated U45, and inverters (with open collector outputs) U1 and U2. The activating lines for activating the desired individual light-emitting diode units are indicated at BD1-9, BD11-19, BD21-29, BD31-39, BD41-49, and BD51-55. In this section the operation is as follows: the unit count from register U34 goes through inverters U15 for inversion and then to each of the decade gates U16 through U21. The proper decade is then selected by BCD-to-decimal decoder U23 which more specifically is a four-line to 10-line decoder. The decade enable line goes to its respective decade gate U16 through U21. The operation thus far has been to decode the units count in all decade gates, but only to enable the highest decade gate used. The enabling and latching of all decades below the uppermost decade used is accomplished by "anding" the decade lines in gates U43, U44, U45, U30 and U15. For example, if it is desired

to light the bar graph display to the light-emitting diode element indicating the 35 percent RPM level, diode element 5 is decoded and enabled in decade 4 (U19). Then, the three decades below decade 4 (U43, U44, and U45) are all enabled and latched. The resulting outputs at BD10, BD20, and BD30, exciting their respective drivers, ground the last diode element in each of decade chains 10, 20, and 30. FIG. 7 indicates the wiring arrangement for the decade chain arrangement of light-emitting diode elements.

The output drivers for individual diode elements themselves are BCD-to-decimal decoder drivers U24 through U29, which receive the coded four-line data, decode it, and ground the desired one of the output lines.

The chain of logic for the numeric display (lower portion of FIG. 4B) consists of decade counters U12 and U13, dual D-type edge-triggered flip-flop units U14, inverter U15, storage registers (quadruple bistable latches) U10 and U11, BCD-to-seven-segment decoder drivers U8 and U9, inverters (with open collector outputs) U2, U3, U4, U5, U6 and U7, current limiting resistors R9-R24 for each numeric segment formed by two light-emitting diode elements (see FIGS. 5 and 6), and numeric segments (formed by two light-emitting diode elements) H1, H2, SA1, SB1, SC1, SD1, SE1, SF1, SG1, SA2, SB2, SC2, SD2, SE2, SF2, and SG2.

This chain of logic for the numeric display is similar to the bar graph display logic with the exception that the counting is linear, there being no divide-by-five feature present. The count is performed in decade counters U12 and U13 and stored in storage registers U10 and U11 on the "store" command, or control signal from the clock and gate generator section. Flip-flop U14 acts both as a 100 count and a storage register. When a count of 100 is reached U14 is triggered. A "store" signal to U14 carries an output signal to pass to inverters U7 and U2 which provide a ground to activate lightemitting diode segments H1 and H2 to display the "one" in the hundreds position in the numeric display. The other numerics are activated by the lighting of the light-emitting diode segments by BCD-to-seven-segment decoders U8 and U9. These decoders decode the BCD signal from the storage registers U10 and U11 to the proper format for each seven-segment numeric character. Inverters U2 through U7 provide the inversion required to put a ground where each light-emitting diode segment is to be lit or illuminated. Resistors R9 through R24 are current limiting resistors for controlling the current passed through each diode segment in the numeric display by the constant voltage power source.

It is believed to be clear from the above description and discussion that applicants have provided a system for digitally counting and indicating count results which is a significant improvement over the prior art systems and achieves the objects of the invention.

Although a preferred embodiment has been described in detail in accordance with the Patent Law, many modifications and variations within the spirit of the invention will occur to those skilled in the art and all such are considered to fall within the scope of the following claims.

What is claimed is:

1. An improved electronic solid state instrument system for digitally counting events and continuously visu-

ally indicating periodically updated results of the counting, said system comprising in combination:

pulse generating means for receiving information corresponding to a given series of events and generating a series of independent electrical input pulses proportional in number to the number of events;

clock means for measuring predetermined time intervals;

electrical counting means cooperating with said pulse generating means;

storage register means cooperating with said counting means;

decoder means cooperating with said storage register means and a plurality of diode elements;

control means cooperating with said clock means, said counting means, and said storage register means;

a plurality of light-emitting diode elements cooperating with said decoder means and arranged in a visual display arrangement comprising a first group of said diode elements aligned serially to form a bar graph presentation of counted events per unit time, and a second group of said diode elements arranged to form a numeric presentation of counted events per unit time adjacent said bar graph presentation; and

power supply means cooperating and operatively connected with said plurality of diode elements to continuously apply to one electrode of each diode element a series of independent electrical power pulses each sufficient to activate said diode element into a light-emitting condition which appears as steady illumination to a human eye, said control means enabling said counting means to count input pulses from said pulse generating means for a predetermined interval, said control means then enabling said storage register means to receive and store the counted pulse information and to apply the same to said decoder means for activation of selected diode elements to visually present counted pulse information simultaneously on both groups of diode elements, said control means then enabling reset of the counting means to zero and reenabling the counting of input pulses for another interval, said decoding means connected and arranged to selectively apply ground potential to the other electrodes of the selected diode elements to activate them to the light-emitting state.

2. The system of claim 1 in which said first group of diode elements cooperates with the counting means, the storage register means, the decoder means, and the control means to indicate RPM changes in larger increments below a given predetermined level and in smaller increments above said level.

3. The system of claim 2 which comprises:

an intensity control means cooperating with said power supply means to control the light intensity of said diode element presentations by varying the duration of said power pulses applied to said diode elements.

4. An airborne electronic solid state instrument system for digitally counting and visually displaying aircraft jet engine shaft RPM, said system comprising in combination:

a lightweight compact housing means;

input means in said housing means for receiving signals corresponding to engine RPM and in response thereto producing a series of electrical pulses with a frequency varying in accordance with engine RPM;

- a first visual display means comprising a first group of light-emitting diode elements having their light outputs matched in a given upper portion of their forward operating current range and arranged in said housing means adjacent a transparent portion thereof in a series configuration to form a variable linear bar graph presentation;
- a second visual display means comprising a second group of light-emitting diode elements having their light outputs matched in a given upper portion of their forward operating current ranges and arranged in said housing means adjacent said first visual display to form a variable numeric display;
- a gate means in said housing means operatively connected with said input means;
- a first pulse counter means in said housing means operatively connected to said input means through said gate means;
- a first storage register means in said housing means operatively connected with said first pulse counter means and said first display means;
- a second pulse counter means in said housing means operatively connected to said input means through said gate means;
- a second storage register in said housing means operatively connected with said second pulse counter means and said second display means;
- a time-measuring clock means in said housing means operatively connected to said gate means, to said first and second counter means, and to said first and second storage register means, said clock means constructed and arranged to generate a plurality of control signals at predetermined intervals and operatively connected to transmit a first control signal to said gate means to enable transmission of input pulses from said input means to each of said counter means for a predetermined pulse-counting time period, and thereafter to transmit a second control signal to said storage register means to enable transfer thereto and storage therein of count information from the cooperating counter means, said count information corresponding to the number of input pulses counted during said predetermined time period, said second control signal also operative to cause activation of selected ones of said two groups of light-emitting diodes by the stored information in the respective storage register means to visually display indications of the stored count information, said gating means further arranged to transmit a third control signal to reset each counter means to its starting point before the next counting period is started by said gate means

again being enabled to transmit input pulses to the counter means;

first power supply means in said housing means operatively connected with said first group of light-emitting diode elements; and

second power supply means in said housing means operatively connected with said second group of light-emitting diode elements, each of said power supply means connected to apply to one electrode of each of said diode elements of the corresponding group, a continuous series of independent electrical power pulses at a frequency above which said diode elements appear to the human eye to be continuously illuminated, said pulses being of variable duration and of sufficient magnitude to activate said light-emitting diode elements to light-emitting state, the outputs of said storage register means selectively operatively connected to apply a ground potential to the other electrode of said light-emitting diode elements in accordance with the stored count information and cause selective illumination thereof during each power pulse.

5. The system of claim 4 in which the first display means indicates RPM changes in large increments below a predetermined RPM level and in smaller increments above said level, and said first counter means comprises control means to correspondingly automatically vary the counting action of the first counter means below and above said predetermined level.

6. The system of claim 4 which further comprises: electrical control means operatively connected with said first and second power supply means to selectively vary the duration of the power pulses and vary the apparent intensity of the display means formed by the light-emitting diode elements.

7. The system of claim 4 in which the light-emitting diode elements of said first and second display means are physically mounted on heat sink means and said system further comprises:

cooling means in said housing means to move a stream of cooling air over said diode elements, over said heat sink means, over said power supply means and out of the housing means to remove heat from the system and housing.

8. The system of claim 4 in which said power supply means comprises means limiting forward current through the light-emitting diode elements to a predetermined upper range in which most efficient emission of light occurs and in which the emitted light outputs of the light-emitting diode elements are substantially evenly matched.

9. The system of claim 4 in which said current limiting means for said first display means comprises a plurality of constant current sources, and said current limiting means for said second display means comprises constant voltage fixed resistance circuitry.

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