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(54) ATOMIC LAYER DEPOSITION OF CMOS GATES WITH VARIABLE WORK FUNCTIONS

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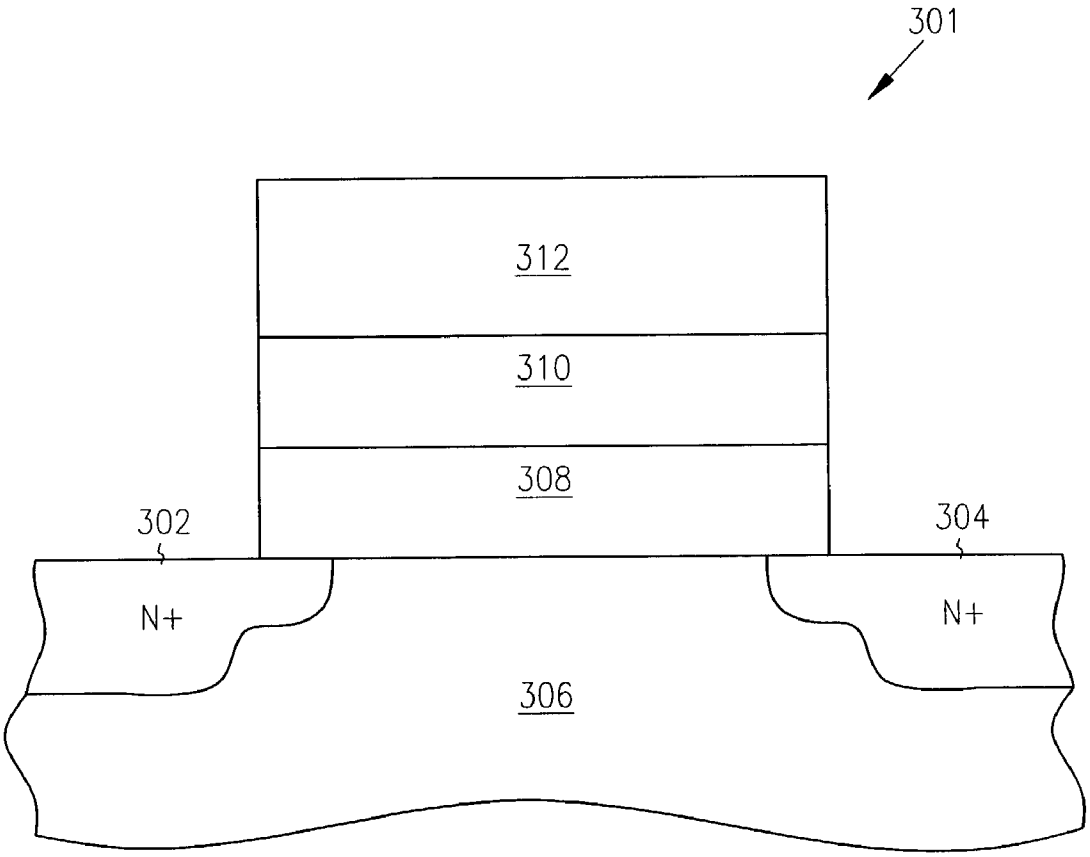
(57) **ABSTRACT**

Structures, systems and methods for transistors having gates with variable work functions formed by atomic layer deposition are provided. One transistor embodiment includes a first source/drain region, a second source/drain region, and a channel region therebetween. A gate is separated from the channel region by a gate insulator. The gate includes a ternary metallic conductor formed by atomic layer deposition.



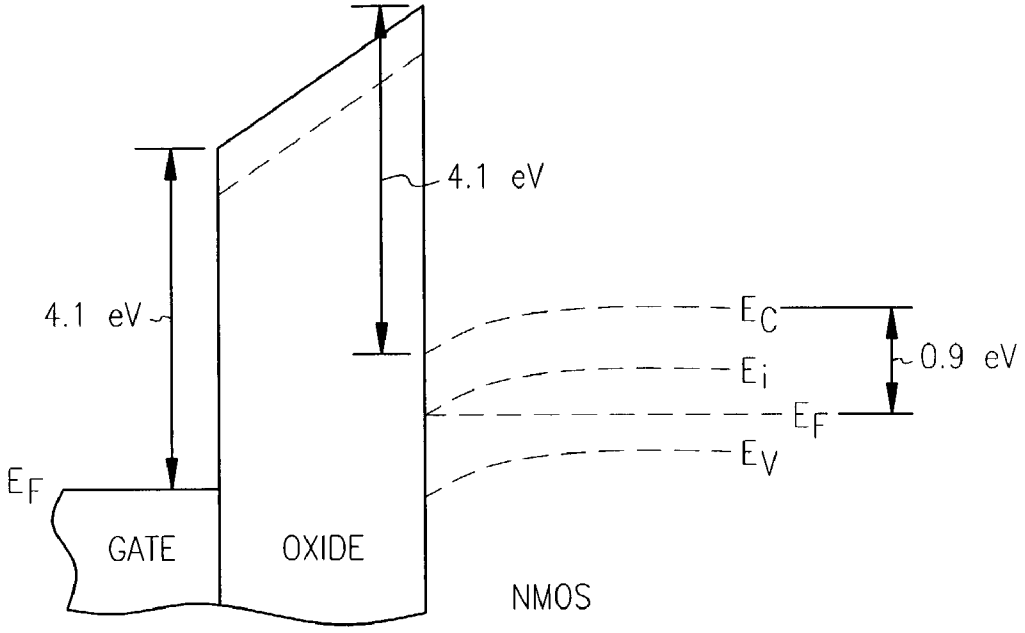

4.1 eV
4.1 eV
E_C
E_i
E_F
E_V
0.9 eV
E_F
GATE
OXIDE
NMOS

FIG. 1A

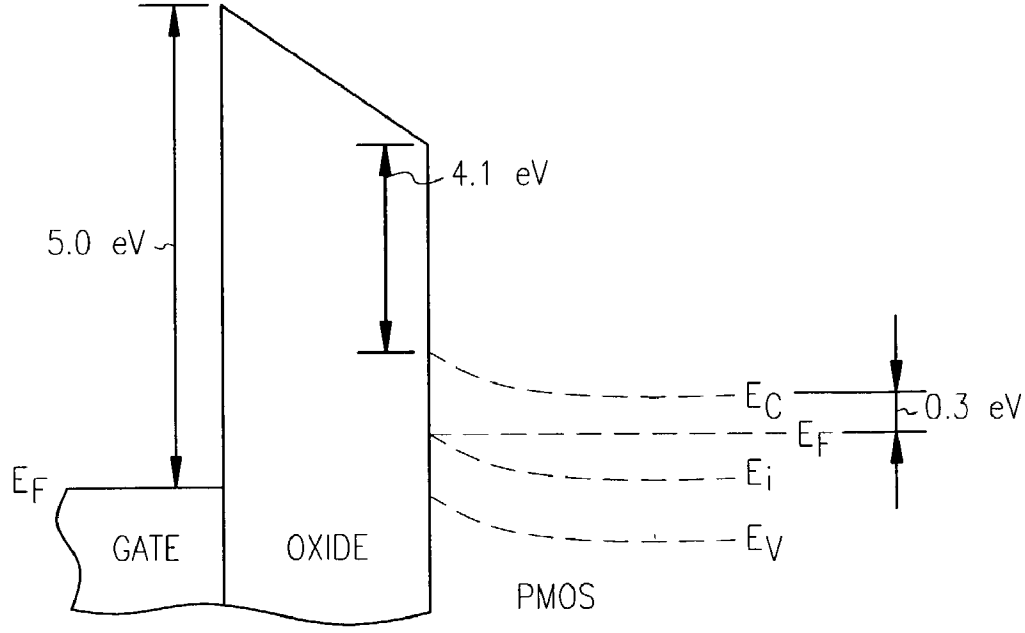

4.1 eV
5.0 eV
E_C
E_F
E_i
E_V
0.3 eV
E_F
GATE
OXIDE
PMOS

FIG. 1B

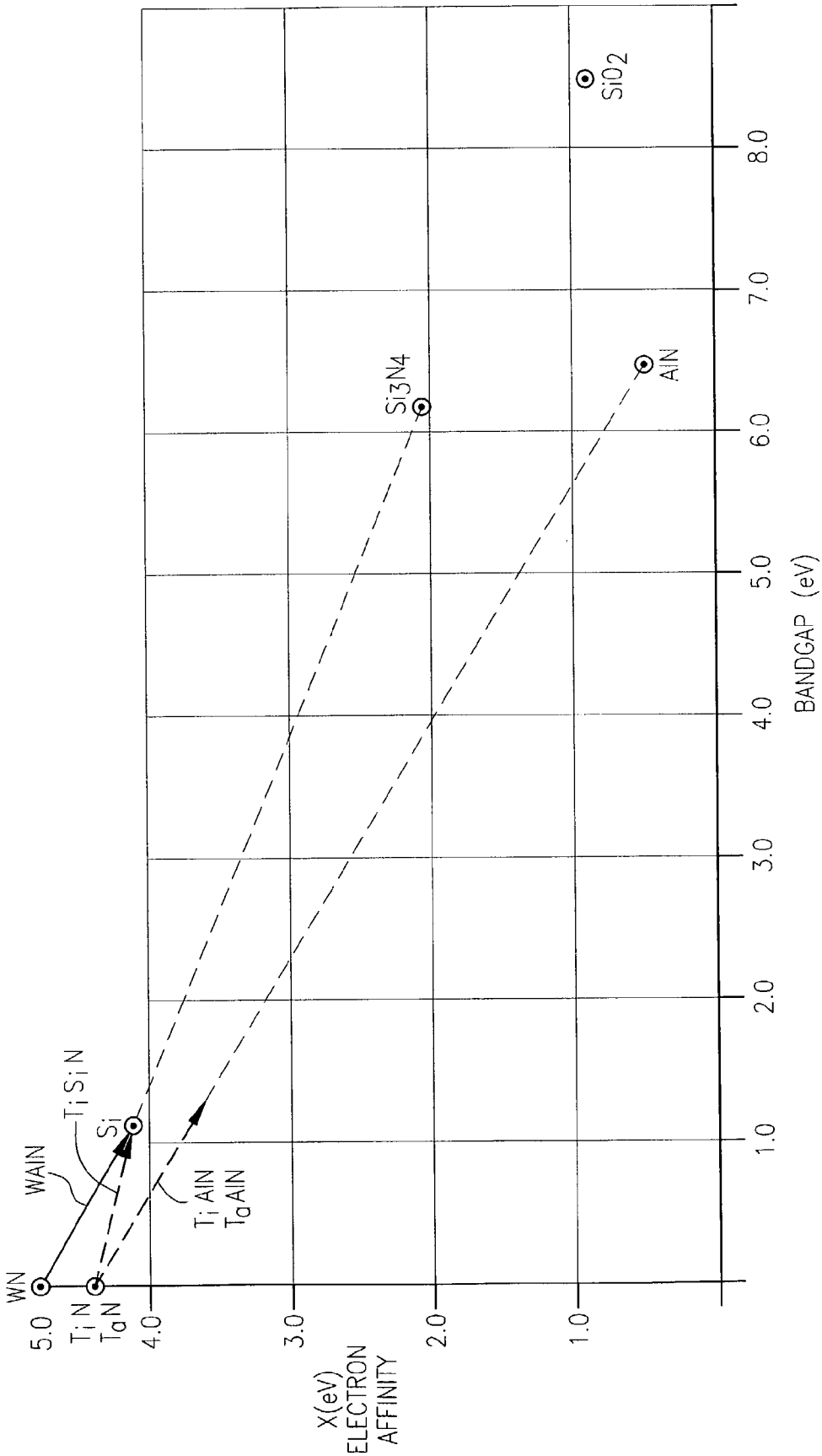

SiO2
Si3N4
AlN
WN
TiN
TaN
WAlN
TiSiN
Si
TiAlN
TaAlN
5.0
4.0
3.0
2.0
1.0
X(eV)
ELECTRON
AFFINITY
1.0
2.0
3.0
4.0
5.0
6.0
7.0
8.0
BANDGAP (eV)

FIG. 2

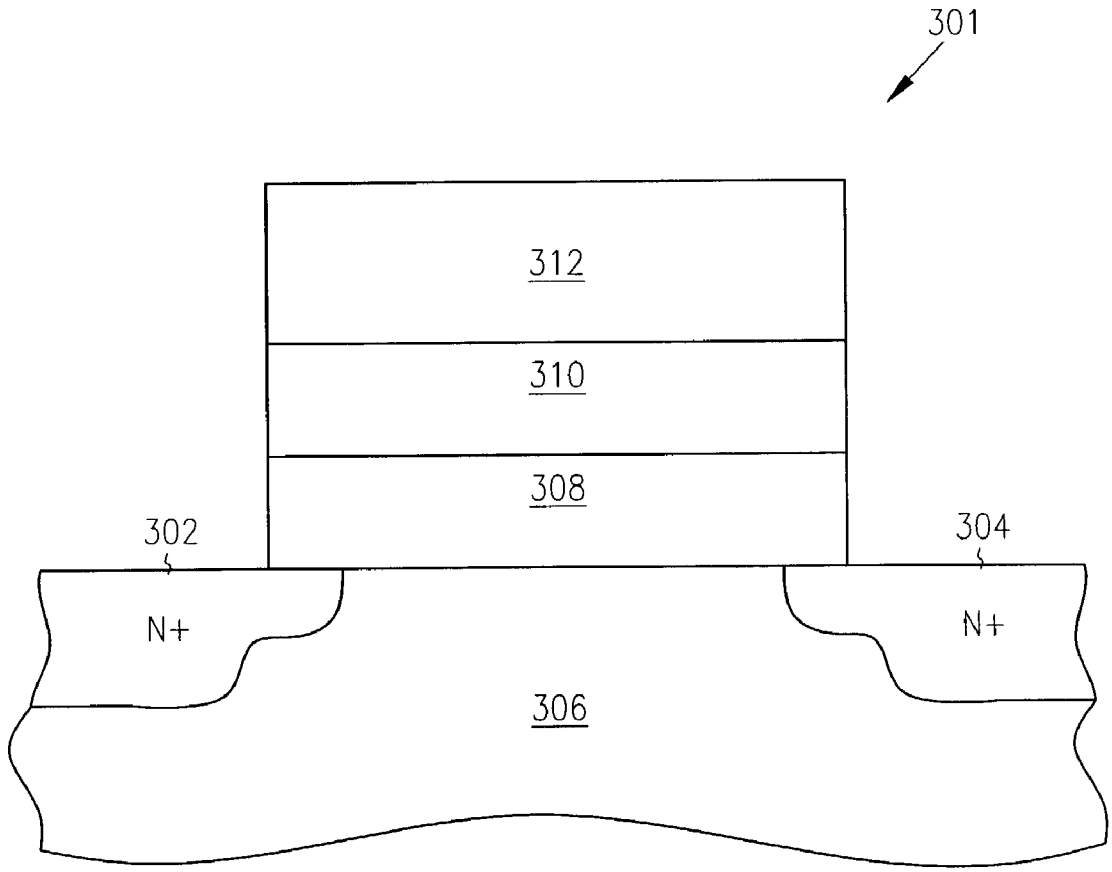


FIG. 3

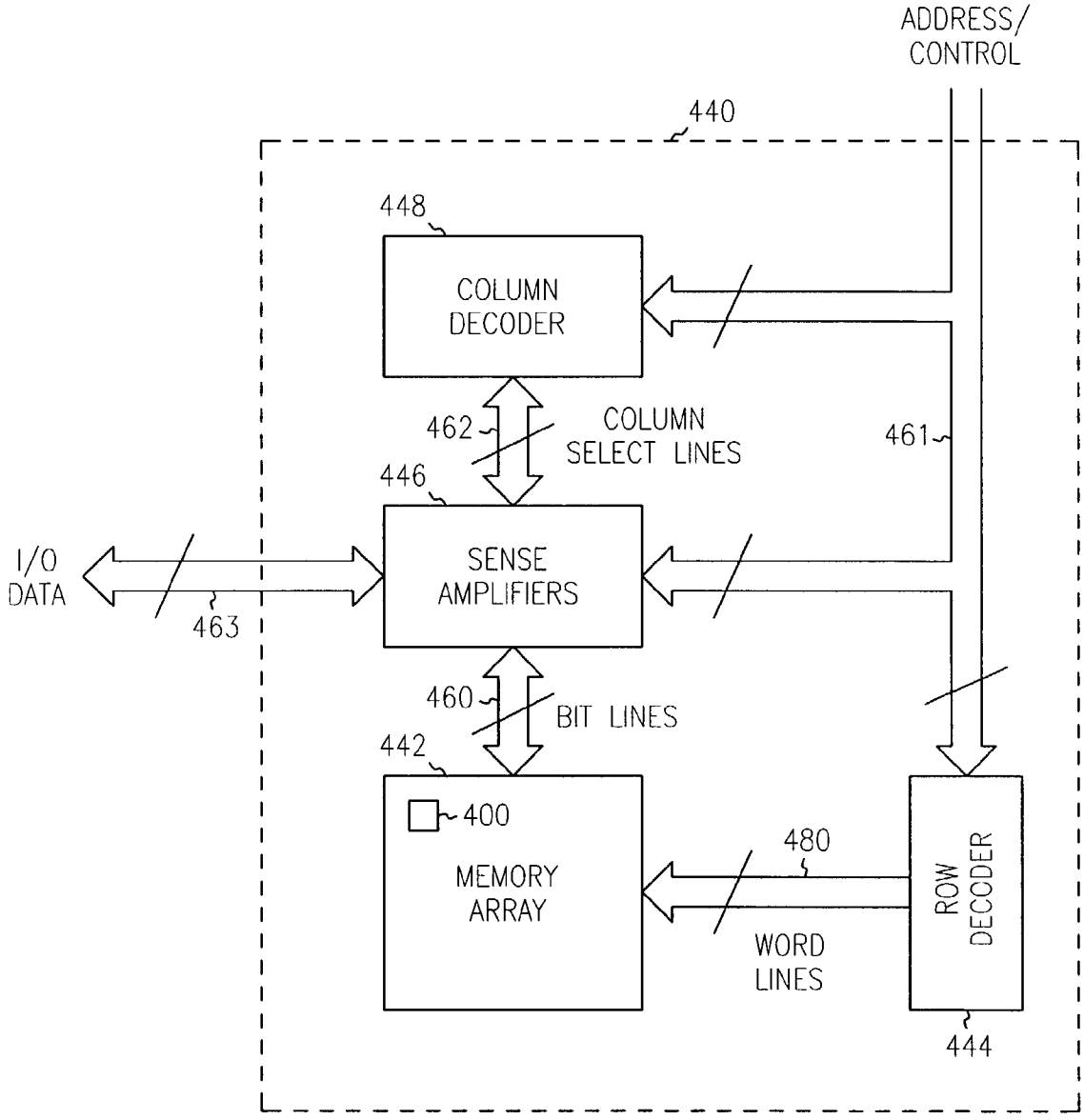

ADDRESS/
CONTROL
440
448
COLUMN
DECODER
462
COLUMN
SELECT LINES
461
446
I/O
DATA
SENSE
AMPLIFIERS
463
460
BIT LINES
442
400
MEMORY
ARRAY
480
WORD
LINES
ROW
DECODER
444

FIG. 4

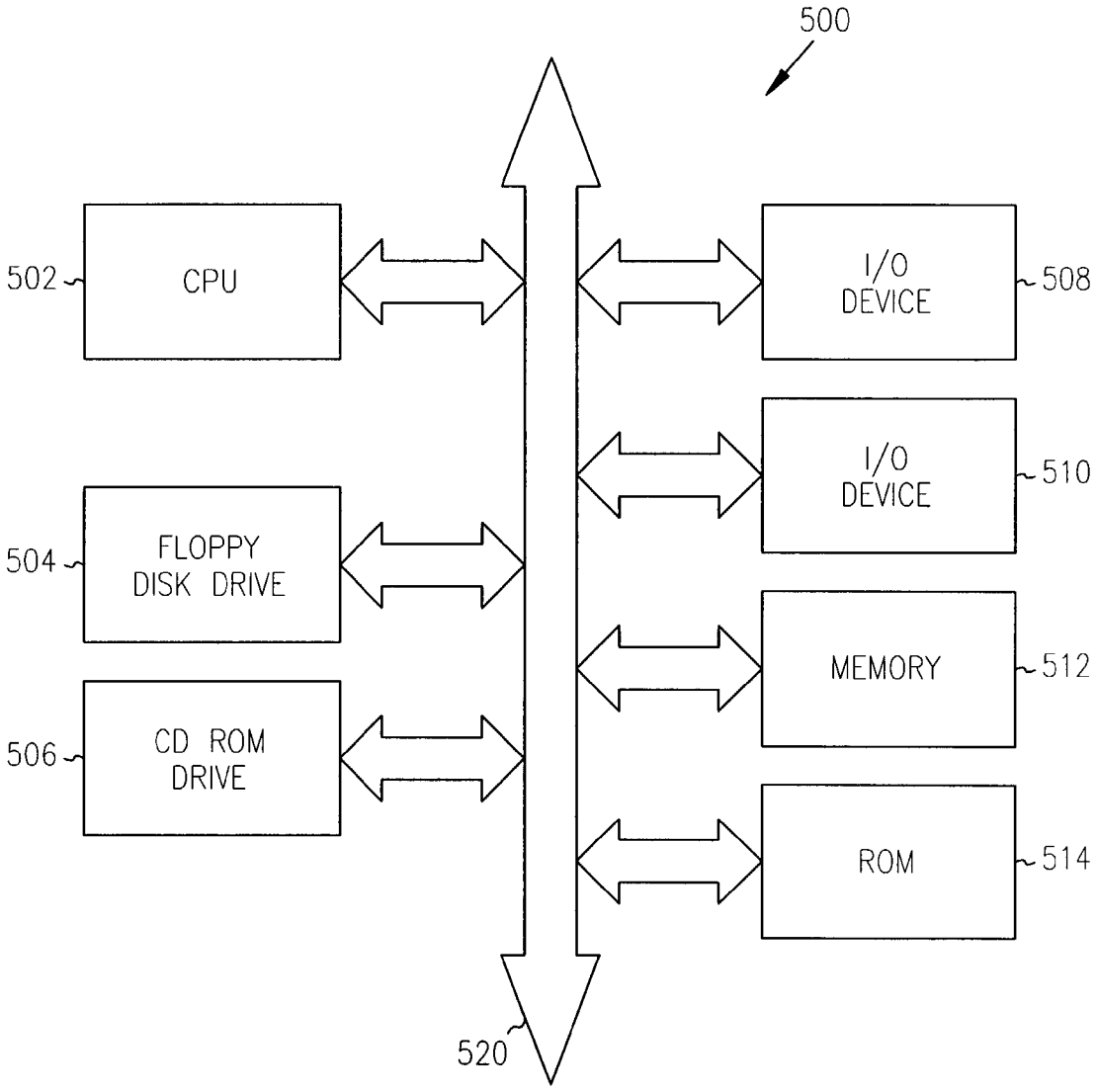

500
502
CPU
504
FLOPPY DISK DRIVE
506
CD ROM DRIVE
I/O DEVICE
508
I/O DEVICE
510
MEMORY
512
ROM
514
520

FIG. 5

ATOMIC LAYER DEPOSITION OF CMOS GATES WITH VARIABLE WORK FUNCTIONS

FIELD OF THE INVENTION

[0001] The present invention relates generally to semiconductor integrated circuits and, more particularly, to atomic layer deposition of CMOS gates with variable work functions.

BACKGROUND OF THE INVENTION

[0002] Conventional n-type doped polysilicon gate electrodes in CMOS technology have two problems. Firstly, the polysilicon is conductive but there can still be a surface region which can be depleted of carriers under bias conditions. This appears as an extra gate insulator thickness and is commonly referred to as gate depletion and contributes to the equivalent oxide thickness. While this region is thin, in the order of a few angstroms (Å), it becomes appreciable as gate oxide thicknesses are reduced below 2 nm or 20 Å. Another problem is that the work function is not optimum for both n-MOS and p-MOS devices, historically this was compensated for by threshold voltage adjustment implantations. However, as the devices become smaller, with channel lengths of less than 1000 Å and consequently surface space charge regions of less than 100 Å, it becomes more and more difficult to do these implantations. Threshold voltage control becomes an important consideration as power supplies are reduced to the range of one volt. Optimum threshold voltages for both PMOS and NMOS transistors need to have a magnitude of around 0.3 Volts.

[0003] A solution to the polysilicon gate depletion problem is to replace the semiconducting gate material with a metal or highly conductive metallic nitrides. (See generally; Y. Yee-Chia et al., "Dual-metal gate CMOS technology with ultrathin silicon nitride gate dielectric IEEE Electron Device Letters, Volume: 22 Issue: 5, May, 2001, pp. 227229; L Qiang, Y. Yee Chia, et al., "Dual-metal gate technology for deep-submicron CMOS transistors," VLSI Technology, 2000; Digest of Technical Papers. 2000 Symposium on, 2000, pp. 72-73.; and H. Wakabayashi et al., "A dual-metal gate CMOS technology using nitrogen-concentration-controlled TiNx film," Electron Devices, IEEE Transactions on, Volume: 48 Issue: 10, October 2001, Page(s): 2363-2369.).

[0004] As with any new circuit material, the gate electrode must be chemically and thermally compatible with both the transistor and the process. Different metals can be employed or the properties of the conductive nitride modified to provide an optimum work function. (See generally; above cited reference).

[0005] The work function of the gate electrode—the energy needed to extract an electron—must be compatible with the barrier height of the semiconductor material. For PMOS transistors, the required work function is about 5.0 eV. Achieving the lower work function needed by NMOS transistors, about 4.1 eV, has been more difficult. **FIGS. 1A and 1B** illustrate the desired energy band diagrams and work functions for NMOS and PMOS transistors respectively. Refractory metals like titanium (Ti) and tantalum (Ta) oxidize rapidly under typical process conditions. One proposed solution to the problem relies on a "tuned" ruthenium—tantalum (Ru—Ta) alloy, which is stable under process conditions. When the Ta concentration is below 20 percent, the alloy's electrical properties resemble Rhubidium (Ru), a good PMOS gate electrode. When the Ta concentration is between 40 percent and 54 percent, the alloy is a good NMOS gate electrode. (See generally; H. Zhong et al., "Properties of Ru—Ta Alloys as gate electrodes for NMOS and PMOS silicon devices," Digest of IEEE Int. Electron Devices Meeting, Washington D.C., 2001, paper 20.05; V. Misra, H. Zhong et al., "Electrical properties of Ru-based alloy gate electrodes for dual metal gate Si-CMOS," IEEE Electron Device Letters, Volume: 23 Issue: 6, June 2002 Page(s): 354-356; and H. Zhong et al., "Electrical properties of RuO/sub 2/gate electrodes for dual metal gate Si-CMOS," IEEE Electron Device Letters, Volume: 21 Issue: 12, December 2000 Page(s): 593-595).

[0006] Promising candidates include metallic nitrides, such as tantalum nitride (TaN) and titanium nitride (TiN). Tantalum nitride, titanium nitride, and tungsten nitride are mid-gap work function metallic conductors commonly described for use in CMOS devices. (See generally, H. Shimada et al., "Low resistivity bcc-Ta/TaN/sub x/metal gate MNSFETs having plane gate structure featuring fully low-temperature processing below 450 degrees C.," 2001 Symposium on VLSI Technology, Jun. 12-14 2001, Kyoto, Japan Page: 67-68; H. Shimada et al., "Tantalum nitride metal gate FD-SOI CMOS FETs using low resistivity self-grown bcc-tantalum, layer," IEEE Trans. on Electron Devices, vol. 48, no. 8, pp. 1619-26, August 2001; B. Claflin et al., "Investigation of the growth and chemical stability of composite metal gates on ultra-thin gate dielectrics," MRS Symposium on Silicon Front-End Technology-Materials Processing and Modelling, Apr. 13-15 1998, San Francisco, Calif., Page: 171-176; A. Yagishita et al., "Dynamic threshold voltage damascene metal gate MOSFET(DT-DMG-MOS) with low threshold voltage, high drive current and uniform electrical characteristics," Digest Technical Papers Int. Electron Devices Meeting, San Francisco, December 2000, pp. 663-6; B. Claflin et al., "Investigation of the growth and chemical stability of composite metal gates on ultra-thin gate dielectrics," MRS Symposium on Silicon Front-End Technology-Materials Processing and Modelling, Apr. 13-15 1998, San Francisco, Calif., Page: 171-176; and M. Moriwaki et al., "Improved metal gate process by simultaneous gate-oxide nitridation during W/WN/sub x/gate formation," Jpn. J. Appl. Phys., vol. 39. No. 4B, pp. 2177-80, 2000). The use of a mid-gap work function makes the threshold voltages of NMOS and PMOS devices symmetrical in that the magnitudes of the threshold voltages will be the same, but both will have a magnitude larger than that which is optimum with low power supply voltages.

[0007] Recently physical deposition, evaporation, has been used to investigate the suitability of some ternary metallic nitrides for use as gate electrodes, these included TiAlN and TaSiN. (See generally, Dae-Gyu Park et al., "Robust ternary metal gate electrodes for dual gate CMOS devices," Electron Devices Meeting, 2001. IEDM Technical Digest. International, 2001 Page(s): 30.6.1-30.6.4). However, these were deposited by physical deposition not atomic layer deposition and only capacitor structures were fabricated, not transistors with gate structures.

[0008] Thus, there is an ongoing need for improved CMOS transistor design.

SUMMARY OF THE INVENTION

[0009] The above mentioned problems CMOS transistor design as well as other problems are addressed by the present invention and will be understood by reading and studying the following specification. This disclosure describes the use of atomic layer deposition of ternary metallic conductors where the composition and work function are varied to control the threshold voltage of both the NMOS and PMOS transistors in CMOS technology to provide optimum performance.

[0010] In particular, an embodiment of the present invention includes a transistor having a source region a drain region and a channel therebetween. A gate is separated from the channel region by a gate insulator. The gate includes a ternary metallic conductor formed by atomic layer deposition. In one embodiment the ternary metallic conductor includes Tantalum Aluminum Nitride (TaAlN). In one embodiment the ternary metallic conductor includes Titanium Aluminum Nitride (TiAlN). In one embodiment the ternary metallic conductor includes Titanium Silicon Nitride (TiSiN). In one embodiment the ternary metallic conductor includes Tungsten Aluminum Nitride (WAlN). In some embodiments the gate further includes a refractory metal formed on the ternary metallic conductor.

[0011] These and other embodiments, aspects, advantages, and features of the present invention will be set forth in part in the description which follows, and in part will become apparent to those skilled in the art by reference to the following description of the invention and referenced drawings or by practice of the invention. The aspects, advantages, and features of the invention are realized and attained by means of the instrumentalities, procedures, and combinations particularly pointed out in the appended claims.

BRIEF DESCRIPTION OF THE DRAWINGS

[0012] **FIGS. 1A and 1B** illustrate the desired energy band diagrams and work functions for NMOS and PMOS transistors respectively.

[0013] **FIG. 2** is a graph which plots electron affinity versus the energy bandgap for various metallic nitrides employed in various embodiments of the present invention.

[0014] **FIG. 3** illustrates an embodiment of a transistor structure formed according to the teachings of the present invention.

[0015] **FIG. 4** illustrates an embodiment of a memory device, utilizing ternary metallic gates formed by atomic layer deposition, according to embodiments of the present invention.

[0016] **FIG. 5** is a block diagram of an electrical system, or processor-based system, utilizing ternary metallic gates formed by atomic layer deposition, according to embodiments of the present invention.

DETAILED DESCRIPTION

[0017] In the following detailed description of the invention, reference is made to the accompanying drawings which form a part hereof, and in which is shown, by way of illustration, specific embodiments in which the invention may be practiced. In the drawings, like numerals describe substantially similar components throughout the several views. These embodiments are described in sufficient detail to enable those skilled in the art to practice the invention. Other embodiments may be utilized and structural, logical, and electrical changes may be made without departing from the scope of the present invention.

[0018] The terms wafer and substrate used in the following description include any structure having an exposed surface with which to form the integrated circuit (IC) structure of the invention. The term substrate is understood to include semiconductor wafers. The term substrate is also used to refer to semiconductor structures during processing, and may include other layers that have been fabricated thereupon. Both wafer and substrate include doped and undoped semiconductors, epitaxial semiconductor layers supported by a base semiconductor or insulator, as well as other semiconductor structures well known to one skilled in the art. The term conductor is understood to include semiconductors, and the term insulator is defined to include any material that is less electrically conductive than the materials referred to as conductors. The following detailed description is, therefore, not to be taken in a limiting sense, and the scope of the present invention is defined only by the appended claims, along with the full scope of equivalents to which such claims are entitled.

[0019] This disclosure describes the use of atomic layer deposition of ternary metallic conductors where the composition is varied and work function varied, see **FIG. 2**, to control the threshold voltage of both the NMOS and PMOS transistors in CMOS technology to provide optimum performance. In the several embodiments, these include the use of:

[0020] (i) TaAlN;

[0021] (ii) TiAlN;

[0022] (iii) TiSiN; and

[0023] (iv) WAlN

[0024] As the ternary metallic conductors. Conventional highly doped polysilicon or refractory metals as W, Ta, Ti are deposited over the metallic conductors to give the gate structure shown in **FIG. 3**. As shown in **FIG. 3**, the transistor **301** structure includes a source region **302**, a drain region **304**, and a channel **306** therebetween. A gate **310** is separated from the channel region by a gate insulator **308**. According to the teachings of the present invention, the gate **310** includes a ternary metallic conductor formed by atomic layer deposition. In one embodiment the ternary metallic conductor includes Tantalum Aluminum Nitride (TaAlN). In one embodiment the ternary metallic conductor includes Titanium Aluminum Nitride (TiAlN). In one embodiment the ternary metallic conductor includes Titanium Silicon Nitride (TiSiN). In one embodiment the ternary metallic conductor includes Tungsten Aluminum Nitride (WAlN). As shown in **FIG. 3**, in some embodiments the gate further includes a layer of highly conductive polysilicon **312**, or alternatively a refractory metal layer **312**, formed on the ternary metallic conductor **310**. In embodiments having a refractory metal layer, the layer **312** includes for example, and not by way of limitation, refractory metals such as tantalum, titanium and tungsten.

[0025] Methods of Formation

[0026] Atomic Layer Deposition developed in the early 70s is a modification of CVD and can also be called as "alternately pulsed-CVD". (See generally, Ofer Sneh et al., "Thin film atomic layer deposition equipment for semiconductor processing", Thin Solid Films, 402 (2002) 248-261). In this technique, gaseous precursors are introduced one at a time to the substrate surface, and between the pulses the reactor is purged with an inert gas or evacuated. In the first reaction step the precursor is saturatively chemisorbed at the substrate surface, and during the subsequent purging the precursor is removed from the reactor. In the second step, other precursor is introduced on the substrate and the desired films growth reaction takes place. After that the reaction byproducts and the precursor excess are purged out from the reactor. When the precursor chemistry is favorable, i.e. the precursor adsorb and react with each other aggressively, one ALD cycle can be preformed in less than one second in the properly designed flow type reactors.

[0027] The striking feature of ALD is the saturation of all the reaction and purging steps which makes the growth self-limiting. This brings the large area uniformity and conformality, the most important properties of ALD, as shown in very different cases, viz. planar substrates, deep trenches, and in the extreme cases of porous silicon and high surface area silica and alumina powers. Also the control of the film thickness is straightforward and can be made by simply calculating the growth cycles. ALD was originally developed to manufacture luminescent and dielectric films needed in electroluminescent displays, and a lot of effort has been put to the growth of doped zinc sulfide and alkaline earth metal sulfide films. Later ALD has been studied for the growth of different epitaxial II-V and II-VI films, nonepitaxial crystalline or amorphous oxide and nitride films are their multilayer structures.

[0028] There has been considerable interest towards the ALD growth of silicon and germanium films but due to the difficult precursor chemistry the results have not been very successful.

[0029] Reaction sequence ALD (RS-ALD) films have several unique and unmatched advantages:

[0030] Continuity at the interface avoiding poorly defined nucleating regions that are typical for CVD (<20 Å) and PVD (<50 Å) films. To achieve this continuity, the substrate surface must be activated to react directly with the first exposure of RS-ALD precursor.

[0031] Unmatched conformality over toughest substrate topologies with robust processes that can only be achieved with a layer-by-layer deposition technique.

[0032] Typically, low temperature and mildly oxidizing processes. This is thought to be a major advantage for gate insulator processing where deposition of non-silicon based dielectrics without oxidizing the substrate (with the oxidation-precursor) is a major concern.

[0033] RS-ALD ability to engineer multilayer laminate films, possibly down to monolayer resolution, as well as alloy composite films appear to be unique. This ability comes from the combination of being able to control deposition with monolayer precision and the ability to deposit continuous monolayers of amorphous films (that is unique to RS-ALD).

[0034] Unprecedented process robustness. RS-ALD processes are free of first wafer effects and the chamber dependence. Accordingly, RS-ALD processes will be easier to transfer from development to production and from 200 to 300 mm wafer size.

[0035] Thickness depends solely on the number of cycles. Thickness can be "dialed in" as a simple recipe change bearing no need for additional process development upon technology generation advance.

[0036] (See generally, Shunsuke Morishita et al., "Atomic-Layer Chemical-Vapor-Deposition of SiO_2 by Cyclic Exposure of $CHOSi(NCO)_3$ and H_2O_2," Jpn. J. Appl. Phys. Vol. 34 (1955) pp. 5738-5742.).

[0037] Atomic Layer Deposition of Nitrides

[0038] Ta—N: Plasma-enhanced atomic layer deposition (PEALD) of tantalum nitride (Ta—N) thin films at a deposition temperature of 260° C. using hydrogen radicals as a reducing agent for Tertbutylimidotris(diethylamido) tantalum have been described. (See generally, Jin-Seong Park et al, "Plasma-Enhanced Atomic Layer Deposition of Tantalum Nitrides Using Hydrogen Radicals as a Reducing Agent", *Electrochemical and Solid-State Lett.*, 4(4) C17-C19, 2001). The PEALD yields superior Ta—N films with an electric resistivity of 400 $\mu\Omega$cm and no aging effect under exposure to air. The film density is higher than that of Ta—N films formed by typical ALD, in which NH_3 is used instead of hydrogen radicals. In addition, the as-deposited films are not amorphous, but rather polycrystalline structure of cubit TaN. The density and crystallinity of the films increases with the pulse time of hydrogen plasma. The films are Ta-rich in composition and contain around 15 atomic % of carbon impurity. In the PEALD of Ta—N films, hydrogen radicals are used a reducing agent instead of NH_3, which is used as a reactant gas in typical Ta—N ALD. Films are deposited on SiO_2 (100 nm)/Si wafers at a deposition temperature of 260° C. and a deposition pressure of 133 Pa in a cold-walled reactor using $(Net_2)_3$ $Ta{=}Nbu_t$ [tertbutylimidotris(diethylamido)tantalum, TBTDET] as a precursor of Ta. The liquid precursor is contained in a bubbler heated at 70° C. and carried by 35 sccm argon. One deposition cycle consist of an exposure to a metallorganic precursor of TBTDET, a purge period with Ar, and an exposure to hydrogen plasma, followed by another purge period with Ar. The Ar purge period of 15 seconds instead between each reactant gas pulse isolates the reactant gases from each other. To ignite and maintain the hydrogen plasma synchronized with the deposition cycle, a rectangular shaped electrical power is applied between the upper and lower electrode. The showerhead for uniform distribution of the reactant gases in the reactor, capacitively coupled with an rf (13.56 MHz) plasma source operated at a power of 100 W, is used as the upper electrode. The lower electrode, on which a wafer resides, is grounded. Film thickness and morphology were analyzed by field emission scanning electron microscopy.

[0039] Ta (Al)N(C): Technical work on thin films have been studied using $TaCl_5$ or $TaBr_5$ and NH_3 as precursors and $Al(CH_3)_3$ as an additional reducing agent. (See gener-

ally, Petra Alen et al., "Atomic Layer Deposition of Ta (Al) N (C) Thin Films Using Trimethylaluminum as a Reducing Agent", *Jour, of the Electrochemical Society*, 148 (10), G566-G571 (2001)). The deposition temperature is varied between 250 and 400° C. The films contained aluminum, carbon, and chlorine impurities. The chlorine content decreased drastically as the deposition temperature is increased. The film deposited at 400° C. contained less than 4 atomic % chlorine and also had the lowest resistivity, 1300 $\mu\Omega$cm. Five different deposition processes with the pulsing orders $TaCl_5$—TMA—NH_3, TMA—$TaCl_5$—NH_3, $TaBr_5$—NH_3, $TaBr_5$—Zn—NH_3, and $TaBr_5$—TMA—NH_3 are used. $TaCl_5$, $TaBr_5$, and Zn are evaporated from open boats held inside the reactor. The evaporation temperatures for $TaCl_4$, $TaBr_5$, and Zn are 90, 140, 380° C., respectively. Ammonia is introduced into the reactor through a mass flowmeter, a needle valve, and a solenoid valve. The flow rate is adjusted to 14 sccm during a continuous flow. TMA is kept at a constant temperature of 16° C. and pulsed through the needle and solenoid valve. Pulse times are 0.5 s for $TaCl_5$, $TaBr_5$, NH_3, and Zn whereas the pulse length of TMA is varied between 0.2 and 0.8 s. The length of the purge pulse is always 0.3 s. Nitrogen gas is used for the transportation of the precursor and as a purging gas. The flow rate of nitrogen is 400 sccm.

[**0040**] TiN: Atomic layer deposition (ALD) of amorphous TiN films on SiO_2 between 170° C. and 210° C. has been achieved by the alternate supply of reactant sources, $Ti[N(C_2H_5CH_3)_2]_4$ [tetrakis(ethylmethylamino)titanium: TEMAT] and NH_3. These reactant sources are injected into the reactor in the following order: TEMAT vapor pulse, Ar gas pulse, NH_3 gas pulse and Ar gas pulse. Film thickness per cycle saturated at around 1.6 monolayers per cycle with sufficient pulse times of reactant sources at 200° C. The results suggest that film thickness per cycle could exceed 1 ML/cycle in ALD, and are explained by the rechemisorption mechanism of the reactant sources. An ideal linear relationship between number of cycles and film thickness is confirmed. (See generally, J. -S. Min et al., "Atomic layer deposition of TiN films by alternate supply on Tetrakis (ethylmethyllamino)-titanium and ammonia,"*Jpn. J. Appl. Phys*., Vol. 37, Part 1, No. 9A, pp. 4999-5004, Sept. 15 1998).

[**0041**] TiAlN: Koo et al published paper on the study of the characteristics of TiAlN thin film deposited by atomic layer deposition method. (See generally, Jaehyong Koo et al., "Study on the characteristics of TiAlN thin film deposited by atomic layer deposition method,"*J. Vac. Sci. Technol. A*, 19(6), 2831-2834 (2001)). The series of metal-Si—N barriers have high resistivity above 1000 $\mu\Omega$cm. They proposed another ternary diffusion barrier of TiAlN. TiAlN film exhibited a NaCl structure in spite of considerable Al contents. TiAlN films are deposited using the $TiCl_4$ and dimethylaluminum hydride ethypiperdine (DMAH-EPP) as the titanium and aluminum precursors, respectively. $TiCl_4$ is vaporized from the liquid at 13-15° C. and introduced into the ALD chamber, which is supplied by a bubbler using the Ar carrier gas with a flow rate of 30 sccm. The DMAH-EPP precursor is evaporated at 60° C. and introduced into the ALD chamber with the same flow rate of $TiCl_4$. The NH_3 gas is also used as a reactant gas and its flow rate is about 60 sccm. Ar purging gas is introduced for the complete separation of the source and reactant gases. TiAlN films are deposited at the temperatures between 350 and 400° C. and total pressure is kept constant to be two torr.

[**0042**] TiSiN: Metal-organic atomic-layer deposition (MOALD) achieves near-perfect step coverage step and control precisely the thickness and composition of grown thin films. A MOALD technique for ternary Ti—Si—N films using a sequential supply of $Ti[N(CH_3)_2]_4$ [tetrakis (dimethylamido) titanium: TDMAT], silane (SiH_4), and ammonia (NH_3), has been developed and evaluated the Cu diffusion barrier characteristics of a 10 nm Ti—Si—N film with high-frequency C—V measurements. (See generally, Jae-Sik Min et al, "Metal-organic atomic-layer deposition of titanium-silicon-nitride films", *Appl. Phys, Lett*., Vol. 75, No. 11, 1521-1523 (1999)). At 180° C. deposition temperature, silane is supplied separately in the sequence of the TDMAT pulse, silane pulse, and the ammonia pulse. The silicon content is the deposited films and the deposition thickness per cycle remained almost constant at 18 at. % and 0.22 nm/cycle, even though the silane partial pressure varied from 0.27 to 13.3 Pa. Especially, the Si content dependence is strikingly different from the conventional chemical-vapor deposition. Step coverage is approximately 100% even on the 0.3 μm diameter hole with slightly negative slope and 10:1 aspect ratio.

[**0043**] WN: Tungsten nitride films have been deposited with the atomic layer control using sequential surface reactions. The tungsten nitride film growth is accomplished by separating the binary reaction $2WF_6+NH_3 \rightarrow W_2N+3HF+9/2\ F_2$ into two half-reactions. (See generally, J. W. Kraus et al, "Atomic Layer Deposition of Tungsten Nitride Films Using Sequential Surface Reactions", 147 (3) 1175-1181 (2000)). Successive application of the WF_6 and NH_3 half-reactions in an ABAB . . . sequence produced tungsten nitride deposition at substrate temperatures between 600 and 800 K. Transmission Fourier transform infrared (FTIR) spectroscopy monitored the coverage of WF_x* and NH_y* surface species on high surface area particles during the WF_6 and NH_3 half-reactions. The FTIR spectroscope results demonstrated the WF_6 and NH_3 half-reactions are complete and self-limiting at temperatures >600 K. In situ spectroscopic ellipsometry monitored the film growth on Si(100) substrate vs. temperature and reactant exposure. A tungsten nitride deposition rate of 2.55 Å/AB cycle is measured at 600-800 K for WF_6 and NH_3 reactant exposure >3000 L and 10,000 L, respectively. X-ray photoelectron spectroscopy depth-profiling experiments determined that the films had a W_2N stoichiometry with low C and O impurity concentrations. X-ray diffraction investigations revealed that the tungsten nitride films are microcrystalline. Atomic force microscopy measurements of the deposited films observed remarkably flat surface indicating smooth film growth. These smooth tungsten nitride films deposited with atomic layer control should be used as diffusion control for Cu on contact and via holes.

[**0044**] AlN: Aluminum nitride (AlN) has been grown on porous silica by atomic layer chemical vapor deposition (ALCVD) from trimethylaluminum (TMA) and ammonia precursors. (See generally, R. L. Pruurunen et al, "Growth of aluminum nitride on porous silica by atomic layer chemical vapor deposition", *Applied Surface Science*, 165, 193-202 (2000)). The ALCVD growth is based on alternating, separated, saturating reactions of the gaseous precursors with the solid substrates. TMA and ammonia are reacted at 423 and

623 Kelvin (K), respectively, on silica which has been dehydroxylated at 1023 K pretreated with ammonia at 823 K. The growth in three reaction cycles is investigated quantitatively by elemental analysis, and the surface reaction products are identified by IR and solid state and Si NMR measurements. Steady growth of about 2 aluminum atoms/nm^2 silica/reaction cycle is obtained. The growth mainly took place through (I) the reaction of TMA which resulted in surface Al—Me and Si Me groups, and (II) the reaction of ammonia which replaced aluminium-bonded methyl groups with amino groups. Ammonia also reacted in part with the silicon-bonded methyl groups formed in the dissociated reaction of TMA with siloxane bridges. TMA reacted with the amino groups, as it did with surface silanol groups and siloxane bridges. In general, the Al—N layer interacted strongly with the silica substrates, but in the third reaction cycle AlN-type sites may have formed.

[0045] Devices

[0046] In **FIG. 4 a** memory device is illustrated according to the teachings of the present invention. The memory device **440** contains a memory array **442**, row and column decoders **444**, **448** and a sense amplifier circuit **446**. The memory array **442** consists of a number of transistor cells **400**, having ternary metallic gates formed by atomic layer deposition, whose word lines **480** and bit lines **460** are commonly arranged into rows and columns, respectively. The bit lines **460** of the memory array **442** are connected to the sense amplifier circuit **446**, while its word lines **480** are connected to the row decoder **444**. Address and control signals are input on address/control lines **461** into the memory device **440** and connected to the column decoder **448**, sense amplifier circuit **446** and row decoder **444** and are used to gain read and write access, among other things, to the memory array **442**.

[0047] The column decoder **448** is connected to the sense amplifier circuit **446** via control and column select signals on column select lines **462**. The sense amplifier circuit **446** receives input data destined for the memory array **442** and outputs data read from the memory array **442** over input/output (I/O) data lines **463**. Data is read from the cells of the memory array **442** by activating a word line **480** (via the row decoder **444**), which couples all of the memory cells corresponding to that word line to respective bit lines **460**, which define the columns of the array. One or more bit lines **460** are also activated. When a particular word line **480** and bit lines **460** are activated, the sense amplifier circuit **446** connected to a bit line column detects and amplifies the conduction sensed through a given transistor cell and transferred to its bit line **460** by measuring the potential difference between the activated bit line **460** and a reference line which may be an inactive bit line. Again, in the read operation the source region of a given cell is couple to a grounded sourceline or array plate (not shown). The operation of Memory device sense amplifiers is described, for example, in U.S. Pat. Nos. 5,627,785; 5,280,205; and 5,042,011, all assigned to Micron Technology Inc., and incorporated by reference herein.

[0048] **FIG. 5** is a block diagram of an electrical system, or processor-based system, **500** utilizing transistor cells having ternary metallic gates formed by atomic layer deposition according to the teachings of the present invention. For example, by way of example and not by way of limitation, memory **512** is constructed in accordance with the present invention to have transistor cells having ternary metallic gates formed by atomic layer deposition. However, the invention is not so limited and the same can apply to transistors in the CPU, etc. The processor-based system **500** may be a computer system, a process control system or any other system employing a processor and associated memory. The system **500** includes a central processing unit (CPU) **502**, e.g., a microprocessor, that communicates with the memory **512** and an I/O device **508** over a bus **520**. It must be noted that the bus **520** may be a series of buses and bridges commonly used in a processor-based system, but for convenience purposes only, the bus **520** has been illustrated as a single bus. A second I/O device **510** is illustrated, but is not necessary to practice the invention. The processor-based system **500** can also includes read-only memory (ROM) **514** and may include peripheral devices such as a floppy disk drive **504** and a compact disk (CD) ROM drive **506** that also communicates with the CPU **502** over the bus **520** as is well known in the art.

[0049] It will be appreciated by those skilled in the art that additional circuitry and control signals can be provided, and that the processor-based system **500** has been simplified to help focus on the invention.

[0050] It will be understood that the embodiment shown in **FIG. 5** illustrates an embodiment for electronic system circuitry in which the novel ternary metallic gate transistor cells, formed by atomic layer deposition, are used. The illustration of system **500**, as shown in **FIG. 5**, is intended to provide a general understanding of one application for the structure and circuitry of the present invention, and is not intended to serve as a complete description of all the elements and features of an electronic system using the novel ternary metallic gate transistor cells, formed by atomic layer deposition. Further, the invention is equally applicable to any size and type of system **500** using the novel ternary metallic gate transistor cells, formed by atomic layer deposition, and is not intended to be limited to that described above. As one of ordinary skill in the art will understand, such an electronic system can be fabricated in single-package processing units, or even on a single semiconductor chip, in order to reduce the communication time between the processor and the memory device.

[0051] Applications containing the novel ternary metallic gate transistor cells, formed by atomic layer deposition as described in this disclosure, include electronic systems for use in memory modules, device drivers, power modules, communication modems, processor modules, and application-specific modules, and may include multilayer, multichip modules. Such circuitry can further be a subcomponent of a variety of electronic systems, such as a clock, a television, a cell phone, a personal computer, an automobile, an industrial control system, an aircraft, and others.

CONCLUSION

[0052] This disclosure describes the use of atomic layer deposition of ternary metallic conductors as transistor gates. The composition is varied and work function varied to control the threshold voltage of both the NMOS and PMOS transistors in CMOS technology to provide optimum performance.

[0053] It is to be understood that the above description is intended to be illustrative, and not restrictive. Many other

embodiments will be apparent to those of skill in the art upon reviewing the above description. The scope of the invention should, therefore, be determined with reference to the appended claims, along with the full scope of equivalents to which such claims are entitled.

What is claimed is:

1. A transistor, comprising:

a first source/drain region

a second source/drain region

a channel region between the first and the second source/drain regions,

a gate separated from the channel region by a gate insulator, wherein the gate includes a ternary metallic conductor formed by atomic layer deposition.

2. The transistor of claim 1, wherein the ternary metallic conductor includes Tantalum Aluminum Nitride (TaAlN).

3. The transistor of claim 1, wherein the ternary metallic conductor includes Titanium Aluminum Nitride (TiAlN).

4. The transistor of claim 1, wherein the ternary metallic conductor includes Titanium Silicon Nitride (TiSiN).

5. The transistor of claim 1, wherein the ternary metallic conductor includes Tungsten Aluminum Nitride (WAlN).

6. The transistor of claim 1, wherein the gate further includes a refractory metal formed on the ternary metallic conductor.

7. A vertical multistate cell, comprising:

a vertical transistor extending outwardly from a substrate, the transistor having a source region, a drain region, a channel region between the source and the drain regions, and a gate separated from the channel region by a gate insulator, wherein the gate includes a ternary metallic conductor formed by atomic layer deposition;

a sourceline coupled to the source region; and

a transmission line coupled to the drain region.

8. The vertical multistate cell of claim 7, wherein the gate further includes a highly conductive polysilicon layer formed on the ternary metallic conductor.

9. The vertical multistate cell of claim 7, wherein the gate further includes a refractory metal formed on the ternary metallic conductor.

10. The vertical multistate cell of claim 9, wherein the refractory metal includes tungsten (W).

11. The vertical multistate cell of claim 9, wherein the refractory metal includes tantalum (Ta).

12. The vertical multistate cell of claim 9, wherein the refractory metal includes titanium (Ti).

13. A vertical multistate cell, comprising:

a vertical transistor extending outwardly from a substrate, the transistor having a source region, a drain region, a channel region between the source region and the drain region, a gate separated from the channel region by a gate oxide, wherein the gate includes a Tantalum Aluminum Nitride (TaAlN) layer;

a wordline coupled to the gate;

a sourceline formed in a trench adjacent to the vertical transistor, wherein the source region is coupled to the sourceline; and

a bit line coupled to the drain region.

14. The vertical multistate cell of claim 13, wherein the gate further includes a refractory metal formed on the Tantalum Aluminum Nitride (TaAlN) layer.

15. The vertical multistate cell of claim 13, wherein the refractory metal includes tantalum (Ta).

16. The vertical multistate cell of claim 13, wherein the Tantalum Aluminum Nitride (TaAlN) layer is formed by atomic layer deposition.

17. A vertical multistate cell, comprising:

a vertical transistor extending outwardly from a substrate, the transistor having a source region, a drain region, a channel region between the source region and the drain region, a gate separated from the channel region by a gate oxide, wherein the gate includes a Titanium Aluminum Nitride (TiAlN) layer;

a wordline coupled to the gate;

a sourceline formed in a trench adjacent to the vertical transistor, wherein the source region is coupled to the sourceline; and

a bit line coupled to the drain region.

18. The vertical multistate cell of claim 17, wherein the gate further includes a refractory metal formed on the Titanium Aluminum Nitride (TiAlN) layer.

19. The vertical multistate cell of claim 17, wherein the refractory metal includes titanium (Ti).

20. The vertical multistate cell of claim 13, wherein the Titanium Aluminum Nitride (TiAlN) layer is formed by atomic layer deposition.

21. A vertical multistate cell, comprising:

a vertical transistor extending outwardly from a substrate, the transistor having a source region, a drain region, a channel region between the source region and the drain region, a gate separated from the channel region by a gate oxide, wherein the gate includes a Titanium Silicon Nitride (TiSiN) layer;

a wordline coupled to the gate;

a sourceline formed in a trench adjacent to the vertical transistor, wherein the source region is coupled to the sourceline; and

a bit line coupled to the drain region.

22. The vertical multistate cell of claim 21, wherein the gate further includes a refractory metal formed on the Titanium Silicon Nitride (TiSiN) layer.

23. The vertical multistate cell of claim 21, wherein the refractory metal includes titanium (Ti).

24. The vertical multistate cell of claim 21, wherein the Titanium Silicon Nitride (TiSiN) layer is formed by atomic layer deposition.

25. A vertical multistate cell, comprising:

a vertical transistor extending outwardly from a substrate, the transistor having a source region, a drain region, a channel region between the source region and the drain region, a gate separated from the channel region by a gate oxide, wherein the gate includes a Tungsten Aluminum Nitride (WAlN) layer;

a wordline coupled to the gate;

a sourceline formed in a trench adjacent to the vertical transistor, wherein the source region is coupled to the sourceline; and

a bit line coupled to the drain region.

26. The vertical multistate cell of claim 25, wherein the gate further includes a refractory metal formed on the Tungsten Aluminum Nitride (WAlN) layer.

27. The vertical multistate cell of claim 25, wherein the refractory metal includes tungsten (W).

28. The vertical multistate cell of claim 25, wherein the Tungsten Aluminum Nitride (WAlN) layer is formed by atomic layer deposition.

29. A transistor array, comprising:

a number of transistor cells formed on a substrate, wherein each transistor cell includes a source region, a drain region, a channel region between the source and the drain regions, and a gate separated from the channel region by a gate insulator, wherein the gate includes a ternary metallic conductor formed by atomic layer deposition;

a number of bit lines coupled to the drain region of each transistor cell along rows of the transistor array;

a number of word lines coupled to the gate of each transistor cell along columns of the memory array; and

a number of sourcelines, wherein the source region of each transistor cell is coupled to the number of sourcelines along rows of the transistor cells.

30. The transistor array of claim 29, wherein the ternary metallic conductor includes Tantalum Aluminum Nitride (TaAlN).

31. The transistor array of claim 29, wherein the ternary metallic conductor includes Titanium Aluminum Nitride (TiAlN).

32. The transistor array of claim 29, wherein the ternary metallic conductor includes Titanium Silicon Nitride (TiSiN).

33. The transistor array of claim 29, wherein the ternary metallic conductor includes Tungsten Aluminum Nitride (WAlN).

34. The transistor array of claim 29, wherein the gate further includes a refractory metal formed on the ternary metallic conductor.

35. A semiconductor device, comprising:

a memory array, wherein the memory array includes a number of vertical pillars formed in rows and columns extending outwardly from a substrate and separated by a number of trenches, wherein the number of vertical pillars serve as transistors including a source region, a drain region, a channel region between the source and the drain regions, and a gate separated from the channel region by a gate insulator, wherein the gate includes a ternary metallic conductor formed by atomic layer deposition;

a number of bit lines coupled to the drain region of each transistor along rows of the memory array;

a number of word lines coupled to the gate of each transistor along columns of the memory array;

a number of sourcelines formed in a bottom of the trenches between rows of the pillars and coupled to the source regions of each transistor along rows of pillars, wherein along columns of the pillars the source region of each transistor in column adjacent pillars couple to the sourceline in a shared trench;

a wordline address decoder coupled to the number of wordlines;

a bitline address decoder coupled to the number of bitlines; and

a sense amplifier coupled to the number of bitlines.

36. The semiconductor device of claim 35, wherein the number of sourcelines formed in a bottom of the trenches between rows of the pillars include a doped region implanted in the bottom of the trench.

37. The semiconductor device of claim 35, wherein the ternary metallic conductor includes Tantalum Aluminum Nitride (TaAlN).

38. The semiconductor device of claim 35, wherein the ternary metallic conductor includes Titanium Aluminum Nitride (TiAlN).

39. The semiconductor device of claim 35, wherein the ternary metallic conductor includes Titanium Silicon Nitride (TiSiN).

40. The semiconductor device of claim 35, wherein the ternary metallic conductor includes Tungsten Aluminum Nitride (WAlN).

41. The semiconductor device of claim 35, wherein the gate further includes a refractory metal formed on the ternary metallic conductor.

42. An electronic system, comprising:

a processor; and

a memory device coupled to the processor, wherein the memory device includes;

a memory array, wherein the memory array includes a number of transistor cells formed on a substrate, wherein each transistor cell includes a source region, a drain region, a channel region between the source and the drain regions, and a gate separated from the channel region by a gate insulator, wherein the gate includes a ternary metallic conductor formed by atomic layer deposition;

a number of bit lines coupled to the drain region of each transistor cell along rows of the transistor array;

a number of word lines coupled to the gate of each transistor cell along columns of the memory array; and

a number of sourcelines, wherein the source region of each transistor cell is coupled to the number of sourcelines along rows of the transistor cells.

43. The electronic system of claim 42, wherein the ternary metallic conductor includes Tantalum Aluminum Nitride (TaAlN).

44. The electronic system of claim 42, wherein the ternary metallic conductor includes Titanium Aluminum Nitride (TiAlN).

45. The electronic system of claim 42, wherein the ternary metallic conductor includes Titanium Silicon Nitride (TiSiN).

46. The electronic system of claim 42, wherein the ternary metallic conductor includes Tungsten Aluminum Nitride (WAlN).

47. The electronic system of claim 42, wherein the gate further includes a refractory metal formed on the ternary metallic conductor.

48. A method for forming a transistor, comprising:

forming a first source/drain region, a second source/drain region, and a channel region therebetween in a substrate;

forming a gate opposing the channel region and separated therefrom by a first gate insulator; and

wherein forming the gate includes forming a ternary metallic conductor by atomic layer deposition.

49. The method of claim 48, wherein forming a ternary metallic conductor by atomic layer deposition includes forming a Tantalum Aluminum Nitride (TaAlN) layer.

50. The method of claim 48, wherein forming a ternary metallic conductor by atomic layer deposition includes forming a Titanium Aluminum Nitride (TiAlN) layer.

51. The method of claim 48, wherein forming a ternary metallic conductor by atomic layer deposition includes forming a Titanium Silicon Nitride (TiSiN) layer.

52. The method of claim 48, wherein forming a ternary metallic conductor by atomic layer deposition includes forming a Tungsten Aluminum Nitride (WAlN) layer.

53. The method of claim 48, wherein method further includes forming a refractory metal on the ternary metallic conductor.

54. A transistor pair, comprising:

a PMOS transistor;

an NMOS transistor;

wherein the NMOS and the PMOS transistor each include a source, a drain, a channel region therebetween, a gate separated from the channel region by a gate insulator; and

wherein the gates of the NMOS and the PMOS transistors include a varied composition and a varied work function to achieve a low threshold voltages of a same magnitude.

55. The transistor pair of claim 54, wherein the low threshold voltages of a same magnitude include a threshold voltage magnitude of less than 0.4 Volts.

56. The transistor pair of claim 54, wherein the low threshold voltages of a same magnitude include a threshold voltage magnitude of approximately 0.3 Volts.

57. The transistor pair of claim 54, wherein one of the gates of the NMOS and the PMOS transistors includes a binary metallic conductor and the other includes a ternary metallic conductor.

58. The transistor pair of claim 57, wherein the binary metallic conductor includes a binary metallic conductor selected from the group of tantalum nitride (TaN), titanium nitride (TiN), and tungsten nitride (WN).

59. A method for forming a transistor pair, comprising:

forming a PMOS transistor;

forming an NMOS transistor; and

wherein forming the NMOS and the PMOS transistors includes forming a varied gate composition having a varied work function on each respective transistor in order to control a threshold voltage for each respective transistor to a same magnitude.

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