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(54) **NONVOLATILE SEMICONDUCTOR MEMORY DEVICE AND METHOD FOR MANUFACTURING SAME**

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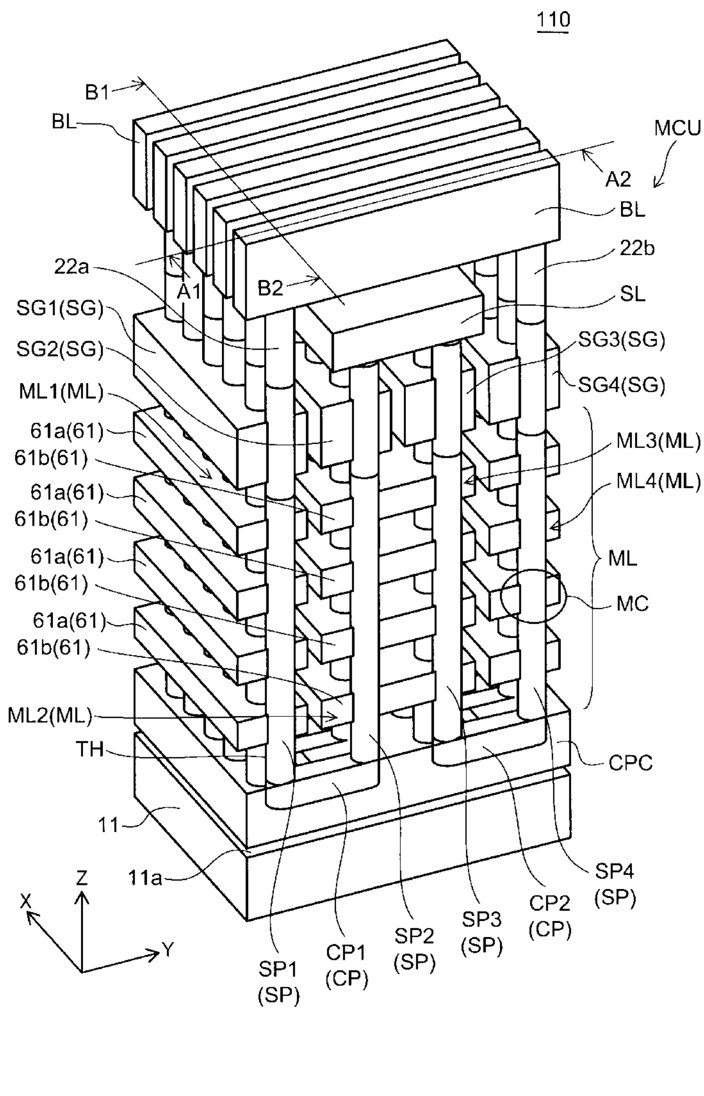
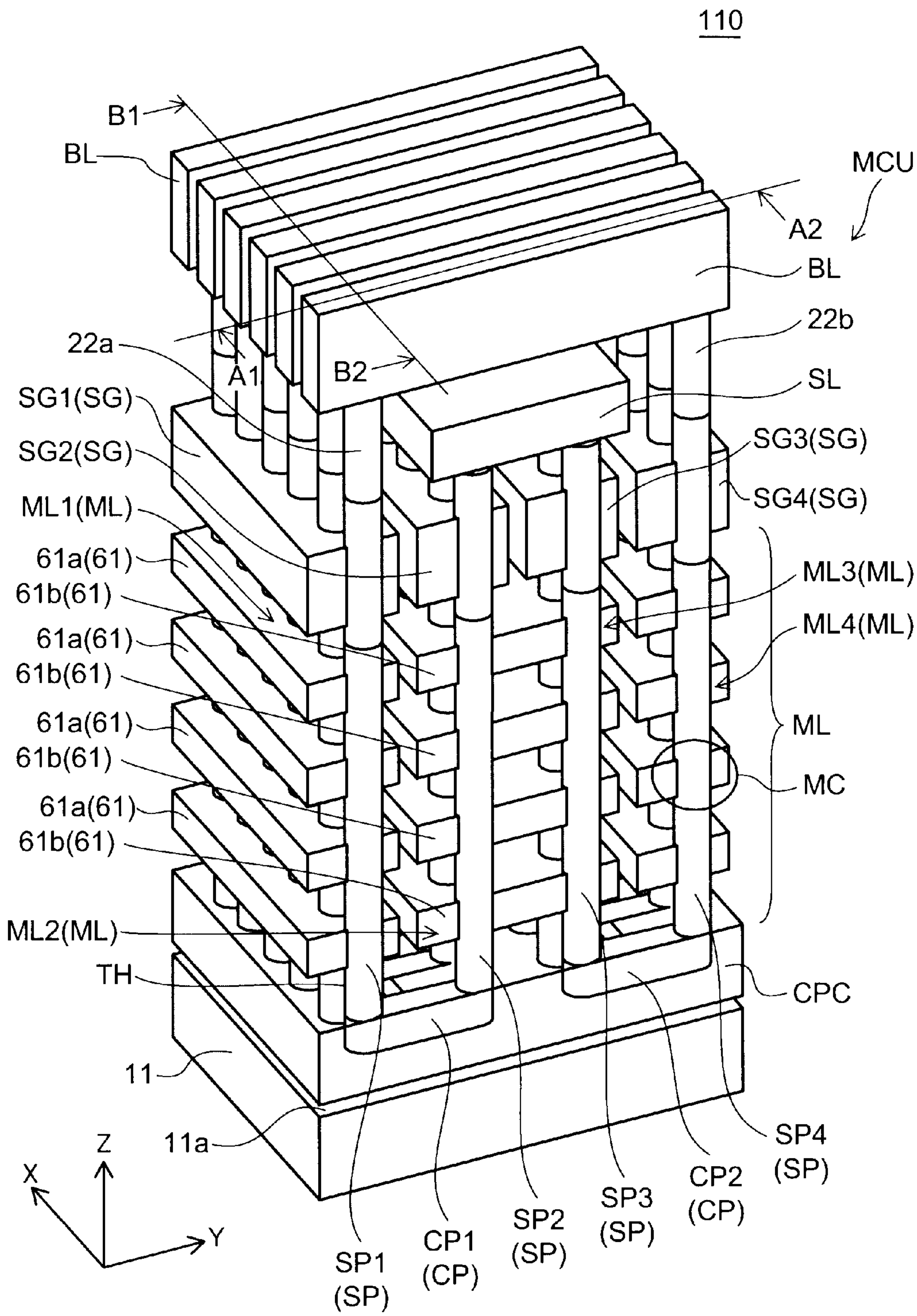
(52) **U.S. Cl.** **257/324**; 438/283; 257/E29.3; 257/E21.41

(57) **ABSTRACT**

According to one embodiment, a nonvolatile semiconductor memory device includes: first and second stacked bodies, first and second semiconductor pillars, a connection portion, a memory film, and a partitioning insulating layer. The stacked bodes include electrode films stacked along a first axis and an inter-electrode insulating film provided between the electrode films. Through-holes are provided in the stacked bodies. The semiconductor pillars are filled into the through-holes. The connection portion electrically connects the semiconductor pillars. The memory film is provided between the semiconductor pillars and the electrode films. The partitioning insulating layer partitions the first and second electrode films. A side surface of the first through-hole on the partitioning insulating layer side and a side surface of the second through-hole on the partitioning insulating layer side have a portion parallel to a plane orthogonal to a second axis from the first stacked body to the second stacked body.

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MCU
A2
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22a
A1
B2
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SG2(SG)
SG3(SG)
SG4(SG)
ML1(ML)
61a(61)
61b(61)
ML3(ML)
61a(61)
61b(61)
ML4(ML)
61a(61)
61b(61)
ML
MC
61a(61)
61b(61)
ML2(ML)
TH
CPC
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11a
Z
X
Y
SP1
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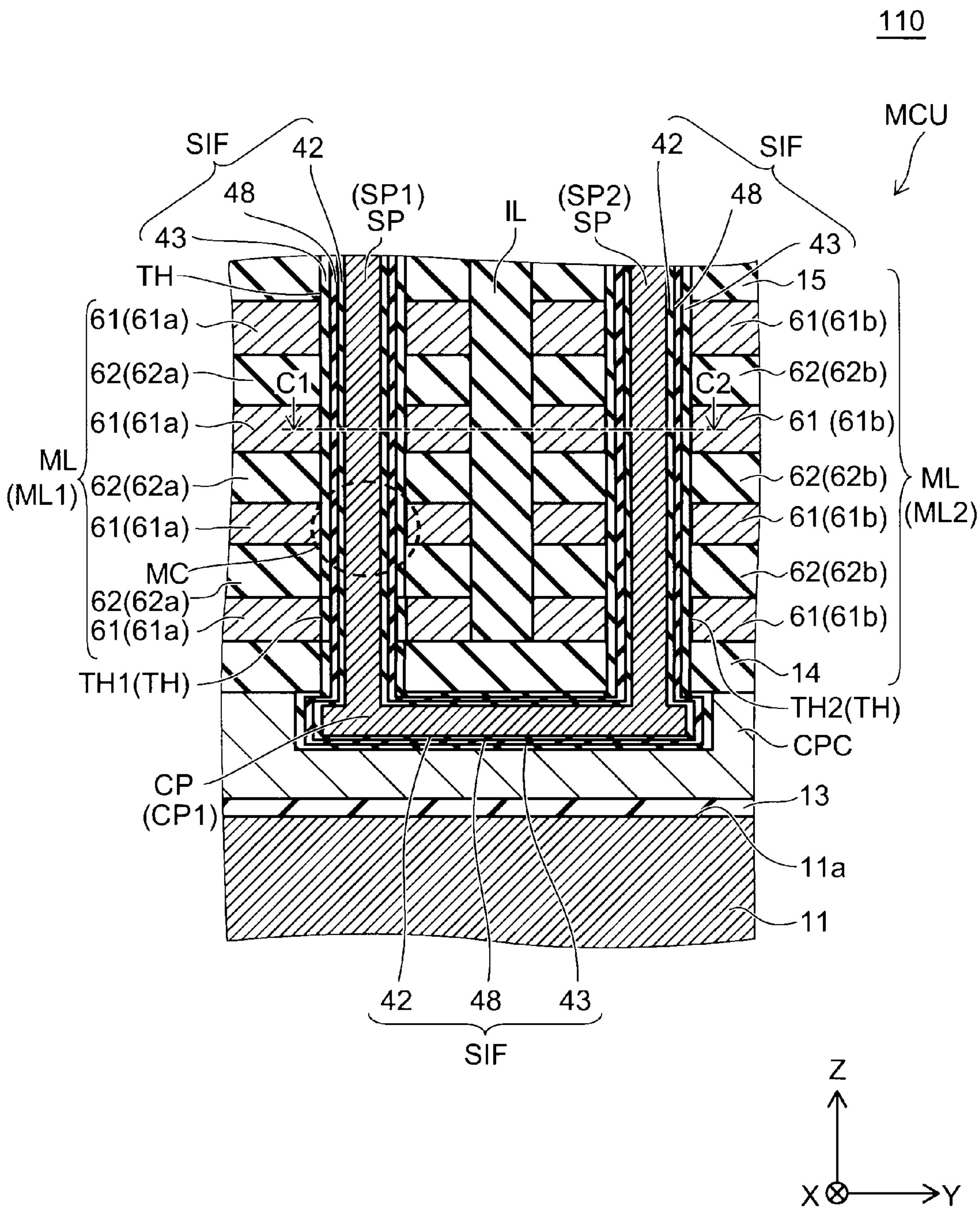
CP1
(CP)
SP2
(SP)
SP3
(SP)
CP2
(CP)
SP4
(SP)

FIG. 1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SP
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(SP2)
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C2
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TH1(TH)
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TH2(TH)
CPC
CP
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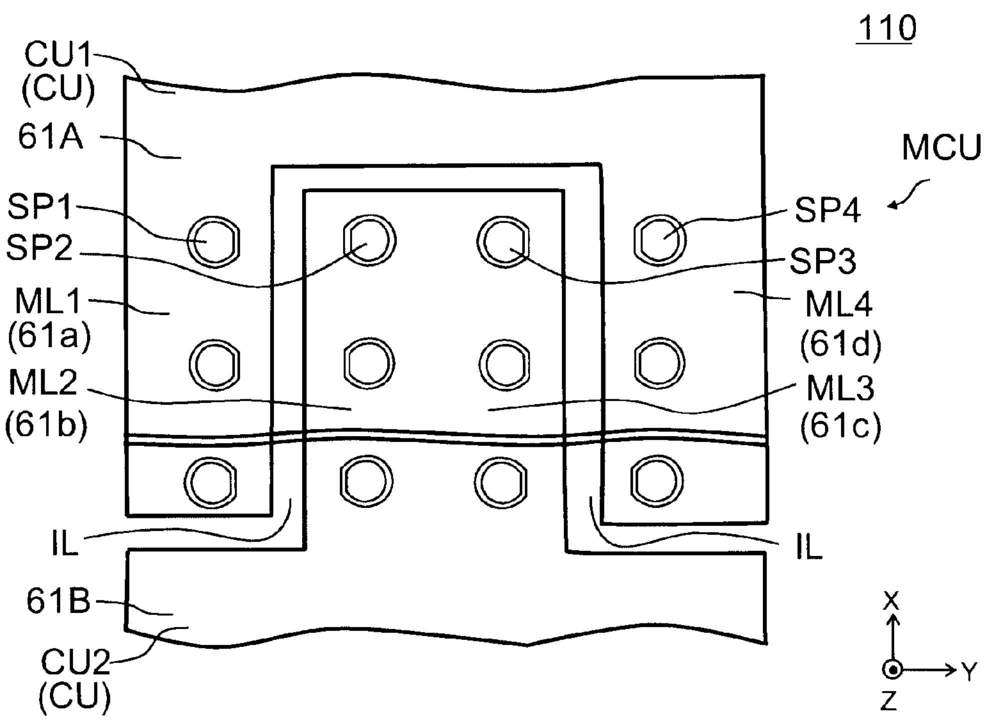
X
Y

FIG. 2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SP1
SP2
SP4
SP3
ML1
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ML4
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ML2
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ML3
(61c)
IL
IL
61B
CU2
(CU)
X
Y
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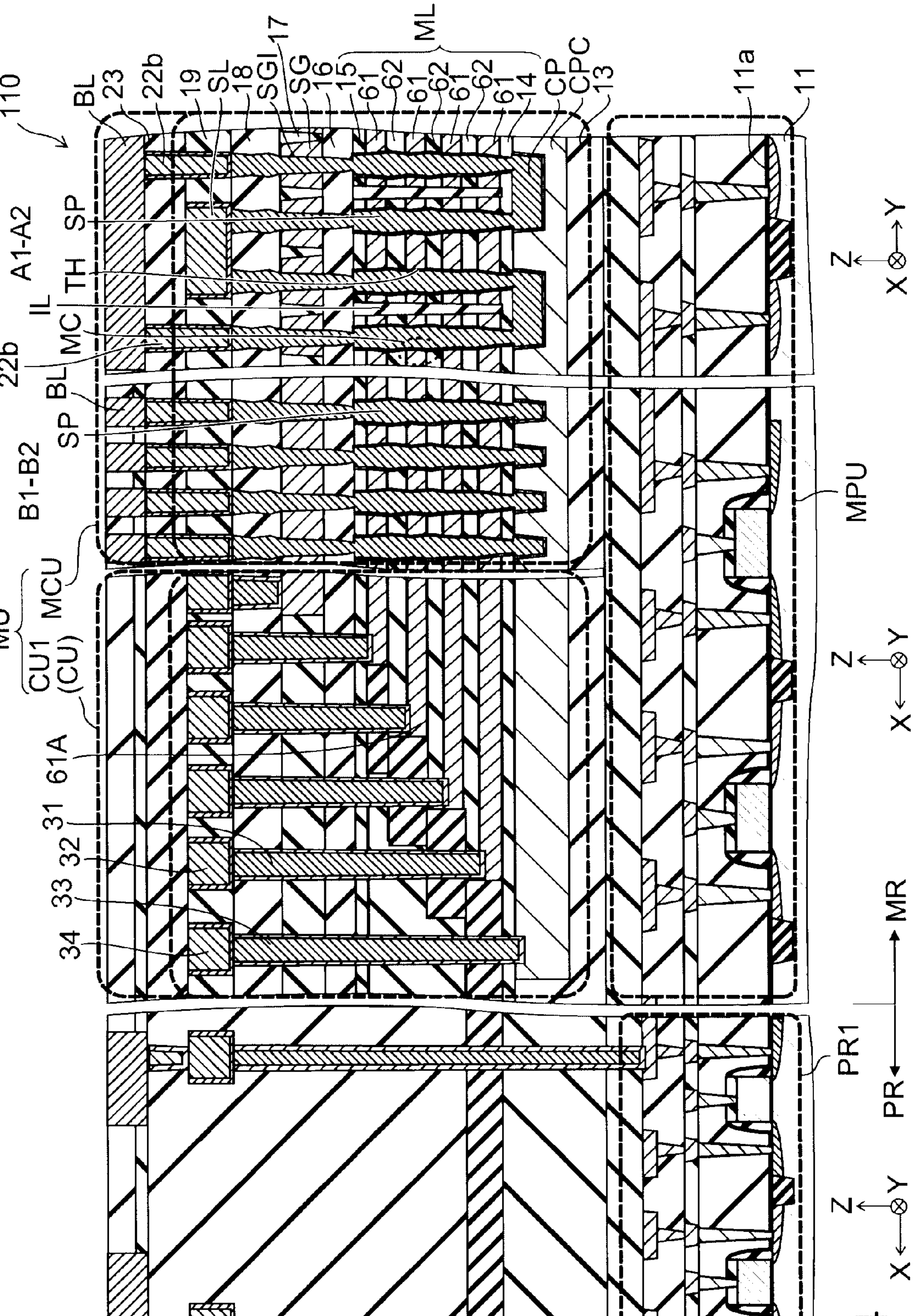
FIG. 3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ML
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CPC
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11a
11
A1-A2
SP
TH
IL
MC
22b
BL
SP
B1-B2
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34
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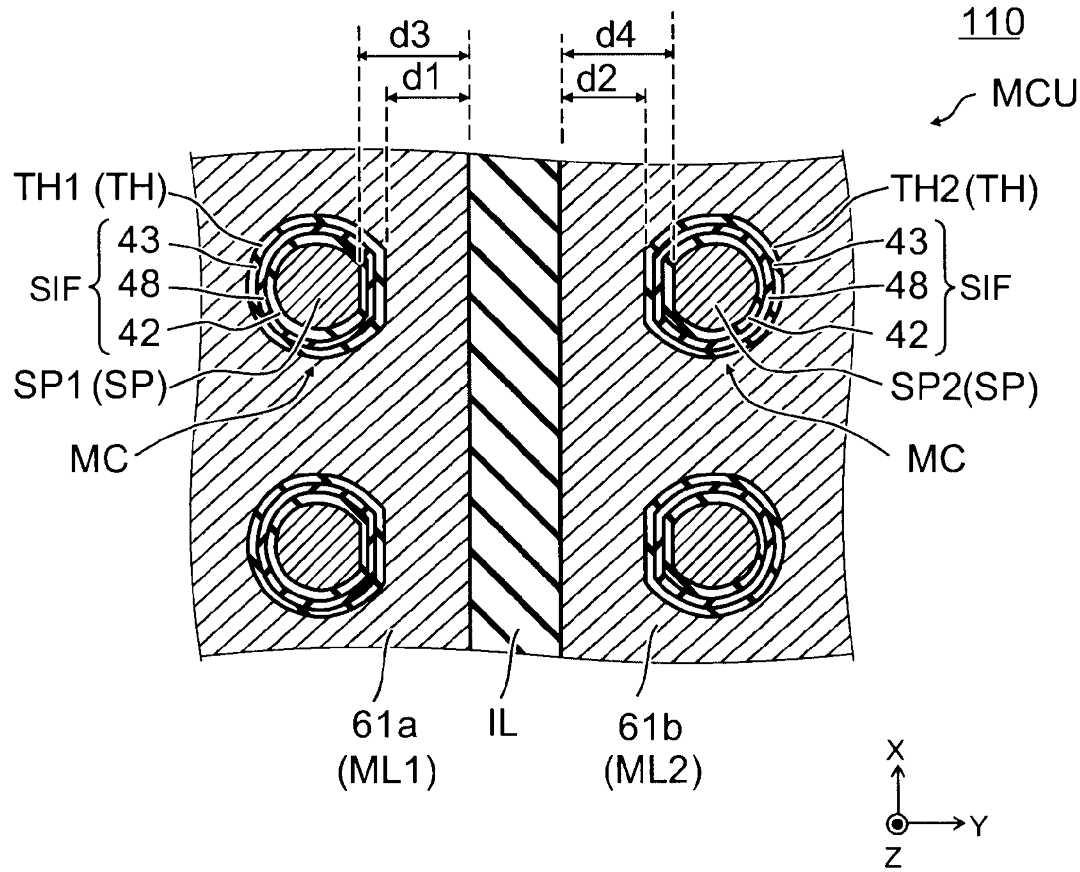
Z
X
Y
MR
PR
PR1

FIG. 4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d4
d2
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SIF
SP1 (SP)
MC
TH2 (TH)
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48
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SIF
SP2 (SP)
MC
61a
(ML1)
IL
61b
(ML2)
X
Y
Z

FIG. 5

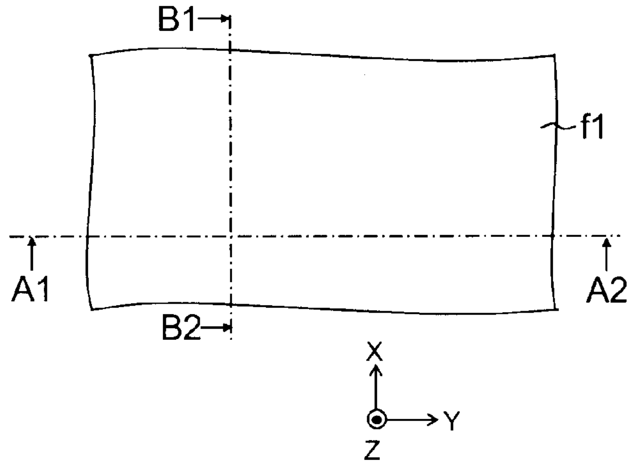


FIG. 6A

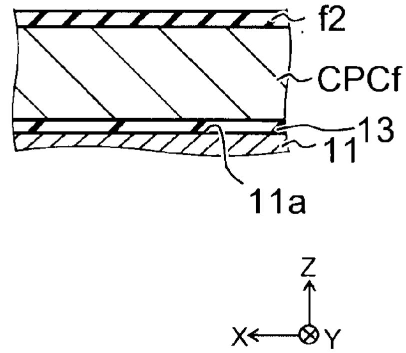


FIG. 6B

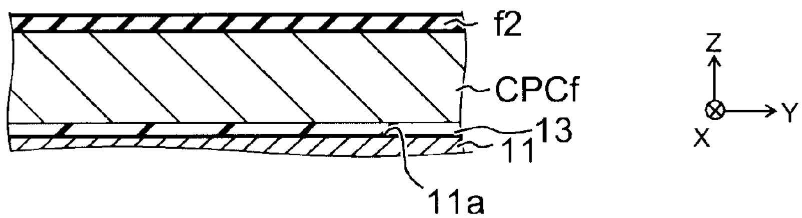


FIG. 6C

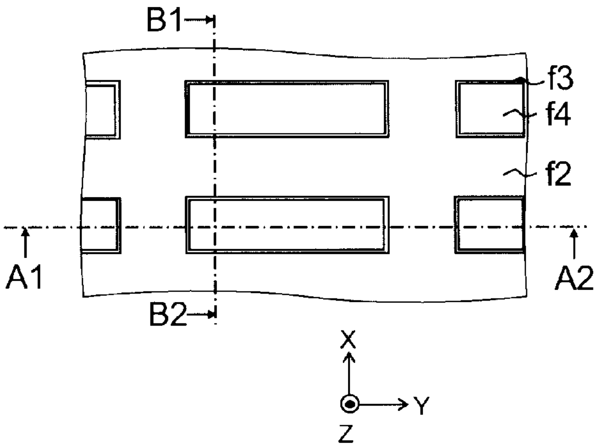


FIG. 7A

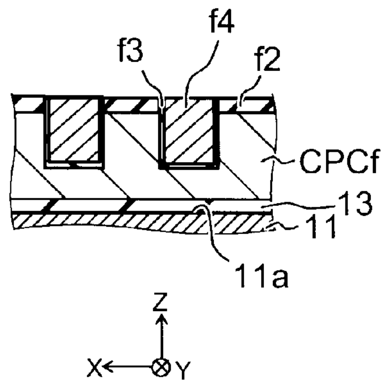


FIG. 7B

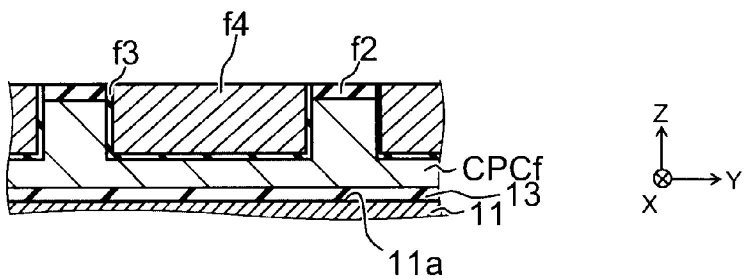


FIG. 7C

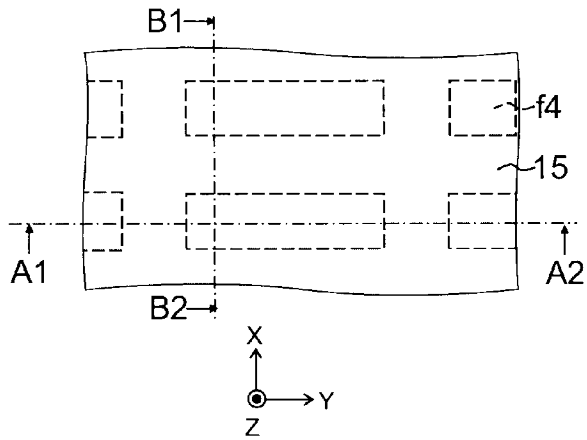


FIG. 8A

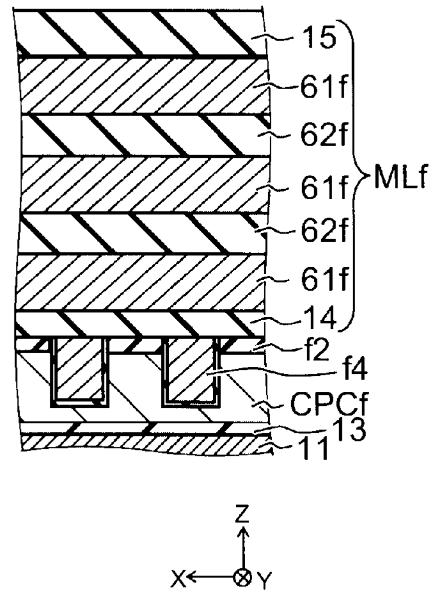


FIG. 8B

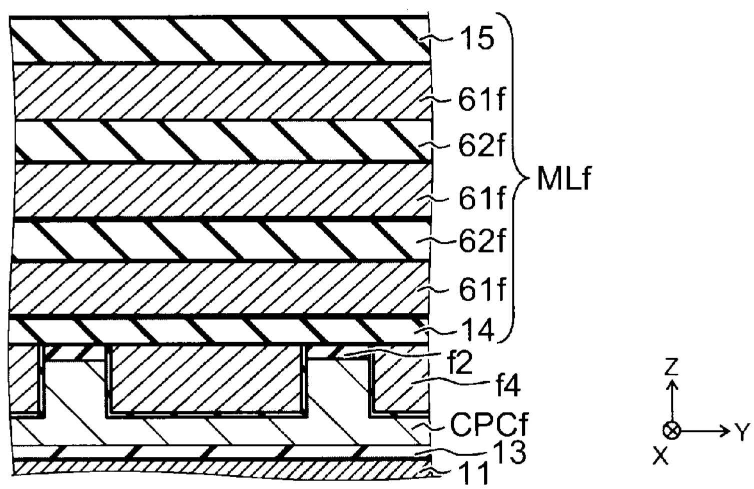


FIG. 8C

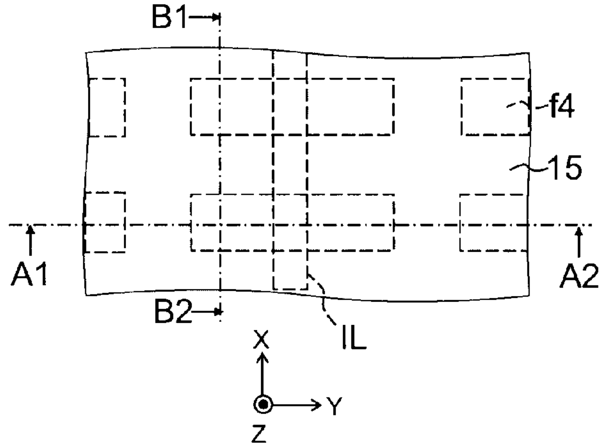


FIG. 9A

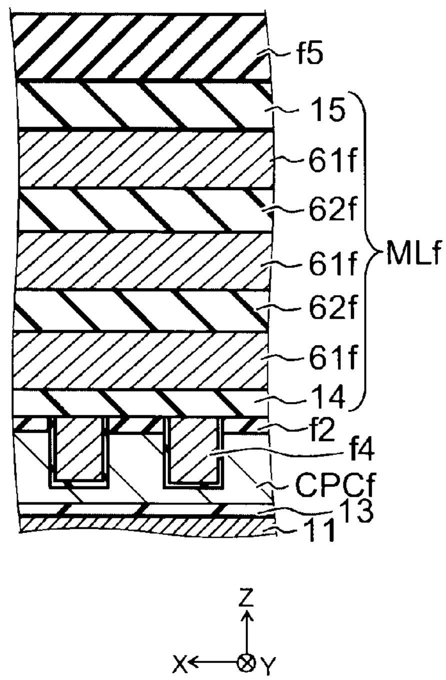


FIG. 9B

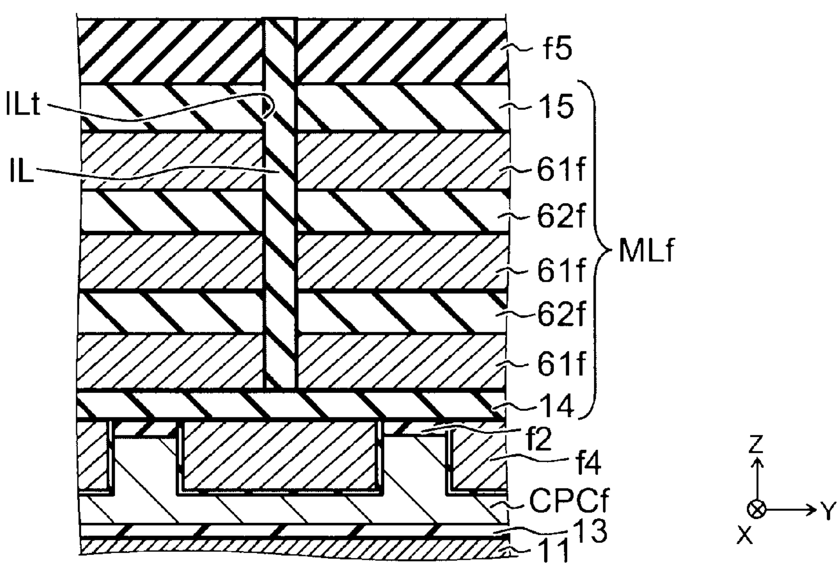


FIG. 9C

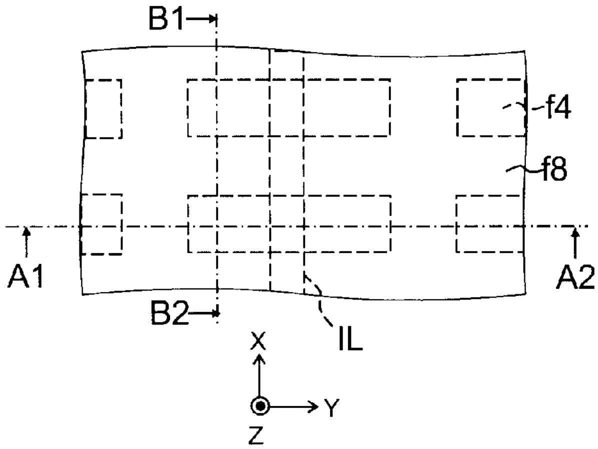


FIG. 10A

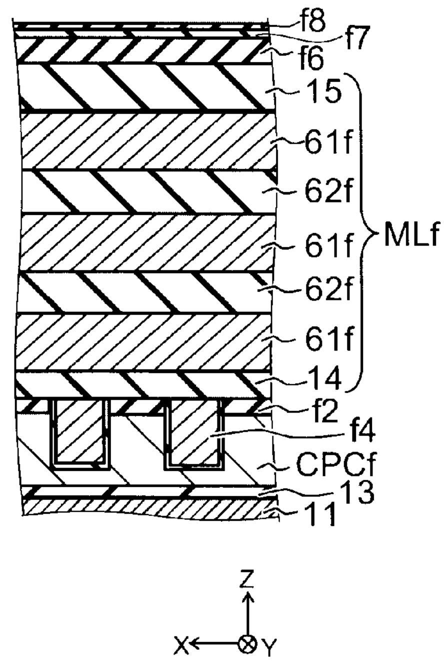


FIG. 10B

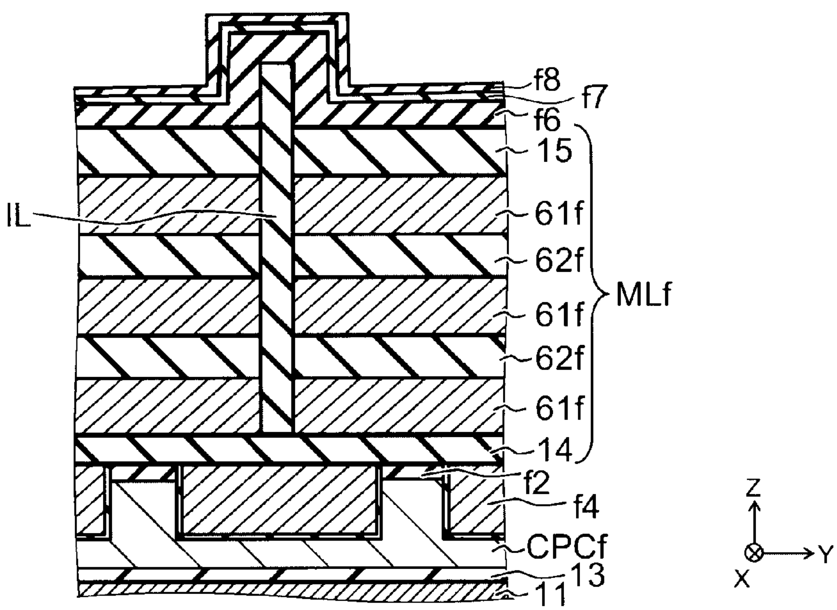


FIG. 10C

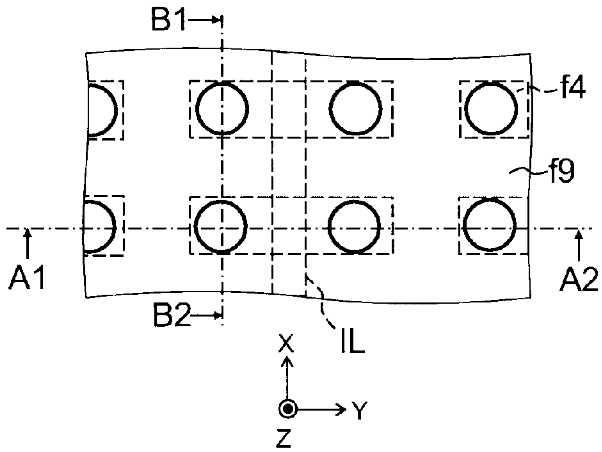


FIG. 11A

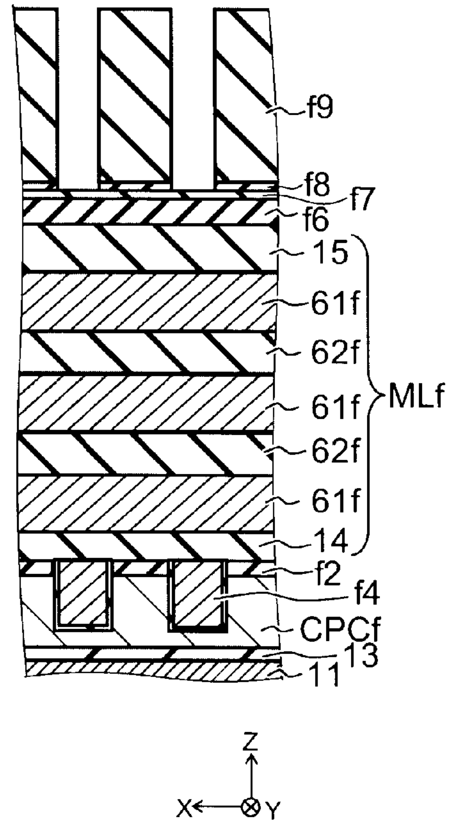


FIG. 11B

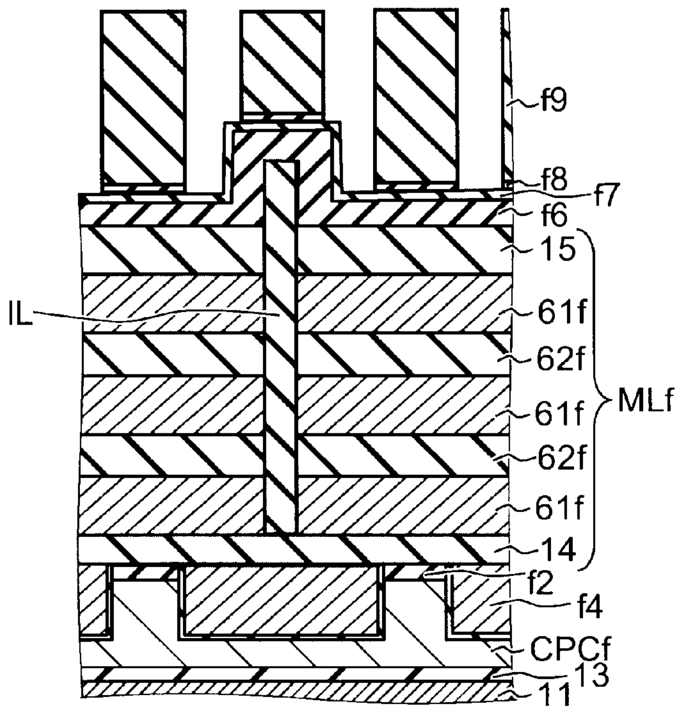


FIG. 11C

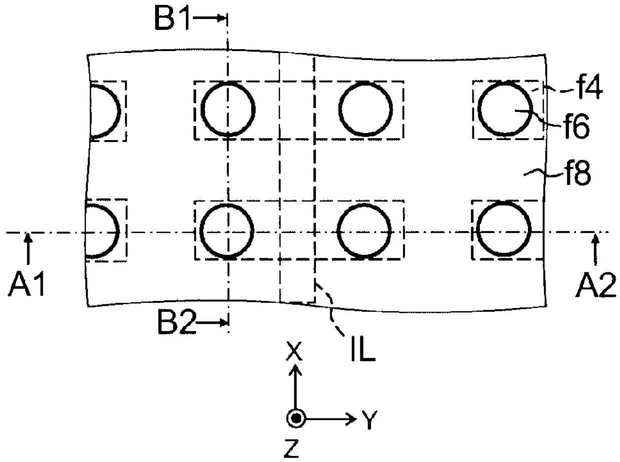


FIG. 12A

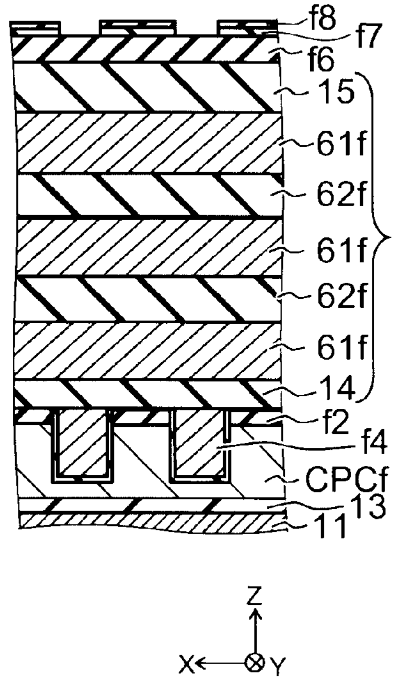


FIG. 12B

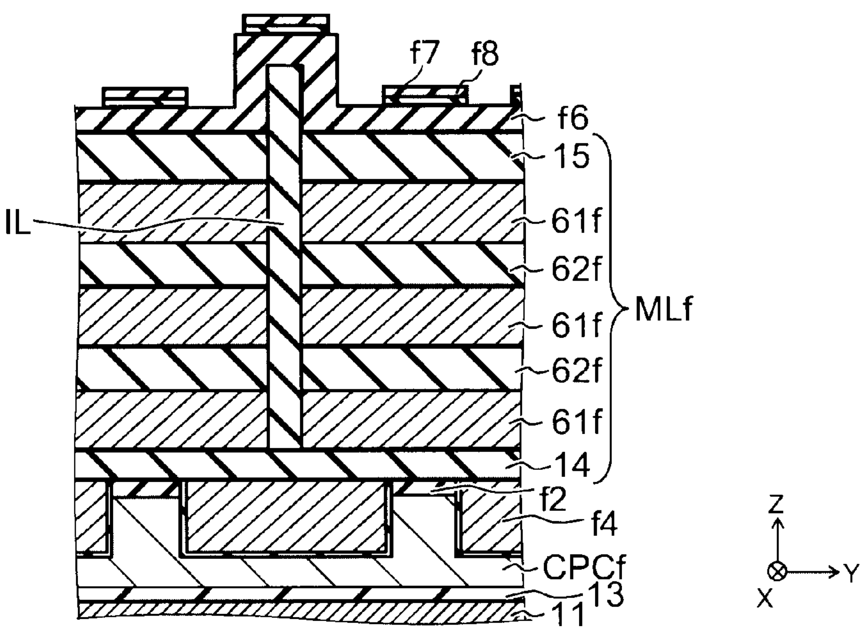


FIG. 12C

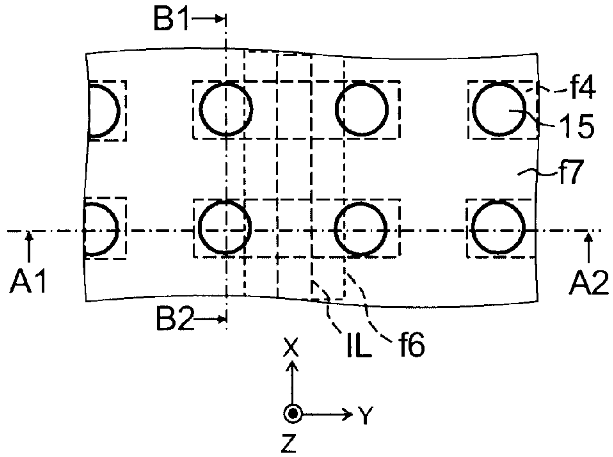


FIG. 13A

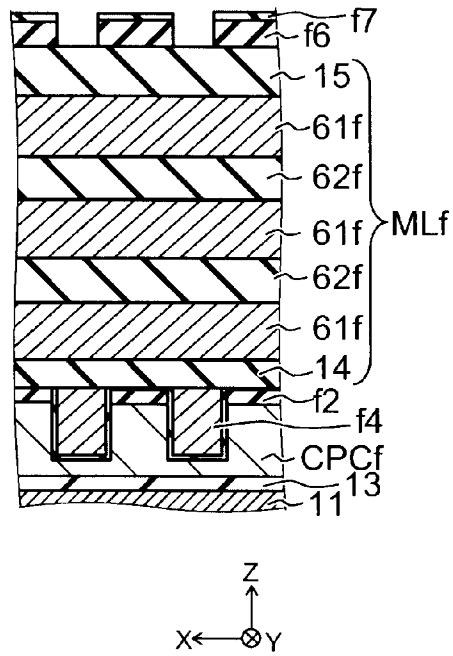


FIG. 13B

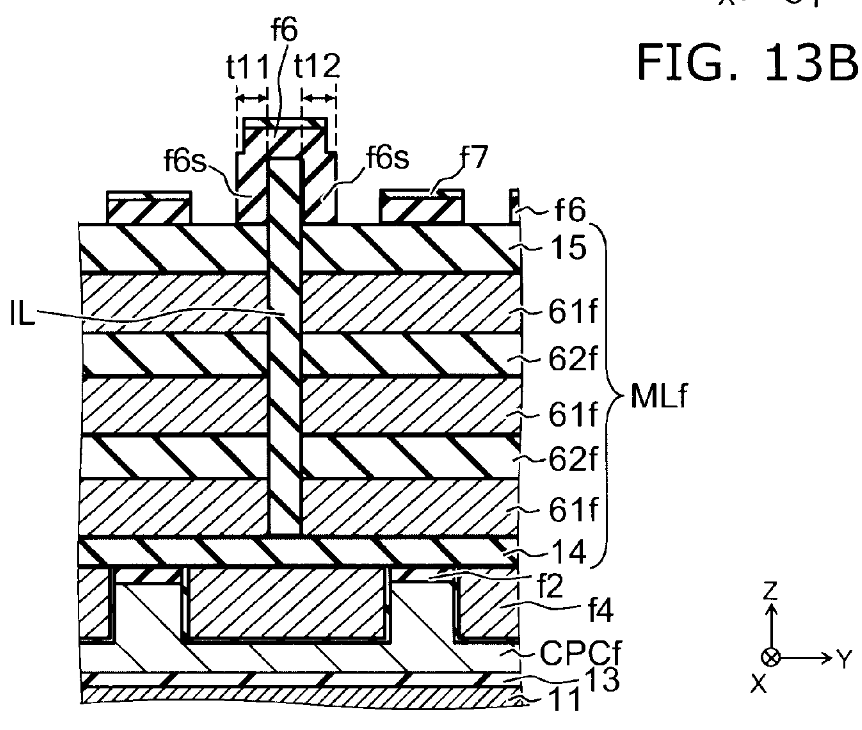


FIG. 13C

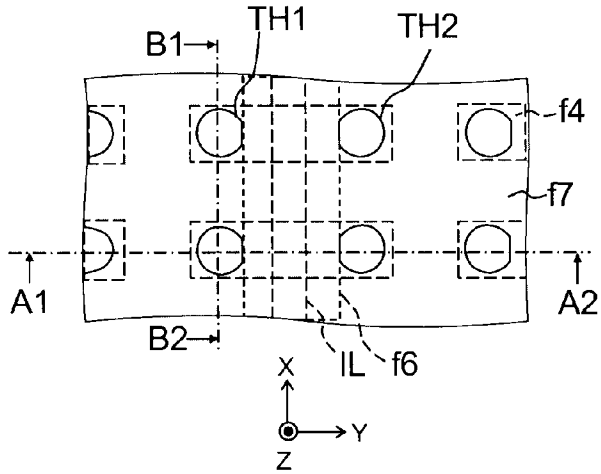


FIG. 14A

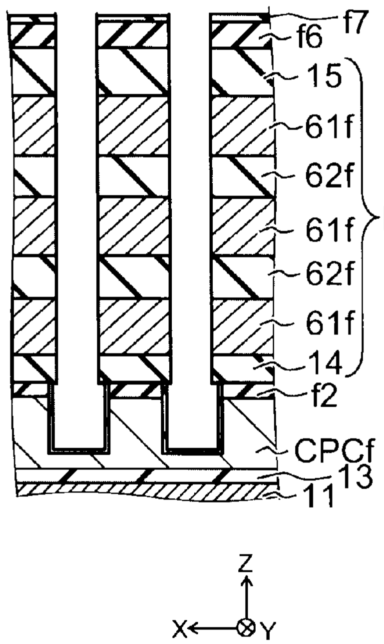


FIG. 14B

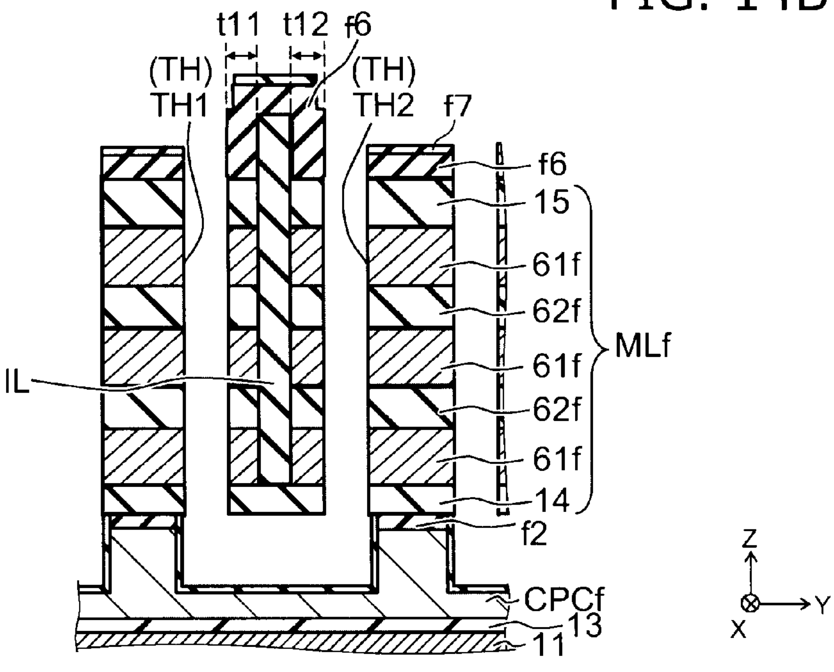


FIG. 14C

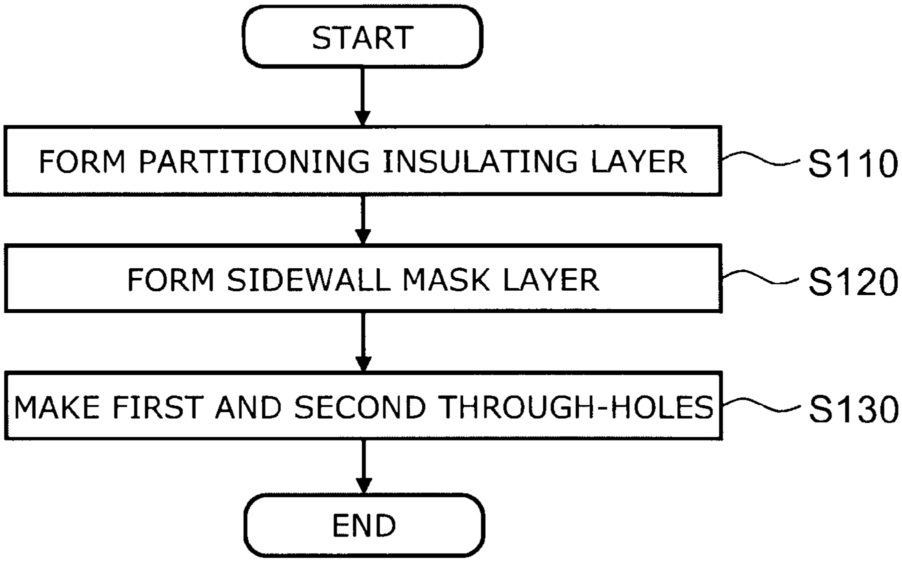
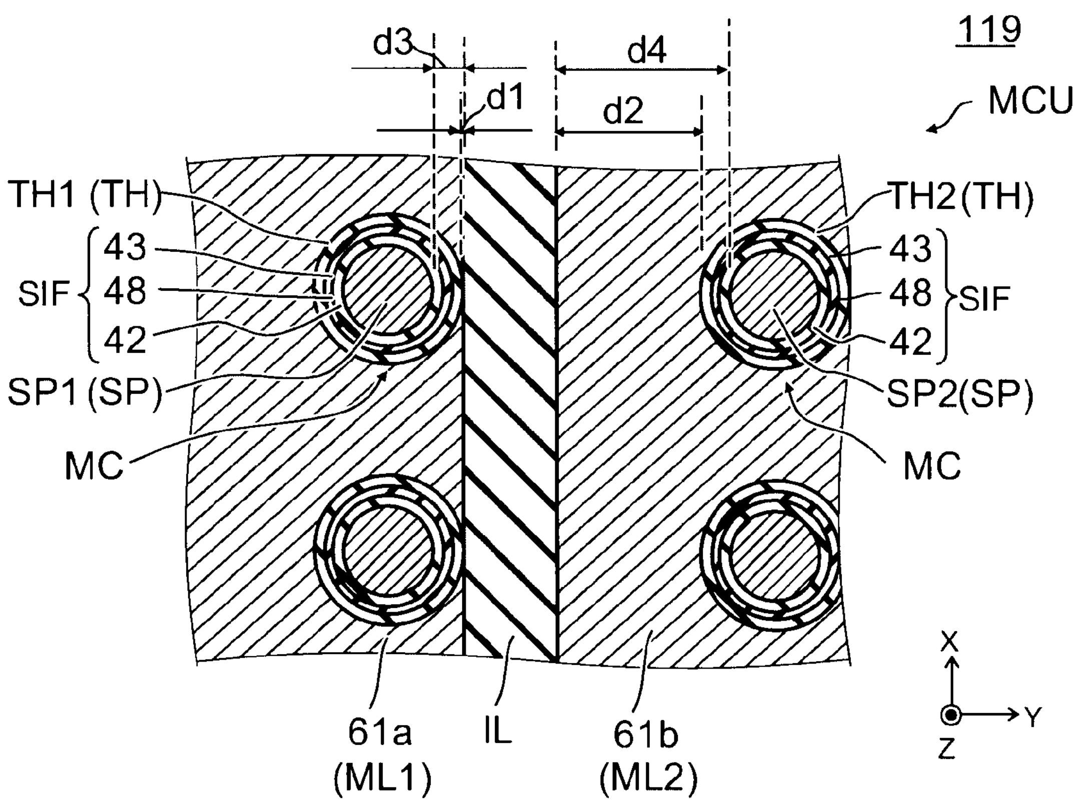

START
FORM PARTITIONING INSULATING LAYER
S110
FORM SIDEWALL MASK LAYER
S120
MAKE FIRST AND SECOND THROUGH-HOLES
S130
END

FIG. 15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MC
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SP2(SP)
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(ML1)
IL
61b
(ML2)
X
Y
Z

FIG. 16

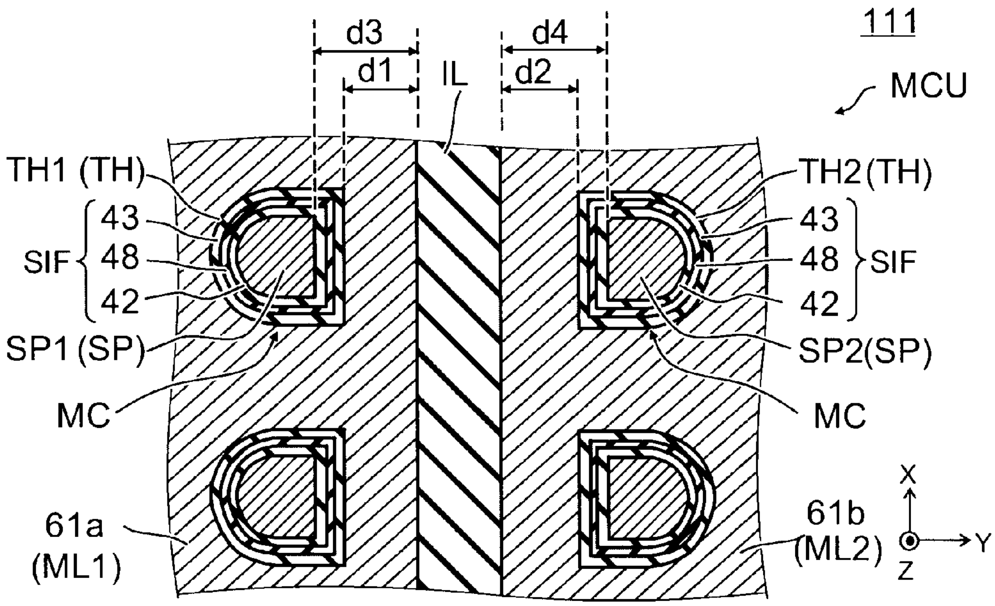


FIG. 17A

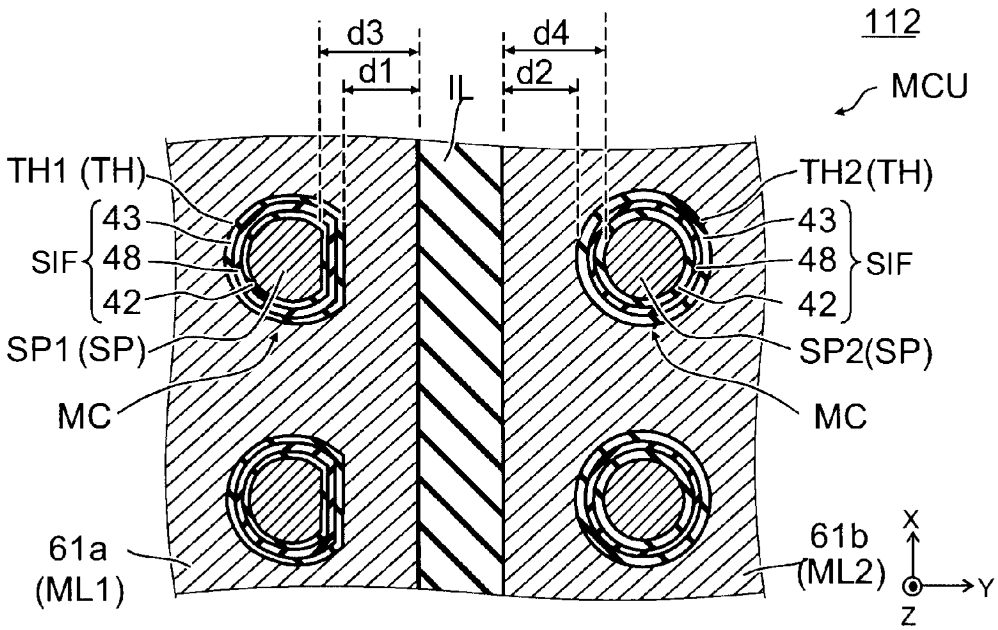
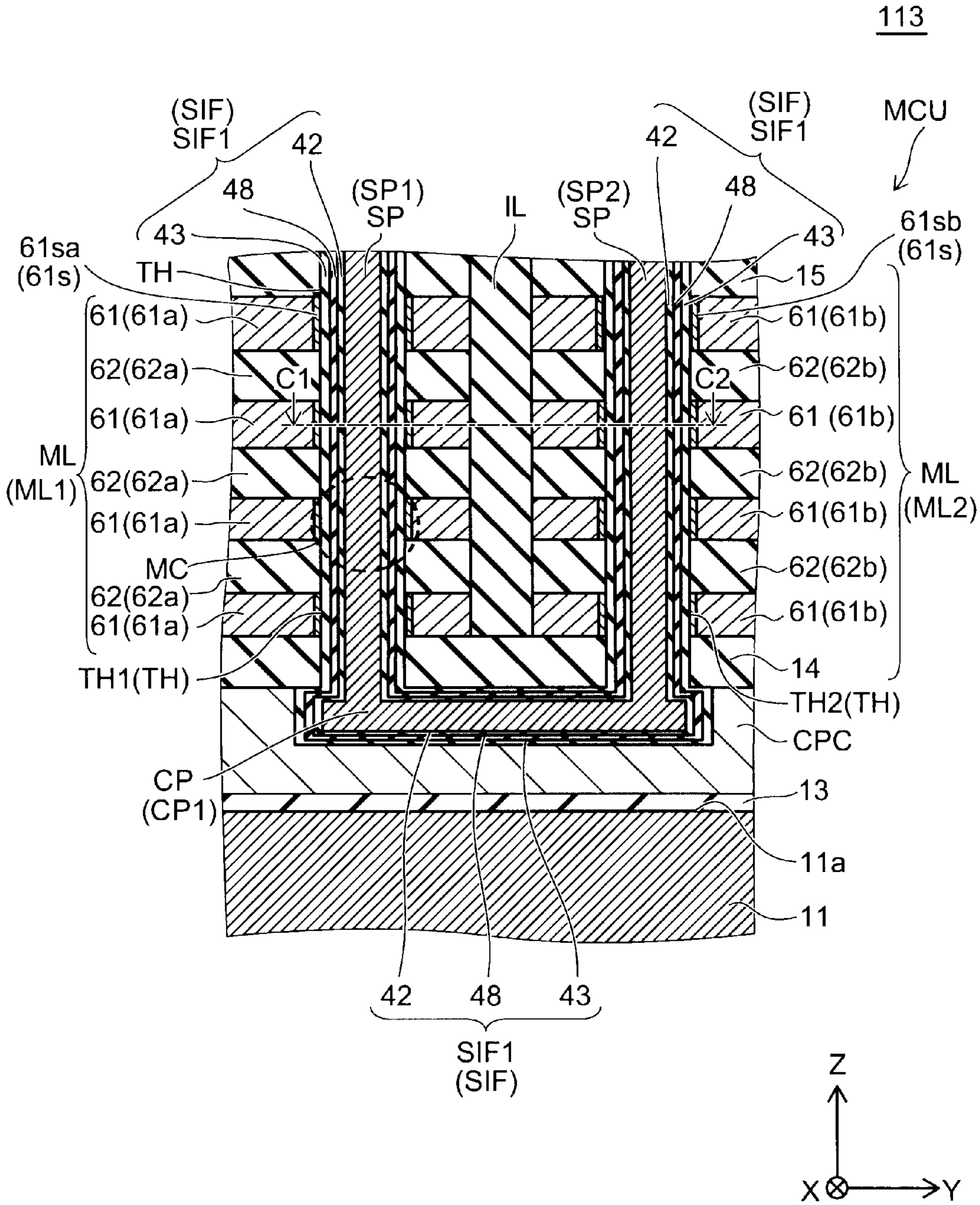


FIG. 17B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TH
61sb
(61s)
15
61(61a)
62(62a)
C1
C2
61(61b)
62(62b)
61 (61b)
ML
(ML1)
ML
(ML2)
MC
TH1(TH)
TH2(TH)
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SIF1
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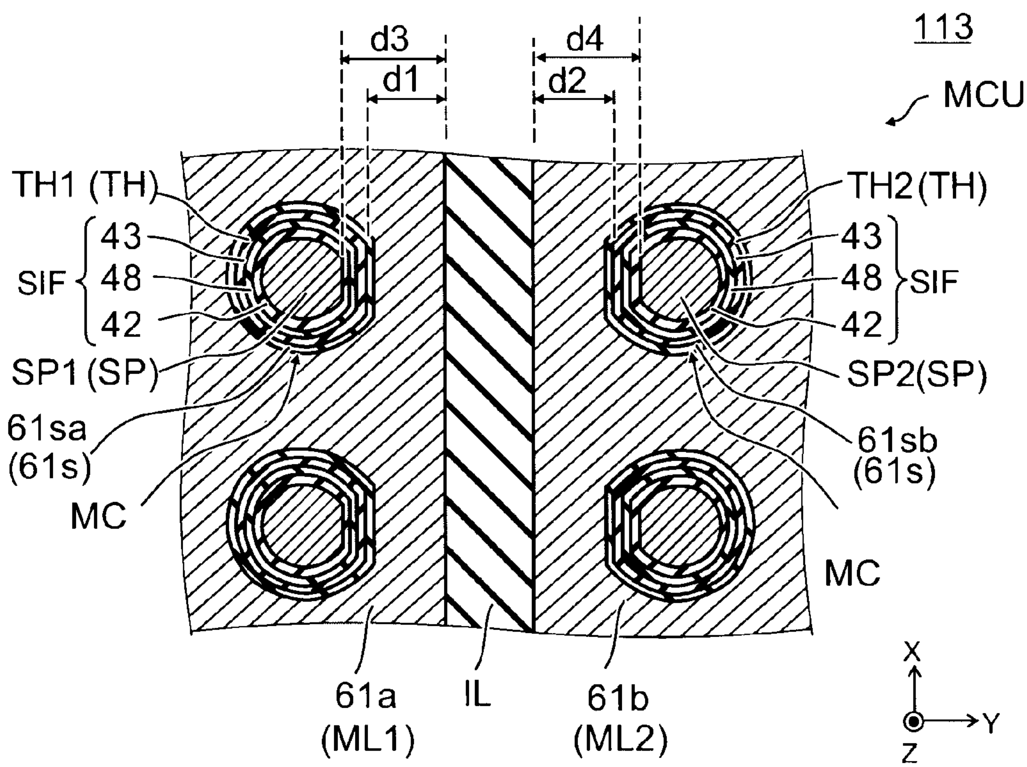
Y

FIG. 18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(61s)
MC
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IL
61b
(ML2)
X
Y
Z

FIG. 19

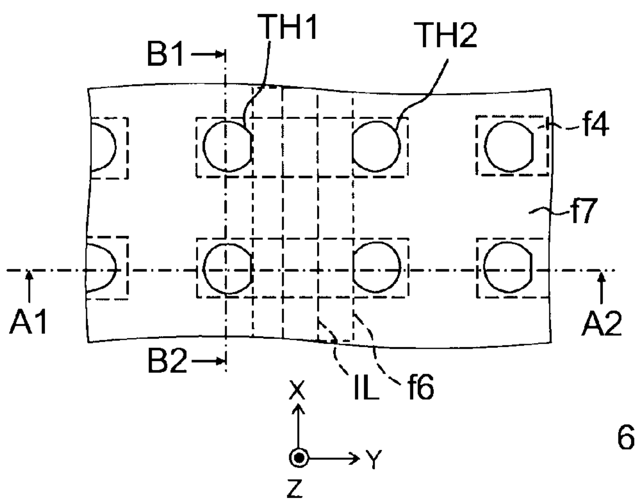

FIG. 20A

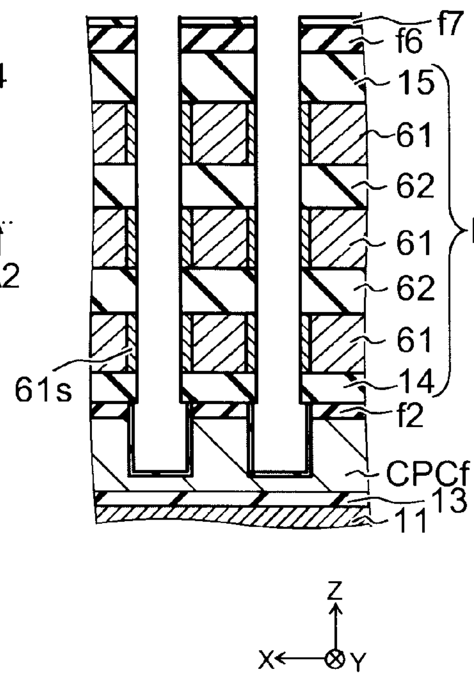

FIG. 20B

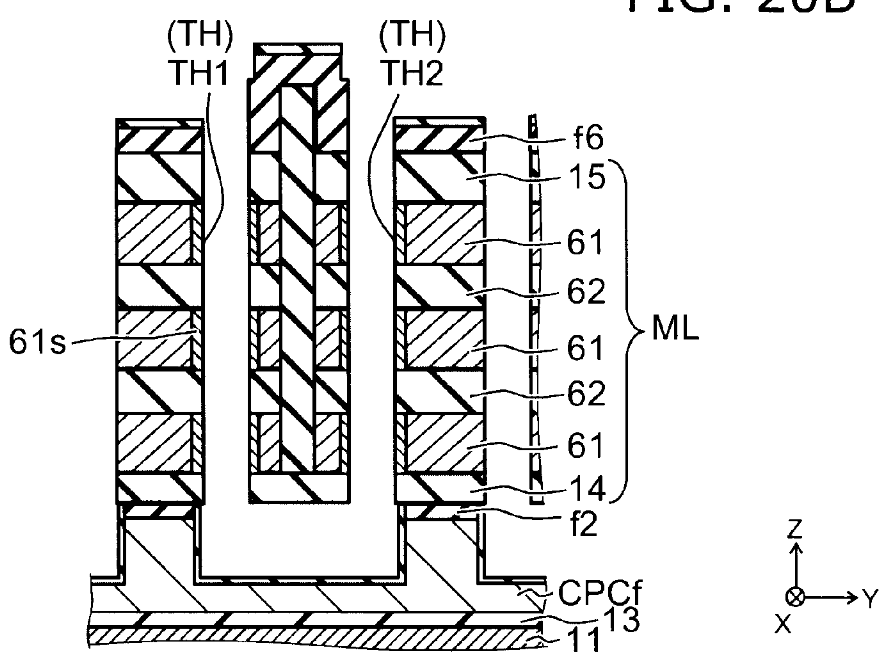

FIG. 20C

NONVOLATILE SEMICONDUCTOR MEMORY DEVICE AND METHOD FOR MANUFACTURING SAME

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This application is based upon and claims the benefit of priority from the prior Japanese Patent Application No. 2011-067635, filed on Mar. 25, 2011; the entire contents of which are incorporated herein by reference.

FIELD

[0002] Embodiments described herein relate generally to a nonvolatile semiconductor memory device, and a method for manufacturing the same.

BACKGROUND

[0003] Three-dimensionally stacked memory has been proposed to increase the storage capacity of nonvolatile semiconductor memory devices. In a three-dimensionally stacked memory, for example, a stacked body including alternately stacked insulating films and electrode films, a silicon pillar that pierces the stacked body in the stacking direction, and a memory film interposed between the silicon pillar and the electrode films are provided. Thereby, a memory cell is provided at the intersection between the silicon pillar and each of the electrode films. Further, a configuration is conceivable in which a memory string has a U-shaped configuration in which two silicon pillars are connected on the substrate side.

[0004] Such a three-dimensionally stacked memory is expected to further reduce the size of the memory cells and further increase the storage density.

BRIEF DESCRIPTION OF THE DRAWINGS

[0005] FIG. **1** is a schematic perspective view illustrating the configuration of a nonvolatile semiconductor memory device according to an embodiment;

[0006] FIG. **2** is a schematic cross-sectional view illustrating the configuration of the nonvolatile semiconductor memory device according to the embodiment;

[0007] FIG. **3** is a schematic plan view illustrating the configuration of the nonvolatile semiconductor memory device according to the embodiment;

[0008] FIG. **4** is a schematic cross-sectional view illustrating the configuration of the nonvolatile semiconductor memory device according to the embodiment;

[0009] FIG. **5** is a schematic cross-sectional view illustrating the configuration of a portion of the nonvolatile semiconductor memory device according to the embodiment;

[0010] FIG. **6**A to FIG. **6**C are schematic views in order of the processes, illustrating the method for manufacturing the nonvolatile semiconductor memory device according to the embodiment;

[0011] FIG. **7**A to FIG. **7**C are schematic views in order of the processes, illustrating the method for manufacturing the nonvolatile semiconductor memory device according to the embodiment.

[0012] FIG. **8**A to FIG. **8**C are schematic views in order of the processes, illustrating the method for manufacturing the nonvolatile semiconductor memory device according to the embodiment;

[0013] FIG. **9**A to FIG. **9**C are schematic views in order of the processes, illustrating the method for manufacturing the nonvolatile semiconductor memory device according to the embodiment;

[0014] FIG. **10**A to FIG. **10**C are schematic views in order of the processes, illustrating the method for manufacturing the nonvolatile semiconductor memory device according to the embodiment;

[0015] FIG. **11**A to FIG. **11**C are schematic views in order of the processes, illustrating the method for manufacturing the nonvolatile semiconductor memory device according to the embodiment;

[0016] FIG. **12**A to FIG. **12**C are schematic views in order of the processes, illustrating the method for manufacturing the nonvolatile semiconductor memory device according to the embodiment;

[0017] FIG. **13**A to FIG. **13**C are schematic views in order of the processes, illustrating the method for manufacturing the nonvolatile semiconductor memory device according to the embodiment;

[0018] FIG. **14**A to FIG. **14**C are schematic views in order of the processes, illustrating the method for manufacturing the nonvolatile semiconductor memory device according to the embodiment;

[0019] FIG. **15** is a flowchart illustrating the method for manufacturing the nonvolatile semiconductor memory device according to the embodiment;

[0020] FIG. **16** is a schematic cross-sectional view illustrating the configuration of a nonvolatile semiconductor memory device of a reference example;

[0021] FIG. **17**A and FIG. **17**B are schematic cross-sectional views illustrating the configuration of another nonvolatile semiconductor memory device according to the embodiment;

[0022] FIG. **18** is a schematic cross-sectional view illustrating the configuration of another nonvolatile semiconductor memory device according to the embodiment;

[0023] FIG. **19** is a schematic cross-sectional view illustrating the configuration of the nonvolatile semiconductor memory device according to the embodiment; and

[0024] FIG. **20**A to FIG. **20**C are schematic views illustrating the method for manufacturing the nonvolatile semiconductor memory device according to the embodiment.

DETAILED DESCRIPTION

[0025] In general, according to one embodiment, a nonvolatile semiconductor memory device includes: a first stacked body, a first semiconductor pillar, a second stacked body, a second semiconductor pillar, a connection portion, a memory film, and a partitioning insulating layer. The first stacked body includes a plurality of first electrode films stacked along a first axis and a first inter-electrode insulating film provided between two of the first electrode films mutually adjacent along the first axis. A first through-hole is provided in the first stacked body to extend along the first axis. The first semiconductor pillar is filled into the first through-hole to extend along the first axis. The second stacked body is juxtaposed with the first stacked body along a second axis orthogonal to the first axis. The second stacked body includes a plurality of second electrode films stacked along the first axis and a second inter-electrode insulating film provided between two of the second electrode films mutually adjacent along the first axis. A second through-hole is provided in the second stacked body to extend along the first axis. The second semiconductor pillar is filled into the second through-hole to extend along the first axis. The connection portion electrically connects the first semiconductor pillar to the second semiconductor pillar. The memory film is provided between the first semiconductor pillar and the plurality of first electrode films and between the second semiconductor pillar and the plurality of second electrode films. The partitioning insulating layer is provided between the first stacked body and the second stacked body to partition the plurality of first electrode films from the plurality of second electrode films. At least one selected from a side surface of the first through-hole on the partitioning insulating layer side and a side surface of the second through-hole on the partitioning insulating layer side is configured to have a portion parallel to a plane including the first axis and a third axis orthogonal to the first and second axes.

[0026] According to another embodiment, a method for manufacturing a nonvolatile semiconductor memory device is disclosed. The device includes: a first stacked body, a first semiconductor pillar, a second stacked body, a second semiconductor pillar, a connection portion, a memory film, and a partitioning insulating layer. The first stacked body includes a plurality of first electrode films stacked along a first axis and a first inter-electrode insulating film provided between two of the first electrode films mutually adjacent along the first axis. A first through-hole is provided in the first stacked body to extend along the first axis. The first semiconductor pillar is filled into the first through-hole to extend along the first axis. The second stacked body is juxtaposed with the first stacked body along a second axis orthogonal to the first axis. The second stacked body includes a plurality of second electrode films stacked along the first axis and a second inter-electrode insulating film provided between two of the second electrode films mutually adjacent along the first axis. A second through-hole is provided in the second stacked body to extend along the first axis. The second semiconductor pillar is filled into the second through-hole to extend along the first axis. The connection portion electrically connects the first semiconductor pillar to the second semiconductor pillar. The partitioning insulating layer provided between the first stacked body and the second stacked body to partition the plurality of first electrode films from the plurality of second electrode films. The memory film is provided between the first semiconductor pillar and the plurality of first electrode films and between the second semiconductor pillar and the plurality of second electrode films. The method can form the partitioning insulating layer in a stacked main body used to form the first stacked body and the second stacked body. The method can form a sidewall mask layer on a sidewall of a portion of the partitioning insulating layer. In addition, the method can make the first through-hole and the second through-hole in the stacked main body by using the sidewall mask layer as a portion of a mask.

[0027] Exemplary embodiments of the invention will now be described in detail with reference to the drawings.

[0028] The drawings are schematic or conceptual; and the relationships between the thickness and width of portions, the proportions of sizes among portions, etc., are not necessarily the same as the actual values thereof. Further, the dimensions and proportions may be illustrated differently among the drawings, even for identical portions.

[0029] In the specification and the drawings of the application, components similar to those described in regard to a drawing thereinabove are marked with like reference numerals, and a detailed description is omitted as appropriate.

Embodiment

[0030] FIG. **1** is a schematic perspective view illustrating the configuration of a nonvolatile semiconductor memory device according to an embodiment.

[0031] For easier viewing of the drawing in FIG. **1**, conductive portions are illustrated and insulating portions are not illustrated. As illustrated in FIG. **1**, the nonvolatile semiconductor memory device **110** according to the embodiment includes a memory cell array unit MCU. Multiple memory cells MC are provided in the memory cell array unit MCU. An example of a configuration of the memory cell MC is described below.

[0032] The memory cell array unit MCU is provided on, for example, a major surface **11***a* of a substrate **11**.

[0033] The substrate **11** may include, for example, a semiconductor substrate. The substrate **11** may include, for example, a silicon substrate.

[0034] Herein, an axis perpendicular to the major surface **11***a* of the substrate **11** is taken as a Z axis (a first axis). One axis perpendicular to the Z axis is taken as a Y axis (a second axis). An axis perpendicular to the Z axis and the Y axis is taken as an X axis (a third axis).

[0035] The memory cell array unit MCU includes a stacked body ML, a semiconductor pillar SP, and a not-illustrated memory film.

[0036] The stacked body ML includes multiple electrode films **61** stacked along the Z axis and an inter-electrode insulating film (not illustrated in FIG. **1**) provided between the multiple electrode films **61**.

[0037] In the specification of the application, stacking includes not only the case of being overlaid in direct contact but also the case of being overlaid with another component inserted therebetween.

[0038] The semiconductor pillar SP pierces the stacked body ML along the Z axis. Namely, the semiconductor pillar SP pierces the electrode films **61** along the Z axis. As described below, the memory film is provided between the semiconductor pillar SP and the multiple electrode films **61**.

[0039] The memory cells MC (the memory cell transistors) are formed at portions where the multiple electrode films **61** intersect the semiconductor pillar SP.

[0040] Specifically, multiple stacked bodies ML include, for example, first to fourth stacked bodies ML**1** to ML**4**, etc. The multiple stacked bodies ML have portions extending along, for example, the X axis. The multiple stacked bodies ML are juxtaposed along, for example, the Y axis. Each of the multiple stacked bodies ML includes the multiple electrode films **61** stacked along the Z axis and an inter-electrode insulating film (not illustrated in this drawing) provided between two electrode films **61** mutually adjacent along the Z axis.

[0041] The first stacked body ML**1** includes multiple first electrode films **61***a*. The second stacked body ML**2** includes multiple second electrode films **61***b*. In this example, the multiple electrode films **61** included in the third stacked body ML**3** are continuous from the multiple second electrode films **61***b* respectively. Although the second stacked body ML**2** and the third stacked body ML**3** are continuous from each other, these are called the second stacked body ML**2** and the third stacked body ML**3** respectively for convenience. In this example as described below, the multiple electrode films **61**

included in the fourth stacked body ML**4** are electrically connected to the multiple first electrode films **61***a*.

[0042] The multiple electrode films **61** have portions extending along the X axis.

[0043] Although the case is illustrated where the number of the electrode films **61** is four for easier viewing of the drawing in FIG. **1**, the number of the electrode films **61** of the embodiment is arbitrary.

[0044] For example, the multiple semiconductor pillars SP are taken as the first to fourth semiconductor pillars SP**1** to SP**4**. The first to fourth semiconductor pillars SP**1** to SP**4** pierce the first to fourth stacked bodies ML**1** to ML**4** respectively.

[0045] The first to fourth semiconductor pillars SP**1** to SP**4** are juxtaposed along, for example, the Y axis. The second semiconductor pillar SP is disposed between the first semiconductor pillar SP**1** and the fourth semiconductor pillar SP**4**. The third semiconductor pillar SP**3** is disposed between the second semiconductor pillar SP**2** and the fourth semiconductor pillar SP**4**.

[0046] One end of the first semiconductor pillar SP**1** is electrically connected to one end of the second semiconductor pillar SP**2** by a first connection portion CP**1** (a connection portion CP). One end of the third semiconductor pillar SP**3** is electrically connected to one end of the fourth semiconductor pillar SP**4** by a second connection portion CP**2**. The one end recited above is the end on the substrate **11** side.

[0047] The other end of the first semiconductor pillar SP**1** is connected to a bit line BL by a contact via **22***a*. The other end of the fourth semiconductor pillar SP**4** is connected to the bit line BL by a contact via **22***b*. The other end of the second semiconductor pillar SP**2** and the other end of the third semiconductor pillar SP**3** are connected to a source line SL.

[0048] First to fourth selection gate electrodes SG**1** to SG**4** are provided between the first stacked body ML**1** and the bit line BL, between the second stacked body ML**2** and the source line SL, between the third stacked body ML**3** and the source line SL, and between the fourth stacked body ML**4** and the bit line BL, respectively. The first to fourth selection gate electrodes SG**1** to SG**4** are any of the multiple selection gate electrodes SG. The first to fourth selection gate electrodes SG**1** to SG**4** extend along the X axis.

[0049] For example, through-holes TH extending in the Z axis are provided in the multiple stacked bodies ML. The semiconductor pillars SP are formed by filling a semiconductor material into the through-holes TH.

[0050] Multiple semiconductor pillars SP may be provided to be juxtaposed along the X axis for one of the electrode films **61**. The multiple semiconductor pillars SP are provided in a matrix configuration along the X axis and the Y axis. The memory cells MC are formed respectively at portions where the multiple semiconductor pillars SP intersect the multiple electrode films **61** stacked along the Z axis. The memory cells MC are provided in a three-dimensional matrix configuration along the Z axis, the X axis, and the Y axis.

[0051] The connection portions CP may include, for example, the semiconductor material used in the semiconductor pillars SP.

[0052] The memory cell array unit MCU may further include a connection portion conductive layer CPC opposing the connection portions CP. For example, trenches are provided in the connection portion conductive layer CPC; and the connection portions CP are formed by filling a semiconductor material into the trenches. The two semiconductor pillars SP connected to each of the connection portions CP are electrically connected to each other by controlling the potential of the connection portion conductive layer CPC.

[0053] The connected first semiconductor pillar SP**1** and second semiconductor pillar SP**2** form a memory string. The connected third semiconductor pillar SP**3** and fourth semiconductor pillar SP**4** form another memory string.

[0054] FIG. **2** is a schematic cross-sectional view illustrating the configuration of the nonvolatile semiconductor memory device according to the embodiment.

[0055] FIG. **2** illustrates a portion of the cross section along line A**1**-A**2** of FIG. **1**.

[0056] As illustrated in FIG. **2**, the first stacked body ML**1** includes the multiple first electrode films **61***a* stacked along the Z axis and a first inter-electrode insulating film **62***a* provided between two first electrode films **61***a* mutually adjacent along the Z axis. A first through-hole TH**1** extending along the Z axis is provided in the first stacked body ML**1**. The first semiconductor pillar SP**1** is filled into the first through-hole TH**1** and extends along the Z axis.

[0057] The second stacked body ML**2** is juxtaposed with the first stacked body ML**1** along, for example, the Y axis. The second stacked body ML**2** includes the multiple second electrode films **61***b* stacked along the Z axis and a second inter-electrode insulating film **62***b* provided between two second electrode films **61***b* mutually adjacent along the Z axis. A second through-hole TH**2** extending along the Z axis is provided in the second stacked body ML**1**. The second semiconductor pillar SP**2** is filled into the second through-hole TH**2** and extends along the Z axis.

[0058] A memory film SIF is provided between the first semiconductor pillar SP**1** and the multiple first electrode films **61***a* and between the second semiconductor pillar SP**2** and the multiple second electrode films **61***b*. The memory film SIF is provided around the side surface of the semiconductor pillars SP along the Z axis. The memory film SIF extends between the connection portion CP (e.g., the first connection portion CP**1**) and the connection portion conductive layer CPC.

[0059] For example, the memory film SIF includes a charge retaining film **48**, an inner insulating film **42**, and an outer insulating film **43**. The charge retaining film **48** is provided between the semiconductor pillar SP and the electrode films **61** and between the connection portion conductive layer CPC and the connection portion CP. The inner insulating film **42** is provided between the semiconductor pillar SP and the charge retaining film **48** and between the connection portion CP and the charge retaining film **48**. The outer insulating film **43** is provided between the charge retaining film **48** and the electrode films **61** and between the charge retaining film **48** and the connection portion conductive layer CPC.

[0060] As illustrated in FIG. **2**, a partitioning insulating layer IL is provided to partition the first stacked body ML**1** from the second stacked body ML**2**. The partitioning insulating layer IL partitions the multiple first electrode films **61***a* from the multiple second electrode films **61***b*. The partitioning insulating layer IL has a portion extending along the X axis.

[0061] In this example as illustrated in FIG. **2**, an insulating film **13** is provided between the substrate **11** and the connection portion conductive layer CPC. An inter-layer insulating film **14** is provided between the connection portion conductive layer CPC and the multiple electrode films **61**. An inter-layer insulating film **15** is further provided. The multiple electrode films **61** are disposed between the inter-layer insulating film **14** and the inter-layer insulating film **15**. For convenience, the inter-layer insulating films **14** and **15** are taken to be included in the stacked body ML.

[0062] The electrode films **61** and the connection portion conductive layer CPC may include, for example, polysilicon. However, the materials of the electrode films **61** and the connection portion conductive layer CPC are arbitrary in the embodiment.

[0063] An inter-electrode insulating film **62**, the inner insulating film **42**, the outer insulating film **43**, the insulating film **13**, the inter-layer insulating film **14**, and the inter-layer insulating film **15** may include, for example, silicon oxide. However, the materials of the inter-electrode insulating film **62**, the inner insulating film **42**, the outer insulating film **43**, and the inter-layer insulating films are arbitrary in the embodiment.

[0064] The charge retaining film **48** may include, for example, silicon nitride. However, the material of the charge retaining film **48** is arbitrary in the embodiment.

[0065] The charge retaining film **48** can function as a portion configured to store information by storing charge in the memory cells MC. The inner insulating film **42** can function as, for example, a tunneling insulating film. The outer insulating film **43** can function as a blocking insulating film. The memory cells MC are transistors having, for example, MONOS configurations. The multiple electrode films **61** can function as word electrodes.

[0066] FIG. **3** is a schematic plan view illustrating the configuration of the nonvolatile semiconductor memory device according to the embodiment.

[0067] Although three semiconductor pillars SP juxtaposed along the X axis for one of the electrode films **61** are illustrated for easier viewing of the drawing in FIG. **3**, the number of the semiconductor pillars SP juxtaposed along the X axis is arbitrary in the embodiment.

[0068] As illustrated in FIG. **3**, for example, the first electrode film **61***a* of the first stacked body ML**1** pierced by the first semiconductor pillar SP**1** is connected to a fourth electrode film **61***d* of the fourth stacked body ML**4** pierced by the fourth semiconductor pillar SP**4** at one X-axis end (e.g., a first contact portion CU**1**). The connected first electrode film **61***a* and fourth electrode film **61***d* form a first linked electrode film **61**A.

[0069] As described above, the second electrode film **61***b* of the second stacked body ML**2** pierced by the second semiconductor pillar SP**2** is connected to a third electrode film **61***c* of the third stacked body ML**3** pierced by the third semiconductor pillar SP**3**. However, the second electrode film **61***b* and the third electrode film **61***c* may be connected at the other X-axis end (a second contact portion CU**2**). The connected second electrode film **61***b* and third electrode film **61***c* form a second linked electrode film **61**B.

[0070] FIG. **4** is a schematic cross-sectional view illustrating the configuration of the nonvolatile semiconductor memory device according to the embodiment.

[0071] Regarding the memory cell array unit MCU, a cross section corresponding to line A**1**-A**2** of FIG. **1** and a cross section corresponding to line B**1**-B**2** of FIG. **1** are illustrated in FIG. **4**. The first contact portions CU**1** are illustrated in FIG. **4**.

[0072] Although the case is illustrated where the number of the electrode films **61** is four for easier viewing of the drawing in FIG. **4**, the number of the electrode films **61** is arbitrary in the embodiment.

[0073] As illustrated in FIG. **4**, for example, a memory region MR and a peripheral region PR are provided in the substrate **11**. The peripheral region PR is juxtaposed with the memory region MR on the major surface **11***a*. A peripheral circuit PR**1** configured to operate the memory cells MC, for example, is provided in the peripheral region PR.

[0074] A memory unit MU and a memory unit peripheral circuit unit MPU, for example, are provided in the memory region MR. For example, the memory unit peripheral circuit unit MPU is provided on the major surface **11***a* of the substrate **11**; and the memory unit MU is provided on the memory unit peripheral circuit unit MPU.

[0075] For example, the memory cell array unit MCU and the contact portions CU (e.g., the first contact portions CU**1**, etc.) are provided in the memory unit MU. The contact portions CU are juxtaposed with the memory cell array unit MCU in the X-Y plane.

[0076] As illustrated in FIG. **4**, the stacked bodies ML are provided on the connection portion conductive layer CPC on the major surface **11***a* in the memory cell array unit MCU. The multiple selection gate electrodes SG are provided on the stacked bodies ML. An inter-layer insulating film **17** is provided between the multiple selection gate electrodes SG. In this specific example, an inter-layer insulating film **16** is provided between the inter-layer insulating film **15** and the selection gate electrodes SG. At least one selected from the inter-layer insulating film **15** and the inter-layer insulating film **16** may be omitted.

[0077] A selection gate insulating film SGI is provided between the selection gate electrodes SG and the semiconductor pillars SP. Selection gate transistors are formed at the intersections between the multiple selection gate electrodes SG and the multiple semiconductor pillars SP.

[0078] The portion of the semiconductor pillar SP piercing the stacked body ML and the portion of the semiconductor pillar SP piercing the selection gate electrode SG may be formed collectively or may be formed in different processes.

[0079] An inter-layer insulating film **18** is provided between the source lines SL and the selection gate electrodes SG. An inter-layer insulating film **23** is provided between the source lines SL and the bit lines BL. The contact vias **22***a* and **22***b* pierce the inter-layer insulating film **23** along the Z axis.

[0080] The selection gate electrodes SG may include, for example, polysilicon. The selection gate insulating film SGI may include, for example, silicon oxide. The selection gate insulating film SGI may include a material used to form at least a portion of the inner insulating film **42**, the charge retaining film **48**, and the outer insulating film **43**.

[0081] The inter-layer insulating film **16**, the inter-layer insulating film **17**, the inter-layer insulating film **18**, and the inter-layer insulating film **23** may include, for example, silicon oxide.

[0082] The source line SL, the bit line BL, and the contact vias **22***a* and **22***b* may include, for example, a metal material, etc. However, the source line SL, the bit line BL, and the contact vias **22***a* and **22***b* may include any conductive material.

[0083] At the first contact portions CU**1**, the lengths along the X axis of the stacked multiple first electrode films **61***a* (the first linked electrode films **61**A) change in a stairstep configuration. The contact electrodes **31** are connected to the multiple first electrode films **61***a* (the first linked electrode films **61**A) respectively. The contact electrodes **31** extend along the Z axis. The contact electrodes **31** connect the multiple first electrode films **61***a* (the first linked electrode films **61**A) to word interconnects **32** respectively.

[0084] Although not illustrated, at the second contact portions CU**2** as well, the lengths along the X axis of the stacked multiple electrode films **61** (the second linked electrode films **61**B) change, for example, in a stairstep configuration. The contact electrodes **31** are connected to the stacked multiple electrode films **61** (the second linked electrode films **61**B) respectively.

[0085] As illustrated in FIG. **4**, the connection portion conductive layer CPC is connected to a back gate interconnect **34** by a contact electrode **33**.

[0086] FIG. **5** is a schematic cross-sectional view illustrating the configuration of a portion of the nonvolatile semiconductor memory device according to the embodiment.

[0087] Namely, FIG. **5** illustrates the configuration of the memory cell array unit MCU of the nonvolatile semiconductor memory device **110**. FIG. **5** is a cross-sectional view along line C**1**-C**2** of FIG. **2**.

[0088] As illustrated in FIG. **5**, the partitioning insulating layer IL is provided between the first stacked body ML**1** (i.e., the first electrode films **61***a*) and the second stacked body ML**2** (i.e., the second electrode films **61***b*).

[0089] The first through-hole TH**1** extending along the Z axis is provided in the first stacked body ML**1**. The first semiconductor pillar SP**1** is provided inside the first through-hole TH**1**. Similarly, the second through-hole TH**2** extending along the Z axis is provided in the second stacked body ML**2**. The second semiconductor pillar SP**2** is provided inside the second through-hole TH**2**. The memory film SIF is provided between the first semiconductor pillar SP**1** and the first electrode films **61***a* and between the second semiconductor pillar SP**2** and the second electrode films **61***b*.

[0090] As illustrated in FIG. **5**, the side surface of the first through-hole TH**1** on the partitioning insulating layer IL side has a portion parallel to a plane (the X-Z plane) that includes the X axis and the Z axis. The side surface of the second through-hole TH**2** on the partitioning insulating layer IL side has a portion parallel to the plane (the X-Z plane) that includes the X axis and the Z axis.

[0091] The embodiment is not limited thereto. As described below, at least one selected from the side surface of the first through-hole TH**1** on the partitioning insulating layer IL side and the side surface of the second through-hole TH**2** on the partitioning insulating layer IL side may have a portion parallel to the X-Z plane.

[0092] As illustrated in FIG. **5**, the side surface of the memory film SIF on the partitioning insulating layer IL side has a portion parallel to the X-Z plane. For example, at least one selected from the side surface of the outer insulating film **43** on the partitioning insulating layer IL side, the side surface of the charge retaining film **48** on the partitioning insulating layer IL side, and the side surface of the inner insulating film **42** on the partitioning insulating layer IL side may have a portion parallel to the X-Z plane.

[0093] For example, at least one selected from the side surface of the first semiconductor pillar SP**1** on the partitioning insulating layer IL side and the side surface of the second semiconductor pillar SP**2** on the partitioning insulating layer IL side may have a portion parallel to the X-Z plane.

[0094] On the other hand, the side surface of the first through-hole TH**1** on the side opposite to the partitioning insulating layer IL and the side surface of the second through-hole TH**2** on the side opposite to the partitioning insulating layer IL have curved configurations parallel to the Z axis (e.g., portions of cylindrical configurations extending along the Z axis).

[0095] Specifically, the side surface of the first through-hole TH**1** on the side opposite to the partitioning insulating layer IL has a protruding configuration protruding in the direction from the partitioning insulating layer IL toward the first through-hole TH**1**. The side surface of the second through-hole TH**2** on the side opposite to the partitioning insulating layer IL has a protruding configuration protruding in the direction from the partitioning insulating layer IL toward the second through-hole TH**2**.

[0096] For example, the configuration of the side surface of the memory film SIF on the side opposite to the partitioning insulating layer IL is a curved surface parallel to the Z axis.

[0097] For example, the curvature of the portion of the inner insulating film **42** on the side opposite to the partitioning insulating layer IL is larger than the curvature of the portion of the outer insulating film **43** on the side opposite to the partitioning insulating layer IL. Thereby, the electric field of the portion of the inner insulating film **42** on the side opposite to the partitioning insulating layer IL can be greater than the electric field of the portion of the outer insulating film **43** on the side opposite to the partitioning insulating layer IL. Thereby, the operations stabilize.

[0098] As illustrated in FIG. **5**, a distance (a first distance d**1**) along the Y axis between the partitioning insulating layer IL and the ends of the multiple first electrode films **61***a* on the partitioning insulating layer IL side is substantially the same as a distance (a second distance d**2**) along the Y axis between the partitioning insulating layer IL and the ends of the multiple second electrode films **61***b* on the partitioning insulating layer IL side.

[0099] For example, a distance (a third distance d**3**) along the Y axis between the partitioning insulating layer IL and the end of the first semiconductor pillar SP**1** on the partitioning insulating layer IL side is substantially the same as a distance (a fourth distance d**4**) along the Y axis between the partitioning insulating layer IL and the ends of the multiple second semiconductor pillars SP**2** on the partitioning insulating layer IL side.

[0100] The memory film SIF is formed on the interior wall surface of the through-hole TH; and the semiconductor pillar SP is formed by filling a semiconductor material into the remaining space. Therefore, the configuration of the memory film SIF cut by the X-Y plane reflects the configuration of the through-hole TH cut by the X-Y plane. The thickness of the memory film SIF is, for example, uniform. Therefore, the configuration of the semiconductor pillar SP cut by the X-Y plane reflects the configuration of the through-hole TH cut by the X-Y plane.

[0101] As described below, the through-holes TH are formed by, for example, patterning using a sidewall mask layer provided on the sidewalls of a portion of the partitioning insulating layer IL as a mask. The distance between the partitioning insulating layer IL and the wall surfaces of the through-holes TH is constant because the thickness of the sidewall mask layer is constant.

[0102] Therefore, in the embodiment, for example, the design margin for the shift of the positional alignment of the photomask for the patterning can be omitted. Thereby, the distance from the partitioning insulating layer IL to the through-holes TH can be reduced. In other words, the spacing between the memory cells MC can be reduced. Thereby, the size per memory cell MC can be reduced further. According to the embodiment, a nonvolatile semiconductor memory device having a higher storage density can be provided.

[0103] An example of a method for manufacturing the nonvolatile semiconductor memory device **110** will now be described.

[0104] FIG. **6**A to FIG. **6**C, FIG. **7**A to FIG. **7**C, FIG. **8**A to FIG. **8**C, FIG. **9**A to FIG. **9**C, FIG. **10**A to FIG. **10**C, FIG. **11**A to FIG. **11**C, FIG. **12**A to FIG. **12**C, FIG. **13**A to FIG. **13**C, and FIG. **14**A to FIG. **14**C are schematic views in order of the processes, illustrating the method for manufacturing the nonvolatile semiconductor memory device according to the embodiment.

[0105] These drawings correspond to the memory cell array unit MCU.

[0106] FIG. **6**A, FIG. **7**A, FIG. **8**A, FIG. **9**A, FIG. **10**A, FIG. **11**A, FIG. **12**A, FIG. **13**A, and FIG. **14**A are schematic plan views.

[0107] FIG. **6**B, FIG. **7**B, FIG. **8**B, FIG. **9**B, FIG. **10**B, FIG. **11**B, FIG. **12**B, FIG. **13**B, and FIG. **14**B are cross-sectional views along line B**1**-B**2** of FIG. **6**A, FIG. **7**A, FIG. **8**A, FIG. **9**A, FIG. **10**A, FIG. **11**A, FIG. **12**A, FIG. **13**A, and FIG. **14**A, respectively.

[0108] FIG. **6**C, FIG. **7**C, FIG. **8**C, FIG. **9**C, FIG. **10**C, FIG. **11**C, FIG. **12**C, FIG. **13**C, and FIG. **14**C are cross-sectional views along line A**1**-A**2** of FIG. **6**A, FIG. **7**A, FIG. **8**A, FIG. **9**A, FIG. **10**A, FIG. **11**A, FIG. **12**A, FIG. **13**A, and FIG. **14**A, respectively.

[0109] As illustrated in FIG. **6**A to FIG. **6**C, the insulating film **13** is formed on the major surface **11***a* of the substrate **11** (e.g., a silicon substrate). If necessary, the peripheral circuit PR**1** and the memory unit peripheral circuit unit MPU may be formed on the major surface **11***a* of the substrate **11**; and the insulating film **13** may be formed thereon.

[0110] A connection portion conductive film CPCf used to form the connection portion conductive layer CPC is formed on the insulating film **13**. In other words, for example, a polysilicon film used to form the connection portion conductive film CPCf is formed. An insulating film f**2** is formed on the connection portion conductive film CPCf. The insulating film f**2** functions as a stopper film of CPM.

[0111] As illustrated in FIG. **7**A to FIG. **7**C, a first photoresist having a first pattern corresponding to the pattern of the connection portions CP is formed using photolithography; and the insulating film f**2** and the connection portion conductive film CPCf are patterned using the first photoresist as a mask. For example, RIE is used in this patterning. Thereby, trenches corresponding to the pattern of the connection portions CP are made.

[0112] An insulating film f**3** is formed on the front surface of the connection portion conductive film CPCf (the polysilicon film). The insulating film f**3** is, for example, a silicon oxide film. For example, RTO (Rapid Thermal Oxidation) may be used to form the insulating film f**3**.

[0113] An amorphous silicon film f**4** is formed on the front surface of the patterning body. The amorphous silicon film f**4** is formed on the insulating film f**3** of the interior walls inside the trenches. For example, LPCVD is used to form the amorphous silicon film f**4**.

[0114] The amorphous silicon film f**4** is etched and planarized using, for example, RIE by using the insulating film f**2** as a stopper.

[0115] The inter-layer insulating film **14** is formed as illustrated in FIG. **8**A to FIG. **8**C. The inter-layer insulating film **14** may include, for example, a silicon oxide film. For example, LPCVD is used to form the inter-layer insulating film **14**.

[0116] The first layers **61***f* are stacked alternately with second layers **62***f* on the inter-layer insulating film **14**. The etching rate of the first layers **61***f* is different from the etching rate of the second layers **62***f*.

[0117] For example, the first layers **61***f* are used to form the electrode films **61**; and the second layers **62***f* are used to form the inter-electrode insulating films **62**. Or, for example, the first layers **61***f* are used to form the inter-electrode insulating films **62**; and the second layers **62***f* are used to form the electrode films **61**. Or, for example, the first layers **61***f* are used to form the electrode films **61**; the second layers **62***f* are removed; and other layers (third layers) formed in the removed portions are used to form the inter-electrode insulating films **62**. Or, for example, the second layers **62***f* are used to form the inter-electrode insulating films **62**; the first layers **61***f* are removed; and other layers (third layers) formed in the removed portions are used to form the electrode films **61**.

[0118] In this specific example, the first layers **61***f* may include, for example, amorphous silicon films doped with an impurity. For example, boron is used as the impurity. The second layers **62***f* may include, for example, non-doped amorphous silicon films.

[0119] Although three first layers **61***f* are illustrated for easier viewing of the drawings in FIG. **8**B and FIG. **8**C, the number of the first layers **61***f* is arbitrary in the embodiment.

[0120] The inter-layer insulating film **15** is formed on the stacked films of the first layers **61***f* and the second layers **62***f*. The inter-layer insulating film **15** may include a silicon oxide film. Thereby, a stacked main body MLf used to form the stacked bodies ML is formed.

[0121] As illustrated in FIG. **9**A to FIG. **9**C, a boron-doped silicon oxide film f**5** is formed on the inter-layer insulating film **15**. The boron-doped silicon oxide film f**5** is used as a mask in a subsequent process.

[0122] A second photoresist having the desired second pattern is formed on the boron-doped silicon oxide film f**5** using photolithography. The second pattern is positionally aligned using, for example, the position of the first pattern (the pattern of the connection portions CP) as a reference.

[0123] The boron-doped silicon oxide film f**5** is etched by RIE using the second photoresist as a mask. Subsequently, the second photoresist is removed.

[0124] Then, the stacked main body MLf is etched by RIE using the boron-doped silicon oxide film f**5** as a mask. Thereby, a trench ILt is made in which the partitioning insulating layer IL is formed. The trench ILt has a configuration extending in a band configuration along the X axis.

[0125] Subsequently, a silicon oxide film is formed. The silicon oxide film is filled into the trench ILt. Then, etch-back and planarization of this silicon oxide film are performed using RIE. Thereby, the partitioning insulating layer IL is formed.

[0126] Then, the boron-doped silicon oxide film f**5** is removed using, for example, VPC (hydrofluoric acid vapor).

[0127] As illustrated in FIG. **10**A to FIG. **10**C, an insulating film f**6** is formed on the front surface of the patterning body. The insulating film f**6** may include, for example, a silicon oxide film. For example, PLCVD is used to form the insulating film f**6**.

[0128] Then, a carbon film f**7** is formed. An insulating film f**8** is formed on the carbon film f**7**. The insulating film f**8** may include, for example, a silicon oxide film. For example, coating or CVD is used to form the carbon film f**7** and the insulating film f**8**.

[0129] As illustrated in FIG. **11**A to FIG. **11**C, a third photoresist f**9** having a third pattern is formed using photolithography. The third pattern is positionally aligned using, for example, the position of the first pattern (the pattern of the connection portions CP) as a reference.

[0130] The insulating film f**8** is etched by, for example, RIE using the third photoresist f**9** as a mask.

[0131] Subsequently the third photoresist f**9** is removed.

[0132] As illustrated in FIG. **12**A to FIG. **12**C, the carbon film f**7** is etched by, for example, RIE using the insulating film f**8** as a mask material.

[0133] As illustrated in FIG. **13**A to FIG. **13**C, the insulating film f**6** is etched by, for example, RIE using the carbon film f**7** as a mask.

[0134] At this time, as illustrated in FIG. **13**C, the insulating film f**6** remains on the sidewalls of the partitioning insulating layer IL. Thus, a sidewall mask layer f**6***s* is formed on the sidewalls of a portion of the partitioning insulating layer IL. The thicknesses (a thickness t**11** and a thickness t**12**) along the Y axis of the insulating film f**6** (the sidewall mask layer f**6***s*) remaining on the sidewalls of the partitioning insulating layer IL reflect, for example, the thickness of the insulating film f**6**.

[0135] Thus, the formation of the sidewall mask layer f**6***s* includes forming a sacrificial layer to cover the upper portion of the partitioning insulating layer IL and removing the sacrificial layer except for the portions opposing the sidewalls of the partitioning insulating layer IL.

[0136] As illustrated in FIG. **14**A to FIG. **14**C, the stacked main body MLf is etched by, for example, RIE using the carbon film f**7** and the insulating film f**6** as a mask. Thereby, the through-holes TH (the first through-hole TH**1** and the second through-hole TH**2**, etc.) are made in the stacked main body MLf.

[0137] Subsequently, the second layers **62***f* are removed, for example, via the through-holes TH**1**. At this time, the amorphous silicon film f**4** also is removed.

[0138] Then, for example, a silicon oxide film is filled into the locations where the second layers **62***f* existed. This silicon oxide film is used to form the inter-electrode insulating films **62**. Continuing, the first layers **61***f* are used to form the electrode films **61**. The silicon oxide film formed at this time can be considered to be at least a portion of the memory film SIF of the connection portions CP.

[0139] Subsequently, for example, the outer insulating film **43**, the charge retaining film **48**, and the inner insulating film **42** are formed sequentially inside the through-holes TH.

[0140] Thereby, the memory film SIF is formed.

[0141] Then, a semiconductor material is filled into the remaining space of the through-holes TH. Thereby, the semiconductor pillars SP and the connection portions CP are formed.

[0142] Thus, the method for manufacturing further includes forming the memory film SIF inside the first through-hole TH**1** and the second through-hole TH**2** and forming the first semiconductor pillar and the second semiconductor pillar by filling a semiconductor into the remaining space inside the first through-hole TH**1** and the second through-hole TH**2**.

[0143] Subsequently, the selection gate electrodes SG, various interconnects, and various inter-layer insulating films are formed; and the nonvolatile semiconductor memory device **110** is formed.

[0144] FIG. **15** is a flowchart illustrating the method for manufacturing the nonvolatile semiconductor memory device according to the embodiment.

[0145] This manufacturing method is a method for manufacturing a nonvolatile semiconductor memory device (e.g., the nonvolatile semiconductor memory device **110**), the device including: the first stacked body ML**1** including the multiple first electrode films **61***a* stacked along the first axis and the first inter-electrode insulating film **62***a* provided between two first electrode films **61***a* mutually adjacent along the first axis, the first through-hole TH**1** being provided in the first stacked body ML**1** to extend along the Z axis; the first semiconductor pillar SP**1** filled into the first through-hole TH**1** to extend along the Z axis; the second stacked body ML**2** juxtaposed with the first stacked body ML**1** along the Y axis orthogonal to the Z axis, the second stacked body ML**2** including the multiple second electrode films **61***b* stacked along the Z axis and the second inter-electrode insulating film **62***b* provided between two second electrode films **61***b* mutually adjacent along the Z axis, the second through-hole TH**2** being provided in the second stacked body ML**2** to extend along the Z axis; the second semiconductor pillar SP**2** filled into the second through-hole TH**2** to extend along the Z axis; the connection portion CP electrically connecting the first semiconductor pillar SP**1** to the second semiconductor pillar SP**2**; the memory film provided between the first semiconductor pillar SP**1** and the multiple first electrode films **61***a* and between the second semiconductor pillar SP**2** and the multiple second electrode films **61***b*; and the partitioning insulating layer IL provided between the first stacked body ML**1** and the second stacked body ML**2** to partition the multiple first electrode films **61***a* from the multiple second electrode films **61***b*.

[0146] As illustrated in FIG. **15**, the partitioning insulating layer IL is formed in the stacked main body MLf used to form the first stacked body ML**1** and the second stacked body ML**2** (step S**110**). In other words, the processing described in regard to, for example, FIG. **9**A to FIG. **9**C is implemented.

[0147] Then, the sidewall mask layer f**6***s* is formed on the sidewalls of a portion of the partitioning insulating layer IL (step S**120**). In other words, the processing described in regard to, for example, FIG. **13**A to FIG. **13**C is implemented.

[0148] Continuing, the first through-hole TH**1** and the second through-hole TH**2** are made in the stacked main body MLf by using the sidewall mask layer f**6***s* as a portion of a mask (step S**130**). In other words, the processing described in regard to, for example, FIG. **14**A to FIG. **14**C is implemented.

[0149] Thus, in the manufacturing method, the through-holes TH are made by patterning using the sidewall mask layer f**6***s* provided on the sidewalls of a portion of the partitioning insulating layer IL as a mask. The thickness of the sidewall mask layer f**6***s* is substantially the same as, for example, the thickness of the insulating film f**6**.

[0150] The thickness t**11** along the Y axis of the sidewall mask layer f**6***s* on the first through-hole TH**1** side illustrated in FIG. **14**C is substantially the same as the first distance d**1** illustrated in FIG. **5**. Also, the thickness t**12** along the Y axis of the sidewall mask layer f**6***s* on the second through-hole TH**2** side is substantially the same as the second distance d**2** illustrated in FIG. **5**.

[0151] Thus, in the nonvolatile semiconductor memory device **110** manufactured using the manufacturing method, the first distance d**1** is substantially equal to the second distance d**2**.

[0152] In other words, in the embodiment, the through-holes TH are formed self-aligningly with respect to the partitioning insulating layer IL.

[0153] Therefore, in the nonvolatile semiconductor memory device according to the embodiment and the method for manufacturing the same, the design margin considering the shift of the positional alignment of the photomask for the patterning can be reduced. Thereby, the distance between the partitioning insulating layer IL and the through-holes TH can be reduced; and the spacing between the memory cells MC can be reduced. Thereby, the size per memory cell MC can be reduced further; and the storage density can be increased.

[0154] FIG. **16** is a schematic cross-sectional view illustrating the configuration of a nonvolatile semiconductor memory device of a reference example.

[0155] In the nonvolatile semiconductor memory device **119** of the reference example as illustrated in FIG. **16**, the distance (the first distance d**1**) along the Y axis between the partitioning insulating layer IL and the ends of the first electrode films **61***a* on the partitioning insulating layer IL side is different from the distance (the second distance d**2**) along the Y axis between the partitioning insulating layer IL and the ends of the second electrode films **61***b* on the partitioning insulating layer IL side.

[0156] In such a nonvolatile semiconductor memory device **119**, the sidewall mask layer f**6***s* is not used as a portion of the mask in the process of making the first through-hole TH**1** and the second through-hole TH**2** in the stacked main body MLf. For example, the through-holes TH are made in the stacked main body MLf using only the mask material having the fourth pattern that has openings corresponding to the through-holes TH. In the method, the position of the fourth pattern shifts with respect to the position of the pattern of the patterning of the partitioning insulating layer IL (e.g., the second pattern). Therefore, the positions of the through-holes TH shift relative to the position of the partitioning insulating layer IL. Then, this shift causes the distance between the partitioning insulating layer IL and the through-holes TH to change.

[0157] In such a nonvolatile semiconductor memory device **119**, for example, as illustrated in FIG. **16**, one of the through-holes TH is too proximal to the partitioning insulating layer IL. In this example, the first through-hole TH**1** is too proximal to the partitioning insulating layer IL; and the widths of the first electrode films **61***a* between the first through-hole TH**1** and the partitioning insulating layer IL are extremely narrow. For example, there also may be cases where the first electrode films **61***a* between the first through-hole TH**1** and the partitioning insulating layer IL are divided. Therefore, the electrical resistance of the first electrode films **61***a* of the portion between the first through-hole TH**1** and the partitioning insulating layer IL is high. Thereby, it becomes difficult to obtain the desired electrical characteristics.

[0158] Therefore, in the reference example, it is necessary to set the distance between the first through-hole TH**1** and the second through-hole TH**2** to be large. In the reference example, it is difficult to sufficiently reduce the size per memory cell MC.

[0159] Conversely, in the nonvolatile semiconductor memory device **110** according to the embodiment and the method for manufacturing the same, the through-holes TH are formed self-alignedly with respect to the partitioning insulating layer IL. Thereby, the size per memory cell MC can be reduced further; and the storage density can be increased.

[0160] FIG. **17**A and FIG. **17**B are schematic cross-sectional views illustrating the configuration of another nonvolatile semiconductor memory device according to the embodiment.

[0161] In the nonvolatile semiconductor memory device **111** according to the embodiment as illustrated in FIG. **17**A, the configurations of the first through-hole TH**1** and the second through-hole TH**2** cut by the X-Y plane are configurations in which a semicircle and a rectangle are combined.

[0162] In other words, the length along the X axis of the planar portion of the sidewall of the first through-hole TH**1** on the partitioning insulating layer IL side is substantially equal to the lengths of the first through-hole TH**1** along the X axis and along the Y axis. The length along the X axis of the planar portion of the sidewall of the second through-hole TH**2** on the partitioning insulating layer IL side is substantially equal to the lengths of the second through-hole TH**2** along the X axis and along the Y axis.

[0163] In such a case as well, the side surface of the first through-hole TH**1** on the partitioning insulating layer IL side and the side surface of the second through-hole TH**2** on the partitioning insulating layer IL side have portions parallel to the X-Z plane. The side surface of the first through-hole TH**1** on the side opposite to the partitioning insulating layer IL and the side surface of the second through-hole TH**2** on the side opposite to the partitioning insulating layer IL have curved configurations parallel to the Z axis.

[0164] The distance (the first distance d**1**) along the Y axis between the partitioning insulating layer IL and the ends of the first electrode films **61***a* on the partitioning insulating layer IL side is substantially the same as the distance (the second distance d**2**) along the Y axis between the partitioning insulating layer IL and the ends of the second electrode films **61***b* on the partitioning insulating layer IL side.

[0165] In another nonvolatile semiconductor memory device **112** according to the embodiment as illustrated in FIG. **17**B, the side surface of the first through-hole TH**1** on the partitioning insulating layer IL side has a portion parallel to the X-Z plane. On the other hand, the side surface of the second through-hole TH**2** on the partitioning insulating layer IL side does not have a portion parallel to the X-Z plane. In other words, in this example, the configuration of the second through-hole TH**2** cut by the X-Y plane is circular (including flattened circular).

[0166] This configuration occurs, for example, when the shift amount of the positional alignment of the mask for making the through-holes TH is large. In this example, the width of the first through-hole TH**1** along the Y axis is different from the width of the second through-hole TH**2** along the Y axis.

[0167] Thus, even in the case where the shift amount of the positional alignment of the mask is large, the first distance d**1** between the first through-hole TH**1** and the partitioning insulating layer IL and the second distance d**2** between the second through-hole TH**2** and the partitioning insulating layer IL are maintained at constants.

[0168] Thus, in the nonvolatile semiconductor memory device **112** as well, the first distance d**1** along the Y axis between the partitioning insulating layer IL and the ends of the first electrode films **61***a* on the partitioning insulating layer IL side is substantially the same as the second distance d**2** along the Y axis between the partitioning insulating layer IL and the ends of the second electrode films **61***b* on the partitioning insulating layer IL side. In other words, the prescribed distance can be set between the first through-hole TH**1** and the partitioning insulating layer IL and between the second through-hole TH**2** and the partitioning insulating layer IL. Therefore, the desired electrical characteristics of the electrode films **61** are obtained. Accordingly, the size per memory cell MC can be reduced further and the storage density can be increased while maintaining the prescribed characteristics.

[0169] FIG. **18** is a schematic cross-sectional view illustrating the configuration of another nonvolatile semiconductor memory device according to the embodiment.

[0170] Namely, FIG. **18** illustrates the configuration of the memory cell array unit MCU of the nonvolatile semiconductor memory device **113** according to the embodiment.

[0171] FIG. **19** is a schematic cross-sectional view illustrating the configuration of the nonvolatile semiconductor memory device according to the embodiment.

[0172] FIG. **19** is a cross-sectional view along line C**1**-C**2** of FIG. **18**.

[0173] In the nonvolatile semiconductor memory device **113** as illustrated in FIG. **18** and FIG. **19**, the multiple first electrode films **61***a* have portions (first silicided portions **61***sa*) including silicide in contact with the memory film SIF. The multiple second electrode films **61***b* have portions (second silicided portions **61***sb*) including silicide in contact with the memory film SIF. Thus, the electrode films **61** may have silicided portions **61***s* including silicide and contacting the memory film SIF.

[0174] In such a case, for example, the first silicided portions **61***sa* (the portions of the first electrode films **61***a* including silicide in contact with the memory film SIF) are disposed around the portions of the memory film SIF opposing the first electrode films **61***a*. The second silicided portions **61***sb* (the portions of the second electrode films **61***b* including silicide and contacting the memory film SIF) are disposed around the portions of the memory film SIF opposing the second electrode films **61***b*.

[0175] Thereby, the electrical characteristics of the electrode films **61** improve; and the operating characteristics of the memory cells MC improve.

[0176] An example of a method for manufacturing the nonvolatile semiconductor memory device **113** will now be described.

[0177] FIG. **20**A to FIG. **20**C are schematic views illustrating the method for manufacturing the nonvolatile semiconductor memory device according to the embodiment.

[0178] Namely, these drawings illustrate processes after the processes illustrated in FIG. **14**A to FIG. **14**C. FIG. **20**A is a schematic plan view. FIG. **20**B is a cross-sectional view along line B**1**-B**2** of FIG. **20**A. FIG. **20**C is a cross-sectional view along line A**1**-A**2** of FIG. **20**A.

[0179] The stacked bodies ML including the inter-electrode insulating films **62** and the electrode films **61** are formed as described in regard to FIG. **14**A to FIG. **14**C. Subsequently, as illustrated in FIG. **20**A to FIG. **20**B, portions of the electrode films **61** (the first electrode films **61***a* and the second electrode films **61***b*, etc.) are silicided via the through-holes TH (the first through-hole TH**1**, the second through-hole TH**2**, etc.). Thereby, the silicided portions **61***s* are formed in the electrode films **61** of the surface portions of the interior surfaces of the through-holes TH.

[0180] Subsequently, similarly to the methods described above, the memory film SIF is formed by sequentially forming the outer insulating film **43**, the charge retaining film **48**, and the inner insulating film **42** inside the through-holes TH. Then, the semiconductor pillars SP and the connection portions CP are formed by filling a semiconductor material into the remaining space of the through-holes TH.

[0181] In other words, the manufacturing method further includes forming the memory film SIF inside the first through-hole TH**1** and the second through-hole TH**2** and forming the first semiconductor pillar SP**1** and the second semiconductor pillar SP**2** by filling a semiconductor into the remaining space inside the first through-hole TH**1** and the second through-hole TH**2**.

[0182] Subsequently, the nonvolatile semiconductor memory device **113** is formed by forming the selection gate electrodes SG, various interconnects, and various inter-layer insulating films.

[0183] In the nonvolatile semiconductor memory device **113** as well, the size per memory cell MC can be reduced further; and the storage density can be increased. Also, the operating characteristics of the memory cells MC can be improved.

[0184] In the manufacturing method recited above, the making of the first through-hole TH**1** and the second through-hole TH**2** (step S**130**) includes patterning the stacked main body MLf using a mask (e.g., the carbon film f**7**, etc.) that has openings of a curved configuration (the first curved configuration) corresponding to the configuration of the side surface of the first through-hole TH**1** on the side opposite to the partitioning insulating layer IL and a curved configuration (the second curved configuration) corresponding to the configuration of the side surface of the second through-hole TH**2** on the side opposite to the partitioning insulating layer IL.

[0185] For example, the first curved configuration has a protruding configuration protruding in the direction from the partitioning insulating layer IL toward the first through-hole TH**1**; and the second curved configuration has a protruding configuration protruding in the direction from the partitioning insulating layer IL toward the second through-hole TH**2**.

[0186] Thereby, the side surface of the first through-hole TH**1** on the side opposite to the partitioning insulating layer IL can have a protruding configuration protruding in the direction from the partitioning insulating layer IL toward the first through-hole TH**1**. The side surface of the second through-hole TH**2** on the side opposite to the partitioning insulating layer IL can have a protruding configuration protruding in the direction from the partitioning insulating layer IL toward the second through-hole TH**2**. Thereby, the curvature of the portion of the inner insulating film **42** on the side opposite to the partitioning insulating layer IL is larger than the curvature of the portion of the outer insulating film **43** on the side opposite to the partitioning insulating layer IL. Thereby, the relationship between the electric field of the inner insulating film **42** and the electric field of the outer insulating film **43** can be corrected; and the operations stabilize.

[0187] According to the embodiment, a nonvolatile semiconductor memory device having a higher storage density and a method for manufacturing the same are provided.

[0188] In the specification of the application, "perpendicular" and "parallel" refer to not only strictly perpendicular and strictly parallel but also include, for example, the fluctuation due to manufacturing processes, etc. It is sufficient to be substantially perpendicular and substantially parallel.

[0189] Hereinabove, exemplary embodiments of the invention are described with reference to specific examples. However, the embodiments of the invention are not limited to these specific examples. For example, one skilled in the art may similarly practice the invention by appropriately selecting specific configurations of components included in nonvolatile semiconductor memory devices such as stacked bodies, electrode films, inter-electrode insulating films, charge retaining films, memory films, connection portions, partitioning insulating layers, substrates, interconnects, etc., from known art. Such practice is included in the scope of the invention to the extent that similar effects are obtained.

[0190] Further, any two or more components of the specific examples may be combined within the extent of technical feasibility and are included in the scope of the embodiments to the extent that the spirit of the embodiments is included.

[0191] Moreover, all nonvolatile semiconductor memory devices and methods for manufacturing nonvolatile semiconductor memory devices practicable by an appropriate design modification by one skilled in the art based on the nonvolatile semiconductor memory devices and the methods for manufacturing nonvolatile semiconductor memory devices described above as embodiments of the invention also are within the scope of the invention to the extent that the spirit of the invention is included.

[0192] Furthermore, various modifications and alterations within the spirit of the invention will be readily apparent to those skilled in the art.

[0193] While certain embodiments have been described, these embodiments have been presented by way of example only, and are not intended to limit the scope of the inventions. Indeed, the novel embodiments described herein may be embodied in a variety of other forms; furthermore, various omissions, substitutions and changes in the form of the embodiments described herein may be made without departing from the spirit of the inventions. The accompanying claims and their equivalents are intended to cover such forms or modifications as would fall within the scope and spirit of the inventions.

What is claimed is:

1. A nonvolatile semiconductor memory device, comprising:

a first stacked body including a plurality of first electrode films stacked along a first axis and a first inter-electrode insulating film provided between two of the first electrode films mutually adjacent along the first axis, a first through-hole being provided in the first stacked body to extend along the first axis;

a first semiconductor pillar filled into the first through-hole to extend along the first axis;

a second stacked body juxtaposed with the first stacked body along a second axis orthogonal to the first axis, the second stacked body including a plurality of second electrode films stacked along the first axis and a second inter-electrode insulating film provided between two of the second electrode films mutually adjacent along the first axis, a second through-hole being provided in the second stacked body to extend along the first axis;

a second semiconductor pillar filled into the second through-hole to extend along the first axis;

a connection portion electrically connecting the first semiconductor pillar to the second semiconductor pillar;

a memory film provided between the first semiconductor pillar and the plurality of first electrode films and between the second semiconductor pillar and the plurality of second electrode films; and

a partitioning insulating layer provided between the first stacked body and the second stacked body to partition the plurality of first electrode films from the plurality of second electrode films,

at least one selected from a side surface of the first through-hole on the partitioning insulating layer side and a side surface of the second through-hole on the partitioning insulating layer side being configured to have a portion parallel to a plane including the first axis and a third axis orthogonal to the first and second axes.

2. The device according to claim **1**, wherein a distance along the second axis from the partitioning insulating layer to an end of the plurality of first electrode films on the partitioning insulating layer side is the same as a distance along the second axis from the partitioning insulating layer to an end of the plurality of second electrode films on the partitioning insulating layer side.

3. The device according to claim **1**, wherein a side surface of the first through-hole on a side opposite to the partitioning insulating layer and a side surface of the second through-hole on a side opposite to the partitioning insulating layer have curved configurations parallel to the first axis.

4. The device according to claim **1**, wherein a side surface of the memory film on the partitioning insulating layer side has a portion parallel to the plane.

5. The device according to claim **1**, wherein at least one selected from a side surface of the first semiconductor pillar on the partitioning insulating layer side and a side surface of the second semiconductor pillar on the partitioning insulating layer side has a portion parallel to the plane.

6. The device according to claim **1**, wherein:

a side surface of the first through-hole on a side opposite to the partitioning insulating layer has a protruding configuration protruding in a direction from the partitioning insulating layer toward the first through-hole; and

a side surface of the second through-hole on a side opposite to the partitioning insulating layer has a protruding configuration protruding in a direction from the partitioning insulating layer toward the second through-hole.

7. The device according to claim **1**, wherein a distance along the second axis from the partitioning insulating layer to an end of the first semiconductor pillar on the partitioning insulating layer side is the same as a distance along the second axis from the partitioning insulating layer to an end of the second semiconductor pillar on the partitioning insulating layer side.

8. The device according to claim **1**, wherein a width of the first through-hole along the second axis is different from a width of the second through-hole along the second axis.

9. The device according to claim **1**, wherein:

the plurality of first electrode films has a portion that contacts the memory film and includes a silicide; and

the plurality of second electrode films has a portion that contacts the memory film and includes a silicide.

10. The device according to claim **9**, wherein:

the portion of the plurality of first electrode films including the silicide and contacting the memory film is disposed along the first axis around a portion of the memory film opposing the first electrode films; and

the portion of the plurality of second electrode films including the silicide and contacting the memory film is disposed along the first axis around a portion of the memory film opposing the second electrode films.

11. The device according to claim **1**, wherein:

the memory film includes a charge retaining film, an inner insulating film, and an outer insulating film;

the charge retaining film is provided between the first semiconductor pillar and the first electrode films and between the second semiconductor pillar and the second electrode films;

the inner insulating film is provided between the first semiconductor pillar and the charge retaining film and between the second semiconductor pillar and the charge retaining film; and

the outer insulating film is provided between the charge retaining film and the first electrode films and between the charge retaining film and the second electrode films.

12. A method for manufacturing a nonvolatile semiconductor memory device, the device including: a first stacked body including a plurality of first electrode films stacked along a first axis and a first inter-electrode insulating film provided between two of the first electrode films mutually adjacent along the first axis, a first through-hole being provided in the first stacked body to extend along the first axis; a first semiconductor pillar filled into the first through-hole to extend along the first axis; a second stacked body juxtaposed with the first stacked body along a second axis orthogonal to the first axis, the second stacked body including a plurality of second electrode films stacked along the first axis and a second inter-electrode insulating film provided between two of the second electrode films mutually adjacent along the first axis, a second through-hole being provided in the second stacked body to extend along the first axis; a second semiconductor pillar filled into the second through-hole to extend along the first axis; a connection portion electrically connecting the first semiconductor pillar to the second semiconductor pillar; a partitioning insulating layer provided between the first stacked body and the second stacked body to partition the plurality of first electrode films from the plurality of second electrode films; and a memory film provided between the first semiconductor pillar and the plurality of first electrode films and between the second semiconductor pillar and the plurality of second electrode films, the method comprising:

forming the partitioning insulating layer in a stacked main body used to form the first stacked body and the second stacked body;

forming a sidewall mask layer on a sidewall of a portion of the partitioning insulating layer; and

making the first through-hole and the second through-hole in the stacked main body by using the sidewall mask layer as a portion of a mask.

13. The method according to claim **12**, wherein the making of the first through-hole and the second through-hole includes patterning the stacked main body by using a mask having openings, the openings having a curved configuration corresponding to a configuration of a side surface of the first through-hole on a side opposite to the partitioning insulating layer and a curved configuration corresponding to a configuration of a side surface of the second through-hole on a side opposite to the partitioning insulating layer.

14. The method according to claim **13**, wherein:

the curved configuration corresponding to the configuration of the side surface of the first through-hole on the side opposite to the partitioning insulating layer has a protruding configuration protruding in a direction from the partitioning insulating layer toward the first through-hole; and

the curved configuration corresponding to the configuration of the side surface of the second through-hole on the side opposite to the partitioning insulating layer has a protruding configuration protruding in a direction from the partitioning insulating layer toward the second through-hole.

15. The method according to claim **12**, wherein the making of the first through-hole and the second through-hole includes forming a portion parallel to a plane including the first axis and a third axis orthogonal to the first and second axes in at least one selected from a side surface of the first through-hole on the partitioning insulating layer side and a side surface of the second through-hole on the partitioning insulating layer side.

16. The method according to claim **12**, wherein the forming of the sidewall mask layer includes forming a sacrificial layer to cover an upper portion of the partitioning insulating layer and removing the sacrificial layer except for a portion of the sacrificial layer opposing the sidewall of the partitioning insulating layer.

17. The method according to claim **12**, further comprising:

forming a memory film inside the first through-hole and the second through-hole; and

forming the first semiconductor pillar and the second semiconductor pillar by filling a semiconductor into a remaining space inside the first through-hole and the second through-hole.

18. The method according to claim **17**, wherein the forming of the first semiconductor pillar and the second semiconductor pillar includes causing a distance along the second axis from the partitioning insulating layer to an end of the first semiconductor pillar on the partitioning insulating layer side to be the same as a distance along the second axis from the partitioning insulating layer to an end of the second semiconductor pillar on the partitioning insulating layer side.

19. The method according to claim **12**, further comprising siliciding a portion of the first electrode film and siliciding a portion of the second electrode film via the first through-hole and the second through-hole.

20. The method according to claim **19**, further comprising

forming a memory film inside the first through-hole and the second through-hole and

forming the first semiconductor pillar and the second semiconductor pillar by filling a semiconductor into a remaining space inside the first through-hole and the second through-hole

after the siliciding of the portion of the first electrode film and the siliciding of the portion of the second electrode film.

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