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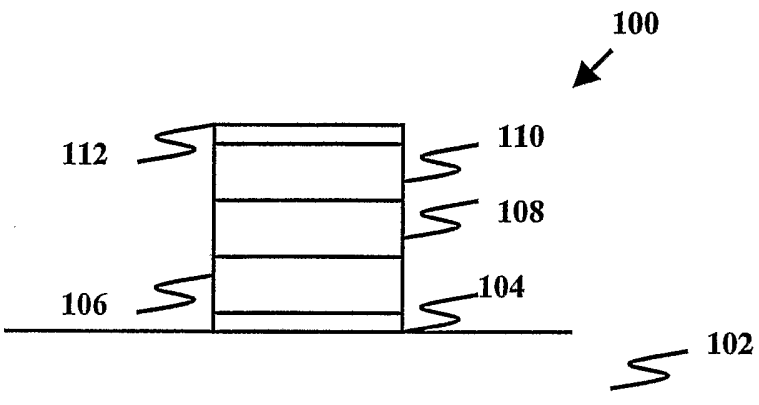
(54) Title: MEMORY GATE STACK STRUCTURE



(57) Abstract: A memory gate stack structure (100) comprising a substrate layer (102) comprising a silicon-based material, a tunnel layer (104) formed on the substrate layer, a charge storage layer (106) formed on the tunnel layer and comprising a hafnium-aluminium-oxide-based material, a blocking layer (108) formed on the charge storage layer, and a gate layer (110) formed on the blocking layer.

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MEMORY GATE STACK STRUCTURE

FIELD OF INVENTION

The present invention relates broadly to a memory gate stack structure, and to a method of fabricating a memory gate stack structure. The present invention will be described herein with reference to a gate stack for a memory transistor structure, however, it will be appreciated that the present invention does have broader applications. For example it may be applied in capacitor memory structures.

BACKGROUND

The applications of digital electronics have resulted in a demand for nonvolatile memories that are densely integrated, fast, and consume little power. The metal-oxide-nitride-oxide-semiconductor (MONOS) device is a promising candidate to replace existing forms of flash memory.

The MONOS structure has better charge retention than for example a polysilicon floating-gate type memory as the charges are stored in spatially isolated deep-level traps. Hence, a single defect in the tunnel oxide will generally not cause the discharge of the memory cell.

In MONOS device operation, electrons are involved in the program operation while both electrons and holes are involved in the erase operation. Hence threshold voltage control after erasing is difficult. If the electrical erase continues beyond a specified point, it will result in more positive charges in the silicon nitride (Si_3N_4) storage layer, resulting in over-erase.

A need exists, therefore, to provide a memory gate stack structure in which over-erase effects are reduced, while maintaining acceptable charge retention. In at least preferred embodiment, the present invention addresses that need.

SUMMARY OF THE INVENTION

In accordance with a first aspect of the present invention there is provided a memory gate stack structure comprising:

a substrate layer comprising a silicon-based material,

a tunnel layer formed on the substrate layer,

a charge storage layer formed on the tunnel layer and comprising a hafnium-aluminium-oxide-based material,

a blocking layer formed on the charge storage layer, and

a gate layer formed on the blocking layer.

The charge storage layer may comprise $(HfO_2)_x(Al_2O_3)_{1-x}$, with x in a range from about 0.4 to 0.95. In one embodiment, x is about 0.9.

The tunnel layer and/or the blocking layer may comprise silica-based materials.

In one embodiment, the tunnel layer comprises a silicon oxide formed by rapid thermal oxidation of the silicon-based material of the substrate layer.

The gate layer may comprise a metal, metal nitride, silicide or polysilicon materials. In one embodiment, the metal material may comprise HfN.

The memory gate stack structure may further comprise a capping layer on the gate layer. In one embodiment the capping layer may comprise TaN.

The blocking layer comprise $(Si(OC_2H_5)_4)$.

In accordance with a second aspect of the present invention there is provided a method of fabricating a memory gate stack structure, comprising the steps of:

providing a substrate layer comprising a silicon-based material,

forming a tunnel layer on the substrate layer,

forming a charge storage layer on the tunnel layer and comprising a hafnium-aluminium-oxide-based material,

forming a blocking layer on the charge storage layer, and

forming a gate layer on the blocking layer.

The charge storage layer may comprise $(HfO_2)_x(Al_2O_3)_{1-x}$, with x in a range from about 0.4 to 0.95. In one embodiment, x is about 0.9.

The tunnel layer and/or the blocking layer may comprise silica-based materials.

In one embodiment, the tunnel layer comprises a silicon oxide formed by rapid thermal oxidation of the silicon-based material of the substrate layer.

The blocking layer may comprise $(Si(OC_2H_5)_4)$. The blocking layer may be formed utilising low-pressure chemical-vapor-deposition (CVD).

The gate layer may comprise a metal, metal nitride, silicide or polysilicon materials. In one embodiment, the metal material may comprise HfN.

The gate layer may be formed utilising sputter deposition techniques.

The method may further comprise the step of forming a capping layer on the gate layer. In one embodiment, the capping layer may comprise TaN.

The capping layer may be formed utilising sputter deposition techniques.

In accordance with a third aspect of the present invention there is provided a memory gate stack structure comprising:

a substrate layer comprising a silicon-based material,

a tunnel layer formed on the substrate layer,

a charge storage layer formed on the tunnel layer,

a blocking layer formed on the charge storage layer, and

a gate layer formed on the blocking layer,

wherein the charge storage layer comprises an amorphous material exhibiting a larger valence band offset with respect to the silicon-based material compared to Si_3N_4, and exhibiting a smaller conduction band offset with respect to the silicon-based material compared to Al_2O_3.

In accordance with a fourth aspect of the present invention there is provided a method of fabricating a memory gate stack structure, comprising the steps of:

providing a substrate layer comprising a silicon-based material,

forming a tunnel layer on the substrate layer,

forming a charge storage layer on the tunnel layer,

forming a blocking layer on the charge storage layer, and

forming a gate layer on the blocking layer,

wherein the charge storage layer comprises an amorphous material exhibiting a larger valence band offset with respect to the silicon-based material compared to Si_3N_4, and exhibiting a smaller conduction band offset with respect to the silicon-based material compared to Al_2O_3.

BRIEF DESCRIPTION OF THE DRAWINGS

Embodiments of the invention will be better understood and readily apparent to one of ordinary skill in the art from the following written description, by way of example only, in conjunction with the drawings, in which:

Fig. 1 is a schematic cross-sectional view of a general memory gate stack structure.

Fig. 2(a) shows capacitance versus charging time (C-t) curves at a charging voltage of 6V, for a memory gate stack structure embodying the present invention and in comparison with other memory gate stack structures.

Fig. 2(b) shows normalised discharge C-t curves during discharging at a gate bias of –1.45V, for a memory gate stack structure embodying the present invention and in comparison with other memory gate stack structures.

Fig. 3(a) shows capacitance versus voltage curves for a memory gate stack structure embodying the present invention.

Fig. 3(b) shows capacitance versus voltage curves of another memory gate stack structure for comparison.

Fig. 3(c) shows capacitance versus voltage curves of another memory gate stack structure for comparison.

Fig. 4(a) shows plots of the density of stored charge, extracted from the curves shown in Figs. 3(a) – (c), and plotted as a function of the range of gate voltage sweep for a memory gate stack structure embodying the present invention and in comparison with other memory gate stack structures.

Fig. 4(b) shows plots of flatband voltage shift against the charging/discharging voltage for a memory gate stack structure embodying the present invention and in comparison with other memory gate stack structures.

Fig. 5 is a schematic cross-sectional view of a memory transistor structure embodying the present invention.

Fig. 6 shows a flow-chart 600 illustrating a method of fabricating a memory gate stack structure in an embodiment of the present invention

DETAILED DESCRIPTION

The preferred embodiment described provides a memory gate stack structure for use in a memory transistor having both an acceptable over-erase characteristic, and an acceptable charge retention capability.

In order to obtain comparative data on the function of gate stack structures for a memory transistor, four different memory gate stack structures were fabricated and analysed. Figure 1 is a schematic cross sectional view of the general memory gate stack structure 100, consisting of a substrate 102, a tunnel layer 104, a charge storage layer 106, a blocking layer 108, a gate layer 110, and a capping layer 112.

For each device, the processing conditions were the same except for the formation of the charge storage layer 106, that is, Si_3N_4 for a conventional MONOS

device, HfO_2 for a comparative device, HfAlO (or $(HfO_2)_x(Al_2O_3)_{1-x}$) for a device embodying the present invention, and Al_2O_3 for another comparative device.

Details of the structures used in conjunction with an example embodiment of the invention were as follows. The substrate 102 used was 4-8 Ω-cm (100) p-type silicon. The 25 Å thick tunnel oxide 104 was grown by rapid thermal oxidation at 1000°C. After tunnel oxide formation, Si_3N_4 (60 Å) was deposited by low-pressure chemical-vapor-deposition (LPCVD) while HfO_2 (60 Å) and Al_2O_3 (60 Å) were deposited by atomic layer deposition (ALD), as the respective charge storage layers 106. $(HfO_2)_x(Al_2O_3)_{1-x}$, with x = 0.9 and abbreviated as HfAlO henceforth, was deposited as a charge storage layer 106 by metal-organic-chemical-vapor-deposition (MOCVD), followed by post-deposition-annealing (PDA) at 700°C in nitrogen ambient for 60 seconds. The blocking oxide 108 (55 Å) was deposited as LPCVD TEOS ($Si(OC_2H_5)_4$). HfN metal gate electrode 110 (~50nm) and TaN (~100nm) capping layer 112 were deposited by reactive sputtering of Hf and Ta targets, respectively, in an Ar + N_2 ambient. The fabricated gate stacks had a gate area of 800 × 800 μm^2

The programming speeds of the various gate stack memory structures with HfO_2, Al_2O_3, HfAlO or Si_3N_4 as the respective charge storage layers were evaluated by measuring the capacitance versus time (C-t) curve during charging at 6 V gate bias, as shown in Fig. 2(a). The slope in the C-t curve is proportional to the rate of change in the stored charge of the gate stack at a constant bias voltage. From Fig. 2(a), it can be seen that the Al_2O_3 device (curve 200) charges up much more slowly as compared to the other memory gate stacks (curves 202, 204, and 206).

The charge retention performance was evaluated by measuring the C-t characteristics, after the device has been charged at 6 V for 80 s, at a constant discharge gate bias of -1.45 V with respect to the initial flatband voltage of the charged device. Figure 2(b) shows the normalized discharge C-t, or C(t)/C(t=0), curves. From Fig. 2(b) it can be seen that HfAlO (curve 210) has comparable charge retention performance to Si_3N_4 (curve 212). Al_2O_3 (curve 214) has the best retention characteristics while HfO_2 (curve 216) has the worst retention. From the results shown in Fig. 2, it was discovered that there is a tradeoff between programming speed and charge retention. It was recognised that as deposited HfO_2 is already crystallized while HfAlO is still amorphous even after annealing at 700°C, 60s. From Fig. 2(b), the amorphous films, which are Si_3N_4, Al_2O_3 and HfAlO (curves 212, 214 and 210 respectively), show significantly better retention performance compared to

crystallized HfO_2 (curve 216). Polycrystallization of thin films may generate grain boundaries, which may act as current leakage paths.

The charge storage performance of memory devices with good retention characteristics, namely those with Al_2O_3, HfAlO or Si_3N_4 as the respective charge storage layers (curves 214, 210 and 212 respectively), was further investigated by measuring the hysteresis in the capacitance-voltage (C-V) curves. The C-V curves with counter-clockwise hysteresis are shown in Figs. 3(a), (b) and (c), for HfAlO, Si_3N_4 and Al_2O_3 respectively. It can be seen from Fig. 3 and Fig. 4(a), which summarises the charge storage characteristics over the gate voltage, that the charge storage capability of Al_2O_3 devices (Fig. 3(c) and curve 400 in Fig. 4(a)) is the smallest while that of HfAlO (Fig. 3(a) and curve 402 in Fig. 4(a)) and Si_3N_4 (Fig. 3(b) and curve 404 in Fig. 4(a)) devices are comparable.

Figure 4(b) shows the shift in flatband voltage from that of the quasi-neutral condition, whereby the gate voltage sweep is restricted to a very small range to minimize charging of the device, for positive (program) and negative (erase) gate voltages. Both HfAlO and Al_2O_3 devices (curves 406 and 408 respectively) show better over-erase performance than Si_3N_4 devices (curve 410), with over-erase free characteristics up to a negative gate voltage sweep of -8 V and -10 V for HfAlO and Al_2O_3 devices, respectively, as compared to -4 V for Si_3N_4 devices. However, the Al_2O_3 device has the smallest charge storage capacity and the slowest charging rate of the three memory structures (see curve 400 in Fig. 4(a) and curve 200 in Fig. 2(a)). Using HfAlO as the charge storage layer in the preferred embodiment results in optimization of the charge storage and erase performance of the memory structure.

The observed differences in charge storage and electron/hole injection (i.e., program/erase) characteristics and programming speed of the various structures may be explained by differences in the bandgap, valence and conduction band offsets of the various films with respect to silicon. The valence band offset of Si_3N_4 with respect to Si is the smallest, at 2eV, compared to 3.3eV for HfAlO and 4.9eV for Al_2O_3. The conduction band offset between HfAlO and Si is the smallest, at 1.6eV, as compared to 2eV for Si_3N_4 and 2.8eV for Al_2O_3.

Figure 5 is a schematic cross-sectional drawing of a memory transistor structure 500. The memory transistor structure 500 comprises a silicon-based substrate layer 502, in which a source region 504 and a drain region 506 are formed, for example through appropriate doping in the respective areas. A tunnel

layer 508 is formed on the substrate layer 502, and extends over the substrate region 510 between the source and drain regions 504 and 506 respectively. The tunnel layer also extends over portions of the source and drain regions 504, 506 respectively.

A charge storage layer 510 comprising a hafnium-aluminium-oxide-based material is formed on the tunnel layer 508. A blocking layer 512 is formed on the charge storage layer 510, and a gate layer 514 is formed on the blocking layer 512, completing the memory transistor structure 500 in an example embodiment.

Figure 6 shows a flow-chart 600 illustrating a method of fabricating a memory gate stack structure in an embodiment of the present invention. It comprises, at step 602, providing a substrate layer comprising a silicon-based material. At step 604, a tunnel layer is formed on the substrate layer. At step 606, a charge storage layer comprising a hafnium-aluminium-oxide-based material is formed on the tunnel layer. A blocking layer is formed on the charge storage layer at step 608, and, at step 610, a gate layer is formed on the blocking layer.

In the foregoing manner, a memory gate stack structure for e.g. a memory transistor and a method for fabricating the same are disclosed. Only several embodiments are described. However, it will be apparent to one skilled in the art in view of this disclosure that numerous changes and/or modifications may be made without departing from the scope of the invention.

For example, it will be appreciated by the person skilled in the art that the present invention is not limited to the deposition techniques and/or dimensioning of the memory gate stack structure of the embodiments described. In other embodiments, the thickness of the tunnel layer may, for example, be in the range from, but is not limited to, about 10 to 100Å, the charge storage layer thickness may be in the range from, but is not limited to, about 30 to 200Å, and the blocking layer thickness may be in the range from, but is not limited to, about 30 to 200Å.

Also, the gate layer may be made from a different material including, for example, one or more of metal, metal nitride, silicide or polysilicon materials. Also, the charge storage layer may be formed from different hafnium-aluminium-oxide-based materials, including e.g. $(HfO_2)_x(Al_2O_3)_{1-x}$, with x in the range from about 0.4 to 0.95.

CLAIMS

1. A memory gate stack structure comprising:

a substrate layer comprising a silicon-based material,

a tunnel layer formed on the substrate layer,

a charge storage layer formed on the tunnel layer and comprising a hafnium-aluminium-oxide-based material,

a blocking layer formed on the charge storage layer, and

a gate layer formed on the blocking layer.

2. The memory gate stack structure as claimed in claim 1, wherein the charge storage layer comprises $(HfO_2)_x(Al_2O_3)_{1-x}$, with x in a range from about 0.4 to 0.95.

3. The memory gate stack structure as claimed in claim 2, wherein x is about 0.9.

4. The memory gate stack structure as claimed in any one of the proceeding claims, wherein the tunnel layer and/or the blocking layer comprise one or more silica-based materials.

5. The memory gate stack structure as claimed in claim 4, wherein the tunnel layer comprises a silicon oxide formed by rapid thermal oxidation of the silicon-based material of the substrate layer.

6. The memory gate stack structure as claimed in claims 4 or 5, wherein the blocking layer comprises $(Si(OC_2H_5)_4)$.

7. The memory gate stack structure as claimed in any one of the preceding claims, wherein the gate layer comprises one or more of a group comprising a metal, metal nitride, silicide and polysilicon materials.

8. The memory gate stack structure as claimed in claim 7, wherein the metal material comprises HfN.

9. The memory gate stack structure as claimed in any one of the preceding claims, wherein the memory gate stack structure further comprises a capping layer on the gate layer.

10. The memory gate stack structure as claimed in claim 9, wherein the capping layer comprises TaN.

11. The memory gate stack structure as claimed in any one of claims 1 to 10, wherein the substrate layer comprises a source region and a drain region.

12. A method of fabricating a memory gate stack structure, comprising the steps of:

providing a substrate layer comprising a silicon-based material,

forming a tunnel layer on the substrate layer,

forming a charge storage layer on the tunnel layer and comprising a hafnium-aluminium-oxide-based material,

forming a blocking layer on the charge storage layer, and

forming a gate layer on the blocking layer.

13. The method as claimed in 12, wherein the charge storage layer comprises $(HfO_2)_x(Al_2O_3)_{1-x}$, with x in arrange from about 0.4 to 0.95.

14. The method that as claimed in claim 13, wherein x is about 0.9.

15. The method as claimed in any one of claims 12 to 14, wherein the tunnel layer and/or the blocking layer comprise one or more silica-based materials.

16. The method as claimed in claim 15, wherein the tunnel layer comprises a silicon oxide formed by rapid thermal oxidation of the silicon-based material of the substrate layer.

17. The method as claimed in claims 15 or 16, wherein the blocking layer comprises $(Si(OC_2H_5)_4)$.

18. The method as claimed in any one of claims 12 to claim 17, wherein the blocking layer is formed utilising low-pressure chemical-vapor-deposition.

19. The method as claimed in any one of claims 12 to 18, wherein the gate layer comprises one or more of a group comprising a metal, metal nitride, silicide and polysilicon materials.

20. The method as claimed in claim 19, wherein the metal material comprises HfN.

21. The method as claimed in claims 19 or 20, wherein the gate layer is formed utilising sputter deposition techniques.

22. The method as claimed in any one of claims 12 to 21, wherein the method further comprises the step of forming a capping layer on the gate layer.

23. The method as claimed in claim 22, wherein the capping layer comprises TaN.

24. The method as claimed in claims 22 or 23, wherein the capping layer is formed utilising sputter deposition techniques.

25. The method as claimed in any one of claims 12 to 24, further comprising the step of forming a source region and a drain region in the substrate layer.

26. A memory gate stack structure comprising:

a substrate layer comprising a silicon-based material,

a tunnel layer formed on the substrate layer,

a charge storage layer formed on the tunnel layer,

a blocking layer formed on the charge storage layer, and

a gate layer formed on the blocking layer,

wherein the charge storage layer comprises an amorphous material exhibiting a larger valence band offset with respect to the silicon-based material compared to Si_3N_4, and exhibiting a smaller conduction band offset with respect to the silicon-based material than Al_2O_3.

27. A method of fabricating a memory gate stack structure, comprising the steps of:

providing a substrate layer comprising a silicon-based material,

forming a tunnel layer on the substrate layer,

forming a charge storage layer on the tunnel layer,

forming a blocking layer on the charge storage layer, and

forming a gate layer on the blocking layer,

wherein the charge storage layer comprises an amorphous material exhibiting a larger valence band offset with respect to the silicon-based material compared to Si_3N_4, and exhibiting a smaller conduction band offset with respect to the silicon-based material than Al_2O_3.

28. A memory gate stack structure substantially as herein described with reference to the accompanying drawings.

29. A method of fabricating a memory gate stack structure, substantially as herein described with reference to the accompanying drawings.

30. A memory transistor structure, substantially as herein described with reference to the accompanying drawings.

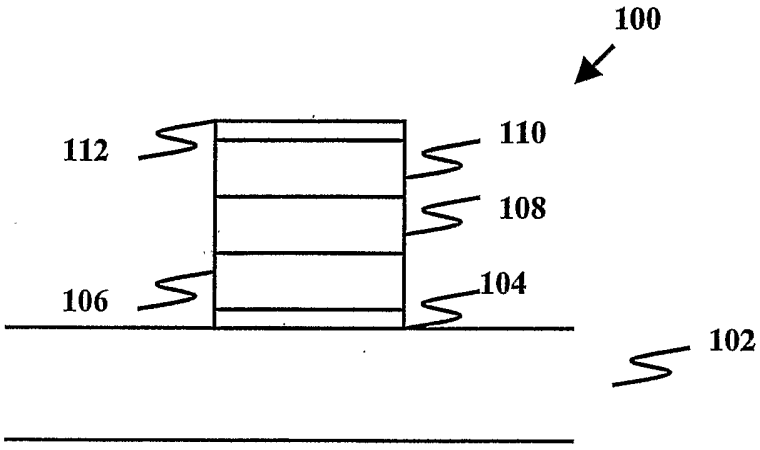

Figure 1

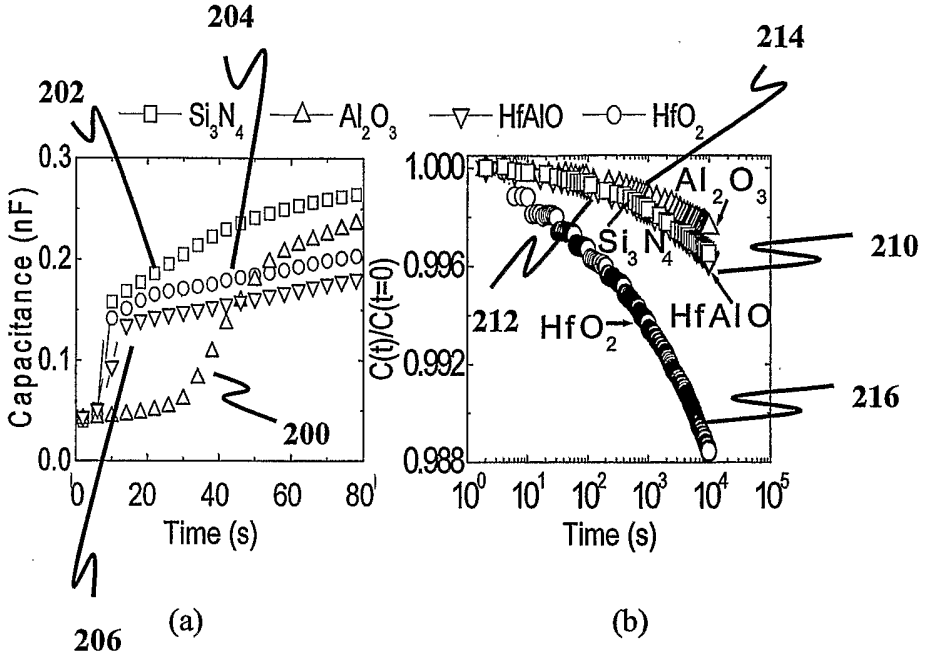
204
202
214
Si3N4
Al2O3
HfAlO
HfO2
Capacitance (nF)
0.3
0.2
0.1
0.0
0
20
40
60
80
Time (s)
200
206
(a)
C(t)/C(t=0)
1.000
0.996
0.992
0.988
Al2O3
Si3N4
HfAlO
HfO2
212
210
216
10^0
10^1
10^2
10^3
10^4
10^5
Time (s)
(b)

Figure 2

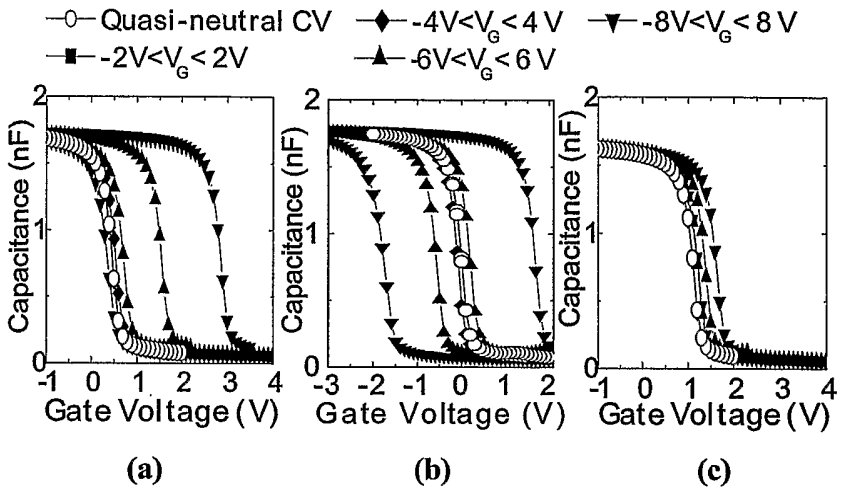
Quasi-neutral CV
-4V<V_G<4 V
-8V<V_G<8 V
-2V<V_G<2V
-6V<V_G<6 V
Capacitance (nF)
Gate Voltage (V)
(a)
(b)
(c)

Figure 3

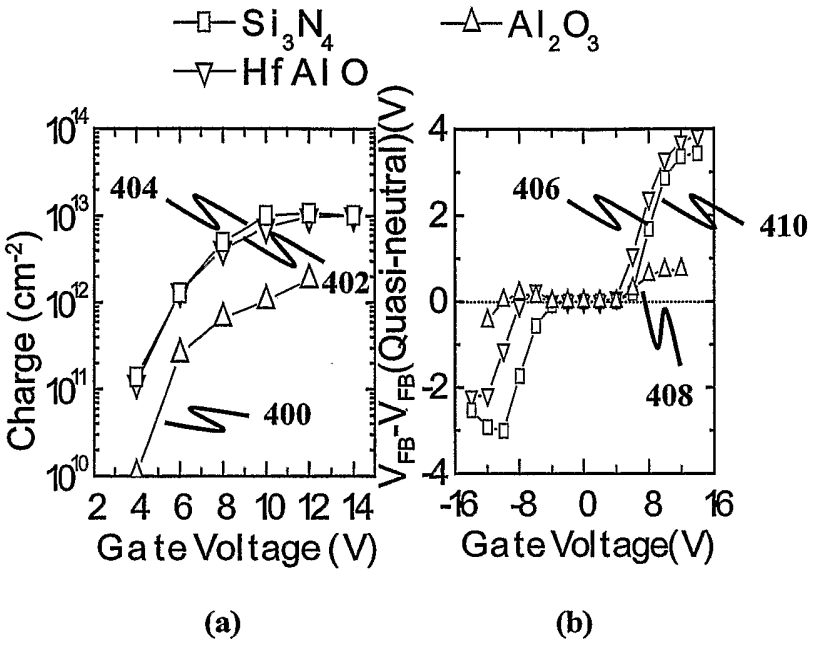
Si3N4
Al2O3
HfAlO
Charge (cm-2)
Gate Voltage (V)
404
402
400
VFB-VFB(Quasi-neutral)(V)
Gate Voltage(V)
406
410
408
(a)
(b)

Figure 4

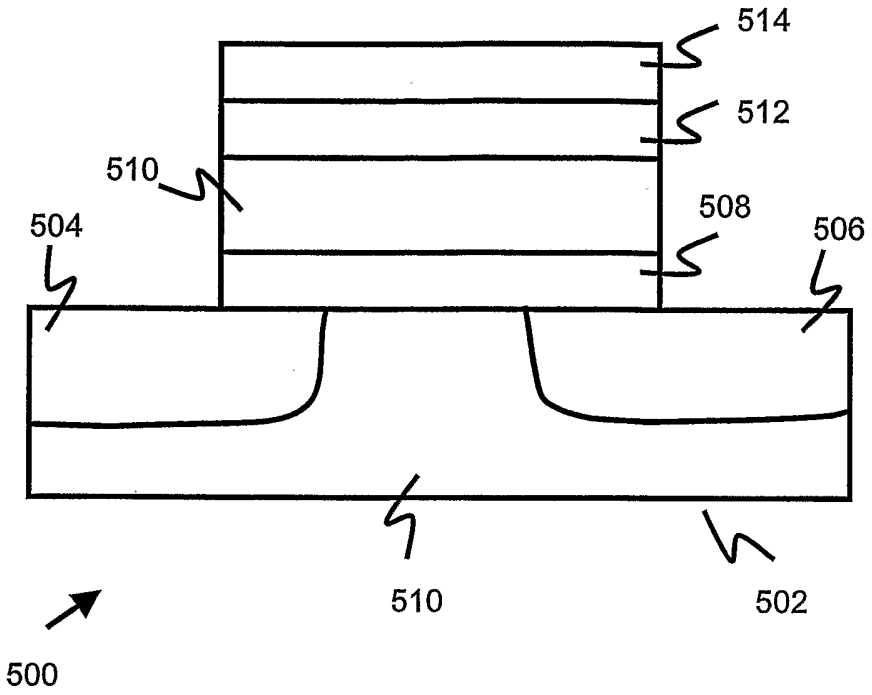

Figure 5

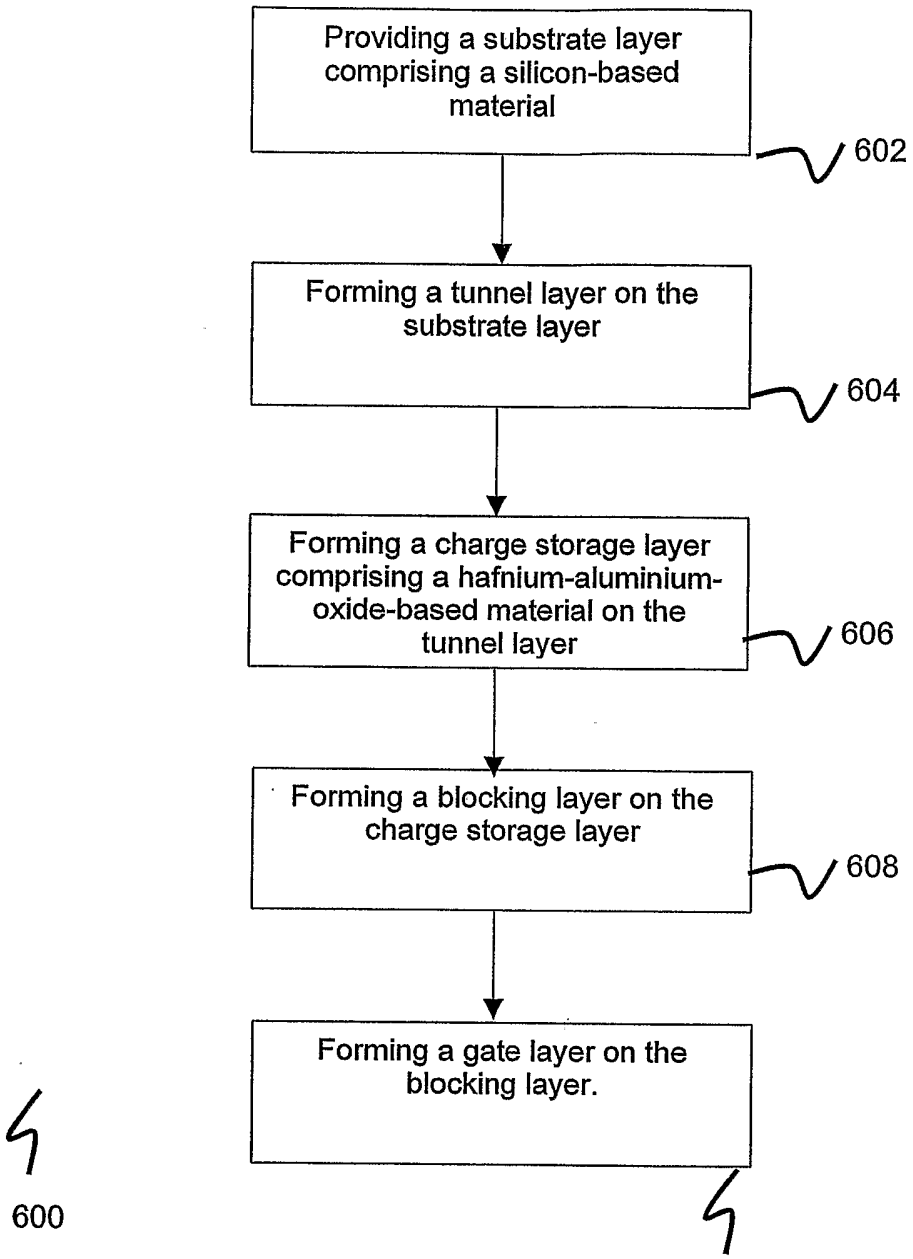
Providing a substrate layer comprising a silicon-based material
602
Forming a tunnel layer on the substrate layer
604
Forming a charge storage layer comprising a hafnium-aluminium-oxide-based material on the tunnel layer
606
Forming a blocking layer on the charge storage layer
608
Forming a gate layer on the blocking layer.
600
610

Figure 6

INTERNATIONAL SEARCH REPORT

International application No.
PCT/SG2004/000050

A. CLASSIFICATION OF SUBJECT MATTER

Int. Cl. [7]: H01L 29/792, 29/51, 21/8247

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols).

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
DWPI: /ic h01l-021 or h01l-027 or h01l-029 or g11c-016, hafnium or hf+, memory or flash or +rom?, stack or gate?, charge (s) (stor+ or accumulat+ or hold+ or retain+ or retention or trap+), eras+ or overeras+, tunnel+, valenc+, hafn+

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 2003/0227033 A1 (AHN et al.) 11 December 2003. Page 8, paragraphs [0080]–[0081]; figure 4.	
A	US 6642573 B1 (HALLIYAL et al.) 4 November 2003. Column 15, line 62–column 16, line 28; figure 8.	
A	US 6639271 B1 (ZHENG et al.) 28 October 2003. Claim 14; figure 2; column 4, line 35–column 5, line 18.	
A	US 6627503 B2 (MA et al.) 30 September 2003. Figure 2; column 4, lines 33–52.	

[X] Further documents are listed in the continuation of Box C [X] See patent family annex

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"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
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Date of the actual completion of the international search	Date of mailing of the international search report
15 June 2004	18 JUN 2004
Name and mailing address of the ISA/AU AUSTRALIAN PATENT OFFICE PO BOX 200, WODEN ACT 2606, AUSTRALIA E-mail address: pct@ipaustralia.gov.au Facsimile No. (02) 6285 3929	Authorized officer **RAJEEV DESHMUKH** Telephone No : (02) 6283 2145

INTERNATIONAL SEARCH REPORT

International application No.
PCT/SG2004/000050

C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 2003/0047755 A1 (LEE et al.) 13 March 2003 Page 4, paragraph [0047]; figure 4; claims 14, 28.	
A	US 6407435 B1 (MA et al.) 18 June 2002 Figure 2; column 4, lines 26–45.	
A	US 6060755 A (MA et al.) 9 May 2000 Abstract; claims 7–8.	
A	US 2004/0012043 A1 (GEALY et al.) 22 January 2004 Abstract; claim 1.	

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/SG2004/000050

This Annex lists the known "A" publication level patent family members relating to the patent documents cited in the above-mentioned international search report. The Australian Patent Office is in no way liable for these particulars which are merely given for the purpose of information.

Patent Document Cited in Search Report		Patent Family Member					
US	2003227033	WO	03105205				
US	6642573						
US	6639271	US	2004021172				
US	6627503	EP	1124262	JP	2001267566	US	6407435
		US	2002130340				
US	2003047755	DE	10228768	JP	2003068897	KR	2003002298
US	6407435	EP	1124262	JP	2001267566	US	6407435
		US	6627503	US	2002130340		
US	6060755	EP	1179837	JP	2001077111	JP	2002033320
		US	6207589	US	6297539		
US	2004012043						

Due to data integration issues this family listing may not include 10 digit Australian applications filed since May 2001.

END OF ANNEX