

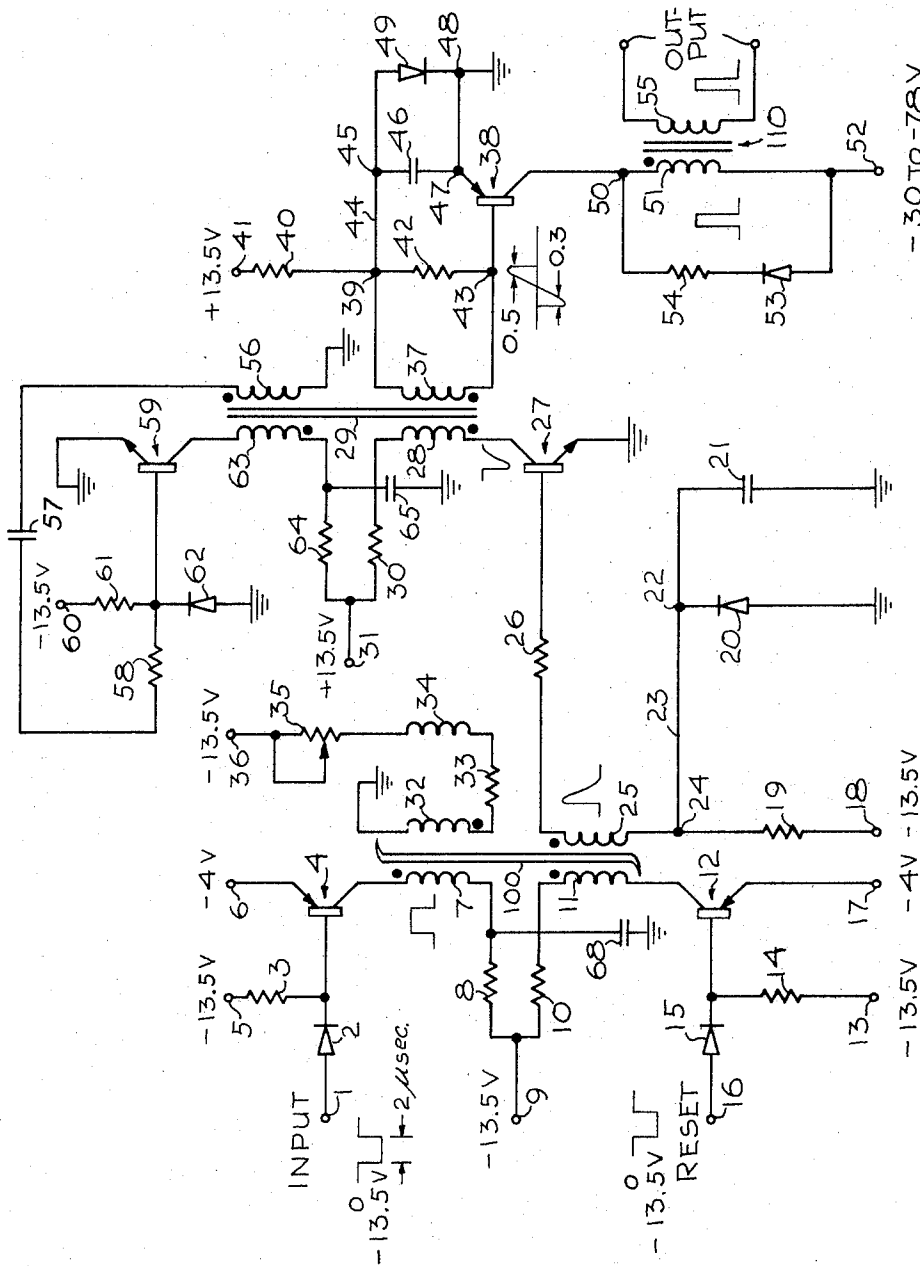
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CLOCK GENERATOR

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3,233,113

## CLOCK GENERATOR

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This invention relates to digital computer timing devices in general and more particularly to a clock device for supplying a set of recurring timing pulses for the synchronous operation of a digital computer.

Inherent in a synchronous digital computer is a clock device which supplies recurring timing pulses for the synchronous operation of the various logical elements contained therein. Often clock devices which employ transmission delay lines are utilized in digital computers. The delay line provides a certain pulse delay which is utilized in the associated clock circuitry as a time base to control the width of the output pulses of the clock.

Generally clock circuits employing delay lines are relatively complex from the standpoint of circuit design and number of components used. Additionally, the current capability of most delay line type clocks is rather low with the result that should relatively high currents be necessary, additional current amplifying stages must be provided. Another shortcoming of clocks which employ delay lines is that, due to the fact that the width of the clock output pulses are based on the delay provided by the delay line, the width of the clock pulses cannot be readily varied. Variation of the width of clock pulses provided by a delay line type clock normally entails unsoldering and physically moving the taps. Thus a vernier adjustment is not available.

It is, therefore, an object of the present invention to provide a clock generator which is relatively inexpensive in cost and simple in design.

Another object of the present invention is to provide a clock generator which is capable of high current output with relatively few current amplifying stages.

Another object of the present invention is to provide a clock generator, the pulse output width of which can be easily and accurately varied.

Other and further objects and advantages of the present invention will become apparent to one skilled in the art from a consideration of the following detailed description when read in light of the accompanying drawings, in which the single figure is a schematic representation of a preferred embodiment of the clock generator of the present invention.

Briefly, the device utilizes a tape-wound bobbin-type magnetic core to provide a time base pulse, the width of which is variable. A bias or opposition winding, wound on the magnetic core, provides a variable opposition current which opposes the main drive current applied to the core. An increase in the opposition current will result in an increase in the amount of time required for the core to switch from one state of saturation to the other while, conversely, a decrease in the opposition current will result in a faster switching time. A sense winding wound on the core detects or receives the time base pulse which is used to drive associated pulse shaping and power amplification circuitry to provide a clock pulse of variable width.

Applicant provides a bias winding on the magnetic core which functions to provide a variable opposition current to the main drive or switching current. In essence, what applicant does is to provide an opposition current in opposition to the main switching current which results in net drive current being applied to the core which is equal to the main drive current less the opposition current. Thus,

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the larger the opposition current, the longer the switching time since the main drive current is held constant which results in a smaller net drive current. As will hereinafter be explained, applicant utilizes the switching time of the core as a time base, the time base being, of course, variable as heretofore described.

To switch the magnetic core, applicant takes the "constant voltage switching approach." Applicant applies a constant voltage across the drive winding of the core to switch it. Initially the combined drive winding and core is a high impedance but once the core saturates, there is no longer a flux change in the core and the combined drive winding and core represent substantially zero impedance. Only during the time that the flux is changing does the drive winding represent an impedance. Consider the basic equation:

$$e = N \frac{d\phi}{dt} \quad (\text{Equation 1})$$

where

$e$  is equal to the voltage induced in the sense winding on the magnetic core;

$N$  is equal to the number of turns in the sense winding on the magnetic core; and

$d\phi/dt$  is equal to the time rate of change of flux in the core.

From the basic equation it can be seen that the voltage across the sense winding on the core is equal to the number of turns in the sense winding on the core times the time rate of change of flux in the core. Consider next the following equation:

$$2\phi_{\max} = \frac{1}{N} \int_{t_1}^{t_2} E dt \quad (\text{Equation 2})$$

where

$E$  = the voltage applied to the drive winding on the core; and

$2\phi_{\max}$  is the total flux change of the core as it switches from one state of saturation to the other.

In order to cause the core to switch from one state of saturation to the other, a constant voltage is applied to the drive winding on the core. This voltage will remain there until the core switches. From a consideration of Equation 2, it can be seen that the parameter, which is important in this approach, is the term  $\phi_{\max}$ . By instructing the manufacturer what material to make the magnetic tape of and how many turns of tape to put on the bobbin, it can be determined what the approximate  $\phi_{\max}$  of the core will be and consequently the approximate time required to switch the core can be predicted.

Applicant provides a bias winding on the core which functions to provide an opposition flux to the main switching flux of the core. The bias winding actually causes a current to flow in the core in opposition to the main drive current applied to the core which essentially changes the net drive current applied to the core. Since the voltage across the core is constant, Equation 2 may be rewritten as follows:

$$2\phi_{\max} + \phi_0 = \frac{E}{N} (t_1 - t_2) \quad (\text{Equation 3})$$

where  $\phi_0$  is the opposition flux caused by the current flowing in the bias winding. The actual total flux change within the core is not altered but Equation 3 approximates the conditions seen by the external circuitry. In essence then, in accordance with the above equation, the time required to switch the core can be controlled by controlling  $\phi_0$ , and  $\phi_0$  can be controlled by controlling the

amount of current in the bias winding. In this manner, the width of the time base pulse which is taken by means of a sense winding on the core can be controlled.

Thus, rather than controlling the drive current from an external source, applicant allows the core itself to control the current by the inherent inductance of the drive winding. Thus the time base pulse provided by the core is controlled by the core itself in that the inductance of the drive winding is determined by the flux change in the core.

Refer next to the drawing which shows a schematic representation of a circuit which represents a preferred embodiment of the present invention. The input to the circuit is along line 1 through diode 2 to the base of transistor 4, which is of the PNP type. A negative potential 5, which for instance may be -13.5 volts, is also applied through a resistor 3 to the base of transistor 4. The emitter of transistor 4 is connected to a negative source 6, which may be for instance -4 volts, while the collector of transistor 4 is connected through winding 7 and resistor 8 to a negative potential 9, which may be -13.5 volts.

Another input to the circuit is along line 16 through diode 15 to the base of transistor 12, which is of the PNP type. A negative source 13, which may be for instance -13.5 volts, is also applied through a resistor 14 to the base of transistor 12. The emitter of transistor 12 is connected to a negative source 17, which for instance may be -4 volts, while the collector of transistor 12 is connected through winding 11 which is wound on core 100 and resistor 10 to the negative potential 9.

Capacitor 21 is connected between ground and junction 22. Diode 20 has its anode grounded while its cathode is connected likewise to junction 22. Junction 22 is also connected through line 23 to junction 24 which is connected through resistor 19 to the negative source 18, which may be for instance -13.5 volts. The negative source 18 is also connected through winding 25 and resistor 26 to the base of transistor 27. The emitter of transistor 27 is grounded while the collector of transistor 27 is connected through winding 28 on transformer core 29 and resistor 30 to the positive potential 31 which may, for instance, be +13.5 volts. The non-dot side of winding 32 on core 100 is grounded while the dot side thereof is connected through resistor 33, coil 34 and variable resistor 25 to the negative potential 36, which may be for instance -13.5 volts.

The dot side of winding 37 is connected to the base of transistor 38 while the non-dot side thereof is connected to junction 39. Junction 39 is connected through resistor 40 to the positive source 41, which may be for instance +13.5 volts and also through resistor 42 to junction 43. Junction 39 is also connected through line 44 to junction 45 which in turn is connected to one side of capacitor 46, the other side of which is connected to junction 47. Junction 47 is also connected to the emitter of transistor 38 and to junction 48 which is grounded. The cathode of diode 49 is also connected to junction 48 while the anode of diode 49 is connected to junction 45. The collector of transistor 38 is connected to junction 50 which in turn is connected through the primary winding 51 to the negative potential 52 which is a variable potential and which may for instance be from -30 to -78 volts. The negative potential 52 is also connected to the anode of diode 53 while the cathode of diode 53 is connected through resistor 54 to junction 50. The output of the circuit is taken across secondary winding 55.

The non-dot side of winding 56 on transformer core 29 is grounded while the dot side thereof is connected to one side of capacitor 57 while the other side of capacitor 57 is connected through resistor 58 to the base of transistor 59. A negative potential 60, which may for instance be -13.5 volts, is also connected through resistor 61 to the base of transistor 59. The base of transistor 59 is also connected to the cathode of diode 62 while the

anode of diode 62 is connected to ground. The emitter of transistor 59 is grounded while the collector is connected through winding 63 on the transformer core 29 and resistor 64 to the positive potential 31. The dot side of winding 63 is connected to one side of capacitor 65 while the other side of capacitor 65 is grounded.

In operation, a square wave input signal is fed into the circuit along line 1. As is illustrated in FIG. 1, this square wave input signal may, for instance, vary from 0 volt to -13.5 volts and may be 2  $\mu$ sec. in width. When the input signal is at 0 volt or ground potential, diode 2 is forward biased since its anode is positive with respect to its cathode which is at -13.5 volts due to the action of the negative potential 5 through resistor 3. Thus, during this time current flows through diode 2 and resistor 3 to the negative potential 5. During this time, assuming that there is a slight voltage drop across diode 2, the base of the transistor 4 will be held slightly negative. The base of transistor 4 will, however, be positive with respect to the negative supply 6 connected to the emitter of transistor 4 and transistor 4 will be OFF. In order to turn transistor 4 ON, its base must be driven negative with respect to its emitter.

When the square wave input signal drops from 0 to -13.5 volts, the diode 2 is cut off or back biased since the base of transistor 4 tries to go to -13.5 volts but the instant that the base goes negative with respect to the emitter, the transistor is turned ON. Thus, the base of the transistor will stay at substantially -4 volts and therefore the diode 2 is back biased whenever the input signal goes more negative than -4 volts. When transistor 4 is turned ON, it becomes effectively a short circuit and the negative potential 6 (-4 volts) is switched across the winding 7. The amount of current which flows in the collector circuit is dependent upon the impedance in the collector circuit. When transistor 4 is first turned ON, the winding 7 represents a high impedance since the current flowing in the collector is small due to the impedance of the winding 7 but, as the flux changes in the core 100, the current increases because the impedance of the winding 7 decreases. When the core 100 finally saturates, the only impedance in the collector circuit will be resistor 8. Resistor 8 is in the collector circuit only to limit the current flow after the core 100 saturates. If resistor 8 were not in the collector circuit, after the core saturates, there would be no impedance in the collector circuit and there would be a large dissipation on the collector of transistor 4.

As is illustrated by the wave form associated with winding 7 of core 100, there is a phase reversal in transistor 4 and thus the voltage which is applied across winding 7 is approximately 180° out of phase with respect to the input signal. Likewise, in accordance with the dot notation which, simply stated, is that when a dot side goes positive, all the other dot sides of the windings in the system go positive and, therefore, a wave form as is illustrated in association with winding 25 is sensed by winding 25 as the core changes from one state of saturation to the other.

Winding 25 may be appropriately referred to as a sense winding. From a consideration of the wave form associated with winding 25, it can be seen that when the input signal is at ground, there is no voltage induced in winding 25 because there is no voltage switched across winding 7. Therefore, during this time current is flowing from ground through diode 20 through junction 22, junction 24, and resistor 19 to the negative potential 18. Therefore, during this time, there is no input signal to the base of transistor 27. Due to the voltage drop across diode 20, the base of transistor 27 is at a slightly negative potential. In this manner, the base of transistor 27 is held at a slightly negative potential during the time that there is no input to the base of transistor 4. Thus, transistor 27, which is of the NPN type, is back biased and the transistor is OFF. Therefore, the only function of resistor 19 diode 20 and capacitor 21 is to establish a slightly

negative back bias voltage which is applied to the base of transistor 27 to hold it OFF while there is no input to transistor 4.

The instant that there is a voltage induced in sense winding 25, the base of transistor 27 is driven in a positive direction and current flows from the positive source 31 through resistor 30, winding 28 and through transistor 27 to ground. Thus transistor 27 is turned ON. When transistor 27 is turned ON, a voltage is induced in the primary winding 28 of transformer 29 which in turn is coupled into the secondary winding 37. Since the input wave form to the base of transistor 27 is positive due to the inversion of the input signal, the output signal taken from the collector of transistor 27 will be a negative signal. This negative signal, as previously stated, is coupled into winding 37 which has its dot side connected through junction 43 to the base of transistor 38. Transistor 38 is thus turned ON and collector current flows through the transistor and primary winding 51 of transformer 110 to the negative potential 52. When transistor 38 is turned ON, voltage is induced in primary winding 51 which is coupled into the secondary winding 55 of transformer 110. Thus the output voltage is taken across secondary winding 55. Transistor 38 turns ON easily and thus gives a fast rise time to the output voltage wave form taken across winding 55, but there is considerable difficulty in turning it OFF once it is in saturation. This is due to the fact that once minority carriers are in the base region, it takes a certain amount of time to clear them out. Thus some means must be provided for rapidly turning transistor 38 OFF since, preferably, the output wave form taken across winding 55 should have a fast fall time.

As the wave form at the dot side of secondary winding 37 tends to go positive, the wave form at the dot side of secondary winding 56 also tends to go positive. During the time that the wave form at the dot side of secondary winding 37 was negative going, a negative pulse was coupled into the dot side of secondary winding 56, which tended to cut off transistor 59.

As the signal at the dot side of secondary winding 37 falls, i.e., goes positive, the dot side of secondary winding 56 likewise goes positive. This positive pulse is applied through capacitor 57 and resistor 58 to the base of transistor 59, thereby turning it ON. When transistor 59 turns ON, the dot side of primary winding 63 goes positive. This positive turnoff pulse is coupled back into secondary winding 37 which causes the dot side of winding 37 to go even more positive, thereby bootstrapping the positive going pulse which is being applied to the base of transistor 38. As is obvious, secondary winding 56, primary winding 63 and transistor 59 represent a blocking oscillator. The positive cutoff pulse, produced by the regeneration of the blocking oscillator, is used to turn transistor 38 OFF more rapidly, thus causing the output voltage taken across secondary winding 55 to have a very fast fall time. In this manner the rise and fall times of the output wave form taken across winding 55 can be made to be in the order of 60 nanoseconds.

Core 100, as previously explained, is now in one of its two states of saturation. Thus, if an input were received along line 1 of the base of transistor 4 at this time, there would be no output from winding 25 since the voltage induced in winding 7 would be in such a direction as to drive the core 100 to the state of saturation which it is already in. Therefore, reset means must be provided in order that an input signal along line 1 will cause a time base pulse to be induced in winding 25.

A reset signal, which may be square wave and which may be identical to the input wave form which was input along line 1, except that it is 180° out of phase, is input along line 16, through diode 15 to the base of transistor 12. In the absence of the reset pulse, diode 15 is forward biased and current flows along line 16, through diode 15 and resistor 14 to the negative potential 13. During this

time, the base of transistor 12 is at a slightly negative potential due to the slight voltage drop across diode 15. When the input signal on line 16 rises to -13.5 volts, the base of transistor 12 tries to go to -13.5 volts with it but, as soon as the base of transistor 12 goes as negative as the negative potential 17 (-4 volts) applied to the emitter, the transistor turns ON. When the transistor turns ON, current flows through the emitter, base and collector to the negative potential 9. A reset voltage is thus induced in winding 11 which is in such a direction so as to reset the core 100.

During this reset operation, transistor 27 remains cut off since the wave form at the dot side of winding 11 is negative going which in turn causes the dot side of winding 25 to be negative going which tends to cut the transistor 27 off further.

Resistor 35 is a variable resistor which controls the amount of current flowing in winding 32 which may be called the bias or opposition winding since it furnishes a current in opposition to the main driving current applied to winding 7. Coil 34 is in the circuit to prevent loss of energy in the opposition winding when the main drive pulse is applied to winding 7. When the main drive pulse is applied to winding 7, coil 34 looks like a high impedance to the fast rising pulse so that very little energy is lost in the bias winding 32. Coil 34 has little or no effect on the D.C. current furnished by the negative source 36 to winding 32.

In the above described manner I have provided a clock generator which is quite simple and which is relatively inexpensive. The clock generator herein provided employs a novel method of pulse delay and is capable of high current output with relatively few current amplifying stages. In addition, the output pulse width generated by the clock generator can be easily and accurately varied since a biased magnetic core is utilized as a time base element. Selection of a suitable magnetic core for use as the time base element is facilitated since a method of allowing the inherent inductance of the drive winding on the core to determine the switching time of the core is taught herein.

While there has been described what is at present considered to be a preferred embodiment of the invention, it will be obvious to those skilled in the art that various changes and modifications may be made therein without departing from the invention, and it is aimed in the appended claims to cover all such changes and modifications as fall within the true spirit and scope of the invention.

What is claimed is:

1. A clock generator capable of supplying a set of recurring timing pulses of variable duration in response to recurring input pulses comprising a magnetic core capable of assuming either one of two states of magnetic saturation, a first winding wound on said magnetic core, transistor drive means responsive to said input pulses capable of selectively switching a constant voltage across said first winding electrically connected thereto to switch said core to a second of said states, a second winding wound on said magnetic core, transistor reset means capable of selectively applying a reset current to said second winding electrically connected thereto to switch said core to a first of said states, a third winding wound on said magnetic core, means for applying a variable current to said third winding tending to switch said core to said first state, and a fourth winding wound on said magnetic core such that timing pulses whose duration is dependent on the magnitude of said variable current are induced therein, said fourth winding being electrically connected to pulse shaping and power amplifying means.

2. A clock generator capable of supplying a set of recurring timing pulses of variable duration in response to recurring input pulses comprising a magnetic core capable of assuming either one of two states of magnetic saturation, a first winding wound on said magnetic core, tran-

sistor drive means responsive to said input pulses capable of selectively switching a constant voltage across said first winding electrically connected thereto to switch said core to a second of said states, a second winding wound on said magnetic core, transistor reset means capable of selectively applying a reset current to said second winding electrically connected thereto to switch said core to a first of said states, a third winding wound on said magnetic core, means for applying a variable current to said third winding tending to switch said core to said first state, a fourth winding wound on said magnetic core such that timing pulses whose duration is dependent on the magnitude of said variable current are induced therein, a first transformer having first and second primary windings wound thereon and first and second secondary windings wound thereon, a first transistor having its base electrically connected to said fourth winding, the collector of said first transistor being electrically connected to said first primary winding of said first transformer, a second transistor having its base electrically connected to said first secondary winding of said first transformer, and a second transformer having a primary and secondary winding, the collector of said second transistor being electrically connected to said primary of said second transistor.

3. A clock generator capable of supplying a set of recurring timing pulses of variable duration in response to recurring input pulses comprises a magnetic core capable of assuming either one of two states of magnetic saturation, a first winding wound on said magnetic core, transistor drive means responsive to said input pulses capable of selectively switching a constant voltage across said first winding electrically connected thereto to switch said core to a second of said states, a second winding wound on said magnetic core, transistor reset means capable of selectively applying a reset current to said second winding electrically connected thereto to switch said core to a first of said states, a third winding wound on said magnetic core, means for applying a variable current to said third winding tending to switch said core to said first state, a fourth winding wound on said magnetic core such that timing pulses whose duration is dependent on the magnitude of said variable current are induced therein, pulse shaping and power amplifying means electrically connected to said fourth winding comprising a first transformer having first and second primary windings and first and second secondary windings wound thereon, a first transistor having an emitter, base and collector, said first transistor having its base electrically connected to said fourth winding, the collector of said transistor being electrically connected to said first primary winding of said first transformer, a second transistor having an emitter, base and collector, said second transistor having its base electrically connected to said first secondary winding of said first transformer, a second transformer having primary and secondary windings, the collector of said second transistor being electrically connected to the primary of said second transformer, a third transistor having an emitter, base and collector, the base of said third transistor being electrically connected to said second secondary winding of said first transformer, and said second primary winding of said first transformer being electrically connected to the collector of said third transistor.

4. A clock generator capable of supplying a set of recurring timing pulses comprises a magnetic core capable of assuming first and second states of magnetic saturation, first, second, third and fourth windings wound on said magnetic core, a first transistor having an emitter, base and collector, a first diode electrically connected to the base of said first transistor, a first reference potential connected to the emitter of said first transistor, the collector of said first transistor being electrically connected to said first winding on said magnetic core so as to drive a current through said first winding tending to cause said

core to assume said second state, a second transistor having an emitter, base and collector, a second diode electrically connected to the base of said second transistor, a second reference potential connected to the emitter of said second transistor, the collector of said second transistor being electrically connected to said second winding on said magnetic core so as to drive a current through said second winding tending to cause said core to assume said first state, a variable current source electrically connected to said third winding on said magnetic core so as to drive a current through said third winding tending to cause said core to assume said first state, a third transistor having an emitter, base and collector, the base of said third transistor being electrically connected to said fourth winding on said magnetic core, a first transformer having first and second primary windings and first and second secondary windings wound thereon, the collector of said third transistor being electrically connected to said first primary winding of said first transformer, a fourth transistor having an emitter, base and collector, the base of said fourth transistor being electrically connected to said first secondary winding of said first transformer, a second transformer having a primary and secondary winding wound thereon, the collector of said fourth transistor being electrically connected to said primary winding of said second transformer, a fifth transistor having an emitter, base and collector, said second secondary winding of said first transformer being electrically connected to the base of said fifth transistor, and the collector of said fifth transistor being electrically connected to said second primary winding of said first transformer.

5. Circuit means for generating a time base pulse in response to an input signal comprising:

- a magnetic core capable of assuming either one of two states of magnetic saturation;
- a first winding wound on said core;
- a second winding wound on said core;
- means driving a selectively variable current through said second winding in a direction tending to cause said core to assume said first state of saturation;
- means responsive to said input signal for applying a constant voltage across said first winding sufficient to switch said core from said first to said second state of saturation, the switching time being dependent upon the saturation characteristics of said core and said second winding current; and
- a third winding wound on said core such that a pulse of said switching time duration will be induced therein.

6. The circuit means of claim 5 wherein said means responsive to said input signal comprises a transistor including a collector, an emitter and a base;

- a first reference potential connected to said emitter;
- a second reference potential;
- said first winding connected between said collector and said second reference potential; and
- means coupling said input signals to said base.

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