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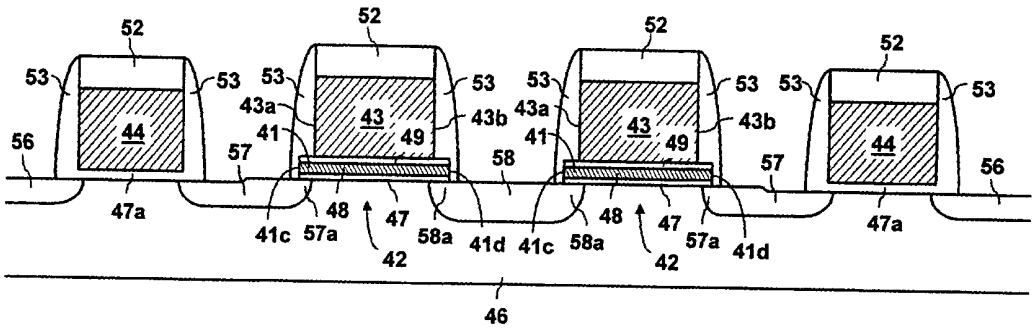

(57) Abstract: Memory cell having a floating gate (41) with lateral edges (41a, 41b) which are aligned directly above edges (42a), (42b) of the active area (42) in the substrate (46), a control gate (43) positioned directly above the floating gate (41), and a select gate (44) spaced laterally from the control gate (43). The memory cell is fabricated by forming a poly-1 layer and an overlying dielectric film on a substrate in areas in which the stack transistors are to be formed, forming a poly-2 layer over the dielectric film and over areas of the substrate in which the select transistors are to be formed, patterning the poly-2 layer to form control gates for the stack transistors and select gates for the select transistors, removing the poly-1 layer and the dielectric film to form floating gates in areas which are not covered by the control gates, and forming source and drain regions in the substrate.

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MEMORY CELL WITH SELF-ALIGNED FLOATING GATE AND SEPARATE SELECT GATE, AND FABRICATION PROCESS

This is a continuation-in-part of Serial No. 09/370,557, filed August 9, 1999.

This invention pertains generally to semiconductor devices and, more particularly, to a nonvolatile memory device and fabrication process.

Electrically programmable read only memory (EPROM) has been widely used as nonvolatile memory which can keep data unchanged even though the power is turned off. However, EPROM devices have a major disadvantage in that they have to be exposed to Ultra-Violet (UV) light for about 20 minutes for data erasure. This is very inconvenient because an EPROM device has to be unplugged from its socket and moved to the UV light source when the data needs to be changed.

Electrically erasable programmable read only memory (EEPROM) overcomes this problem and permits data to be erased electrically in a much shorter period of time, typically less than 2 seconds. However, it still has a disadvantage in that the data must be erased on a byte-by-byte basis.

Flash EEPROM is similar to EEPROM in that data is erased electrically and relatively quickly. However, with flash EEPROM, the data is erased in blocks which typically range in size from 128 to 64K bytes per block, rather than on a byte-by-byte basis.

In general, there are two basic types of nonvolatile memory cell structures: stack-gate and split-gate. The stack-gate memory cell usually has a floating gate and a control gate, with the control gate being positioned directly above the floating gate. In a split-gate cell the control gate is still positioned above the floating gate, but it is offset laterally from it. The fabrication process for a stack-gate cell is generally simpler than that for a split-gate cell. However, a stack-gate cell has an over-erase problem which a split-gate cell does not have. This problem is commonly addressed by maintaining the threshold voltage of the cell in a range of about 0.5 - 2.0 volts after an erase cycle, which adds complexity to the circuit design.

A split-gate memory cell has an additional gate known as a select gate which avoids the over-erase problem and makes circuit design relatively simple. Such cells are typically fabricated in double-poly or triple-poly processes which are relatively complex, and they are more susceptible to various disturbances during programming and read operations.

EEPROM devices have typically included a stack-gate transistor and a separate select gate transistor. With no over-erase problem, circuit design has been relatively simple, but these devices have a relatively high die cost due to larger cell size as compared to split-gate and stack-gate memory cells.

A memory cell is erased by forcing electrons to migrate away from the floating gate so that it becomes charged with positive ions. This is commonly accomplished by Fowler-Nordheim tunneling in which a tunnel oxide having a thickness on the order of 70-120Å is formed between the monocrystalline silicon substrate and the floating gate. A relative strong electric field (greater than 10mV/cm) is then applied to the tunnel oxide, and the electrons tunnel from the floating gate toward the underlying source, drain or channel region. This technique is widely used both in

stack-gate cells and in split-gate cells, and is described in greater detail in U.S. Patents 5,792,670, 5,402,371, 5,284,784 and 5,445,792.

Another way of forming an erase path is to grow a dielectric film between two polysilicon (poly-Si) layers as a tunneling dielectric. U.S. Patent 5,029,130 discloses the formation of a sharp edge on the floating gate to enhance the local electric field around it, with the erase path being formed between the sharp edge and the control gate. By adding a third polycrystalline silicon layer as an erase layer which crosses over, or overlies, the floating gate and the control gate, an erase path can be formed between the side wall of floating gate and the erase layer. This technique is disclosed in U.S. Patents 5,847,996 and 5,643,812.

Fowler-Nordheim tunneling can also be used to program a memory cell by forcing electrons to tunnel into the floating gate so that it becomes charged negatively. U.S. Patents 5,792,670 and 5,402,371 show examples in which electrons are forced to tunnel into the floating gate from the channel region beneath it.

Another way of programming a memory cell is by the use of channel hot carrier injection. During a programming operation, the electrons flowing from the source to the drain are accelerated by a high electric field across the channel region, and some of them become heated near the drain junction. Some of the hot electrons exceed the oxide barrier height and are injected into floating gate. This technique is found in U.S. Patent 4,698,787.

Figure 1 illustrates a prior art NOR-type flash EEPROM cell array in which the floating gates 16 have end caps 16a, 16b which extend over the adjacent isolation oxide regions 19. The floating gate is typically made of polysilicon or amorphous silicon with a thickness on the order of 1500 - 2500 Å. Control gates 21 cross over the floating gates, and are

typically made of heavily doped polysilicon or polycide. Select gates 22 are separated from and parallel to the control gates. Bit lines 23, which are typically formed by a metallization layer, connect all of the drain of the memory cells in the respective columns, with adjacent ones of the bit lines being isolated from each other. All of the sources of the memory cells in a given row are connected together by a common source line 24 which is typically formed by an N+ or a P+ diffusion layer in the single crystalline silicon substrate.

The floating gate end caps 16a, 16b are required because of a corner-rounding effect or a shift of the floating gate which occurs during the photolithographic step by which the floating gate is formed. The corner-rounding effect may make the edges 16c, 16d of the floating gate shorter, and the shift of the floating gate may make one or both of the edges 16c, 16d move beyond the edges 28a, 28b of active area 28. Both of these effects can cause malfunction of the memory cell because a leakage path may occur when the floating gate does not completely cover the active area or its channel length becomes too short.

Figures 2A and 2B illustrate the memory cell array of Figure 1 with shallow trench and LOCOS (local oxidation of silicon) isolation, respectively. As seen in these figures, an inter-poly dielectric film 31 is formed between the conduction layers which form the floating gates 16 and the control gates 21. Those layers are commonly referred to as the poly-1 and poly-2 layers, respectively, and the dielectric film is typically formed of either pure oxide or a combination of oxide and nitride films.

The end caps 16a, 16b which extend over the adjacent isolation oxide regions 19 help in the formation of large capacitance areas between the control gates 21 and the floating gates 16. Consequently, the coupling ratio from the control gate to the floating gate becomes large, and this makes it possible to couple more voltage from the control gate to the

floating gate during programming and erase operations. In order to insure that the floating gate will completely cover the active area and that the channel length will not become too short due to variations during the fabrication process, it is necessary to add tolerance to the memory cell layout by making the floating gate caps wider. In addition, the distance 32 between the end caps has to be kept wide enough to avoid shorts from developing between the floating gates. As a result, the size of the memory cell increases, and the cost gets higher.

It is in general an object of the invention to provide a new and improved memory cell and process for fabricating the same.

Another object of the invention is to provide a memory cell and process of the above character which overcome the limitations and disadvantages of the prior art.

These and other objects are achieved in accordance with the invention by providing a memory cell having a floating gate with lateral edges which are aligned directly above edges of the active area in the substrate, a control gate positioned directly above the floating gate, and a select gate spaced laterally from the control gate. The floating gate has a bottom wall and side walls which face corresponding walls of the control gate in capacitive coupling relationship, with the height of the side walls being on the order of 80 to 160 percent of the width of the bottom wall. In some embodiments, the floating gate is wider than the overlying control gate and has projecting portions which overlie the source and drain regions of the stack transistor.

The memory cell is fabricated by forming a poly-1 layer and an overlying dielectric film on a substrate in areas in which the stack transistors are to be formed, forming a poly-2 layer over the dielectric film and over areas of the substrate in which the select transistors are to be formed, patterning

the poly-2 layer to form control gates for the stack transistors and select gates for the select transistors, removing the poly-1 layer and the dielectric film to form floating gates in areas which are not covered by the control gates, and forming source and drain regions in the substrate. The floating gates are aligned with active areas in the substrate by forming isolation oxide regions which extend above the substrate at the edges of the active areas, and forming the floating gates on the sides of the isolation oxide regions in alignment with the edges of the active areas.

Figure 1 is a top plan view of a prior art NOR-type flash EEPROM memory cell array.

Figures 2A and 2B are enlarged, fragmentary cross-sectional views taken along line 2 - 2 of Figure 1.

Figure 3 is a top plan view of one embodiment of a NOR-type flash EEPROM memory cell array fabricated in accordance with the invention.

Figures 4A - 4F are enlarged, schematic cross-sectional views taken along line 4 - 4 of Figure 3, illustrating the steps in one embodiment of a process for fabricating the memory cell array of Figure 3.

Figures 5A - 5C are schematic cross-sectional views similar to Figures 4A - 4F, illustrating the steps in another embodiment of a process for fabricating the memory cell array of Figure 3.

Figure 6 is a top plan view of another embodiment of a NOR-type flash EEPROM memory cell array fabricated in accordance with the invention.

Figures 7A and 7B are enlarged, schematic cross-sectional views taken along line 7 - 7 of Figure 6, illustrating the steps in one embodiment of a process for fabricating the memory cell array of Figure 6.

Figures 8A and 8B are enlarged cross-sectional views taken along lines 8 - 8 of Figures 3 and 6.

Figures 9A - 9F are enlarged, schematic cross-sectional views taken in a direction similar to that indicated by line 7 - 7 of Figure 6, illustrating the steps in another embodiment of a process for fabricating the memory cell array of Figure 6.

Figure 10 is a circuit diagram of the memory cell arrays of Figures 3 and 6.

As illustrated in Figure 3, a NOR-type flash EEPROM memory cell array fabricated in accordance with the invention has floating gates 41 with two edges 41a, 41b which are self-aligned with the edges 42a, 42b of the active areas 42. The end caps of the prior art devices are eliminated, and as discussed more fully hereinafter, the control gates 43 and the select gates 44 are defined simultaneously in a single photolithographic masking step. The other two edges 41c, 41d of the floating gates are defined after the side edges 43a, 43b of the control gates are formed, and the floating gates are wider than the control gates. With the self-aligned floating gates, cell size and die cost are both greatly reduced.

As illustrated in Figure 4A, the memory cell is fabricated on a silicon substrate 46 which can be an N-well, P-well or P-substrate material. An oxide layer 47 having a thickness on the order of 70 - 120 Å is thermally grown on the substrate to form the gate oxides of the floating gate transistors. A conduction layer 48 of polysilicon or amorphous silicon (poly-1) having a thickness on the order of 100 - 1000 Å is deposited on the thermal oxide. The poly-1 layer is doped with phosphorus, arsenic or boron to a level on the order of 10^{17} to 10^{20} per cm^3 either *in-situ* during deposition of the silicon or by ion implantation. A dielectric film 49 is then formed on the poly-1 layer. This film can be either a pure oxide or a combination of oxide and nitride, and in one presently preferred

embodiment, it consists of a lower oxide layer having a thickness on the order of 30 - 100 Å, a central nitride layer having a thickness on the order of 60 - 300 Å, and an upper oxide layer having a thickness on the order of 30 - 100 Å.

A photolithographic mask (not shown) is then formed over the areas in which stack transistors are to be formed, and the poly-1 layer and the dielectric film are then etched away in the areas in which select transistors are to be formed, as illustrated in Figure 4B. Another thermal oxidation is then performed to form the gate oxide 47a for the select transistors. That oxide preferably has a thickness on the order of 150 - 350 Å.

Referring now to Figure 4C, a second polysilicon layer 51 (poly-2) is deposited across the wafer to form the conduction layer 51a, 51b for the control gates and the select gates. The poly-2 layer has a thickness on the order of 1500 - 3000 Å, and is doped with phosphorus, arsenic or boron to a level on the order of 10^{20} to 10^{21} per cm^3. If desired, a polycide film can be formed on the poly-2 layer to reduce its sheet resistance. A dielectric film 52 of oxide or nitride is then deposited on the poly-2 layer.

A photolithographic mask (not shown) is positioned over dielectric film 52 to define the control gates and the select gates, and an anisotropic etch is performed to remove film 52 and the poly-2 layer in the unmasked areas, leaving the structure shown in Figure 4D in which control gates 43 and select gates 44 are formed. The poly-I layer which forms the floating gates is protected by dielectric layer 49 and is not etched at this time.

An oxide film is then deposited across the wafer, and then removed from the flat areas in an anisotropic dry etch to form oxide spacers 53 which surround the control gates and select gates, as shown in Figure 4E.

Referring now to Figure 4F, using the control gates and the oxide spacers as a mask, the floating gates 41 are formed by etching away the dielectric film 49 and the poly-1 material which are not covered by the mask. The oxide spacers are then widened by depositing an oxide film and etching it away anisotropically. Source and drain regions 56-58 are then formed by ion implantation, with the junction depth of the source regions 58 of the stack transistors being made greater to withstand the relatively high voltages applied to the source nodes during an operations.

With the floating gates being wider than the overlying control gates, an erase path or window is formed between one protruding portion of each of the floating gates and the underlying source region 58a. The other protruding portion is positioned above the drain region 57a of the stack transistor.

Figures 5A - 5C illustrate an alternate embodiment for processing the cell array after it has reached the point shown in Figure 4D. In this embodiment, a poly-oxide layer 59 is formed by thermal oxidation on the side walls of the control gates and the select gates to a thickness which is preferably on the order of about 100 - 400 Å. Using the control gates and the poly-oxide layers as a mask, the floating gates 41 are formed by etching away the dielectric film 49 and the poly-1 material outside the masked area, as shown in Figure 5B. Thereafter, oxide spacers 61 are formed around the select gates and the control gates. In this embodiment, the spacers surround the floating gates as well as the control gates. Source and drain regions 56-58 are formed by ion-implantation, and the source junctions 58 is made deeper to withstand the high voltages that are applied to the source nodes during erase operations.

The embodiment of the NOR-type flash EEPROM memory cell array illustrated in Figure 6 is similar to the embodiment of Figure 3 in that the edges 41a, 41b of the floating gates are self-aligned with the edges 42a,

42b of the active areas 42, and the control gates 43 and select gates 44 are defined simultaneously in a single photolithographic masking step. However, it differs in that the other two edges 41c, 41d of the floating gates are aligned with the side edges 43a, 43b of the control gates, rather than having the floating gates be wider than the control gates.

This embodiment is fabricated in accordance with the steps illustrated in Figures 4A - 4D, following which control gates 43 are used as a mask in the etching of dielectric film 49 and the poly-1 layer 48 to form floating gates 41, as illustrated in Figure 7A. With the control gates as a mask, the edges 41c, 41d of the floating gates are aligned with the edges 43a, 43b of the control gates. Thereafter, as illustrated in Figure 7B, oxide spacers 62 are formed around the select gates and the control gates by depositing an oxide film and then etching it away anisotropically in the flat areas. As in the previous embodiment, the spacers surround the floating gates as well as the control gates. Source and drain regions 56-58 are formed by ion-implantation, and the source junctions 58 is made deeper to withstand the high voltages that are applied to the source nodes during erase operations.

Figures 8A and 8B show cross-sections of the embodiments of the memory cell arrays of Figures 3 and 6 utilizing shallow trench and LOCOS isolation for aligning the edges 41a, 41b of the floating gates with the edges 42a, 42b of the active areas. Those techniques are described in detail in Serial No. 09/255,360, the disclosure of which is incorporated herein by reference.

In the embodiment illustrated in Figure 8A, shallow trenches 63 are formed in the silicon substrate 46, and an isolation oxide 64 is deposited in the trenches and planarized. When the poly-1 layer 48 is deposited, it covers the isolation oxide as well as the thermal oxide 47, and when it is etched to form the floating gates, it remains on the side walls of the isolation

oxide as well as on the thermal oxide. Thus, the floating gates have side walls 41e and bottom walls 41f, with the height of the side walls being on the order of 80 to 160 percent of the width of the bottom walls. The control gates 43 extend into the regions bounded by the side walls, and the areas of the side walls add significantly to the capacitance between the gates.

Since the trenches in which the isolation oxide is formed define the edges 42a, 42b of the active areas, the edges 41a, 41b of the floating gates are automatically aligned with those edges when the floating gates are formed on the sides of the isolation oxide. Again in this embodiment, the floating gates have side walls 41e and bottom walls 41f, with the height of the side walls being on the order of 80 to 160 percent of the width of the bottom walls. By making the poly-1 layer thin and having it extend along the side walls as well as the bottom walls of the control gates, the capacitance between the control gates and the floating gates is made high. By increasing the height 66 of the isolation oxide above the surface of the poly-1 material, the capacitance can be further increased. This results in a large coupling ratio between the control gates and the floating gates.

The embodiment of Figure 8B is similar to the embodiment of Figure 8A except that it uses LOCOS isolation instead of shallow trenching. In this embodiment, the isolation oxide 67 is thermally grown to define the edges 42a, 42b of the active areas, and the poly-1 layer which forms the floating gates is deposited over that oxide. Since the floating gates extend along the side walls of the isolation oxide, the edges 41a, 41b of the floating gates are automatically aligned with the edges of the active areas. With the thin poly-1 layer extending along both the side walls and the bottom walls of the control gates, the capacitance between the control gates and the floating gates is once again high, and can be made even higher by increasing the height 69 of the isolation oxide. This again results in a large coupling ratio between the control gates and the floating gates.

Figures 9A - 9F illustrate another process for fabricating the memory cell array of Figure 6. This process is similar in certain respects to the process of Figures 4A - 4D and 7A - 7B, and like reference numerals designate corresponding elements in the two embodiments.

As illustrated in Figure 9A, an oxide layer 47 having a thickness on the order of 70 - 120 Å is thermally grown on a silicon substrate 46, and a conduction layer 48 of polysilicon or amorphous silicon (poly-1) having a thickness on the order of 100 - 1000 Å is deposited on the thermal oxide. The poly-1 layer is doped with phosphorus, arsenic or boron to a level on the order of 10^{17} to 10^{20} per cm^3 either *in-situ* during deposition of the silicon or by ion implantation.

A photolithographic mask (not shown) is then formed over the poly-1 layer to define the floating gate pattern, and the poly-1 layer not covered by the photoresist is removed by anisotropic dry etching, as illustrated in Figure 9B. After stripping the photoresist, a dielectric film 49 is formed on the remaining areas of the poly-1 layer and on the substrate surrounding them. This film can be either a pure oxide or a combination of oxide and nitride, and in one presently preferred embodiment, it consists of a lower oxide layer having a thickness on the order of 30 - 100 Å, a central nitride layer having a thickness on the order of 60 - 300 Å, and an upper oxide layer having a thickness on the order of 30 - 100 Å.

As illustrated in Figure 9C, the areas for the stack transistors are then separated from the areas for the select transistors by forming a photolithographic mask 70 over the areas in which stack transistors are to be formed, and removing the dielectric film in the remaining area where the select transistors are to be formed. After the photoresist is stripped, a thermal oxide layer 47a having a thickness on the order of 150 - 350 Å is formed on the substrate as a gate oxide for the select transistors.

A second polysilicon layer (poly-2) 51 is deposited across the wafer to form the conduction layer 51a, 51b for the control gates and the select gates, as illustrated in Figure 9D. The poly-2 layer has a thickness on the order of 1500 - 3000 Å, and is doped with phosphorus, arsenic or boron to a level on the order of 10^{20} to 10^{21} per cm^3. If desired, a polycide film can be formed on the poly-2 layer to reduce its sheet resistance.

A photolithographic mask (not shown) is positioned over the poly-2 layer to define the control gates and the select gates, and an anisotropic etch is performed to remove the poly-2 layer in the unmasked areas and thereby form control gates 43 and select gates 44. As illustrated in Figure 9E, the control gates are narrower than the floating gates and are well centered on them.

As illustrated in Figure 9F, oxide spacers 61 are formed around the control gates, floating gates and select gates by depositing an oxide film across the wafer, then removing it from the flat areas by an anisotropic dry etch. Source and drain regions 56 - 58 are formed in the substrate by ion implantation with impurities opposite to the substrate material, with the junction depth of source region 58 or drain region 57 of the stack transistor being made deeper to sustain the high voltages that are applied to it during erase operations.

A circuit diagram for the memory cell arrays of Figures 3 and 6 is shown in Figure 10. All of the memory cells in a given column have their drains connected to bit lines BL_{n-1}, BL_n, BL_{n+1}, etc., which are typically metal lines 71-73 that cross over the active areas, and are isolated from each other by a dielectric film (not shown). All of the cells in a given row are connected to a source line 74, which is typically an N+ or P+ diffusion layer in the silicon substrate 46. In a given row, all of the control gates 43 are connected together by the portion of the poly-2 layer 51a of which they are formed, and all of the select gates 44 are connected to a word line

comprising the portion of the poly-2 layer 51b of which they are formed. The control gates and the select gates cross over the active areas and the isolation oxides.

Operation of the memory cells fabricated in accordance with the processes of Figures 4A-4F, 5A-5C, 7A-7B and 9A-9F is as follows, with bias voltages applied to the four node terminals as set forth in Table 1.

Table 1

Mode	Control Gate	Select Gate	Drain	Source
Erase (1)	0 volts	Floating	Floating	12 to 15 volts
Erase (2)	-5 to -10 volts	Floating	Floating	5 to 10 volts
Erase (3)	-5 to -10 volts	7 to 12 volts	5 to 10 volts	Floating
Program (1)	8 to 12 volts	6 to 8 volts	5 volts	0 volts
Program (2)	12 to 15 volts	0 volts	Floating	0 volts
Program (3)	12 to 15 volts	2 to 5 volts	0 volts	Floating
Read	1.5 to 3 volts	3 to 5 volts	1.5 to 3 volts	0 volts

In the erase mode, electrons are forced to travel from the floating gates 41 to the overlapped source regions 58a or the overlapped drain regions 57a by Fowler-Nordheim tunneling. During erase operations, a relatively high electric field (greater than 10mV/cm) is established across tunnel oxide 47. Erase paths between the floating gates 41 and the overlapped source nodes 58a are established either by applying 0 volts to the control gates and about 12 to 15 volts to the source nodes, or by applying a negative voltage of about -5 to -10 volts to the control gates and a positive voltage of about 5 to 10 volts to the source nodes. Those are the two modes which are designated Erase (1) and Erase (2) in Table 1. In both cases, the select gate and the drain node are kept floating.

Alternatively, erase paths can be established between the floating gates 41 and the overlapped drain nodes 57a by applying a negative voltage of about -5 to -10 volts to the control gates, a positive voltage of about 5 to 10 volts to the drain nodes, a positive voltage of about 7 to 12 volts to the select gates, and keeping the source nodes floating. This is the Erase (3) mode shown in Table 1.

In all of these embodiments, the coupling ratio from the control gate to the floating gate in the erase mode is typically on the order of 85 percent. Accordingly, most of the voltage difference between the source or drain and control gates is applied across the tunnel oxide, initiating Fowler-Nordheim tunneling and forcing electrons to migrate from the floating gates to the overlapped source or drain regions. After an erase operation, the floating gates are positively charged, the threshold voltage of the cell becomes lower, and the cell is in a conducting, or logic "1", state.

In the program mode, electrons are injected into the floating gates, and the floating gates become negatively charged. This can be done either by hot carrier injection or by Fowler-Nordheim tunneling. In hot carrier injection, shown as the Program (1) mode in Table 1, the control gates are biased about 8 to 12 volts, the select gates are biased at about 6 to 8 volts, the drains are biased at about 5 volts, and the sources are biased at 0 volts. When electrons flow from the sources 58 to the drains 57, they are accelerated by the high electric field in the channel regions 42, and some of them become heated near the drain junctions. Some of the hot electrons exceed the oxide barrier height of about 3.1 eV and are injected into the floating gates.

Fowler-Nordheim tunneling can be utilized for programming by biasing the nodes in either of the two ways indicated as the Program (2) and Program (3) modes in Table 1. In the Program (2) mode, programming paths are established between the floating gates 41 and the overlapped source nodes

58a by applying about 12 to 15 volts to the control gates and 0 volts to the source nodes and the select gates at 0 volts, with the drain nodes floating. In the Program (3) mode, programming paths are established between the floating gates and the overlapped drain nodes 57a by applying about 12 to 15 volts to the control gates, 0 volts to the drain nodes, and about 2 to 5 volts to the select gates, with the source nodes floating. Following a programming operation, the floating gates are negatively charged, the threshold voltage of the cell becomes higher, and the cell is in a non-conducting, or logic "0", state.

In the read mode, the control gates are biased to about 1.5 to 3 volts, the select gates are biased to about 3 to 5 volts, the sources are biased to 0 volts, and the drains are biased to about 1.5 to 3 volts. When a memory cell is in an erase state, the read shows a conducting state, and the sense amplifier reads a logic "1". When the cell is in the programming state, the read shows a non-conducting state, and the sense amplifier reads a logic "0".

When memory cells are constructed in P-wells, a programming operation using Fowler-Nordheim tunneling can be performed by applying 0 volts to the P-well nodes and about 12 to 18 volts to the control gates, with the source and drain nodes floating. In this mode, electrons migrate from the channel regions 42 to the floating gates 41, and the floating gates become negatively charged.

It is apparent from the foregoing that a new and improved memory cell and fabrication process have been provided. While only certain presently preferred embodiments have been described in detail, as will be apparent to those familiar with the art, certain changes and modifications can be made without departing from the scope of the invention as defined by the following claims.

CLAIMS

1. In a memory cell: a substrate having an active area and source and drain regions, a floating gate having lateral edges which are aligned directly above edges of the active area, a control gate positioned directly above the floating gate, and a select gate spaced laterally from the control gate.

2. The memory cell of Claim 1 wherein the floating gate has a bottom wall and side walls which face corresponding walls of the control gate in capacitive coupling relationship, with the height of the side walls being on the order of 80 to 160 percent of the width of the bottom wall.

3. The memory cell of Claim 2 wherein the bottom wall and the side walls of the floating gate have a thickness no greater than about 1000 Å.

4. The memory cell of Claim 1 wherein the floating gate is wider than the control gate, and portions of the floating gate protrude laterally beyond the control gate.

5. The memory cell of Claim 4 wherein one of the protruding portions of the floating gate overlies the source region, and the other overlies the drain region.

6. The memory cell of Claim 5 wherein an erase window is formed between the source region and the protruding portion of the floating gate which overlies it.

7. The memory cell of Claim 1 wherein an erase path is formed between the floating gate and the source region.

8. The memory cell of Claim 1 wherein the control gate, the select gate and the source and drain regions are biased to establish a Fowler-Nordheim

tunneling path from the floating gate to the source region during an erase operation.

9. The memory cell of Claim 1 wherein the control gate, the select gate and the source and drain regions are biased to establish a Fowler-Nordheim tunneling path from the floating gate to the drain region during an erase operation.

10. The memory cell of Claim 1 wherein the control gate, the select gate and the source and drain regions are biased to establish a Fowler-Nordheim tunneling path from the source region to the floating gate during a programming operation.

11. The memory cell of Claim 1 wherein the control gate, the select gate and the source and drain regions are biased to establish a Fowler-Nordheim tunneling path from the drain region to the floating gate during a programming operation.

12. The memory cell of Claim 1 wherein the control gate, the select gate and the source and drain regions are biased to establish hot carrier injection from the active region to the floating gate during a programming operation.

13. In a process of fabricating a memory cell, the steps of: forming an active area in a substrate, forming a floating gate having lateral edges which are aligned directly above edges of the active area, forming a control gate directly above the floating gate, forming a select gate which is spaced laterally from the control gate, and forming source and drain regions in the substrate.

14. The process of Claim 13 wherein the floating gate is formed with a bottom wall and side walls which face corresponding walls of the control

gate in capacitive coupling relationship, with the height of the side walls being on the order of 80 to 160 percent of the width of the bottom wall.

15. The process of Claim 14 wherein the bottom wall and the side walls of the floating gate are formed with a thickness no greater than about 1000 Å.

16. The process of Claim 13 wherein the floating gate is formed wider than the control gate, with portions of the floating gate protruding laterally beyond the control gate.

17. The process of Claim 16 wherein one of the protruding portions of the floating gate is formed to overly the source region, and the other is formed to overly the drain region.

18. The process of Claim 17 wherein an erase window is formed between the source region and the protruding portion of the floating gate which overlies it.

19. The process of Claim 13 wherein an erase path is formed between the floating gate and the source region.

20. The process of Claim 13, including the steps of biasing the control gate, the select gate and the source and drain regions to establish a Fowler-Nordheim tunneling path from the floating gate to the source region during an erase operation.

21. The process of Claim 13, including the steps of biasing the control gate, the select gate and the source and drain regions to establish a Fowler-Nordheim tunneling path from the floating gate to the drain region during an erase operation.

22. The process of Claim 13, including the steps of biasing the control gate, the select gate and the source and drain regions to establish a Fowler-Nordheim tunneling path from the source region to the floating gate during a programming operation.

23. The process of Claim 13, including the steps of biasing the control gate, the select gate and the source and drain regions to establish a Fowler-Nordheim tunneling path from the drain region to the floating gate during a programming operation.

24. The process of Claim 13, including the steps of biasing the control gate, the select gate and the source and drain regions to establish hot carrier injection from the active region to the floating gate during a programming operation.

25. In a process of fabricating a memory cell having stack transistors and select transistors, the steps of: forming a poly-1 layer and an overlying dielectric film on a substrate in areas in which the stack transistors are to be formed, forming a poly-2 layer over the dielectric film and over areas of the substrate in which the select transistors are to be formed, patterning the poly-2 layer to form control gates for the stack transistors and select gates for the select transistors, removing the poly-1 layer and the dielectric film to form floating gates in areas which are not covered by the control gates, and forming source and drain regions for the transistors in the substrate.

26. The process of Claim 25 wherein the poly-1 layer and the overlying dielectric film are formed in the areas for the stack transistors by depositing the poly-1 layer and the dielectric film over the entire substrate, and then removing the poly-1 layer and the dielectric film in areas outside the areas in which the stack transistors are to be formed.

27. The process of Claim 25 including the steps of forming oxide spacers on the sides of the control gates, and using the control gates and the oxide spacers as a mask in the removal of the poly-1 layer and the dielectric film so that floating gates extend laterally beyond the control gates.

28. The process of Claim 25 including the steps of forming a thermal oxide layer on the side walls of the control gates, and using control gates and the thermal oxide layer as a mask in the removal of the poly-1 layer and the dielectric film so that floating gates extend laterally beyond the control gates.

29. The process of Claim 25 where in the floating gates are aligned with active areas in the substrate by forming isolation oxide regions which extend above the substrate at the edges of the active areas, and forming the floating gates on the sides of the isolation oxide regions in alignment with the edges of the active areas.

30. The process of Claim 29 wherein the isolation oxide regions are formed by forming shallow trenches in the substrate to define the active areas, and depositing the isolation oxide in the trenches.

31. The process of Claim 29 wherein the isolation oxide regions are formed by thermally growing the isolation oxide on the substrate to define the active areas.

32. In a process of fabricating a memory cell having stack and select transistors, the steps of: forming floating gates for the stack transistors from a poly-1 layer on a substrate, forming a dielectric film over the floating gates, forming a gate oxide on the substrate for the select transistors, forming control gates and select gates of a poly-2 material on the dielectric film and the gate oxide, with the control gates being narrower

around the control gates, floating gates and select gates, and forming source and drain regions in the substrate for the stack transistors and the select transistors.

33. The process of Claim 32 wherein the floating gates are formed by forming the poly-1 layer on the substrate, patterning the poly-1 layer to define the floating gates, and removing portions of the poly-1 layer to form the floating gates.

34. The process of Claim 32 wherein the poly-1 layer is formed of amorphous or poly-silicon having a thickness on the order of 100 - 1000 Å.

35. The process of Claim 34 including the step of doping the silicon with phosphorus, arsenic or boron to a level on the order of 10^{17} to 10^{20} per cm^3.

36. The process of Claim 32 wherein the dielectric film is deposited over the entire substrate, then removed from areas in which the select transistors are to be formed.

37. The process of Claim 36 wherein the gate oxide for the select transistors is formed after the dielectric film is removed from the areas in which the select transistors are to be formed.

38. The process of Claim 32 wherein the control gates and the select gates are formed by depositing a poly-2 layer over the entire substrate, then patterning the poly-2 layer to form the control gates and the select gates.

39. The process of Claim 32 wherein the control gates are formed above the floating gates, and are narrower than the floating gates.

40. The process of Claim 32 wherein the floating gates are formed in one lithographic step, and the control gates and the select gates are formed in a second photolithographic step.

Fig. 1 (Prior Art)

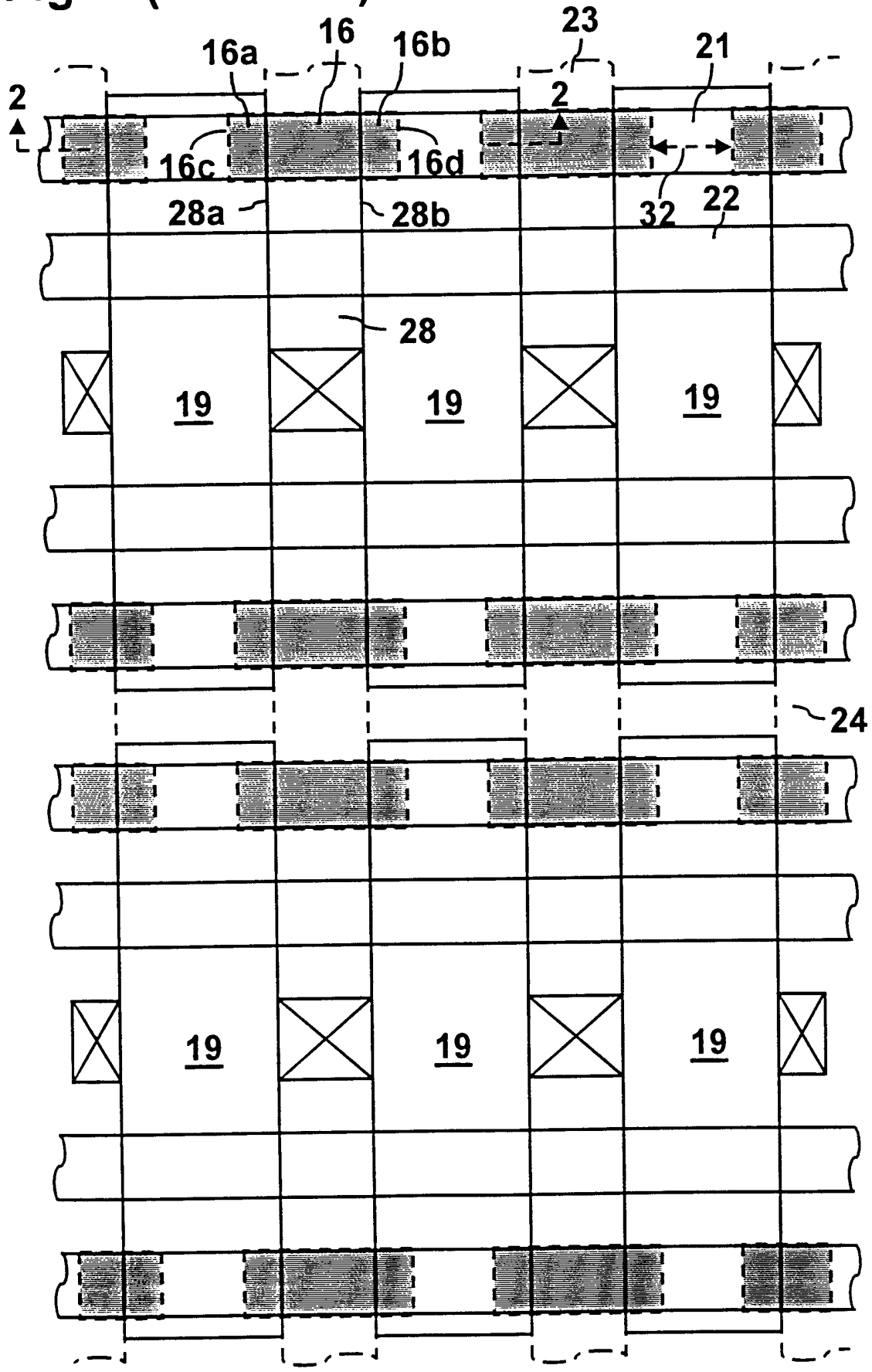


Fig. 2A (Prior Art)

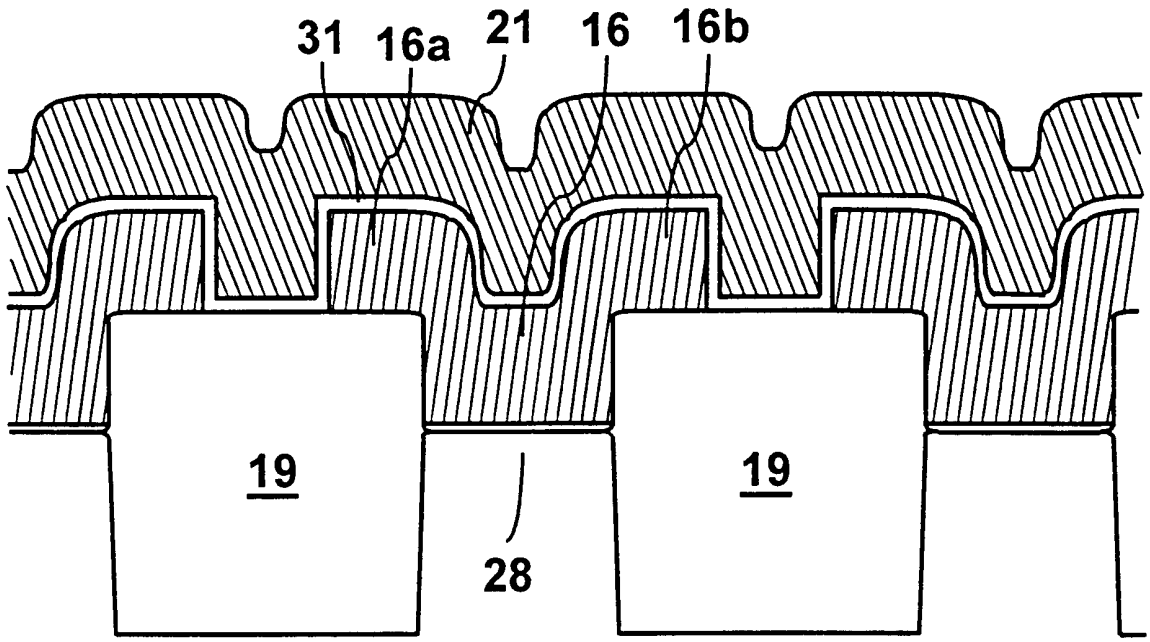


Fig. 2B (Prior Art)

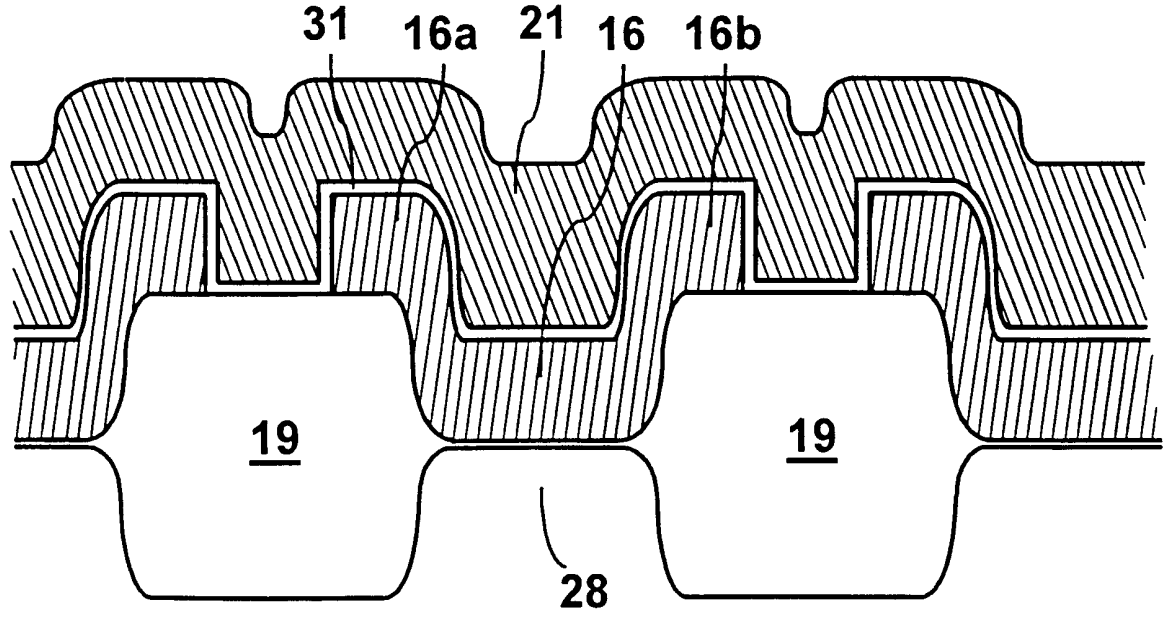
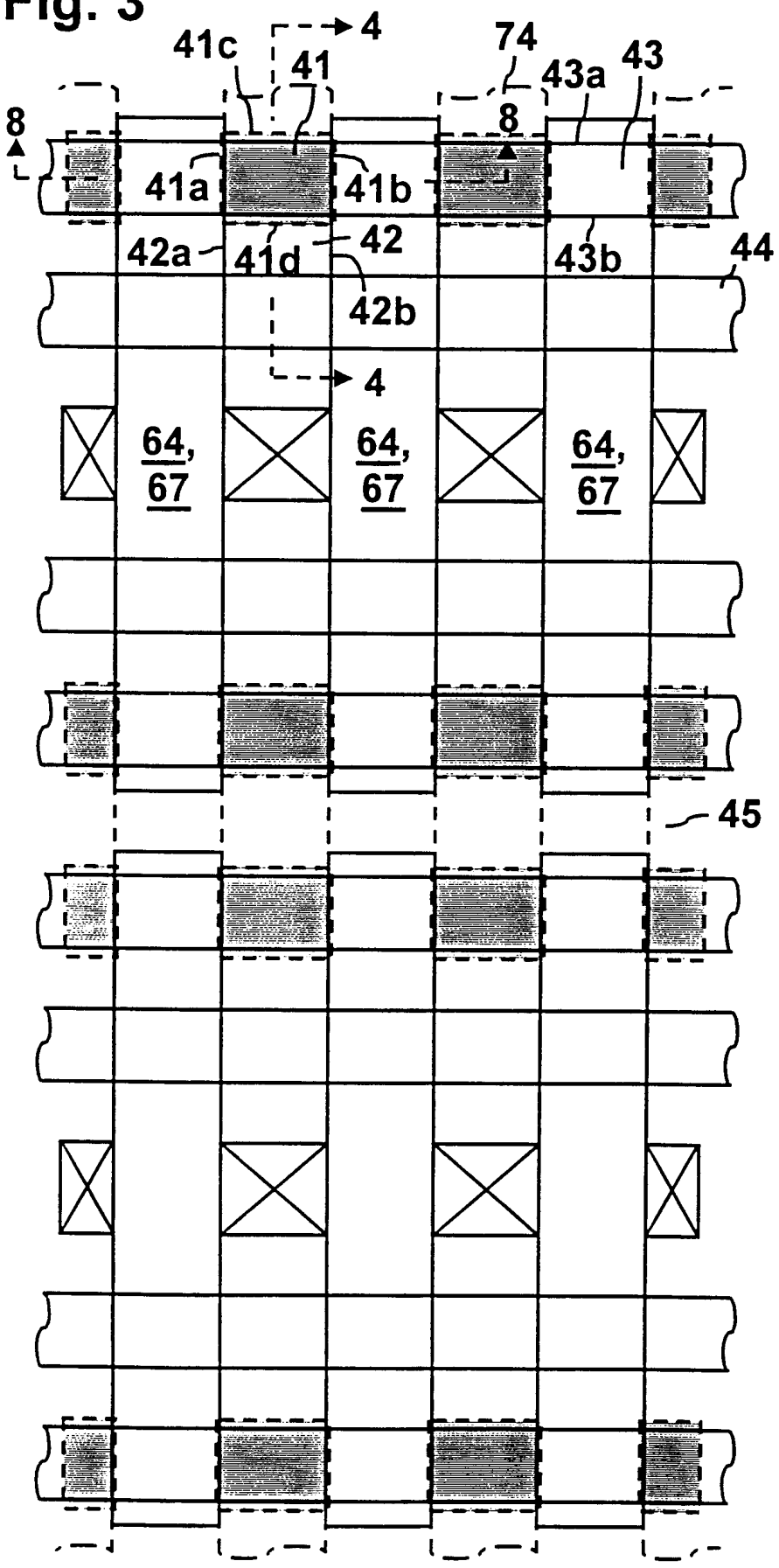


Fig. 3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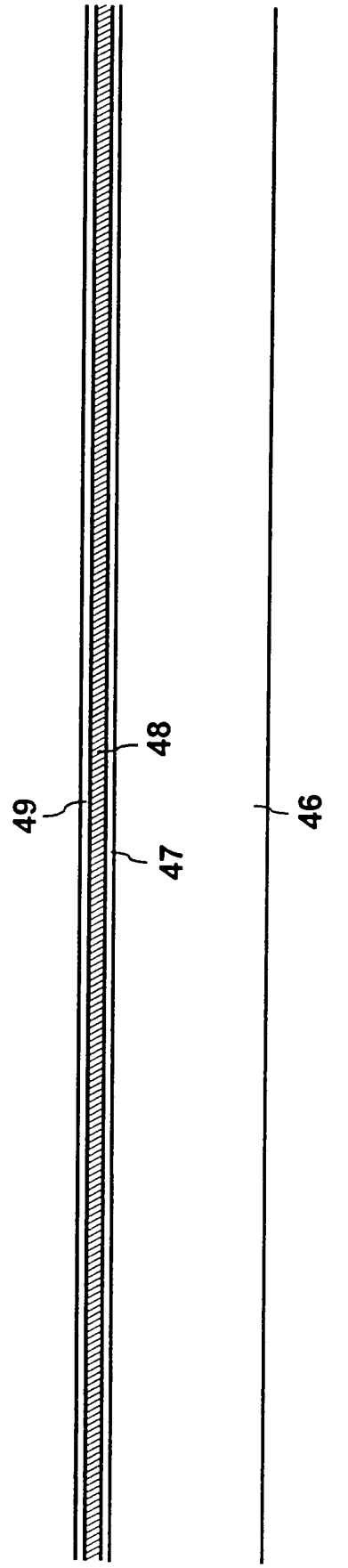

Fig. 4A

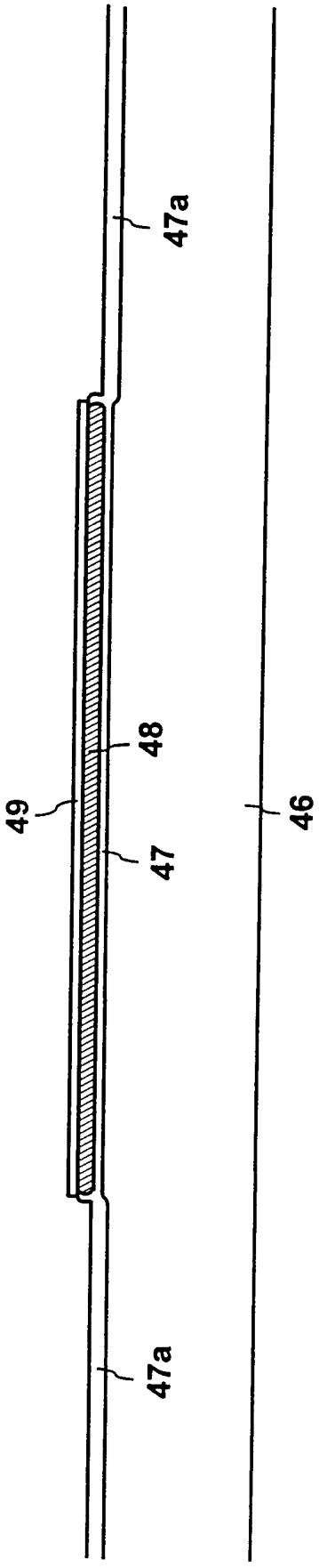

Fig. 4B

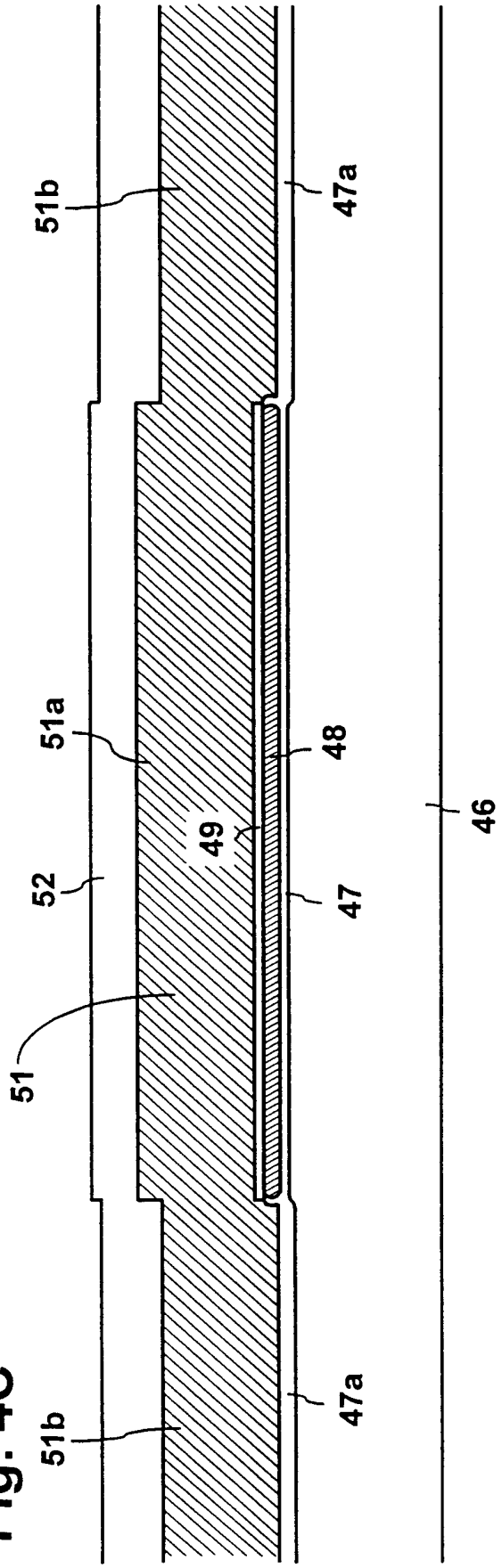
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Fig. 4C

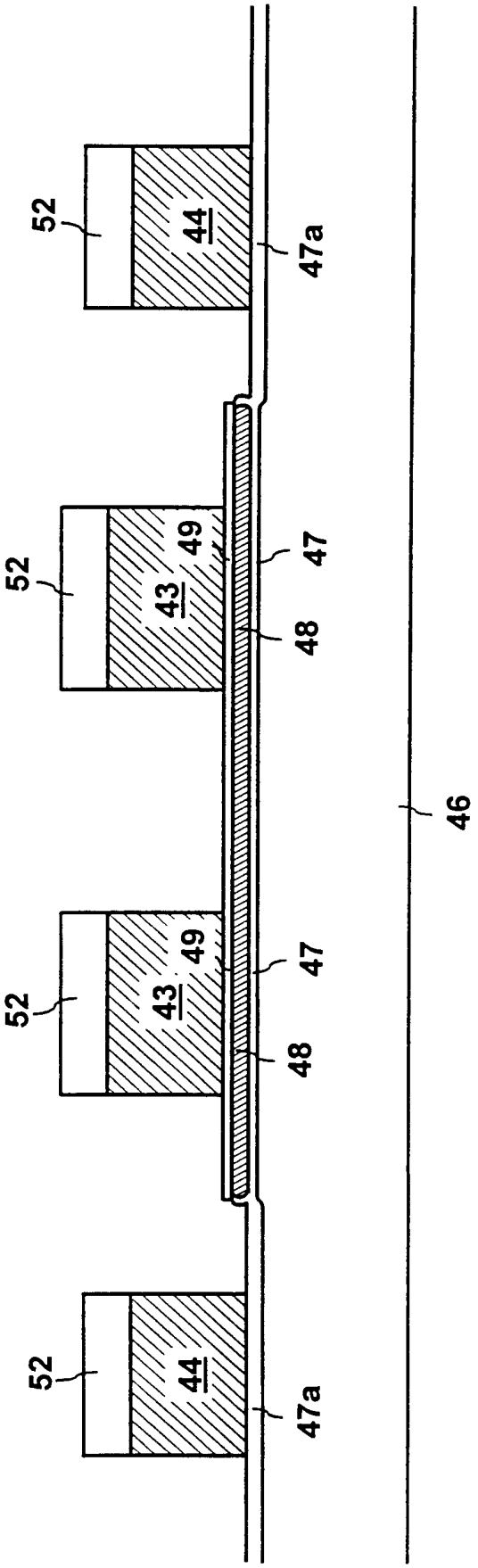
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Fig. 4D

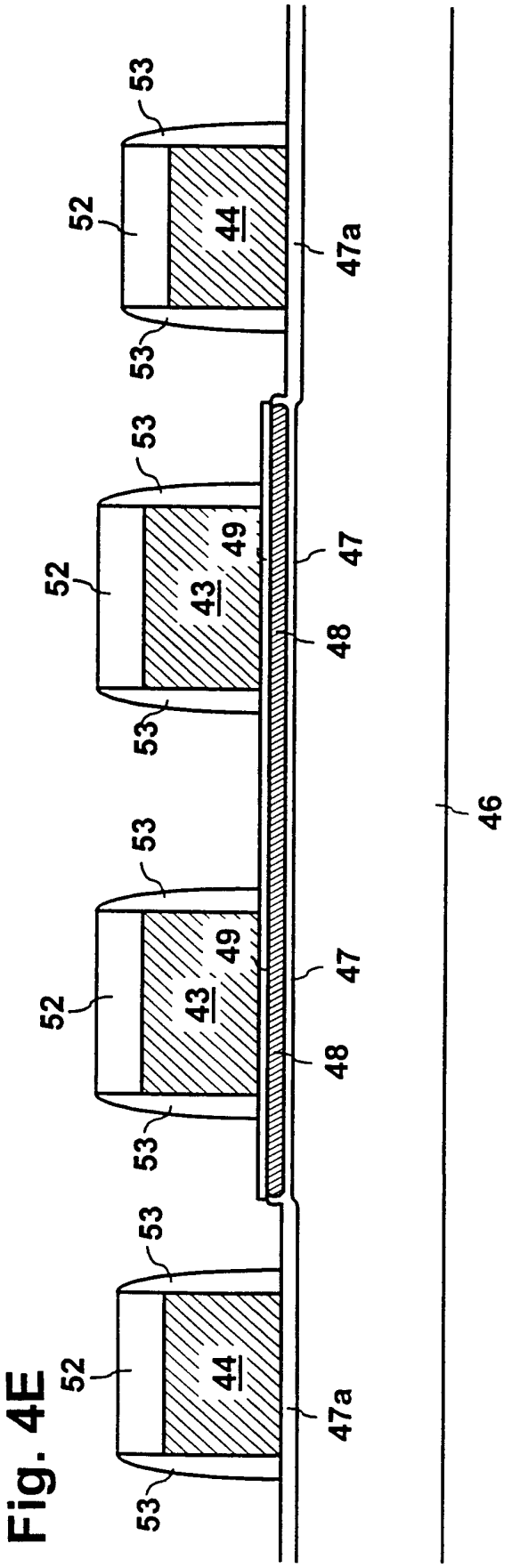
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Fig. 4E

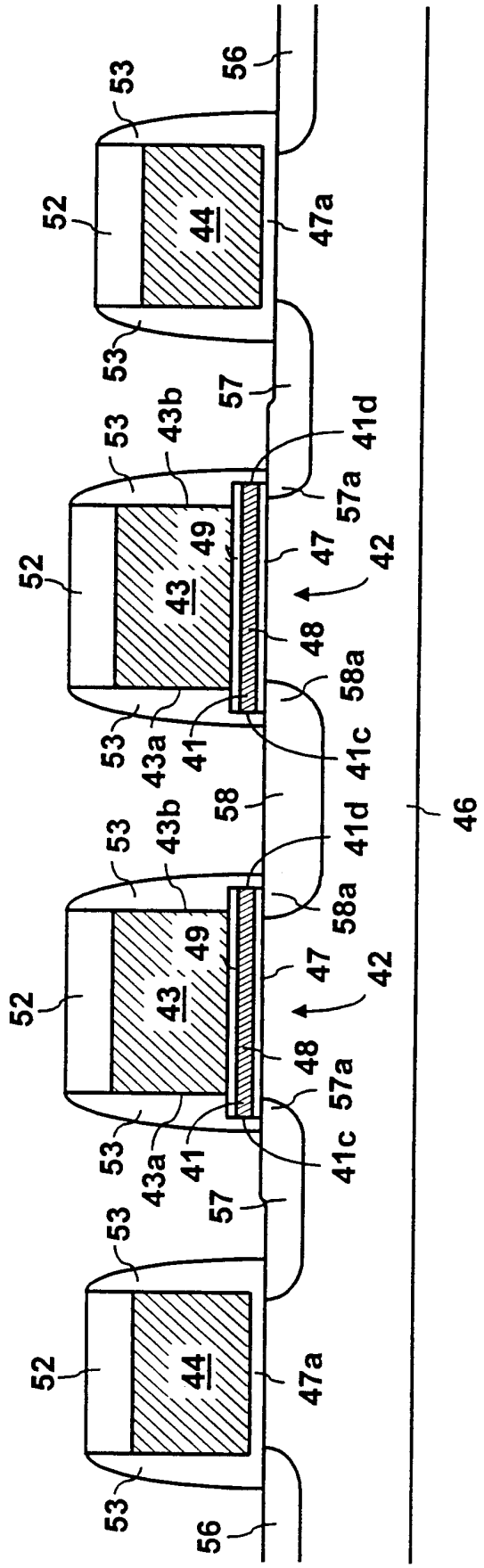
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Fig. 4F

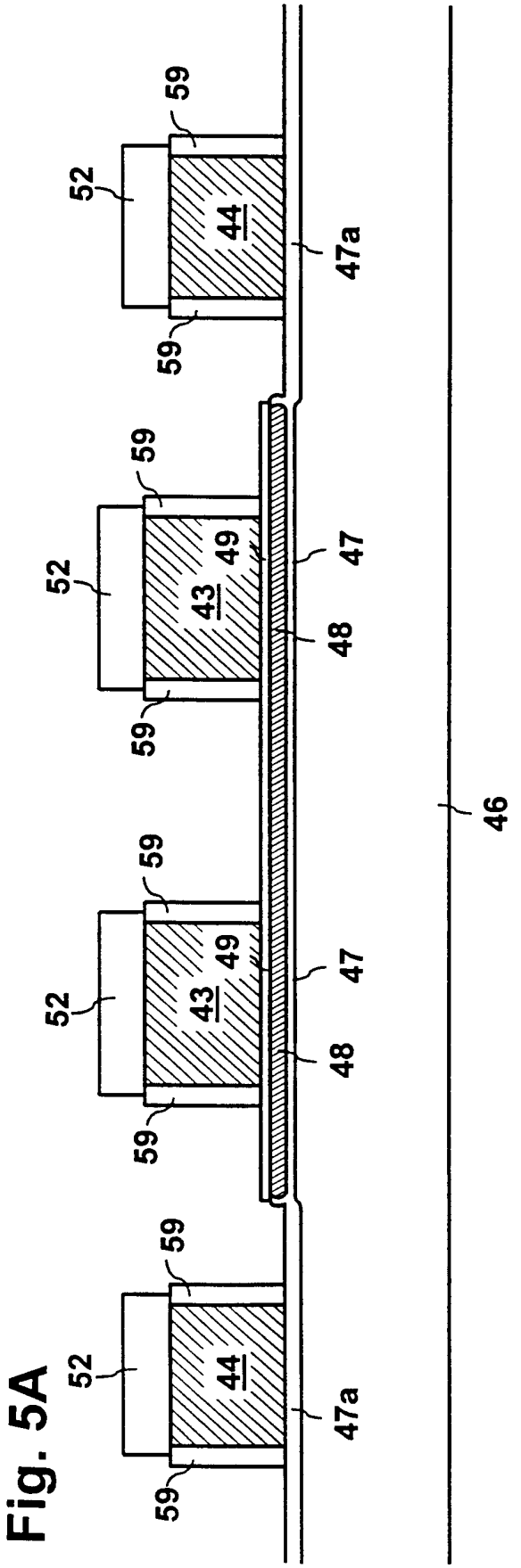
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Fig. 5A

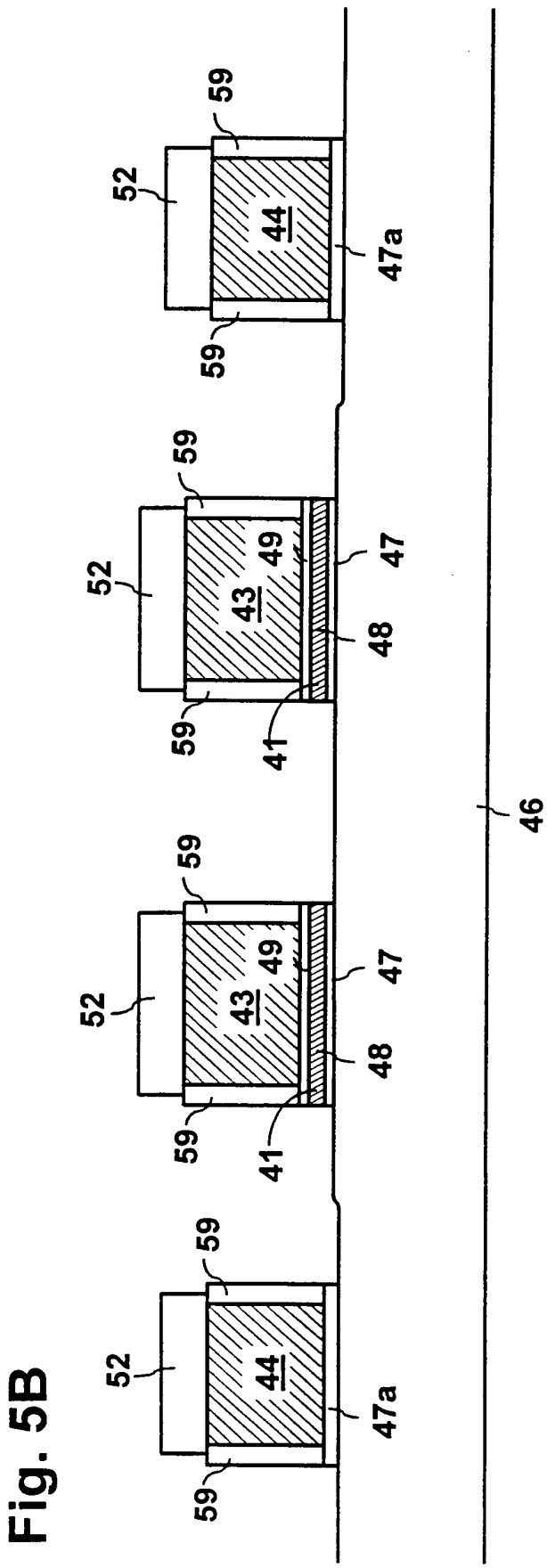
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Fig. 5B

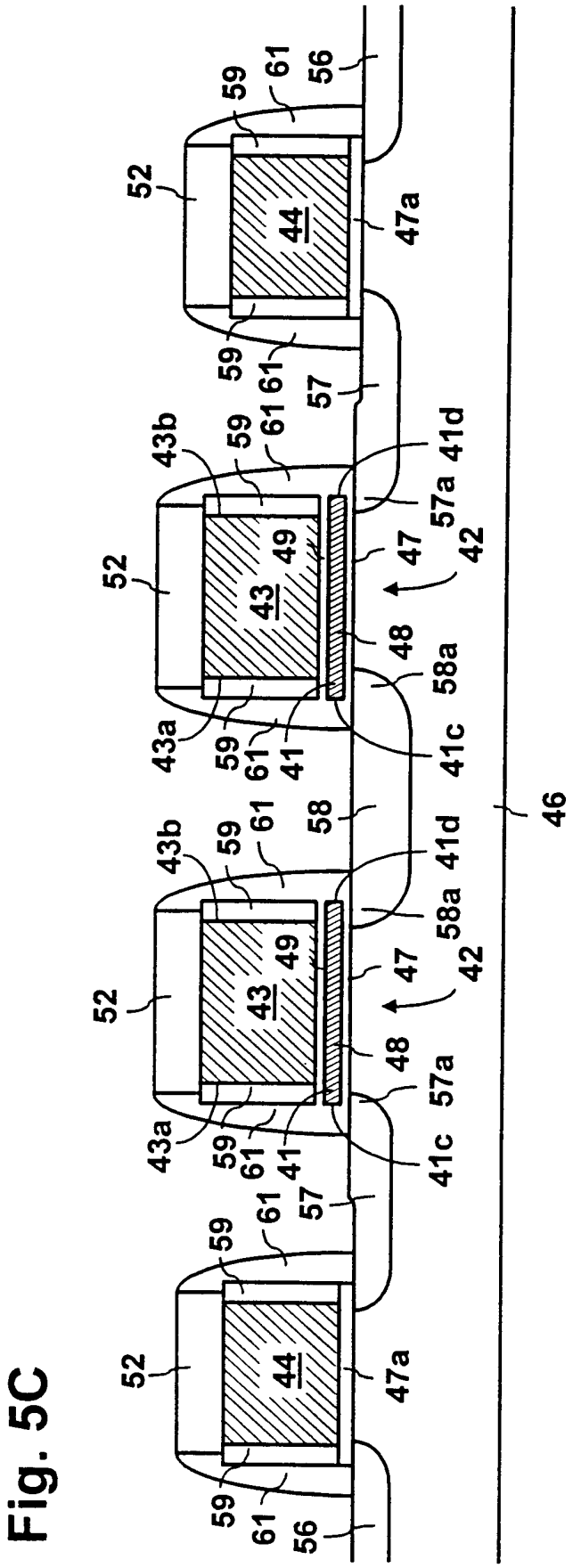
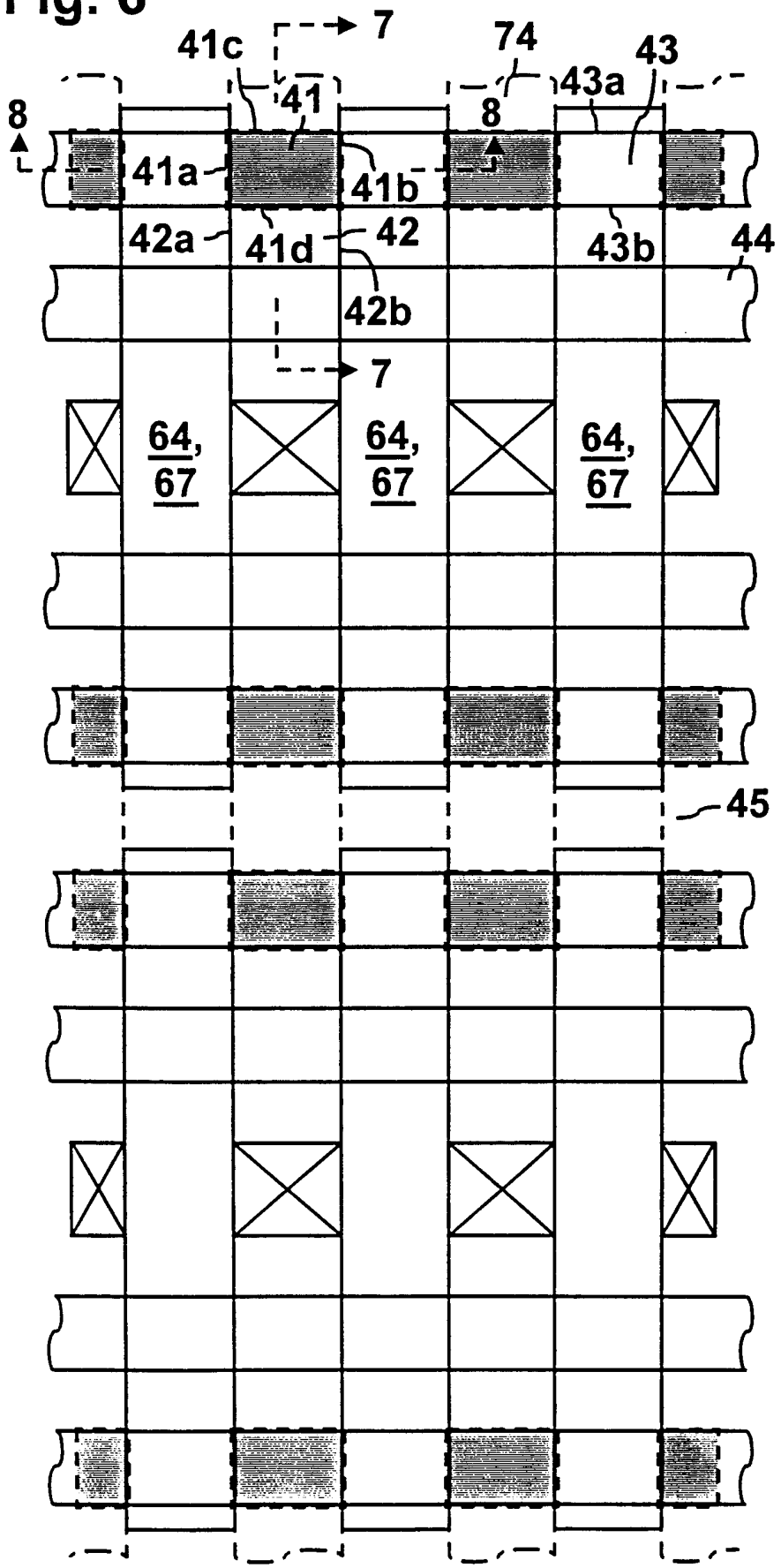


Fig. 5C

Fig. 6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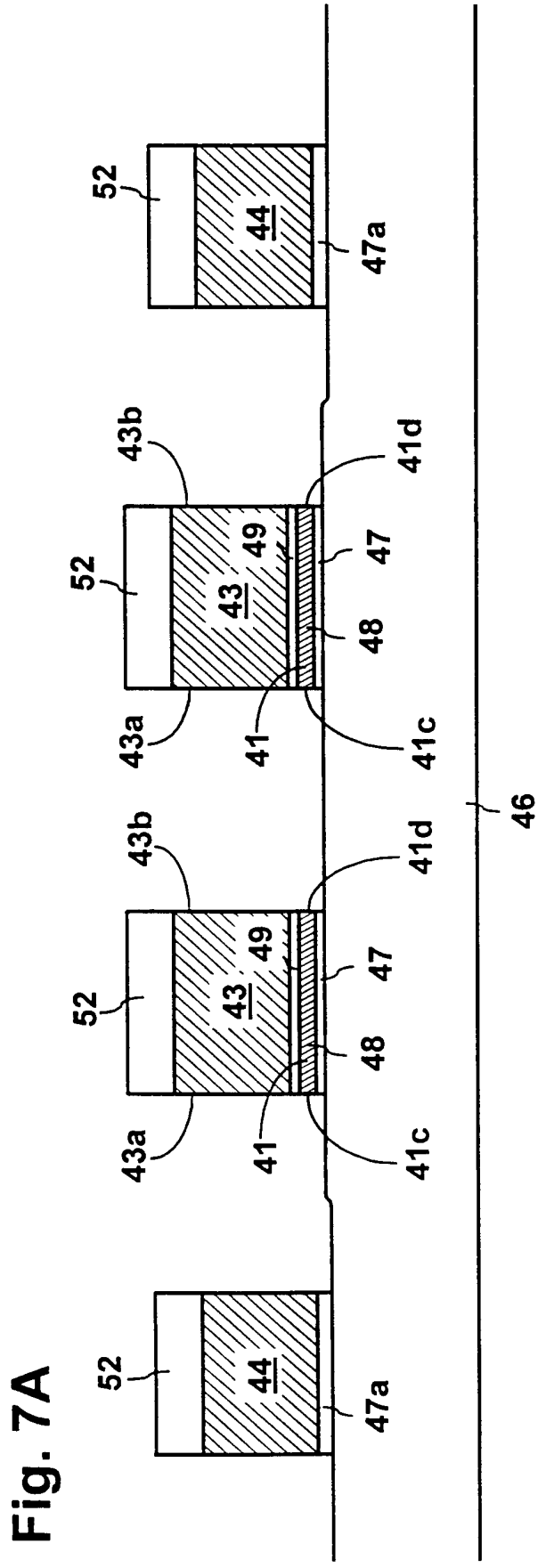
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Fig. 7A

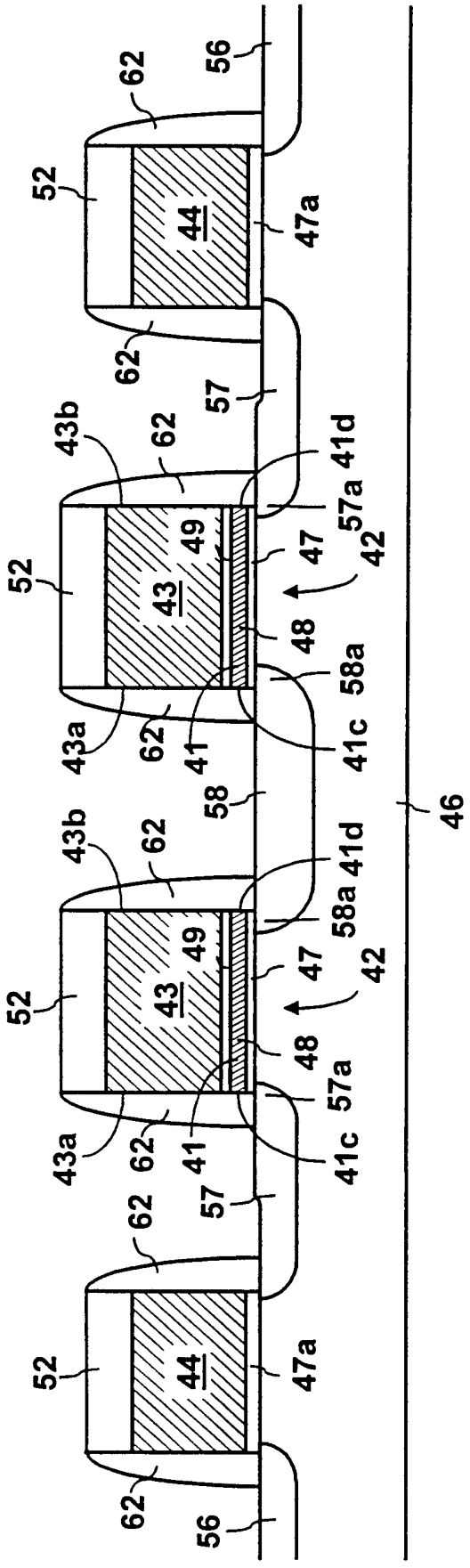
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Fig. 7B

Fig. 8A

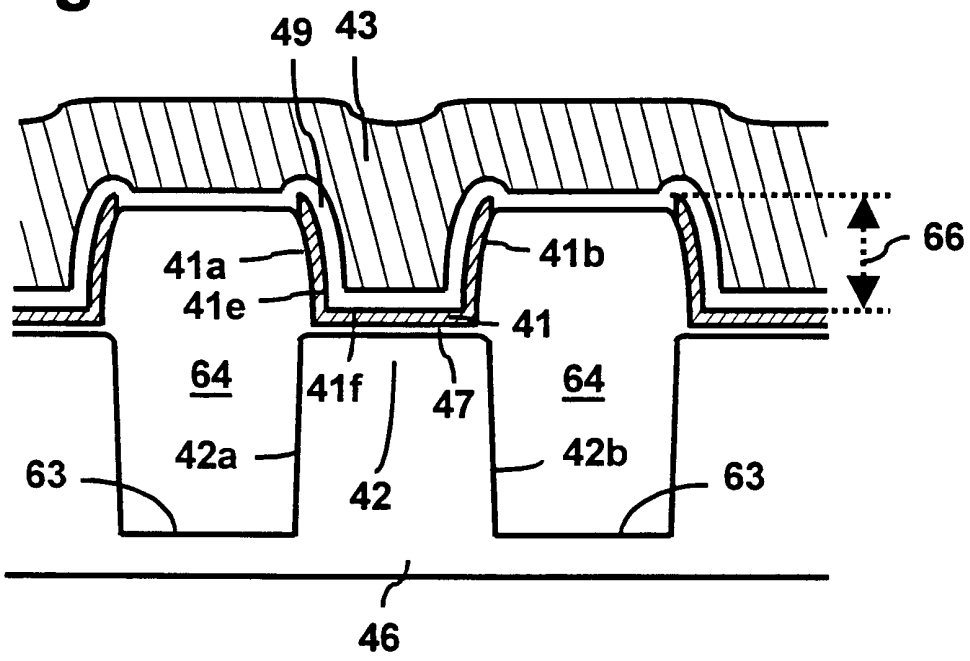
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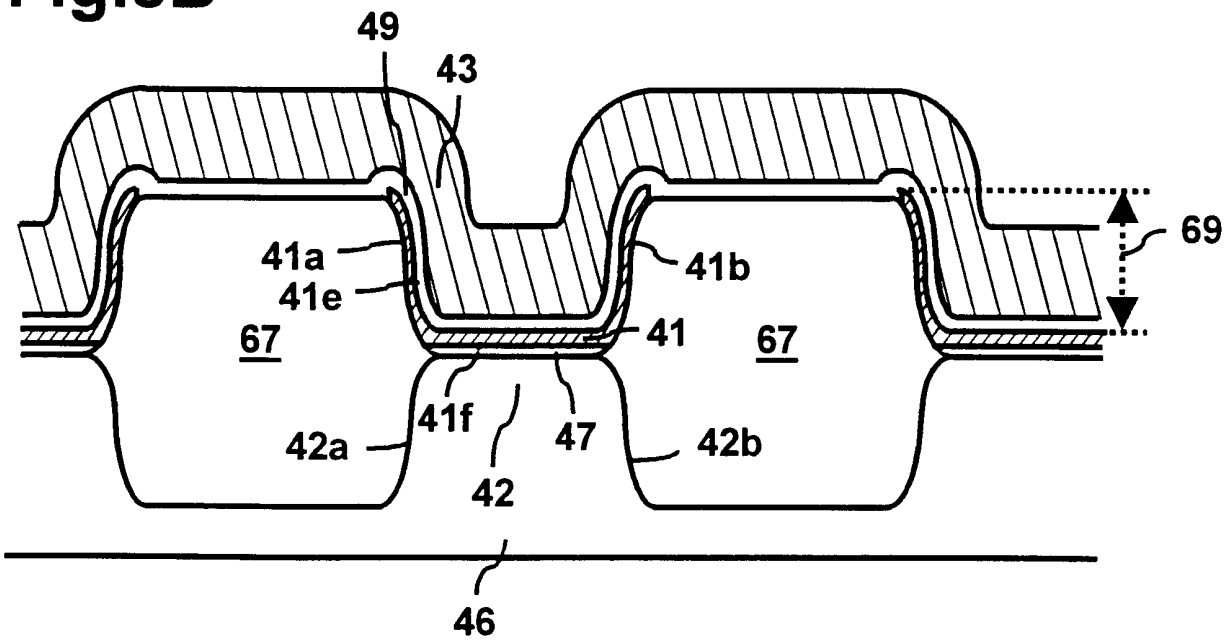
Fig.8B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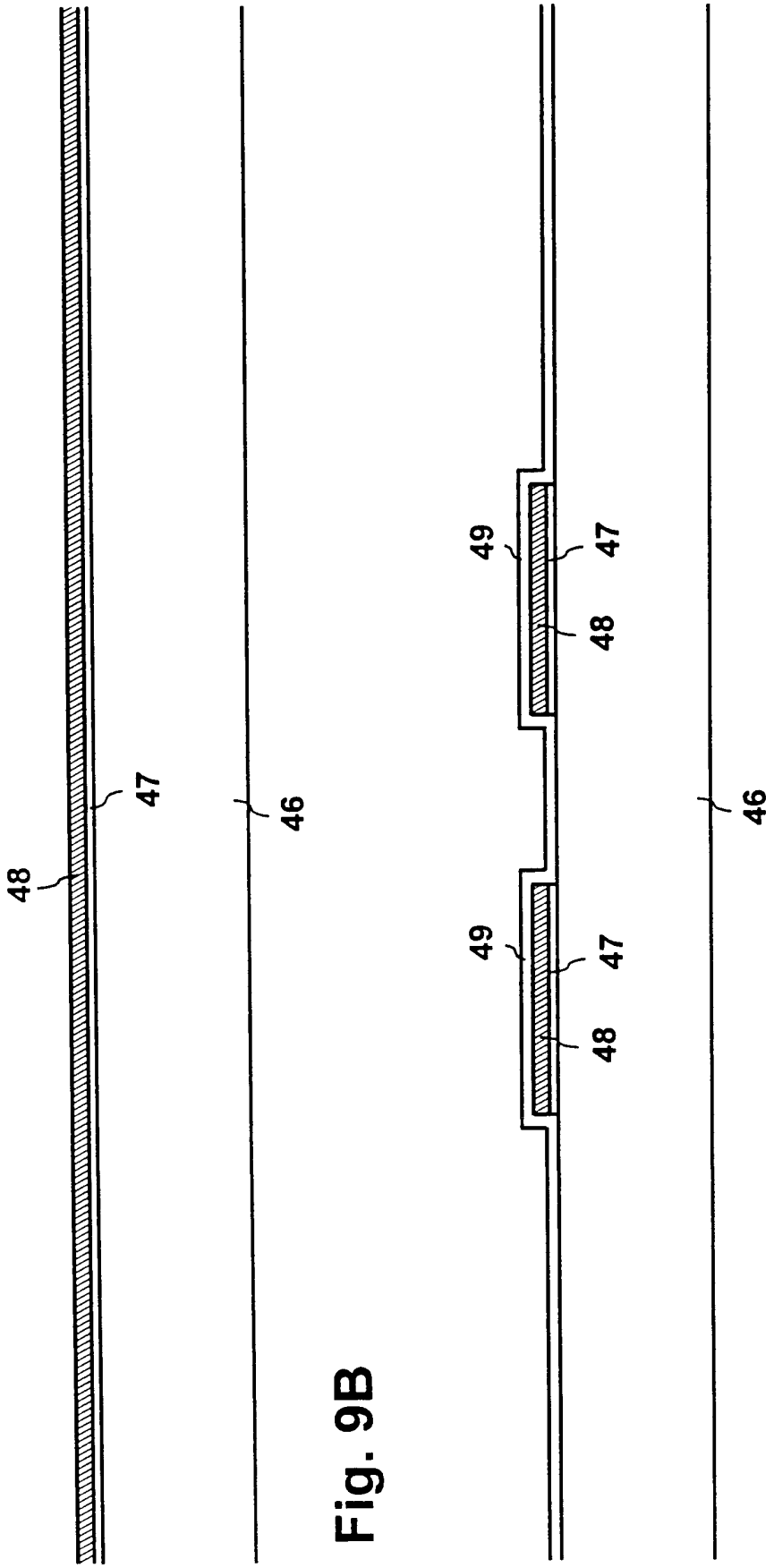

Fig. 9A

Fig. 9B

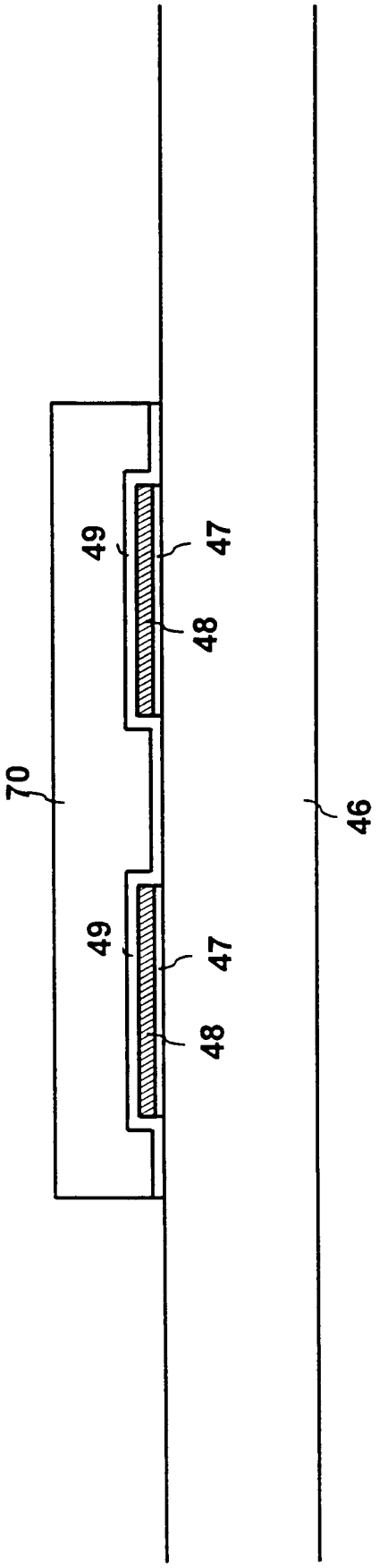
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Fig. 9C

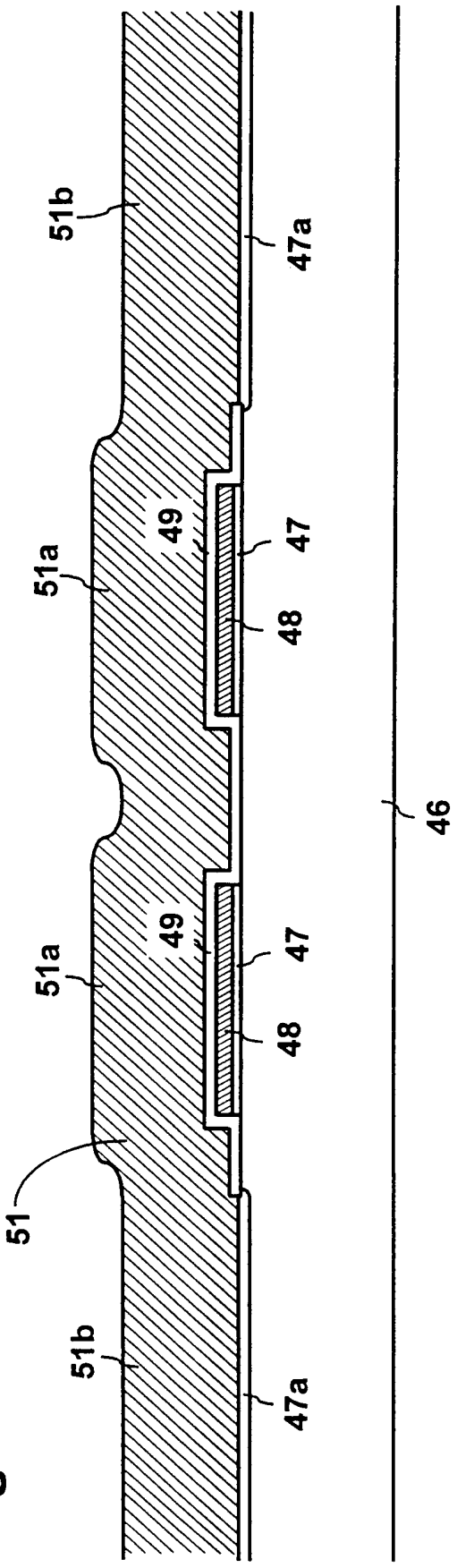
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Fig. 9D

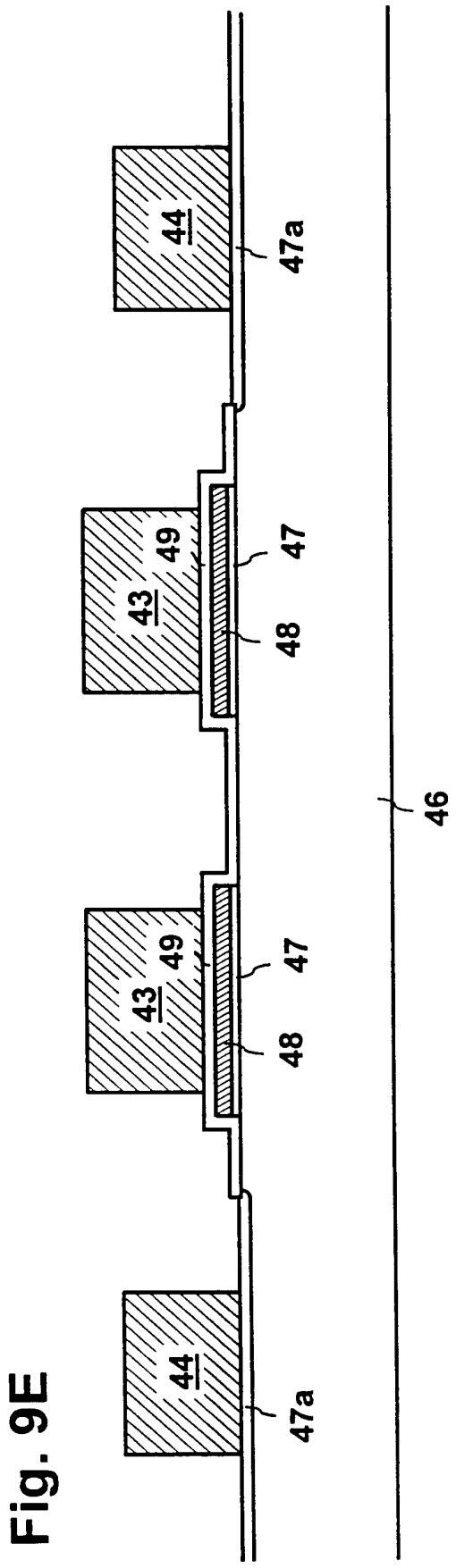
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Fig. 9E

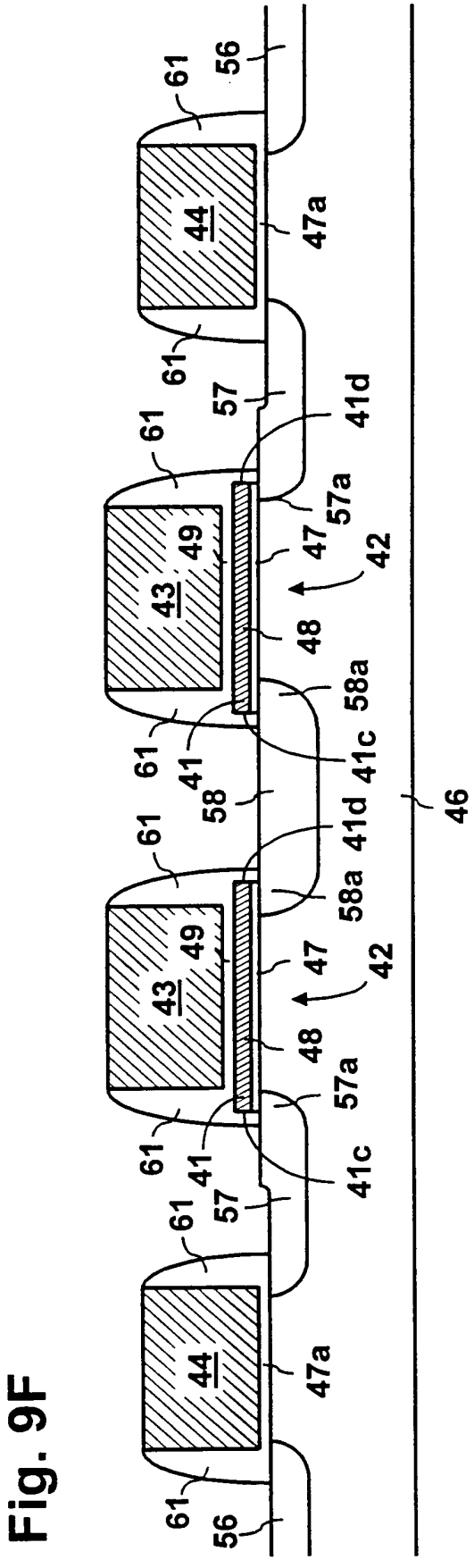
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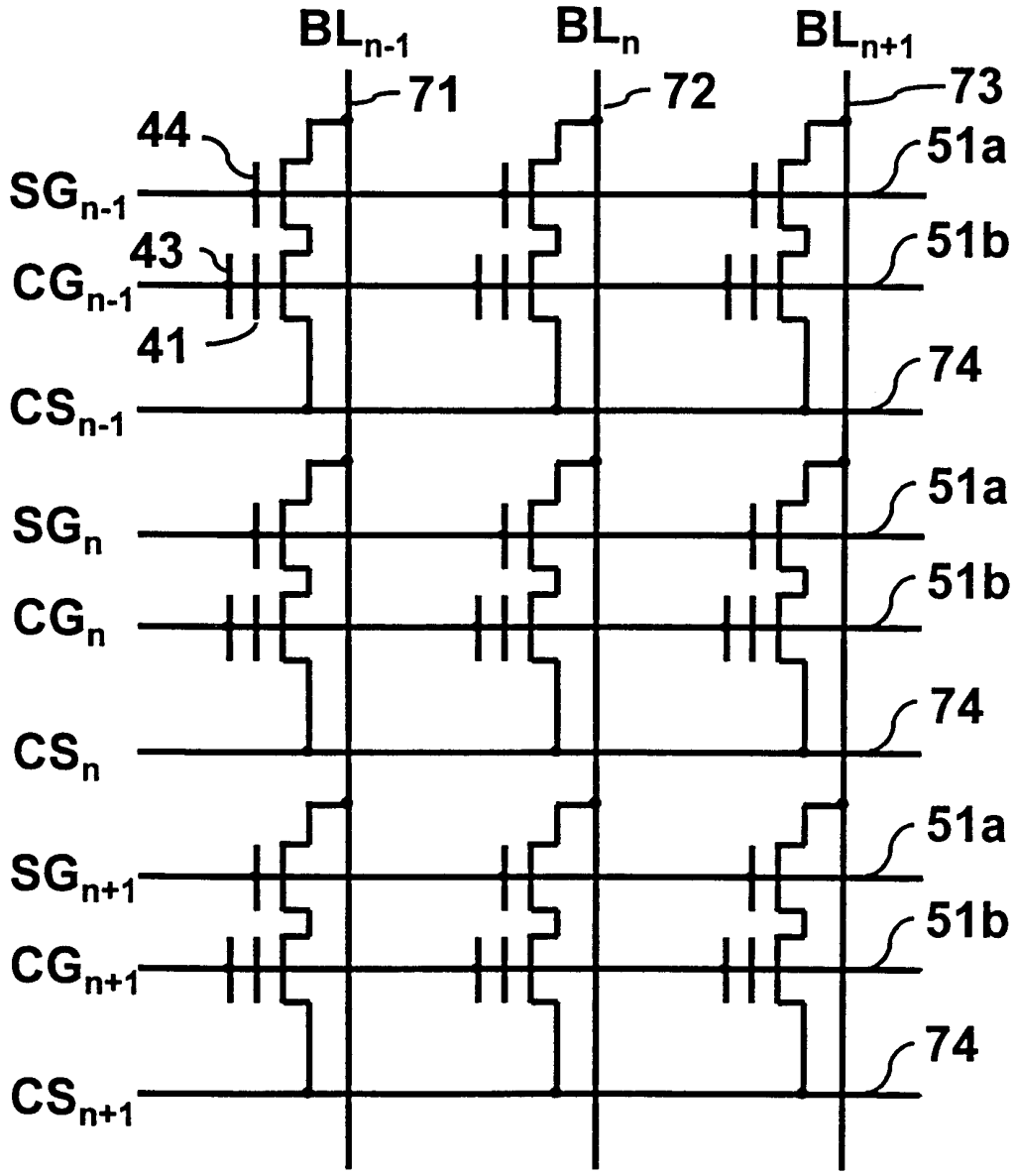
Fig. 9F

Fig. 10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INTERNATIONAL SEARCH REPORT

International application No.
PCT/US00/20235

A. CLASSIFICATION OF SUBJECT MATTER

IPC(7) :H01L 29/788
US CL :257/316, 318

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S. : none

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

none

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

none

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
	Please See Continuation of Second Sheet.	

[X] Further documents are listed in the continuation of Box C. [ ] See patent family annex.

*	Special categories of cited documents:	"T"	later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"A"	document defining the general state of the art which is not considered to be of particular relevance	"X"	document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"E"	earlier document published on or after the international filing date	"Y"	document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"L"	document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)	"&"	document member of the same patent family
"O"	document referring to an oral disclosure, use, exhibition or other means		
"P"	document published prior to the international filing date but later than the priority date claimed		

Date of the actual completion of the international search	Date of mailing of the international search report
19 SEPTEMBER 2000	14 NOV 2000
Name and mailing address of the ISA/US Commissioner of Patents and Trademarks Box PCT Washington, D.C. 20231 Facsimile No. (703) 305-3230	Authorized officer TRONG PHAN Telephone No. (703) 308-4870

Form PCT/ISA/210 (second sheet) (July 1998)★

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US00/20235

C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 5,883,409, A (GUTERMAN ET AL.) 16 March 1999 (16.03.,1999) entire document.	1-24
A,P	US 5,495,441 A (HONG) 27 February 1996 (27.02.1996), entire document.	1-24
A	US 6,011,288 A (LIN ET AL.) 04 January 2000 (04.01.2000), entire document	1-24
A	US 5,280,446 A (MA ET AL.) 18 January 1994 (18.01.1994), entire document.	1-24
A	US 5,047,814 A (HAZANI) 10 September 1991 (10.09.1991), entire document.	25-31
A	US 5,404,037 A (MANLEY) 04 April 1995 (04.04.1995), entire document.	25-31
A	US 5,504,706 A (D'ARRIGO ET AL.) 02 April 1996 (02.04.1996), entire document.	25-31
A	US 5,844,271 A (SETHI ET AL.) 01 December 1998 (01.12.1998), entire document.	25-31
A	US 5,841,165 A (CHANG ET AL.) 24 November 1998 (24.11.1998), entire document.	25-31

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US00/20235

Box I Observations where certain claims were found unsearchable (Continuation of item 1 of first sheet)

This international report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. ☐ Claims Nos.:
because they relate to subject matter not required to be searched by this Authority, namely:

2. ☐ Claims Nos.:
because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out, specifically:

3. ☐ Claims Nos.:
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

Box II Observations where unity of invention is lacking (Continuation of item 2 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:

Please See Extra Sheet.

1. ☒ As all required additional search fees were timely paid by the applicant, this international search report covers all searchable claims.

2. ☐ As all searchable claims could be searched without effort justifying an additional fee, this Authority did not invite payment of any additional fee.

3. ☐ As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims for which fees were paid, specifically claims Nos.:

4. ☐ No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:

Remark on Protest

☐ The additional search fees were accompanied by the applicant's protest.

☐ No protest accompanied the payment of additional search fees.

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US00/20235

BOX II. OBSERVATIONS WHERE UNITY OF INVENTION WAS LACKING
This ISA found multiple inventions as follows:

This application contains the following inventions or groups of inventions which are not so linked as to form a single inventive concept under PCT Rule 13.1. In order for all inventions to be searched, the appropriate additional search fees must be paid.

Group I, claims 1-24, drawn to a memory cell.

Group II, claims 25-31, drawn to a process of fabricating a memory cell.

The inventions listed as Groups I and II do not relate to a single inventive concept under PCT Rule 13.1 because, under PCT Rule 13.2, they lack the same or corresponding special technical features for the following reasons: the memory cell as claimed in claims 25-31 of Group II can be made by another and materially different process such as recited in claims 1-24 of Group I.