

(51) International Patent Classification:
H01L 29/40 (2006.01)(21) International Application Number:
PCT/US2020/015252(22) International Filing Date:
27 January 2020 (27.01.2020)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
62/829,192 04 April 2019 (04.04.2019) US
16/773,090 27 January 2020 (27.01.2020) US

(63) Related by continuation (CON) or continuation-in-part (CIP) to earlier application:

US 62/829,192 (CON)
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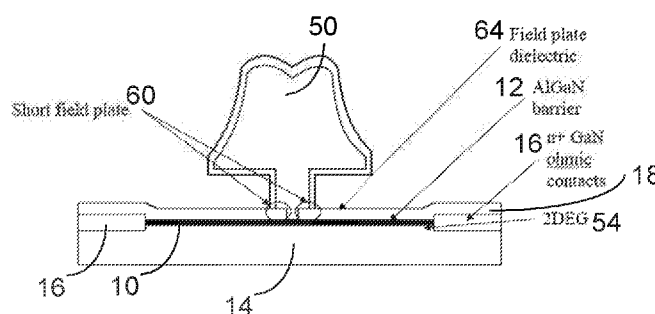
(81) Designated States (unless otherwise indicated, for every kind of national protection available): AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DJ, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IR, IS, JO, JP, KE, KG, KH, KN, KP, KR, KW, KZ, LA, LC, LK, LR, LS, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SA, SC, SD, SE, SG, SK, SL, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, WS, ZA, ZM, ZW.

(84) Designated States (unless otherwise indicated, for every kind of regional protection available): ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, ST, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, KM, ML, MR, NE, SN, TD, TG).

Published:

— without international search report and to be republished upon receipt of that report (Rule 48.2(g))

(54) Title: MINIATURE FIELD PLATE T-GATE AND METHOD OF FABRICATING THE SAME

**FIG. 2**

(57) Abstract: A method of fabricating a gate with a mini field plate includes forming a dielectric passivation layer over an epitaxy layer on a substrate, coating the dielectric passivation layer with a first resist layer, etching the first resist layer and the dielectric passivation layer to form a first opening in the dielectric passivation layer, removing the first resist layer, and forming a tri-layer gate having a gate foot in the first opening, the gate foot having a first width, a gate neck extending from the gate foot and extending for a length over the dielectric passivation layer on both sides of the first opening, the gate neck having a second width wider than the first width of the gate foot, and a gate head extending from the gate neck, the gate head having a third width wider than the second width of the gate neck.



**MINIATURE FIELD PLATE T-GATE
AND METHOD OF FABRICATING THE SAME**

CROSS REFERENCE TO RELATED APPLICATIONS

[0001] This application is related to and claims priority from U.S. Provisional Application Serial No. 62/829,192, filed 4/4/2019, which is incorporated herein as though set forth in full. This application is also related and claims priority from U.S. Non-Provisional Patent Application Serial No. 16/773,090, filed 1/27/2020, which is being filed concurrently and is incorporated herein by reference as though set forth in full.

STATEMENT REGARDING FEDERAL FUNDING

[0002] This invention was made under U.S. Government contract FA8650-18-C-7802. The U.S. Government has certain rights in this invention.

TECHNICAL FIELD

[0003] This disclosure relates to high electron mobility transistors (HEMTs).

BACKGROUND

[0004] AlGa_N/Ga_N high electron mobility transistors (HEMTs) are promising for high frequency transistors because of their two dimensional electron gas (2DEG) with high electron saturation velocity and high electron concentration. These HEMTs can also provide high power transistors due to the high critical breakdown field of Ga_N. However, in general, field effect transistors under high voltage operation suffer from high electric fields at the drain edge of the gate leading to the breakdown of

transistors and/or an increased dynamic on-resistance during high voltage switching operation. In order to reduce the maximum electric field intensity, field plate structures are widely used. One drawback of a field plate structure is that it increases the gate capacitance and has an adverse effect on cutoff-frequency (f_T) and maximum frequency (f_{max}).

[0005] In the prior art, gates have been used that are conformal to the field plate dielectric, resulting in a higher-than-necessary capacitance. The prior art has described devices with one or multiple field plates. Traditionally, a longer field plate will help suppress traps across the gate-drain region, but the drastic increase in capacitance greatly inhibits high frequency operation.

[0006] References [1] to [5], below, which are incorporated herein by reference, describe prior art field plate structures.

[0007] References

The following references are incorporated herein as though set forth in full.

[1] Y. Pei, Z. Chen, D. Brown, S. Keller, S. P. Denbaars, and U. K. Mishra "Deep-Submicrometer AlGaIn/GaN HEMTs With Slant Field Plates", IEEE Electron Device Letters, vol 30, no. 4, pp. 328 - 330, April 2009.

[2] K. Kobayashi, S. Hatakeyama, T. Yoshida, D. Piedra, T. Palacios, T. Otsuji, and T. Suemitsu "Current Collapse Suppression in AlGaIn/GaN HEMTs by Means of Slant Field Plates Fabricated by Multi-layer SiCN", Solid State Electronics, vol 101, pp. 63 - 69, November 2014.

[3] G. Xie, E. Xu, J. Lee, N. Hashemi, F. Fu, B. Zhang, and W. Ng, "Breakdown voltage enhancement for power AlGaIn/GaN HEMTs with Air-bridge Field Plate", 2011 IEEE International Conference of Electron Devices and Solid-State Circuits, 17 - 18 November 2011.

[4] J. Wong, K. Shinohara, A. Corrion, D. Brown, Z. Carlos, A. Williams, Y. Tang, J. Robinson, I. Khalaf, H. Fung, A. Schmitz, T. Oh, S. Kim, S. Chen, S. Burnham, A. Margomenos, and M. Micovic, "Novel Asymmetric Slant Field Plate Technology for High-Speed Low-Dynamic Ron E/D-mode GaN HEMTs", IEEE Electron Device Letters, vol. 38, no. 1, pp. 95 - 98, January 2017.

[5] D. Brown, K. Shinohara, A. Corrion, R. Chu, A. Williams, J. Wong, I. Alvarado-Rodriguez, R. Grabar, M. Johnson, C. Butler, D. Santos, S. Burnham, J. Robinson, D. Zehnder, S. Kim, T. Oh, M. Micovic, "High-Speed, Enhancement-Mode GaN Power Switch With Regrown n+ GaN Ohmic Contacts and Staircase Field Plates", IEEE Electron Device Letters, vol. 34, no. 9, pp. 1118 - 1120, September 2013.

[0008] What is needed is an improved transistor structure that provides high-frequency operation, low dynamic on-resistance, reduced parasitic capacitance and high-voltage operation. The embodiments of the present disclosure answer these and other needs.

SUMMARY

[0009] In a first embodiment disclosed herein, a method of fabricating a gate with a mini field plate for a transistor comprises forming a dielectric passivation layer over an epitaxy layer on a substrate, coating the

dielectric passivation layer with a first resist layer, etching the first resist layer and the dielectric passivation layer to form a first opening in the dielectric passivation layer, removing the first resist layer, and forming a tri-layer gate having a gate foot in the first opening, the gate foot having a first width, a gate neck extending from the gate foot and extending for a length over the dielectric passivation layer on both sides of the first opening, the gate neck having a second width wider than the first width of the gate foot, and a gate head extending from the gate neck, the gate head having a third width wider than the second width of the gate neck.

[0010] In another embodiment disclosed herein, a transistor having a gate with a mini field plate comprises a substrate, an epitaxy layer on the substrate, a dielectric passivation layer on the epitaxy layer, a first opening in the dielectric passivation layer, and a tri-layer gate, the tri-layer gate comprising a gate foot in the first opening, the gate foot having a first width, a gate neck extending from the gate foot and extending for a length over the dielectric passivation layer on both sides of the first opening, the gate neck having a second width wider than the first width of the gate foot, and a gate head extending from the gate neck, the gate head having a third width wider than the second width of the gate neck.

[0011] These and other features and advantages will become further apparent from the detailed description and accompanying figures that follow. In the figures and description, numerals indicate the various features, like numerals referring to like features throughout both the drawings and the description.

BRIEF DESCRIPTION OF THE DRAWINGS

[0012] FIGs. 1A, 1B, 1C, 1D, 1E, 1F and 1G show a mini field plate gate fabrication process in accordance with the present disclosure;

[0013] FIG. 2 shows the locations of the short/mini field plate in accordance with the present disclosure; and

[0014] FIG. 3 shows dimensions of the gate and field plate length and field plate dielectric thickness in accordance with the present disclosure.

DETAILED DESCRIPTION

[0015] In the following description, numerous specific details are set forth to clearly describe various specific embodiments disclosed herein. One skilled in the art, however, will understand that the presently claimed invention may be practiced without all of the specific details discussed below. In other instances, well known features have not been described so as not to obscure the invention.

[0016] The present disclosure describes a transistor that combines the benefit of a high f_T and f_{max} T-gate structure with a short field plate to increase the performance of radio frequency (RF) GaN transistors. The field plate closest to the 2DEG has the greatest effect in reducing dynamic on-resistance. In the present disclosure a small or "mini" field plate is used to spread the electric field while retaining a relatively low gate parasitic capacitance. Additionally, the transistors of the present disclosure have a higher manufacturing yield and better repeatability due to a mechanically stronger gate neck.

[0017] The miniature field plates 60 are at the edges of the gate foot 80, as best shown in FIG. 3, to reduce the peak electric field while leaving an air-gap between the bulk of the T-gate head and the underlying semiconductor structures to reduce the parasitic capacitance. Process time may be slightly increased compared to a prior art GaN T-gate process, but because of the mini field plate, the gate stem or gate neck thickness increases, allowing for a more mechanically robust T-gate. By combining a lift-off T-gate with a mini field plate structure, devices made according to the present disclosure can obtain the benefits of a field plate while improving high-frequency operation.

[0018] The presently disclosed transistor may be a tri-layer gate and a dielectric is used split the gate process into two individual lithographic steps to obtain a small gate length or width, which may be 40 nanometers or less, as shown in FIG. 3, while improving the electric field profile and minimizing gate capacitance to achieve high frequency operation. Most prior art devices with field plates are for low frequency applications and operation and have a large (>100nm) gate foot.

[0019] FIGs. 1A, 1B, 1C, 1D, 1E, 1F and 1G show a mini field plate gate fabrication process in accordance with the present disclosure. The process illustrates a process flow for GaN-based HEMTs, but the process and the features of the invention herein described are not limited to GaN. Other semiconductor materials such as GaAs, InP, Si, and InSb may be used as well.

[0020] The fabrication steps are as follows. As shown in FIG. 1A an epitaxy layer 10, which may include an AlGaIn barrier layer 12, is grown for a HEMT structure on a suitable substrate 14, which is shown as GaN, but which could also be sapphire, silicon carbide (SiC), silicon (Si), GaAs, InP, or InSb. Then, ohmic contacts 16 are formed. A

preferred embodiment for the formation of ohmic contacts is by an n+ GaN regrowth process, which may be performed to provide low resistance ohmic contacts 16.

[0021] Then, as shown in FIG. 1B, a dielectric passivation layer 18 may be formed over the structure using, for example, chemical vapor deposition (CVD), plasma enhanced CVD (PECVD) or atomic layer deposition (ALD). The dielectric may be Al_2O_3 , Si_3N_4 or SiO_2 .

[0022] Next, as shown in FIG. 1C, an electron-beam (E-beam) resist 20 may be coated over the structure, followed by gate foot patterning, and etching an E-beam defined gate foot pattern 22 through the resist 20 and the dielectric passivation layer 18, and stopping at the epitaxy layer 10. A dry etch process is preferable, because a wet etch is much harder to control. The chemistry depends on the dielectric, but fluorine- or chlorine-based dry etches are generally applicable. In a preferred embodiment, CF_4 may be used.

[0023] Then as shown in FIG. 1D, the resist 20 is removed, leaving opening 24 in the dielectric passivation layer 18. The resist may be removed using a solvent bath.

[0024] Next, as shown in FIG. 1E, another E-beam process is performed to define a tri-layer gate 50 (see Figs. 1F and 1G) on top of opening 24. This process starts by depositing resist 26 over the device, which is typically one of a plurality of identical devices fabricated simultaneously on a wafer or substrate. The resist is preferentially deposited by a spin-coat process, then patterned using typical lithographic techniques. The result of the patterning is an opening 28 in the resist above the opening 24. The opening 28 has a larger lateral dimension than the opening 24. In the embodiment displayed in Figs. 1E - 1G, the opening 28 is shown as centered above the

opening 24; however, in general, the two openings need not be centered with respect to one another.

[0025] Then another E-beam resist 30 is deposited on the resist 26 on either side of the opening 28, so that the E-beam resist 30 has an opening 32, which is wider than opening 28. Then another E-beam resist 34 is deposited on the resist 30 on either side of the opening 32, so that the E-beam resist 34 has an opening 36, which is wider than opening 28, but narrower than opening 32.

[0026] Other lithography techniques may be used, as long as the feature resolution can be obtained. The top and bottom resists may be ZEP, and the middle may be PMGI; alternatively, the top and bottom may be PMMA and the middle may be MMA. Other stacks may be used, as long as the middle resist has a selective developer relative to the top and bottom, and the features can be resolved.

[0027] Then, as shown in FIG. 1F, metal 38 is evaporated to form tri-layer gate 50. The metal 38 may be Ni, Ti, Pt, W, TaN, or TiN. The gate may also be composed of more than one metal. Typically, the bottom of the gate stack is a metal with a high work function; the remainder can be any low resistance metal. In a preferred embodiment, the bottom 20 nm is Pt and the remainder is Au.

[0028] As shown in FIG. 1F the metal 38 fills openings 24 and 28 and partially fills opening 32. The metal 38 coats a portion of the top of dielectric passivation layer 18, which forms field plates 70, as further described below. The metal 38 also coats a portion of the top of resist 26 and resist 34.

[0029] The shape of gate 50 and of the metal 38 on resist 34 is an artifact and feature of the method of metal deposition. That is, the pattern of metal deposition is a result of the metal having been thermally evaporated.

Other deposition techniques such as chemical vapor deposition, atomic layer deposition, or other techniques could result in a different gate 50 shape.

[0030] Then, as shown in FIG. 1G, the resists 26, 30 and 34 are removed along with the metal 38 coated on resist 34. This step may be performed using a metal lift-off process using a solvent, such as acetone, isopropyl alcohol, or PRS.

[0031] Finally, as shown in FIG. 1G, a dielectric 52 may optionally be deposited over the tri-layer gate 50 and would also typically cover the surface of dielectric 18. Dielectric 52 may be deposited by PECVD or ALD or even sputtering.

[0032] As shown in FIG. 1G the tri-layer gate 50 has a gate foot 80, a gate neck 82 and a gate head 84.

[0033] FIG. 2 shows the locations of the short/mini field plates 60 that are formed by the tri-layer gate 50. The width of the short/mini field plates 60 are defined by the difference between the width of opening 24 and the width of opening 28, which as described above has a greater width than opening 24. Also shown in FIG. 2 is the two dimensional electron gas (2DEG) 54 which forms below the barrier layer 12 in a GaN-based HEMT.

[0034] FIG. 3 shows a dimension of the gate foot 80, which may have a length or width 83 of 40 nanometers or less. The gate foot 80 is formed in opening 24. The length 81 of the mini field plates 60 may range from 10 nanometers to 40 nanometers length. The mini field plates 60 may have different lengths. For example, a mini field plate 60 may be longer on the side toward a drain for a transistor. The field plate dielectric 64 is the portion of the dielectric 18 that is under the mini field plates 60. As shown, the height of the mini field plate 60 above the epitaxy layer 10 may be 5 nanometers to 75 nanometers.

[0035] The field plates 70, which are part of tri-layer gate 50, are formed when metal 38 is evaporated and coats a portion of the top of resist 26. The field plates 70 are separated from the field plate dielectric 64 by air gap 72, which may be 10 nm to 200nm in height. The length of the field plates 70 may be one half the gate head 84 width minus one half the gate neck 82 width. The gate head 84 width is greater than the width of gate neck 82.

[0036] The mini field plates 60, which are supported by field plate dielectric 64, provide a stronger gate foot 80 than the gate foot in prior art T-gate structures, because in prior art T-gate structures the gate foot extends all the way up from the epitaxy layer to the gate head, which results in a weak gate foot. In the present disclosure, the width of the gate neck 82 from the top of the gate foot 80, which may be 5 nm to 75 nm above the epitaxy layer 10, to the bottom of the gate head 84 is roughly 3 times wider than the gate foot and supported by field plate dielectric 64, as shown in FIG. 3, thereby greatly increasing the mechanical strength of the gate. The result is higher yield devices and better repeatability.

[0037] HEMT transistors fabricated according to the present disclosure improve the electric field profile and minimize gate capacitance, which provides for high frequency operation.

[0038] Having now described the invention in accordance with the requirements of the patent statutes, those skilled in this art will understand how to make changes and modifications to the present invention to meet their specific requirements or conditions. Such changes and modifications may be made without departing from the scope and spirit of the invention as disclosed herein.

[0039] The foregoing Detailed Description of exemplary and preferred embodiments is presented for purposes of illustration and disclosure in accordance with the requirements of the law. It is not intended to be exhaustive nor to limit the invention to the precise form(s) described, but only to enable others skilled in the art to understand how the invention may be suited for a particular use or implementation. The possibility of modifications and variations will be apparent to practitioners skilled in the art. No limitation is intended by the description of exemplary embodiments which may have included tolerances, feature dimensions, specific operating conditions, engineering specifications, or the like, and which may vary between implementations or with changes to the state of the art, and no limitation should be implied therefrom. Applicant has made this disclosure with respect to the current state of the art, but also contemplates advancements and that adaptations in the future may take into consideration of those advancements, namely in accordance with the then current state of the art. It is intended that the scope of the invention be defined by the Claims as written and equivalents as applicable. Reference to a claim element in the singular is not intended to mean "one and only one" unless explicitly so stated. Moreover, no element, component, nor method or process step in this disclosure is intended to be dedicated to the public regardless of whether the element, component, or step is explicitly recited in the Claims. No claim element herein is to be construed under the provisions of 35 U.S.C. Sec. 112, sixth paragraph, unless the element is expressly recited using the phrase "means for. . ." and no method or process step herein is to be construed under those provisions unless the step, or steps, are expressly recited using the phrase "comprising the step(s) of. . ."

[0040] Broadly, this application discloses at least the following: A method of fabricating a gate with a mini field plate includes forming a dielectric passivation layer over an epitaxy layer on a substrate, coating the dielectric passivation layer with a first resist layer, etching the first resist layer and the dielectric passivation layer to form a first opening in the dielectric passivation layer, removing the first resist layer; and forming a tri-layer gate having a gate foot in the first opening, the gate foot having a first width, a gate neck extending from the gate foot and extending for a length over the dielectric passivation layer on both sides of the first opening, the gate neck having a second width wider than the first width of the gate foot, and a gate head extending from the gate neck, the gate head having a third width wider than the second width of the gate neck.

CONCEPTS

At least the following concepts have been disclosed.

Concept 1. A method of fabricating a gate with a mini field plate for a transistor comprising:

- forming a dielectric passivation layer over an epitaxy layer on a substrate;
- coating the dielectric passivation layer with a first resist layer;
- etching the first resist layer and the dielectric passivation layer to form a first opening in the dielectric passivation layer;
- removing the first resist layer; and
- forming a tri-layer gate having a gate foot in the first opening, the gate foot having a first width, a gate neck extending from the gate foot and extending for a

length over the dielectric passivation layer on both sides of the first opening, the gate neck having a second width wider than the first width of the gate foot, and a gate head extending from the gate neck, the gate head having a third width wider than the second width of the gate neck.

Concept 2. The method of concept 1 wherein forming a tri-layer gate, wherein the tri-layer gate has a gate foot in the first opening, the gate foot having a first width, a gate neck extending from the gate foot and extending for a length over the dielectric passivation layer on both sides of the first opening, the gate neck having a second width wider than the first width of the gate foot, and a gate head extending from the gate neck, the gate head having a third width wider than the second width of the gate neck comprises:

depositing a second resist layer on the dielectric passivation layer on either side of the first opening so that the second resist layer has a second opening in the second resist layer and so that the second opening is wider than the first opening;

depositing a third resist layer on the second resist layer on either side of the second opening so that the third resist layer has a third opening in the third resist layer and so that the third opening is wider than the second opening;

depositing a fourth resist layer on the third resist on either side of the third opening so that the fourth resist layer has a fourth opening in the fourth resist layer and so that the fourth opening is wider than the second opening and narrower than the third opening;

evaporating metal over the fourth resist layer so that the metal fills the first opening and the second opening and partially fills the third opening; and

removing the second, third and fourth resist layers.

Concept 3. The method of concept 1 or 2 further comprising:
forming low resistance ohmic contacts using a regrowth process.

Concept 4. The method of concept 1, 2 or 3 wherein the substrate comprises GaN, sapphire, silicon carbide (SiC), silicon (Si), GaAs, InP, or InSb.

Concept 5. The method of concept 1, 2, 3 or 4 further comprising depositing a dielectric over the tri-layer gate.

Concept 6. The method of concept 2 wherein:
the first resist layer comprises an E-beam resist layer;
the second resist layer comprises an E-beam resist layer;
the third resist layer comprises an E-beam resist layer; and
the fourth resist layer comprises an E-beam resist layer.

Concept 7. The method of concept 1, 2, 3, 4, 5 or 6 wherein etching the first resist layer and the dielectric passivation layer to form a first opening in the dielectric passivation layer comprises etching an E-beam defined gate foot pattern.

Concept 8. The method of concept 1, 2, 3, 4, 5, 6 or 7 wherein the epitaxy layer comprises an AlGaIn barrier layer.

Concept 9. The method of concept 1, 2, 3, 4, 5, 6, 7 or 8 wherein the transistor comprises a high electron mobility transistor.

Concept 10. The method of concept 1, 2, 3, 4, 5, 6, 7, 8, or 9 wherein the gate neck extending for a length over the dielectric passivation layer on both sides of the first opening forms a first mini field plate on one side of the first opening and forms a second mini field plate on another side of the first opening.

Concept 11. The method of concept 1, 2, 3, 4, 5, 6, 7, 8, 9 or 10:

wherein the gate head having a third width wider than the second width of the gate neck forms a third field plate on one side of the gate neck and forms a fourth field plate on another side of the gate neck;

wherein the third field plate is separated from the dielectric passivation layer by an air gap; and

wherein the fourth field plate is separated from the dielectric passivation layer by an air gap.

Concept 12. The method of concept 1, 2, 3, 4, 5, 6, 7, 8, 9, 10 or 11 wherein the dielectric passivation layer has a thickness of 5 nanometers to 75 nanometers.

Concept 13. The method of concept 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11 or 12 wherein the gate foot has a width of 40 nanometers or less.

Concept 14. The method of concept 10:

wherein the first mini field plate has a width of 10 nanometers to 40 nanometers; and

wherein the second mini field plate has a width of 10 nanometers to 40 nanometers.

Concept 15. The method of concept 10:

wherein the height of the first mini field plate above the epitaxy layer is 5 nanometers to 75 nanometers; and

wherein the height of the second mini field plate above the epitaxy layer is 5 nanometers to 75 nanometers.

Concept 16. A transistor having a gate with a mini field plate comprising:

- a substrate;

- an epitaxy layer on the substrate;

- a dielectric passivation layer on the epitaxy layer;

- a first opening in the dielectric passivation layer;

- a tri-layer gate, the tri-layer gate comprising:

 - a gate foot in the first opening, the gate foot having a first width;

 - a gate neck extending from the gate foot and extending for a length over the dielectric passivation layer on both sides of the first opening, the gate neck having a second width wider than the first width of the gate foot; and

 - a gate head extending from the gate neck, the gate head having a third width wider than the second width of the gate neck.

Concept 17. The transistor of concept 16 further comprising ohmic contacts.

Concept 18. The transistor of concept 16 or 17 wherein the substrate comprises GaN, sapphire, silicon carbide (SiC), silicon (Si), GaAs, InP, or InSb.

Concept 19. The transistor of concept 16, 17 or 18 further comprising a dielectric over the tri-layer gate.

Concept 20. The transistor of concept 16, 17, 18 or 19 wherein the epitaxy layer comprises an AlGaN barrier layer.

Concept 21. The transistor of concept 16, 17, 18, 19 or 20 wherein the transistor comprises a high electron mobility transistor.

Concept 22. The transistor of concept 16, 17, 18, 19, 20 or 21:

wherein the gate neck extending for a length over the dielectric passivation layer on both sides of the first opening comprises:

a first mini field plate on one side of the first opening; and

a second mini field plate on another side of the first opening.

Concept 23. The transistor of concept 16, 17, 18, 19, 20, 21 or 22:

wherein the gate head having a third width wider than the second width of the gate neck comprises:

a third field plate on one side of the gate neck; and

a fourth field plate on another side of the gate neck.

Concept 24. The transistor of concept 23:

wherein the third field plate is separated from the dielectric passivation layer by an air gap; and

wherein the fourth field plate is separated from the dielectric passivation layer by an air gap.

Concept 25. The transistor of concept 16, 17, 18, 19, 20, 21, 22, 23 or 24 wherein the dielectric passivation layer has a thickness of 5 nanometers to 75 nanometers.

Concept 26. The transistor of concept 16, 17, 18, 19, 20, 21, 22, 23, 24 or 25 wherein the gate foot has a width of 40 nanometers or less.

Concept 27. The transistor of concept 22:

wherein the first mini field plate has a width of 10 nanometers to 40 nanometers; and

wherein the second mini field plate has a width of 10 nanometers to 40 nanometers.

Concept 28. The transistor of concept 22:

wherein the height of the first mini field plate above the epitaxy layer is 5 nanometers to 75 nanometers; and

wherein the height of the second mini field plate above the epitaxy layer is 5 nanometers to 75 nanometers.

WHAT IS CLAIMED IS:

1. A method of fabricating a gate with a mini field plate for a transistor comprising:

forming a dielectric passivation layer over an epitaxy layer on a substrate;

coating the dielectric passivation layer with a first resist layer;

etching the first resist layer and the dielectric passivation layer to form a first opening in the dielectric passivation layer;

removing the first resist layer; and

forming a tri-layer gate having a gate foot in the first opening, the gate foot having a first width, a gate neck extending from the gate foot and extending for a length over the dielectric passivation layer on both sides of the first opening, the gate neck having a second width wider than the first width of the gate foot, and a gate head extending from the gate neck, the gate head having a third width wider than the second width of the gate neck.

2. The method of claim 1 wherein forming a tri-layer gate, wherein the tri-layer gate has a gate foot in the first opening, the gate foot having a first width, a gate neck extending from the gate foot and extending for a length over the dielectric passivation layer on both sides of the first opening, the gate neck having a second width wider than the first width of the gate foot, and a gate head extending from the gate neck, the gate head having a third width wider than the second width of the gate neck comprises:

depositing a second resist layer on the dielectric passivation layer on either side of the first opening so that the second resist layer has a second opening in the

second resist layer and so that the second opening is wider than the first opening;

depositing a third resist layer on the second resist layer on either side of the second opening so that the third resist layer has a third opening in the third resist layer and so that the third opening is wider than the second opening;

depositing a fourth resist layer on the third resist on either side of the third opening so that the fourth resist layer has a fourth opening in the fourth resist layer and so that the fourth opening is wider than the second opening and narrower than the third opening;

evaporating metal over the fourth resist layer so that the metal fills the first opening and the second opening and partially fills the third opening; and

removing the second, third and fourth resist layers.

3. The method of claim 1 further comprising:

forming low resistance ohmic contacts using a regrowth process.

4. The method of claim 1 wherein the substrate comprises GaN, sapphire, silicon carbide (SiC), silicon (Si), GaAs, InP, or InSb.

5. The method of claim 1 further comprising depositing a dielectric over the tri-layer gate.

6. The method of claim 2 wherein:

the first resist layer comprises an E-beam resist layer;

the second resist layer comprises an E-beam resist layer;

the third resist layer comprises an E-beam resist layer; and

the fourth resist layer comprises an E-beam resist layer.

7. The method of claim 1 wherein etching the first resist layer and the dielectric passivation layer to form a first opening in the dielectric passivation layer comprises etching an E-beam defined gate foot pattern.

8. The method of claim 1 wherein the epitaxy layer comprises an AlGaN barrier layer.

9. The method of claim 1 wherein the transistor comprises a high electron mobility transistor.

10. The method of claim 1 wherein the gate neck extending for a length over the dielectric passivation layer on both sides of the first opening forms a first mini field plate on one side of the first opening and forms a second mini field plate on another side of the first opening.

11. The method of claim 1:

wherein the gate head having a third width wider than the second width of the gate neck forms a third field plate on one side of the gate neck and forms a fourth field plate on another side of the gate neck;

wherein the third field plate is separated from the dielectric passivation layer by an air gap; and

wherein the fourth field plate is separated from the dielectric passivation layer by an air gap.

12. The method of claim 1 wherein the dielectric passivation layer has a thickness of 5 nanometers to 75 nanometers.

13. The method of claim 1 wherein the gate foot has a width of 40 nanometers or less.
14. The method of claim 10:
 wherein the first mini field plate has a width of 10 nanometers to 40 nanometers; and
 wherein the second mini field plate has a width of 10 nanometers to 40 nanometers.
15. The method of claim 10:
 wherein the height of the first mini field plate above the epitaxy layer is 5 nanometers to 75 nanometers; and
 wherein the height of the second mini field plate above the epitaxy layer is 5 nanometers to 75 nanometers.
16. A transistor having a gate with a mini field plate comprising:
 a substrate;
 an epitaxy layer on the substrate;
 a dielectric passivation layer on the epitaxy layer;
 a first opening in the dielectric passivation layer;
 a tri-layer gate, the tri-layer gate comprising:
 a gate foot in the first opening, the gate foot having a first width;
 a gate neck extending from the gate foot and extending for a length over the dielectric passivation layer on both sides of the first opening, the gate neck having a second width wider than the first width of the gate foot; and
 a gate head extending from the gate neck, the gate head having a third width wider than the second width of the gate neck.
17. The transistor of claim 16 further comprising ohmic contacts.

18. The transistor of claim 16 wherein the substrate comprises GaN, sapphire, silicon carbide (SiC), silicon (Si), GaAs, InP, or InSb.

19. The transistor of claim 16 further comprising a dielectric over the tri-layer gate.

20. The transistor of claim 16 wherein the epitaxy layer comprises an AlGaN barrier layer.

21. The transistor of claim 16 wherein the transistor comprises a high electron mobility transistor.

22. The transistor of claim 16:

wherein the gate neck extending for a length over the dielectric passivation layer on both sides of the first opening comprises:

a first mini field plate on one side of the first opening; and

a second mini field plate on another side of the first opening.

23. The transistor of claim 16:

wherein the gate head having a third width wider than the second width of the gate neck comprises:

a third field plate on one side of the gate neck; and

a fourth field plate on another side of the gate neck.

24. The transistor of claim 23:

wherein the third field plate is separated from the dielectric passivation layer by an air gap; and

wherein the fourth field plate is separated from the dielectric passivation layer by an air gap.

25. The transistor of claim 16 wherein the dielectric passivation layer has a thickness of 5 nanometers to 75 nanometers.

26. The transistor of claim 16 wherein the gate foot has a width of 40 nanometers or less.

27. The transistor of claim 22:

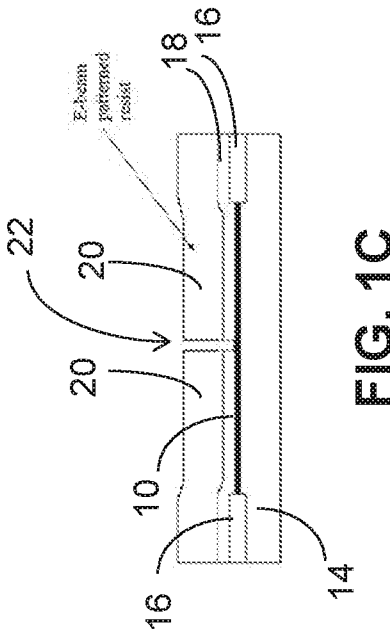
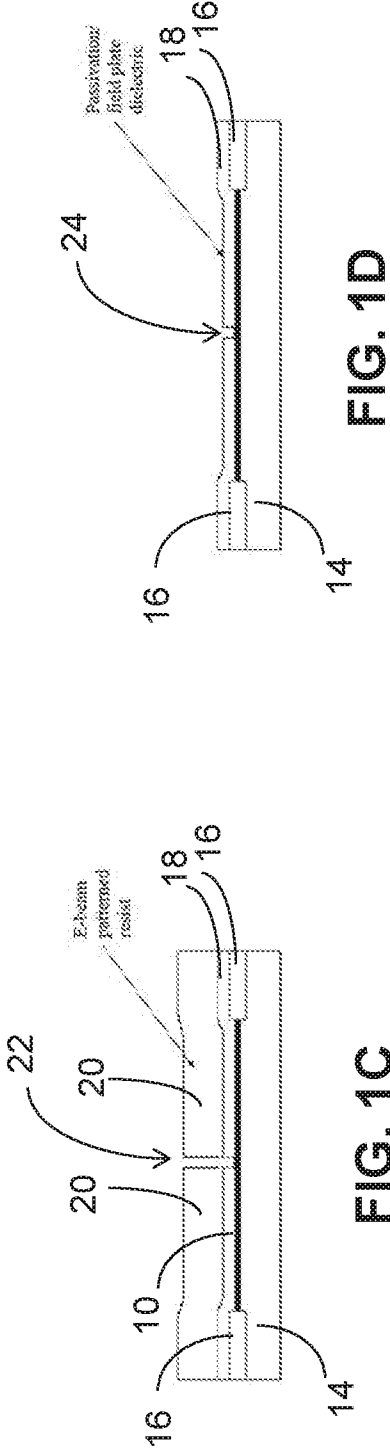
wherein the first mini field plate has a width of 10 nanometers to 40 nanometers; and

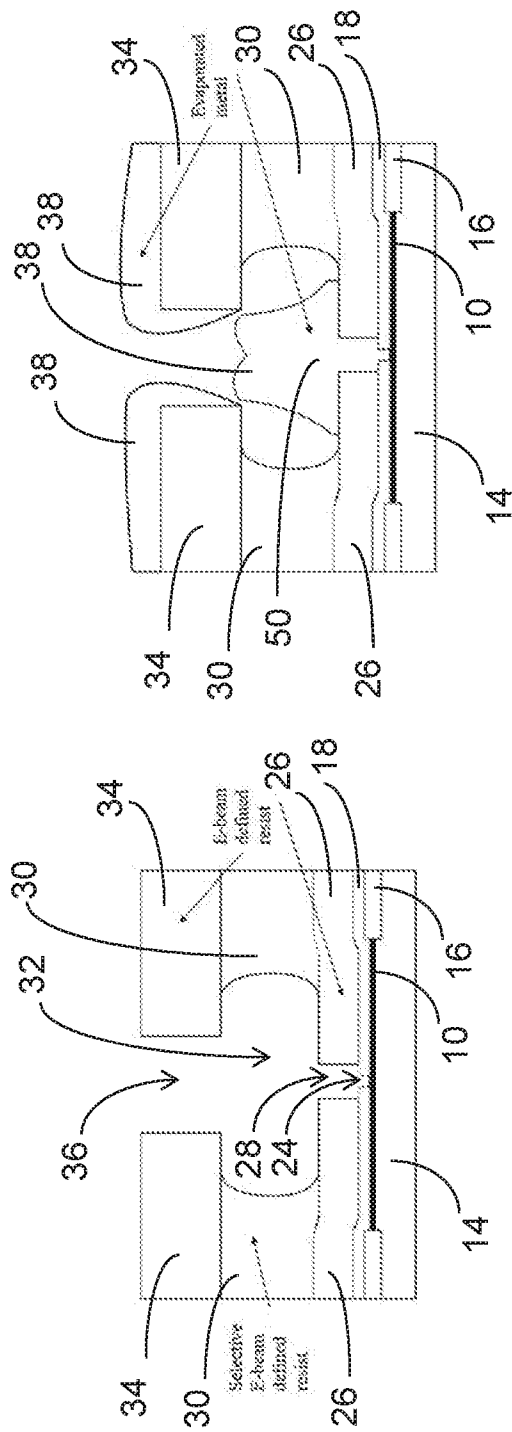
wherein the second mini field plate has a width of 10 nanometers to 40 nanometers.

28. The transistor of claim 22:

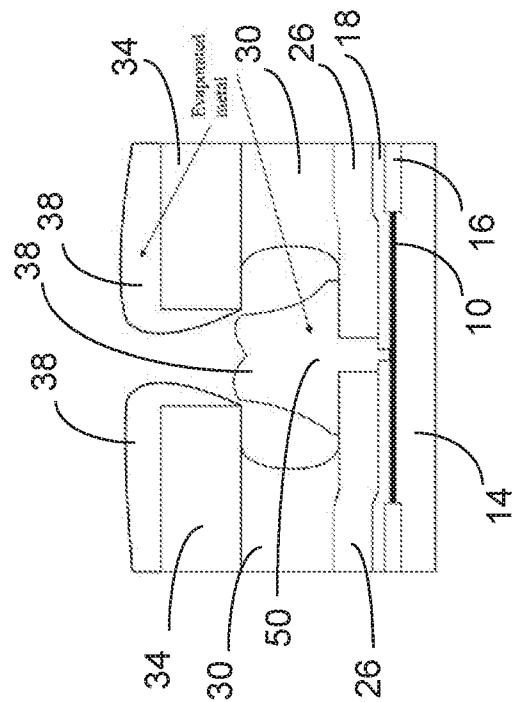
wherein the height of the first mini field plate above the epitaxy layer is 5 nanometers to 75 nanometers; and

wherein the height of the second mini field plate above the epitaxy layer is 5 nanometers to 75 nanometers.

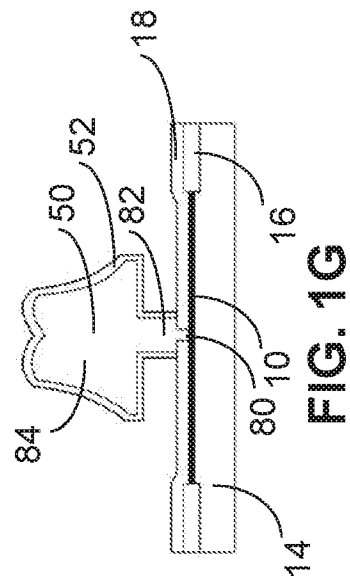


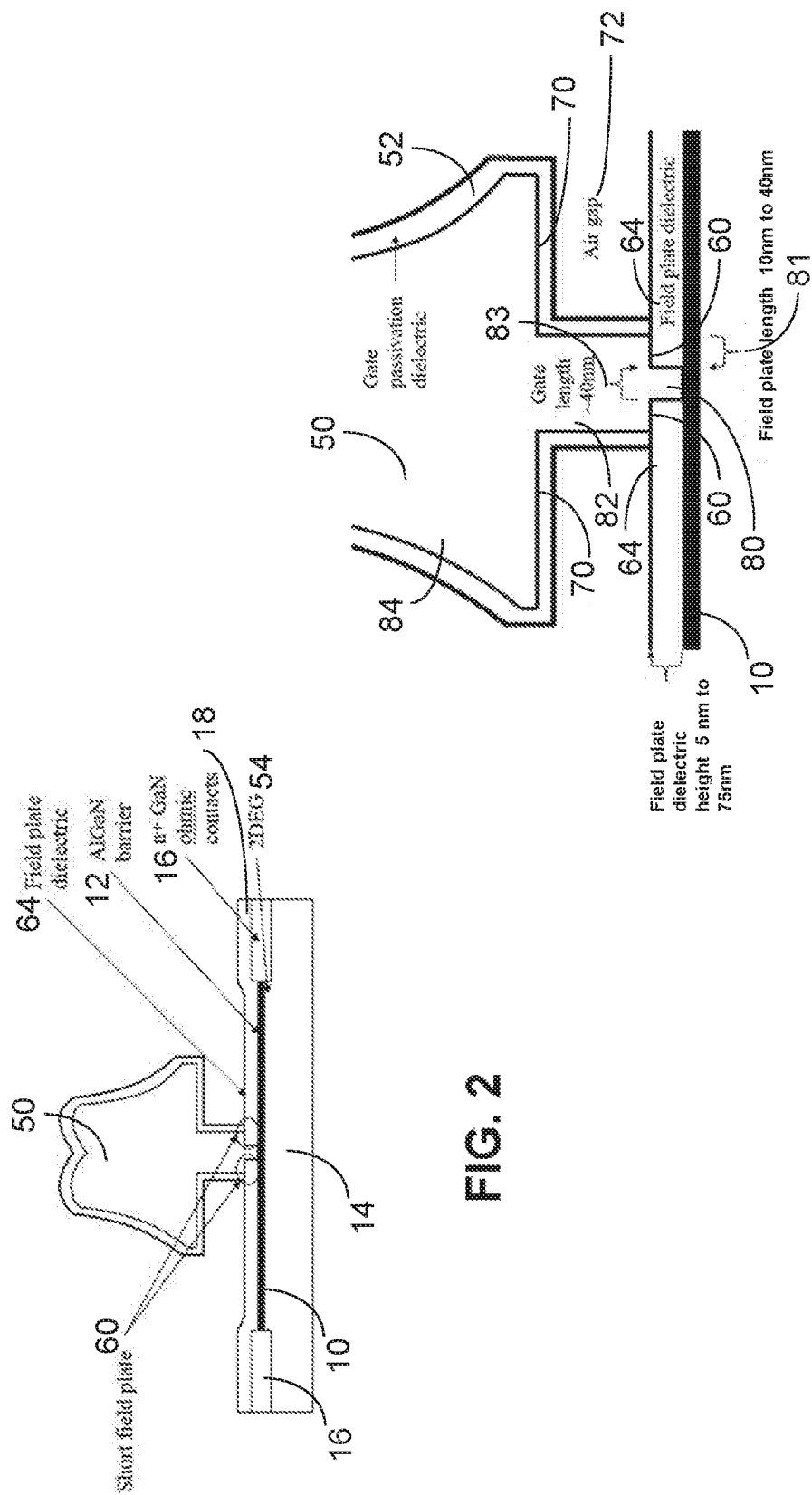


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