

(19)
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(B1)

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10-0423693
2004 03 08

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(22) 2001 02 17

(65)
(43)

10-2001-0082742
2001 08 30

(30) 2000-040992 2000 02 18 (JP)
2000-141263 2000 05 15 (JP)

(73) 가 가
3681
가 가
가 4 6

(72) 가 1336-11
가 가 1657-1
가 460
3550
가 297
4783-16
가
가 460
312-3
1389

(74)

:

(54)

(1)

(2)

(EMI)
가

1

1

1

2 1

3

4

5

6

7

8

9 (a) 9 (b)

, 2
9 (a)

, 9 (b)

10

3

11 (a) 11 (b)
, 11 (a)

, 3
9 (b)

12

4

13 (a) 13 (b) 10
, 13 (a)

, 13 (b)

14 (a) 14 (b)

/

, 14

(a) , 14 (b)

15 (a) 15 (b) 5
, 15 (a) , 15 (b)

16 (a) 16 (b) 6
, 16 (a) , 16 (b)

17a 17b 7

, 17a

18 8 17b

19 11 .
 20 12 .
 21 13 .
 22 14 21 가 .
 23 14 .
 24 15 .
 25 16 .
 26 .
 27 .
 28 .
 29 20 .
 30 FPC .
 31 21 FPC .
 32 21 FPC .
 33 3l 21 FPC .
 34 22 .
 35 23 .
 36 24 .
 37 25 .
 38 가 .
 39 .
 40 가 .
 41 .
 42 .
 43a 43b 38 , 43a .
 44a 44b 38 , 44a .
 45 , 44b .
 < > .
 SUB 1 :
 SUB 2 :
 TCON :
 CHC :
 :
 ST :

IC
 ,
 ,
 가
 TFT , () 가 , 가 , 가 가
 42 , 43a, 43b,
 44a, 44b 42 ()

42 , TFT-LCD (, 가)
 (TCON , 2 , 가 (,
 (CLI),) D2 (CL2), 가 (G)

42 , (가 1024 × 3) × (768) , ,1
 (R), (G), (b) 1 , 38 1
 (, 1). 1
 024 × 768 , 65 MHz 가 , 1
 TFT-LCD , 가 (TFT
) , TFT (1), TFT
 (LSI) , , 1
 18 (R, G, B 6) . , 1
 CMOS , LVDS , 65 MHz
 , 32.5 MHz

43a, 43b, 44a, 44b , 1 TFT
 (1) , 1
 , 1 가 , 1
 , 가
 ,
 /
 FCA , FCA 1 , IC()
 () () (COG)
 IC()
 FPC

45 SUB2 PNL (,)
 (fold) FPC2가 , HOP (PNL)
 CT3 (PCB , CTR3) FPC1 ,
 CTR4가 , FPC2 CT4
 TCON LVDS CT1,
 (LVDS-R) TCON ,
 PNL (SUB2) POL1 , 가
 AR
 FGP , FHL IC1 ,
 IPS , 42 , (,
), TCON ()
 C) () FPC2 (, FP
 , FPC , FPC

, FPC , 가 IC , 6-13724
, FCA IC , IC , 가 , 가 ,
, IC (, 가 , 가 ,)
, 가 , , 가 ,
, 가 , , 가 , , 가 ,
, ()가 (狹額緣化)가
()가 , 가 ,
가 , 가 , 가 ,
(EMI ; Electro Magnetic Interference)가 가 ,
가 , 가 ,
가 , 가 ,
가 , 가 ,

, 가 ,
, , , ,
FPC , (,
FPC , ,) FPC , (,
, 6-13724 , TFT , IC
, 가 , , ,
, , , ,
, 가 , 가 ,
, , , ,
() , , ,
, , , ,
, 가 , , ,
, 가 , , ,

- (1) , 가 , 가 ,
- (2) , 가 , 가 ,
- (3) , 가 , 가 ,

(4)

(5)

(6)

(7)

(8)

(9)

(10)
次段)

2

(前段)

(

2

(11)

FPC

FPC

(12)

(13)

(14) FPC

가

FPC

(FPC)

(片)

가

1)

2)

3)

4)

5)

가, $= (t_{\text{cycle}} - t_{\text{setup}} - t_{\text{hold}}) / 2$ 가
 $t_{\text{cycle}}, t_{\text{setup}}, t_{\text{hold}}$

가

/

- 6) / , , ,
- 7) / 가 . 0
- 8) 90 2 , ,
- 9) 2 , 2 ,2 , EMI , 가
- 10) 가 , , 가
- 11) 10) , EMI 가 가 TCON , TCON 「
x 」
- 12) TCON IC , ,
- 13) , , TCON LVDS , TCON (= : TFT
)가 , .
- 14) TCON TFT , 가
가 가
(TFT) 가 .
- 15) DAC , C-DAC , DAC 가 R-
가 가
가 가
가 .
- 16) () , .
- 17) () , .
(:)
가 :
- 18) , (TFT) , FPC
가 C , FP
- 19) 18) FPC , FPC ,
- 20)) , FPC 가 () FPC 가
FPC 가 , 가
FPC ,
FPC FPC FPC
FPC .
, (A)
1 1
2) () ()
, (B) 1 가 , (D)
C) 2 , (D)

(E) 1 (I) (II) (F) (G) (H)

1 AR 가 () TCON LVDS () TCON TCO IC1 IC1 () TCON AR 2 FPC1 PCB(45) FPC1 (45) PCB I/F) CHC 가 FPC1 가 FPC2 () W FPC2 () COG (, FCA : 5 (10) 64 (128) . 3 (Vref1, Vref2)

Vref1 (V0) Vref2(V1)
 (Vref1, Vref2)가
 Operational Amplifier)
 4 Vref1, Vref2 BA BA ()
 Vref2(V1) 3 Vref1(V0)
 BA (TFT)(SUB1) Vref Vr
 ef가 5 5 2 GVL 6
) , 가 TFT
 , GVL (Vref) , 5 10
 6 , . . . 가 . 6 ,
 , 가 DATA0, DATA1, CL1, CL2,
 M, V0, V1 ,
 , 가 , 18 DATA0, DATA1 2
 10 2 GVL, CC, (1) LT1,
 (2) LT2, LS, FF1a, FF1b, BA (1) LT1
 DATA0, DATA1 FF1a, FF1b
 (2) LT2, LS DEC DEC GVL
 가 . BA
 7 CL2 2 CL2-A, CL2-B 6 가
 8 CL2 2 2 7
 가 . (,)
 , (EMI) IC1 EMI
 9 (a) 9 (b) 2
 CL2 9 (a) 9 (b)
 t cycle 가 , 가,
 = (t cycle - t setup - t hold) / 2 가 , 「 가
 , t setup t hold , 가
 가 , , EMI
 가 , 가 ,
 가 , , 가 ,
 가 , , 가
 가 , IC(,)

가 ,
 FF1a, FF1b

6 8

10 , 3 6 8 (FF1a, FF1b)
 가) . ()
 () , FF2a, FF2b
 XGA 20 + (CL1) ,
 (FF1a, FF1b, FF2a, FF2b)
 FF1a, FF1b CL2 (1) LT1
 FF2a FF2b CL2
 D
 FF2a, FF2b () .
 가 가 ,
 1)
 , EMI()
 가 EMI
 11 (a) 11 (b) 3
 6 , 11 (a)
 11 (b) () . , 11 (b)
 11 (a) 11 (b) , VIH, VIL, t setup, t hold EMI 9 (a) 9 (b) 가 .
 , 10
 가 .
 FF2a, FF2b (, 가 , 10
) .
 12 , 4 () ,
 13 (a) 13 (b) 10
 (13 (b)) (13 (a)) . 13 (a) 13 (b) ,
 t setup / t hold
 14 (a) 14 (b) (14 (b))
 (14 (b)) . t s
 etup / t hold
 , IC t setup t hold ,
 0 (,) (가 ,) 13 (a)
 가 가 , ,
 0 (,) 0 t setup / t hold
 ,
 15 (a) 15 (b) 5
 15 (a) , TCON 90 2 A, B , 15 (b)
 ,
 , 14 (a) , A A
 B B 가 / , 1
 16 (a) 16 (b) 6
 16 (a) 16 (b) , 2 ,
 2 , 15 (b)

A 15 (a) A 15 (a) B , A
 B , 15 (b) C가 B , B
 , 15 (a) D , A

가 2 , , (GND)가 , EMI
 17a 17b 7 , 17a , 17b

a, GATb, GATc , 17a , , GAT
 , GATa, GATb, GATc , 가

가 (1) LT1 가 , ,
 17b , ,
 17a GATa, GATb, GATc GAT1 DD1 DD5 . . .
 TCON , DD1 , DD1 GT D
 1 DD2 ,
 D2 DD3, DD4, . . . ,
 DD1 , GAT1 ,
 DD2 DD2 ,
 DD1 DD2가 (DD1)
 DD2 , 가 DD3 ,
 , 가 DD3
 , EMI ,
 , 17a , FF1a, FF1b, FF2a, FF2b
 , FF1a, FF1b, FF2a, FF2b

17a 6 8 , 가 , TC
 ON 8 GATa, GATb, GATc , , 가 가
 , , , , TCON 가 가
 ((遠端)) IC , ,
 () 가 가 , IC가
 , , 가 가 IC
 , IC , IC ,
 , 17a ,
 9 TCON , 「1 × IC 」 ,
 10 , 가 , 1 (10 ,
 , 2). TCON , TCON ,
 , 가 「 TCON ×
 , EMI 가 , TCON

18 TCON , 10 PNL , TFT ,
TCON , ,가 ()가
, TCON PNL IC1 가 ,
, 가 TCON , EMI
11 , , 가 TCON LVDS LVDS TCON LVDS TCON
, TCON , LVDS , TCON
, 가 , 가 가 , V0, V1
12 BA , 6 8 , V0, V1
, 가 , 가 가 , FPC
가 , 가 가 (, R-DAC , C-DAC , 가),
, 가 , ,
, , 10 20 , 1 ,
가 , 가 ,
19 13 () ,
가 ,
가 IC , ACF() ,
20 () 14 , 가 , 가 ,
20 PNL , 20 , A AR , 가 ,
() ST , ST
PNL , TFT ,
ST , 17a , () ST ()
, () 가 , 가 () ST ,
, FCA , TCP , 20 (가) ST ,
, () ST , 가 , 가 ,
가 가 21 () 15 , , 가
() AR , , 가

21 , , (GND) , d , W (

FPC , (GND) 가 가 ,)

FPC 가 FPC , (GND) ,

FPC2 , () ,

가 FPC2 , ,

22 , 16 21 가 PR

J , PRJ FPC CHC 가

23 17 , SUB2

(: CF) , FPC2 (d)

21 22 가 가

가 TFT

TFT 27 d FPC

23 , FPC ,

24 18 , ,

가 가 , ,

25 19 , ,

() (FPC2)가

FPC2 AR , 가 FPC2

26 27 , 26

26 27 , A1 1 1 A1 2 , A2 2

가 A 1 1 A1 2 2 A2

AR 가 ANL

AR 가

CL2 DF 가

CL1 ANL M AR DS AR

DF

ST , BP BP AR ()

BP 가 27 BP ,

28 , 가 , OUT AR " "가

가 , " (가) ,

() , 가

29 , 20 ,

(OUT) IC1 (OUT) AR IC1 AR

29 A 가 , 29 가 ,

IC1 가 OUT ,

가 VCC, GND, VL

CD , DM1, DM2, DM3 , DBP 2

VCC, GND, VLCD ,

26 , 27 BP AR , 2 ,

CTL , ST ,

BP , 2 , ICIA1

30 ICIA2 , FPC2 30 FPC2 FPC2

() , ACF , FPC2 FPC2 가

가 ,

31 21 , FPC2

CHC , (22 PRJ) TH , TH ,

(2, 22) , TH ,

32 , FPC2 FPC2 , 31

FPC2 TH ,

33 31 21 FPC2
 TH 가 , FPC ,
 34 22 () 가, ()
 34 IC1 , FCA (,)
 가 FPC2가
 FPC2 , (1) (, (2))
 PWL-D PWL-D PWL-D
 DE, DDL GDL
 I/F-FPC PWL-G I/F-FPC , 34 , 34 ,
 (IC1 I/F-FPC)
 FPC2 I/F-FPC
 PWL-D
 34 PWL-D FPC2
 DDL
 PWL-D DDL
 FPC2 I/F/FPC
 CT4가 PCB PCB IC1 ()
 (PCB IC1)
 (A) PAD-A 가
 FPC2 I/F/FPC
 가
 35 23 FPC2 I/F/FPC
 34 IC1 (短冊狀)
 FPC2 PWL-D
 PWL-D PWL
 -DD가 35 DDL, G (B) PAD-B
 22 () 35
 FPC2 PWL-D
 PWL-DD I/F/FPC G PWL-G
 DDL, (A) PAD-A 34 22 35
 가 FPC2가 가 22
 가 가
 36 24 I/F/FPC IC
 35 23

36 35 PWL-D PWL-DD I/F/FPC I/F/
 FPC IC1 DDL, GDL, PAD-C(
 PWL-DD I/F/FPC C I/F/FPC가
 PWL-G) 23 가 TCON
 PCB
 37 가 25 FPC2 ()
 36 24 CT5 I/F/FPC I/F/FPC
 24 FPC2가 CT5 PAD-D
 37 FPC2가 CT5 FPC2 d
 23 FPC2 FPC2 CT5
 PCB FPC2 CT5
 23 가 FPC2
 가
 38 가 (103)가 (104), (TFT-LCD)
 (102)가 (101) (102) (104) (101)
 TFT 2 (104)
 DiG, DiB, . . . Di+1R, Di+1G, Di+1B, GTM (G-1, G0, , G2, . . . Gend, Gend+1), DiR,
 , Cadd
 39 PC () (, 18 , 65 MHz)
 () LVDS : LVDS () LVDS-T (LVDS)
 (, TFT) (LVDS : LVDS)
 LVDS-R LVDS-R (18 , 65 MHz) 가
 TCON 가
 LVDS LVDS-T LVDS LVDS-R , 가
 가
 EMI가 가 CPU가
 40 가 가
 가 PNL, PCB, FPC1, IV
 FPC2, , LPC LVDS IV
 PNL

40, 41

가

가

가

()
가가

(TFT
, FPC)

가
가

가

가

(57)

1.

1

2

1

가

1

가

1

(, 17B DD3)가 GAT3) ,

(, 17B DD4)
(, 17B DD3)
(, 17B DD4)

가

2.

3.

1

1

4.

1

5.

1

1

, , , , ,
 , .
 5 6. ,
 ,
 6 7. ,
 7 8. ,
 5 9. ,
 1 10. ,
 5 11. ,
 1 2
 5 12.
 5 13. ,
 1 14. 1 , 1
 13 15. 가 (35) 1
 14 16. (22) 가 ,
 14 17. 가 1
 1 1 2 , 1 2 2 ,
 1 1 1 , 1 2
 1 1 ,
 1 가 ,

1 가 2 , ,
1 2 가 가 (, 17B DD1) , ,
1 1 , , 1
2 가 가 , 1 (, 17B DD1) , 1
1

18.

1 , 1 2 , 1 2 , ,
1 1 , 1 2 ,
1 , ,
1 가 , ,
1 가 2 , ,
2 가 가 (, 17B DD1) , ,
1 1 , ,
1 1 , 1
2 1 2 , ,
2 가 가 , 1 (, 17B DD1) , 1
1

19.

18 , ,

20.

1 , 1 2 , 1 2 , ,
1 1 , 1 2 ,
1 , ,
39 102)가 , (38 101) (,
1 2 , , 2 가 가 (, 17B DD1)
1 1 , 1 2 ,
1 , 1

1
 2 가 가 , 1 1 2 , 1 1 DD1 ,
 1
21.
 1 1 2 , 1 2 1 ,
 2 1 1 2 ,
 1 1 가 ,
 1 2 ,
 , 1
 1 (17B DD1) ,
 1 (DD1) (,
 17B DD2-5) (, 17B DD3) ,
 (, 17B GAT3) , (, DD3)가
 (, GAT3) (, DD3)
 (, 17B DD4) (, GAT3)

22.
 21 , ,

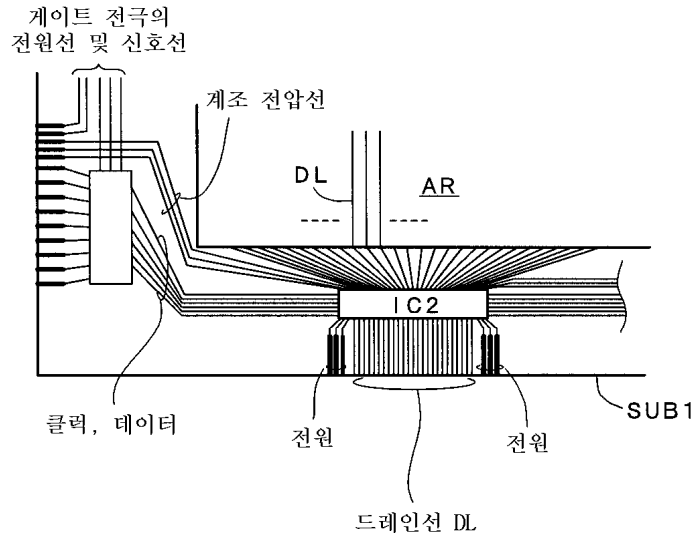
23.
 21 , ,

24.
 ,

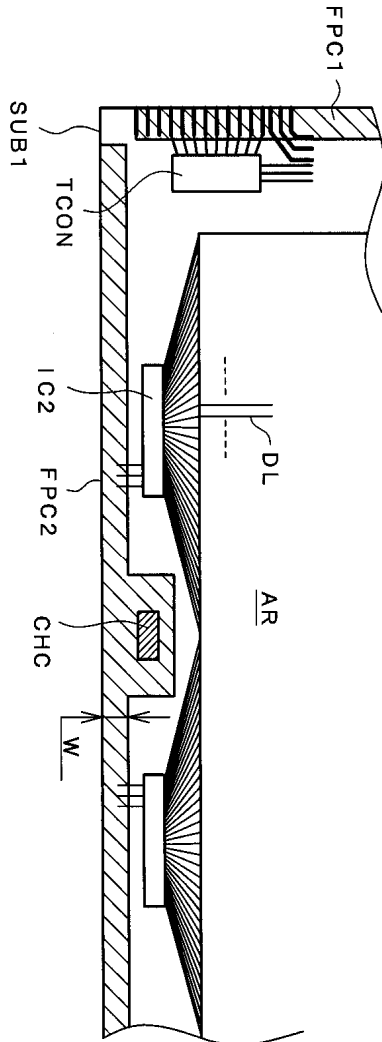
25.
 21 , (, GAT3) (, DD3) ,
 (, DD3)

26.
 21 1 (DD1) ,
 (, DD3) (, DD3) ,
 (, DD3) (, DD4) (, DD3) ,
 (, DD4) (, DD3)

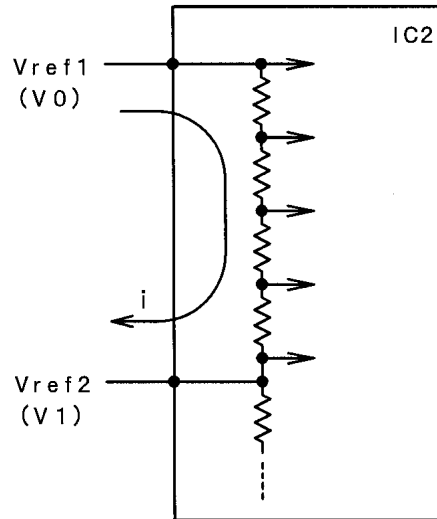
1



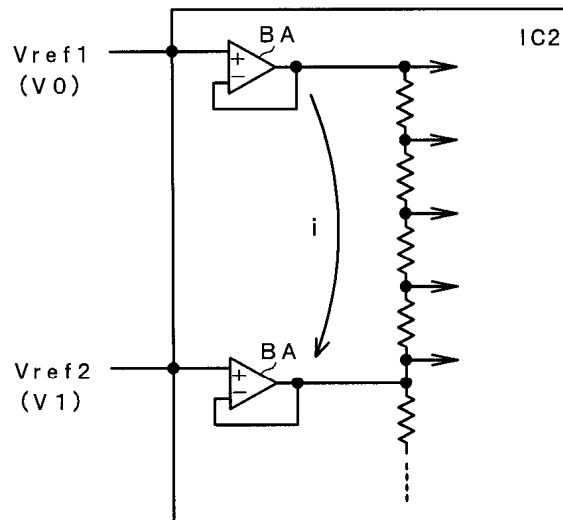
2



3

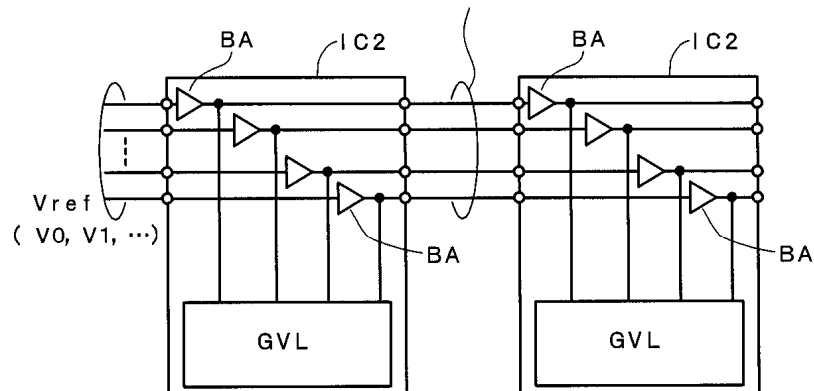


4

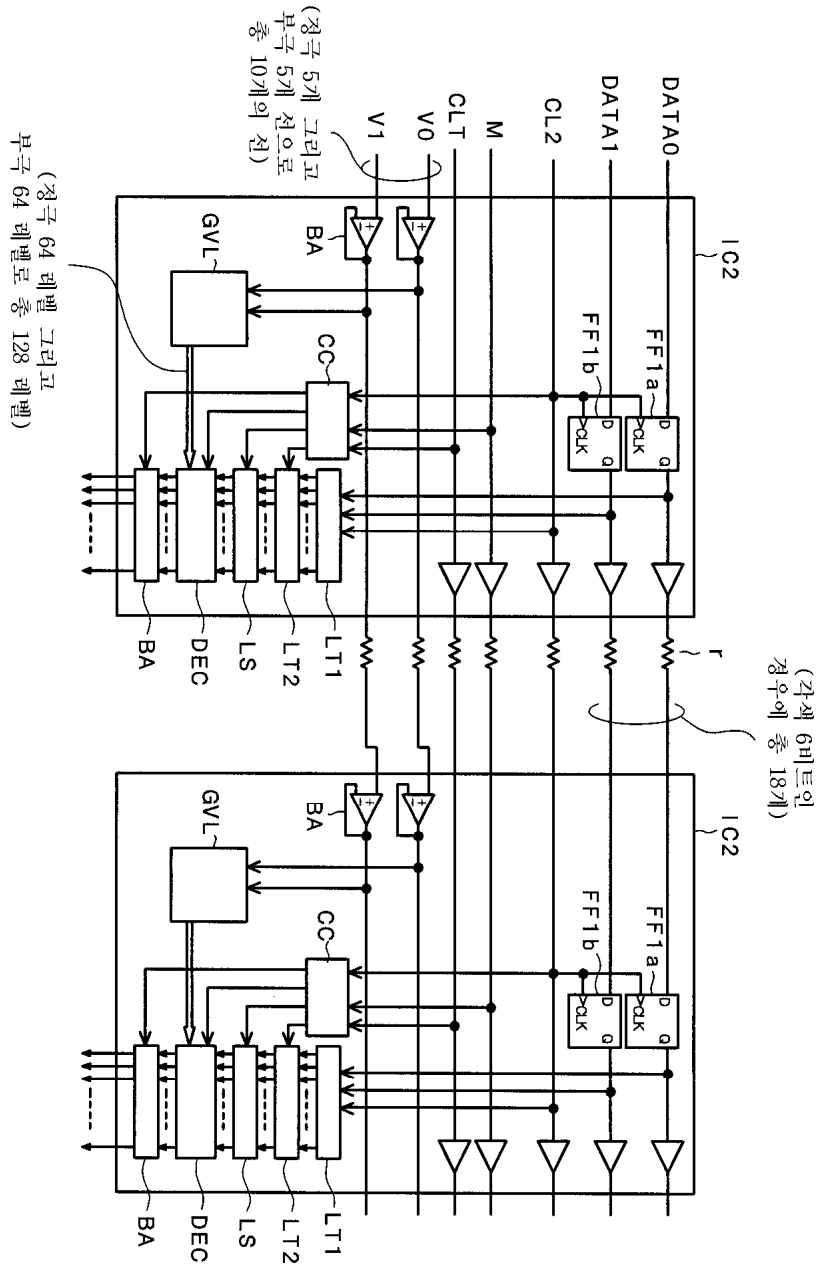


5

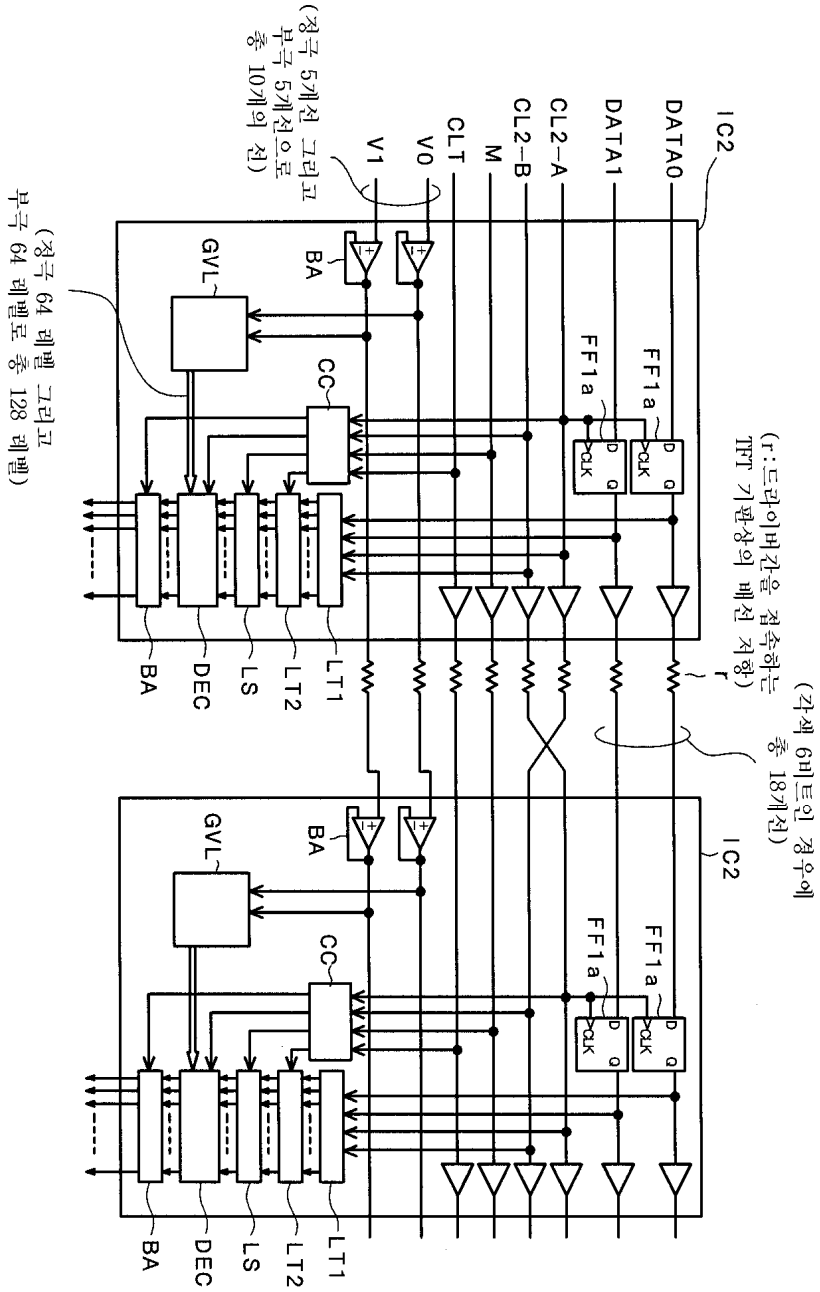
TFT 기판상의 배선



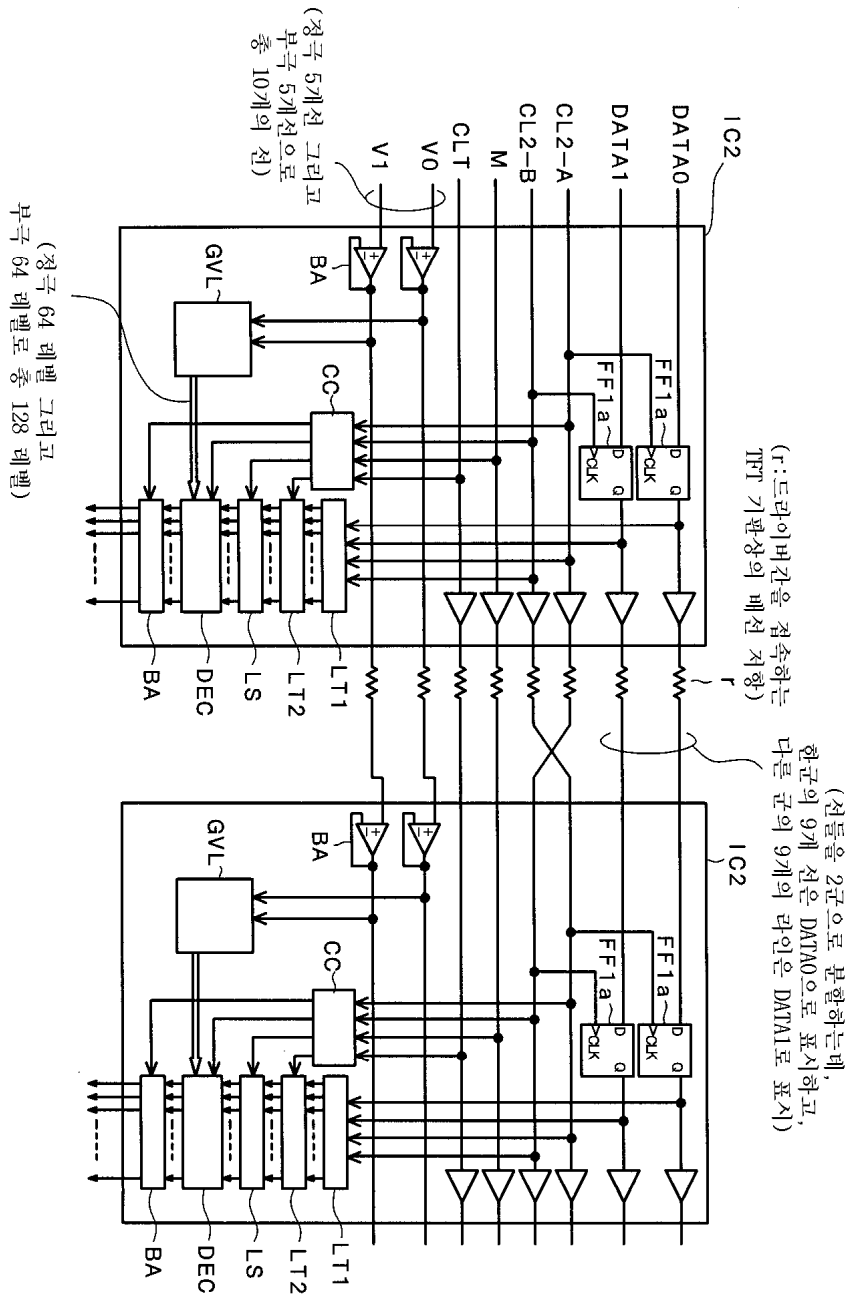
6



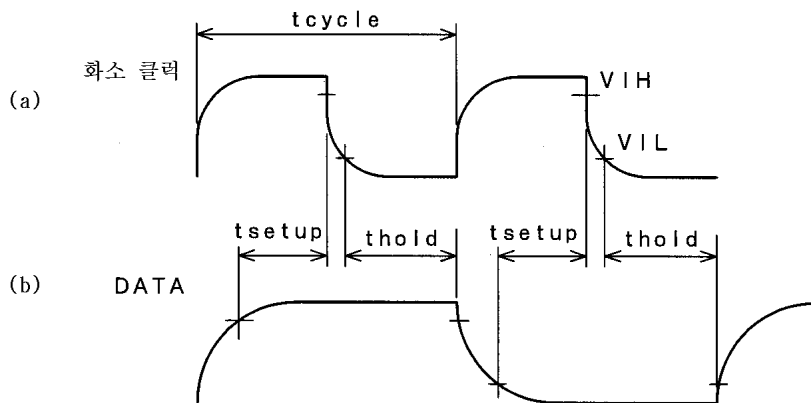
7



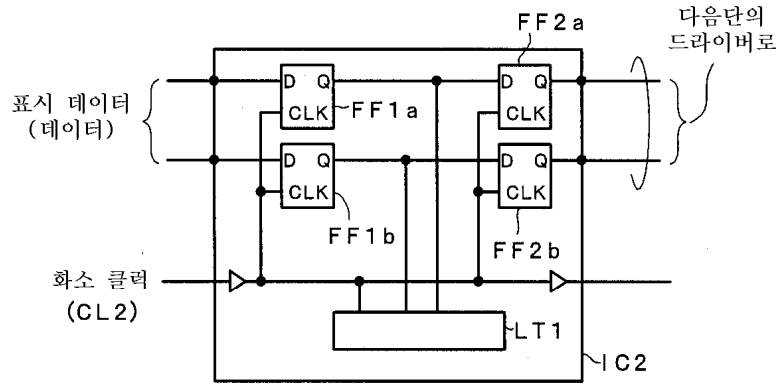
8



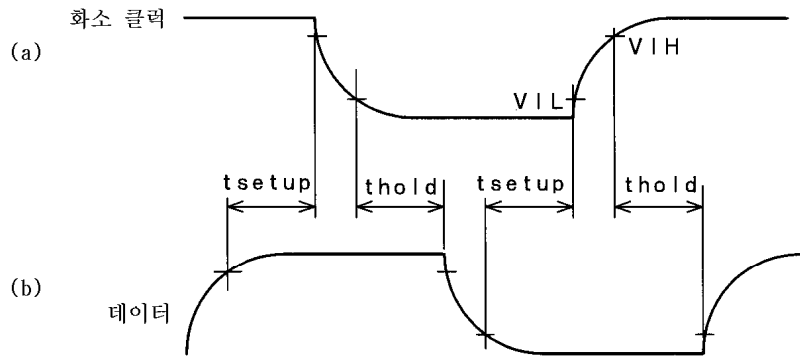
9



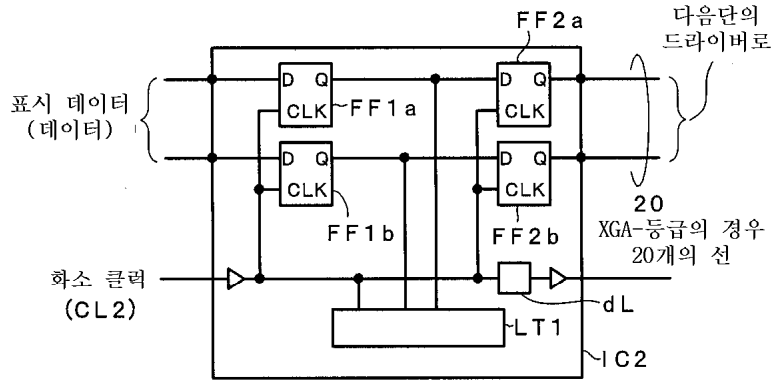
10



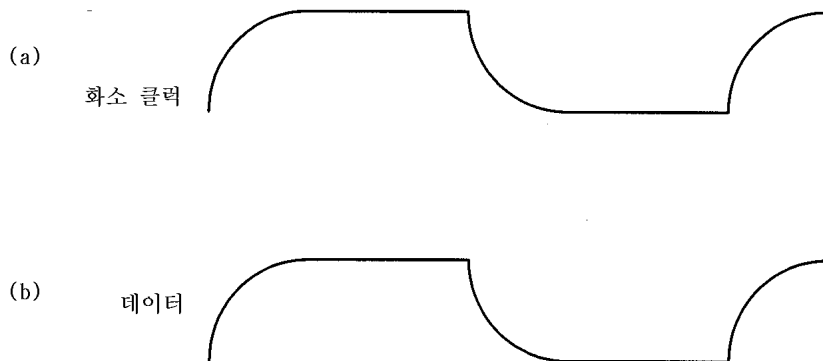
11



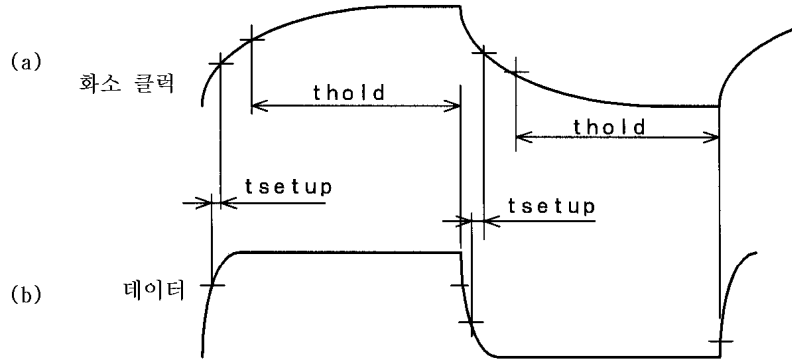
12



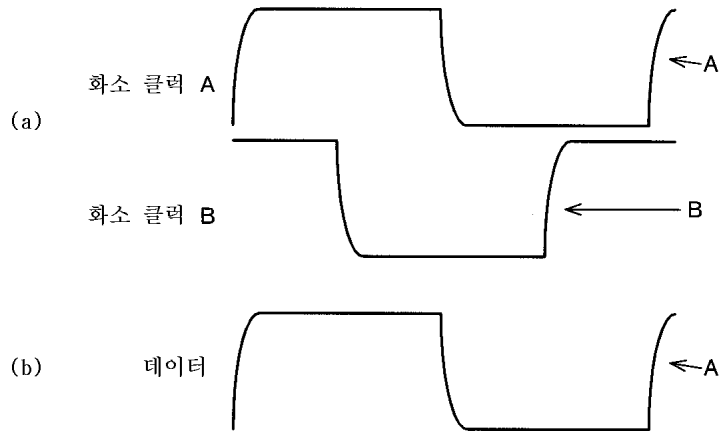
13



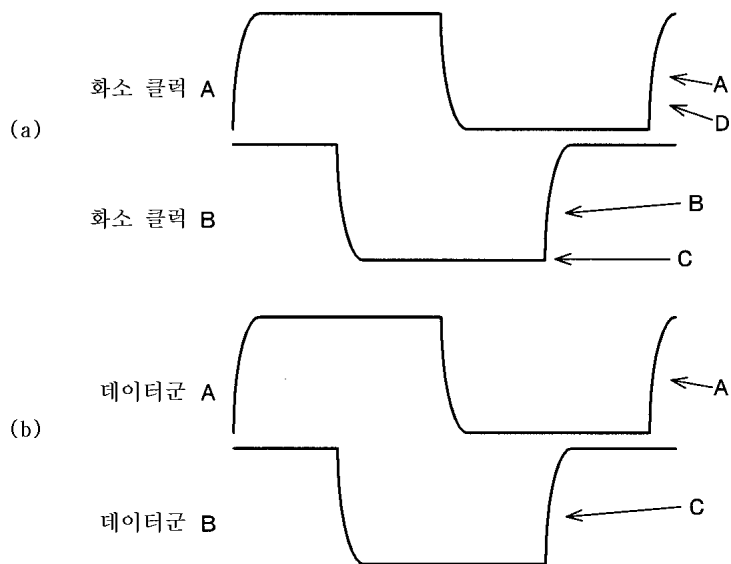
14



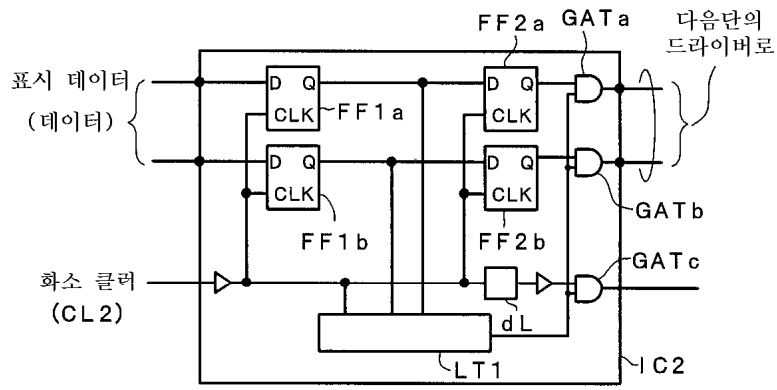
15



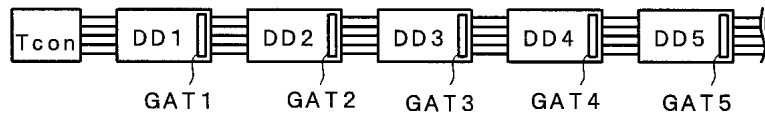
16



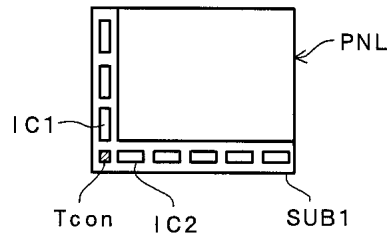
17a



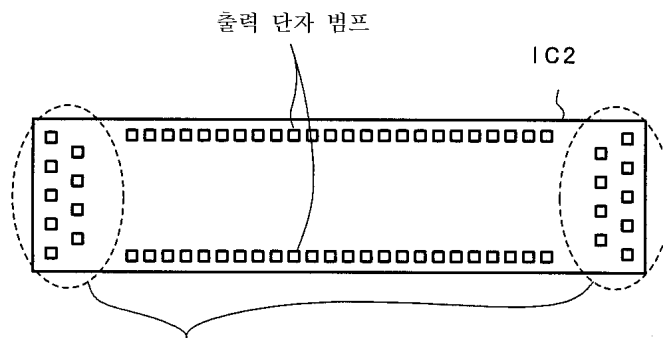
17b



18

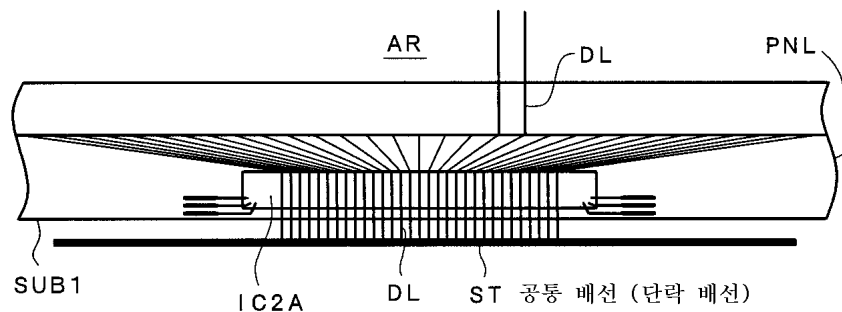


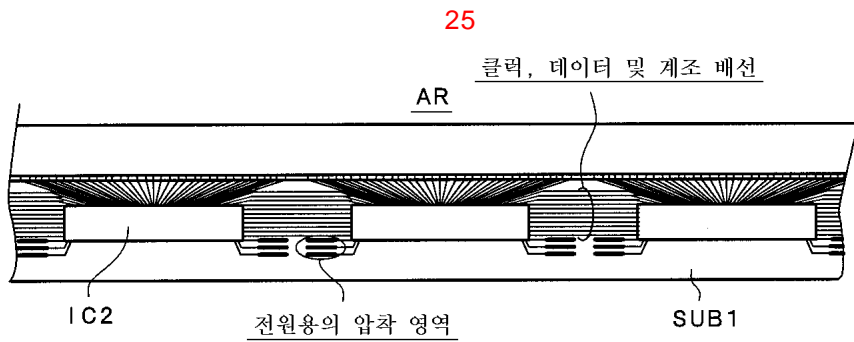
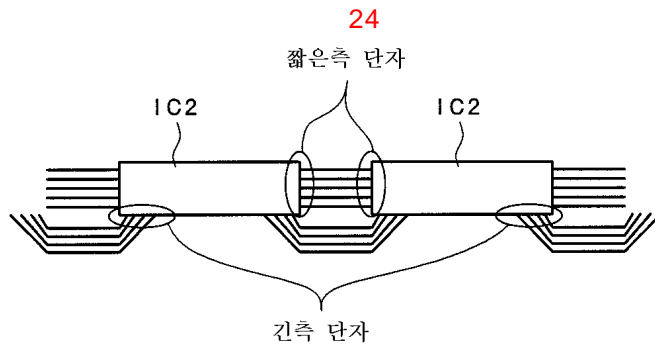
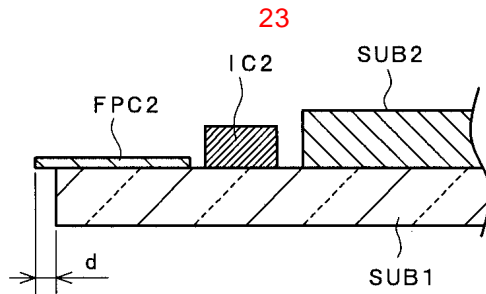
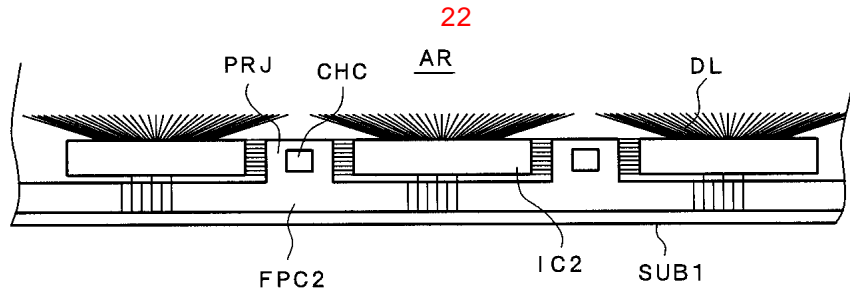
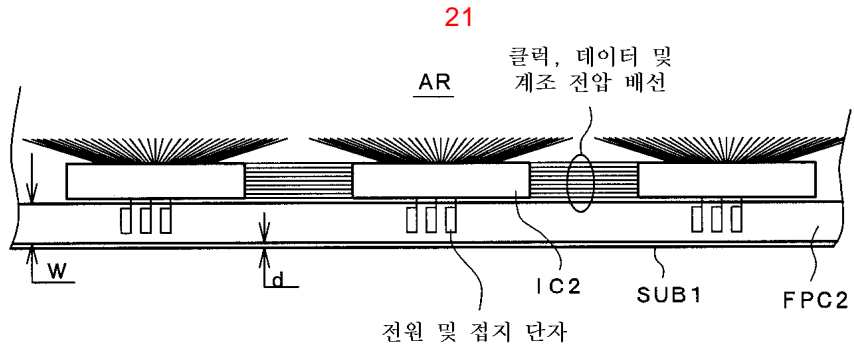
19



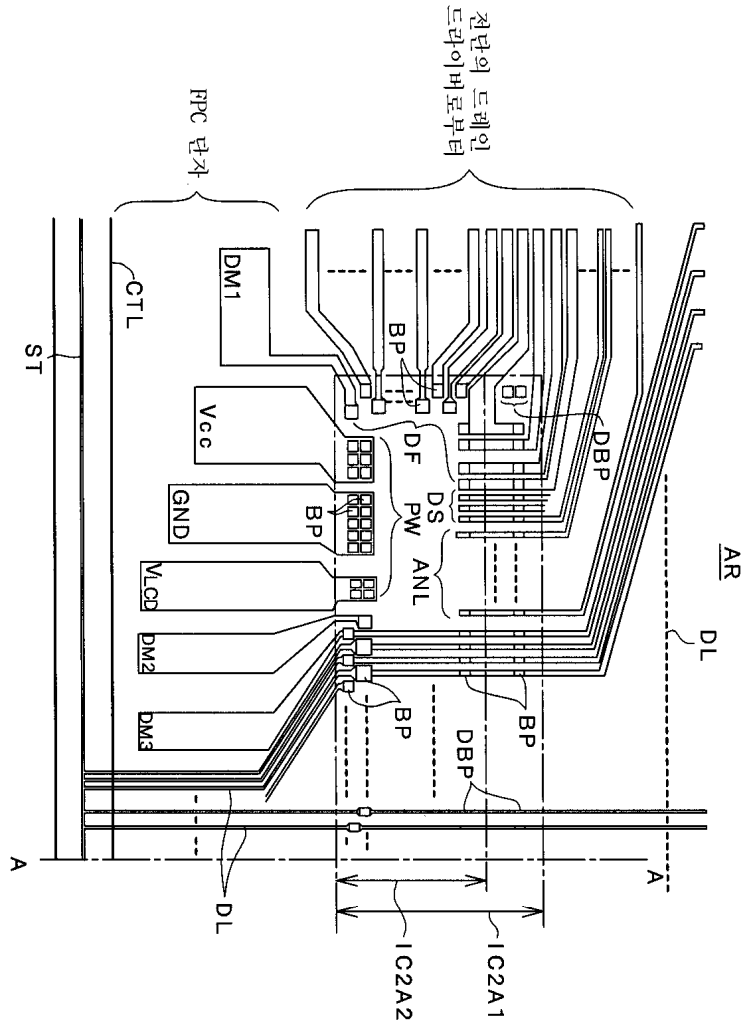
전단, 다음단의 드라이버의 사이에서 신호의 수신이나 제공을 하는 단자 범프

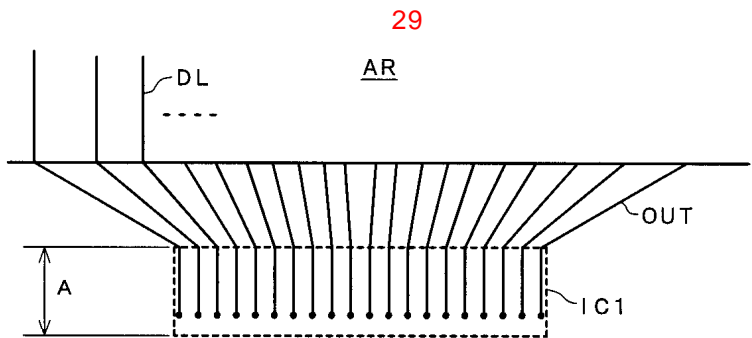
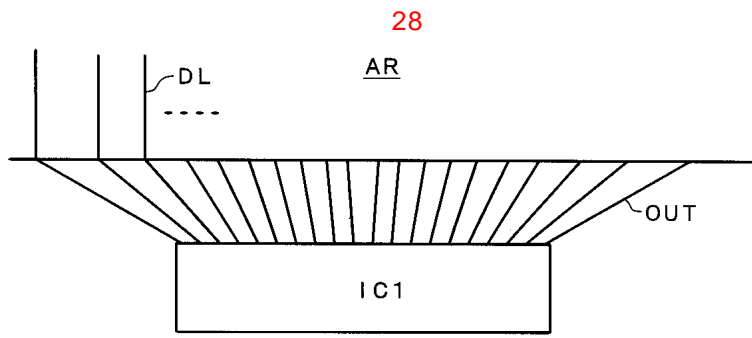
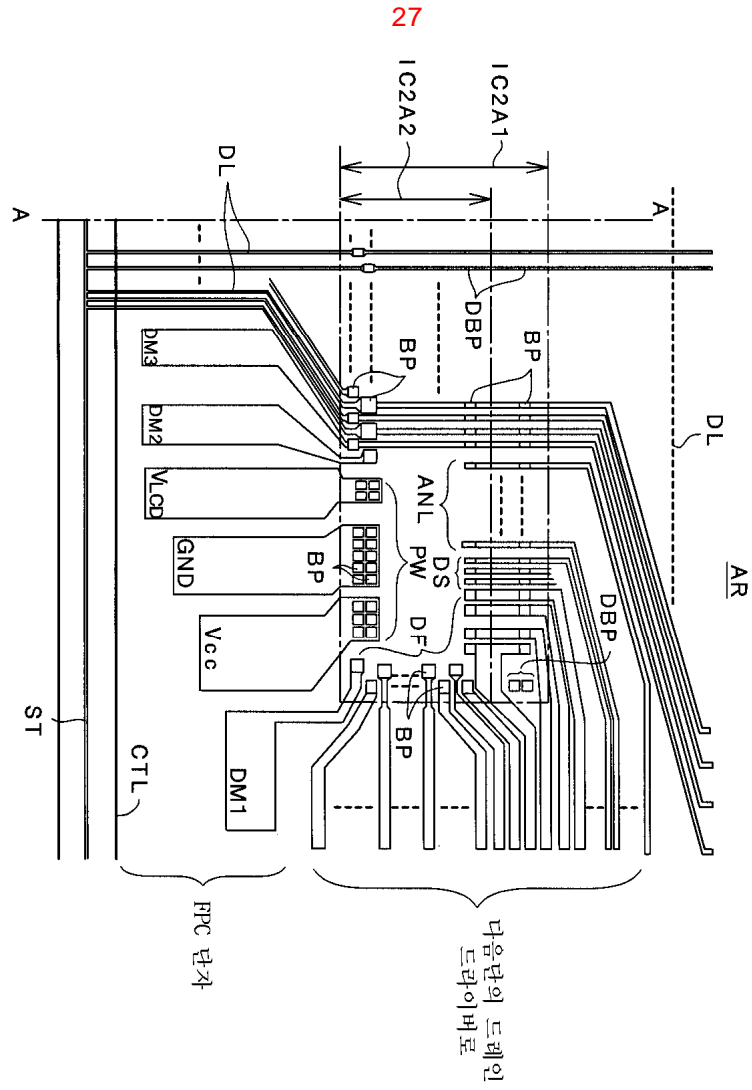
20

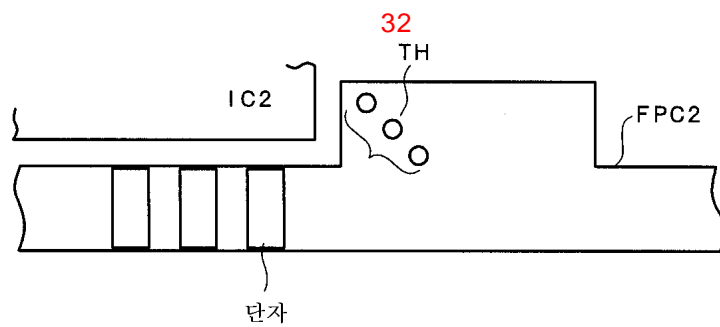
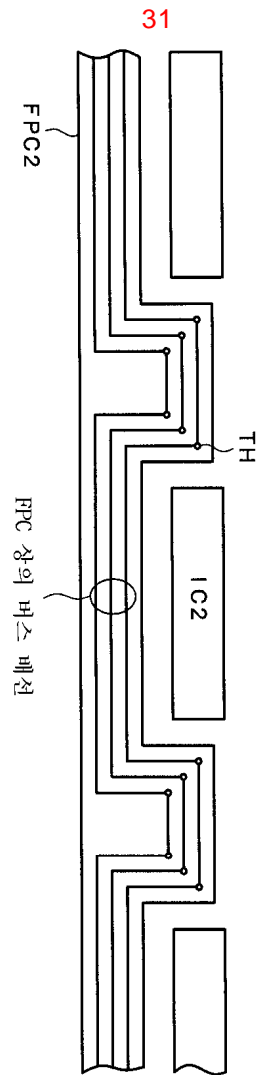
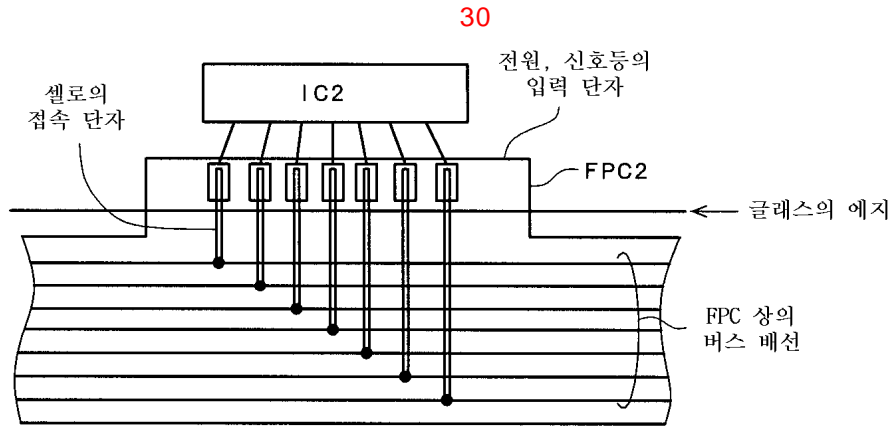


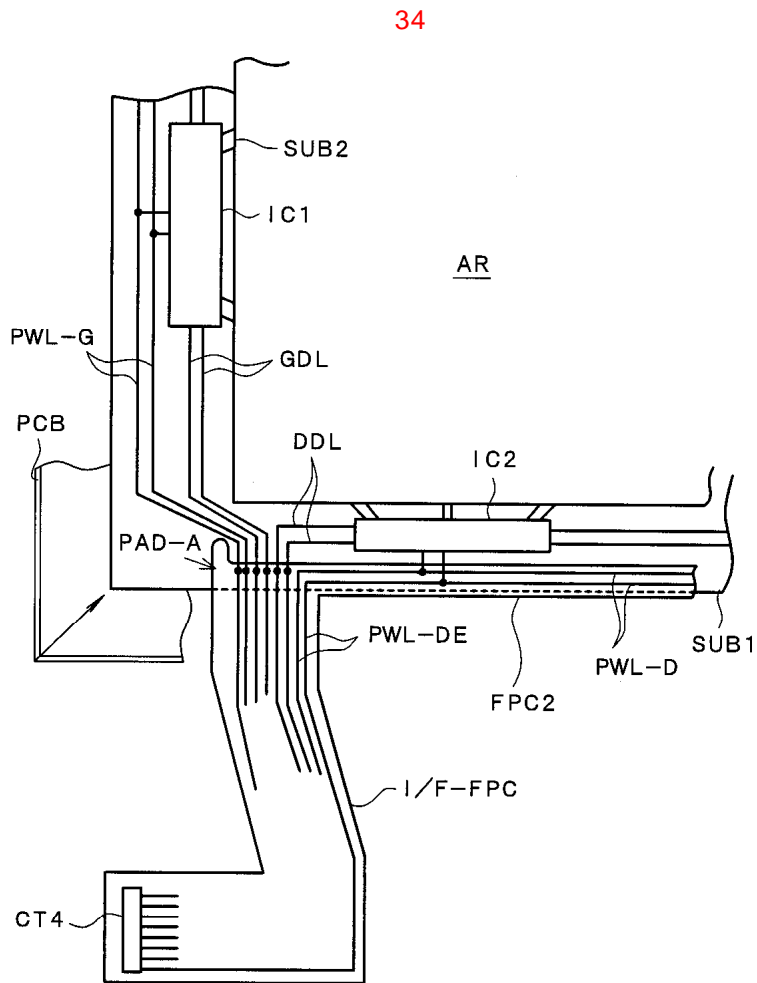
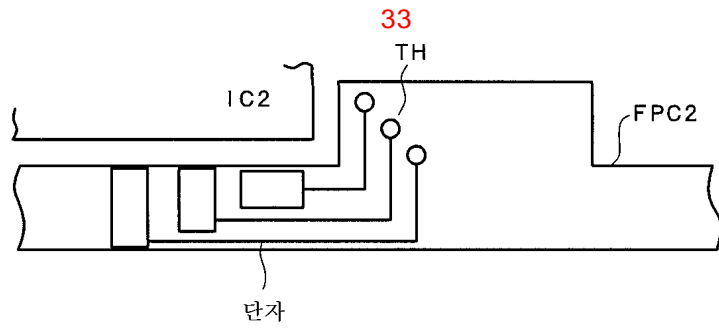


26

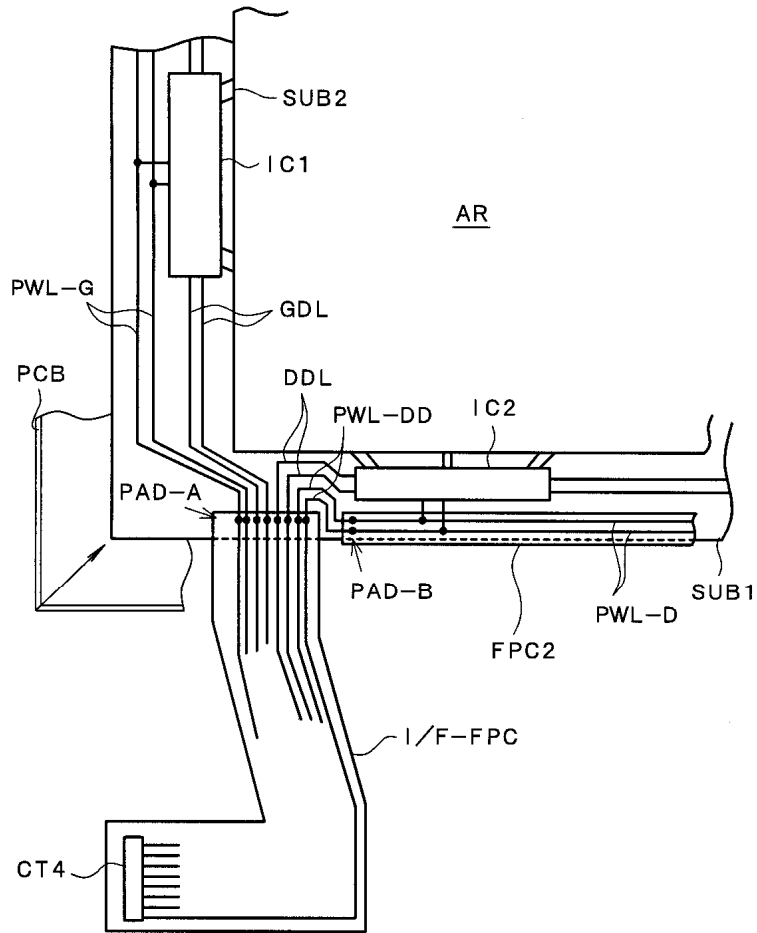




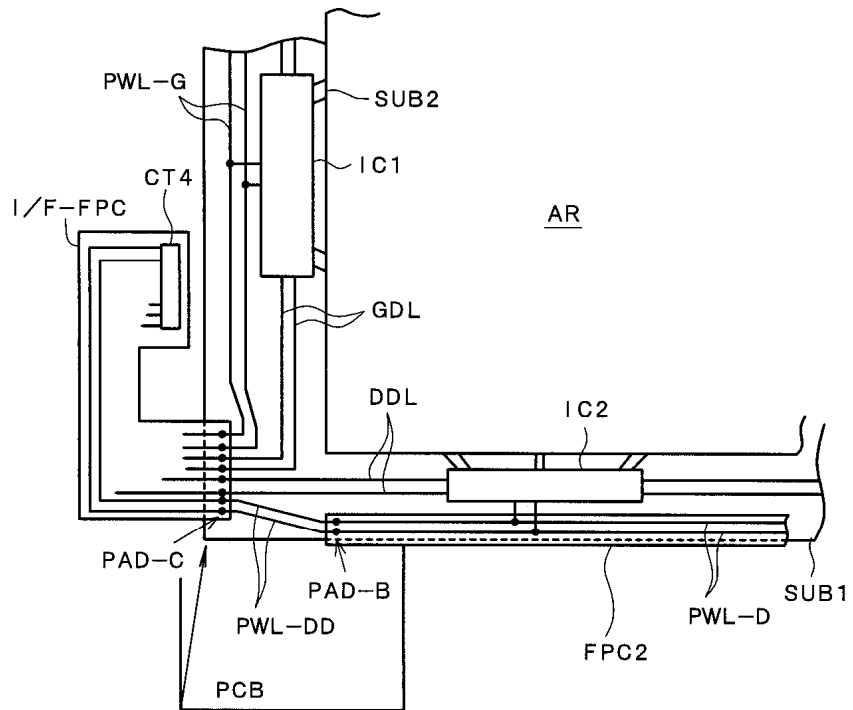




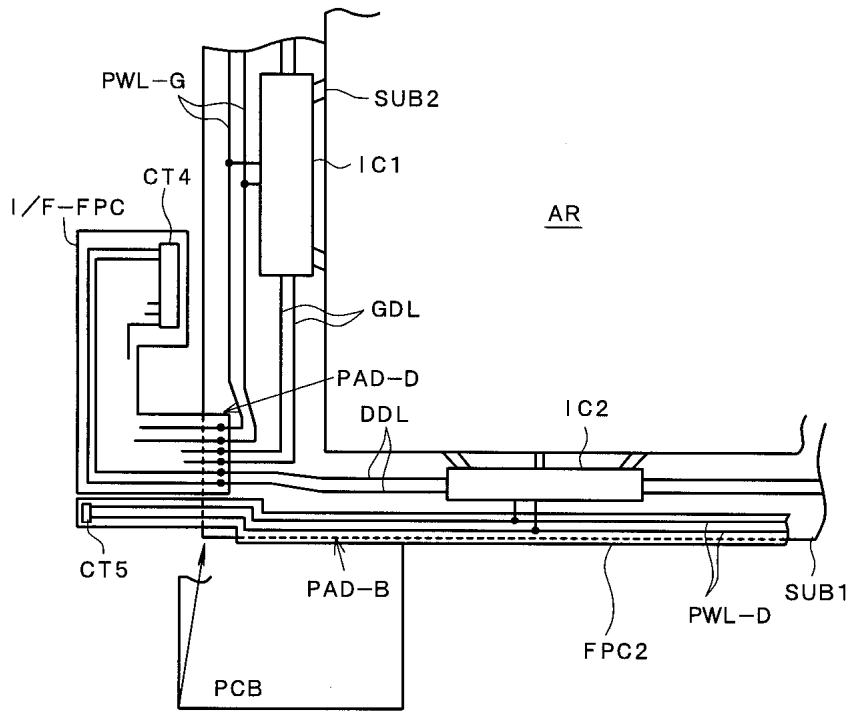
35



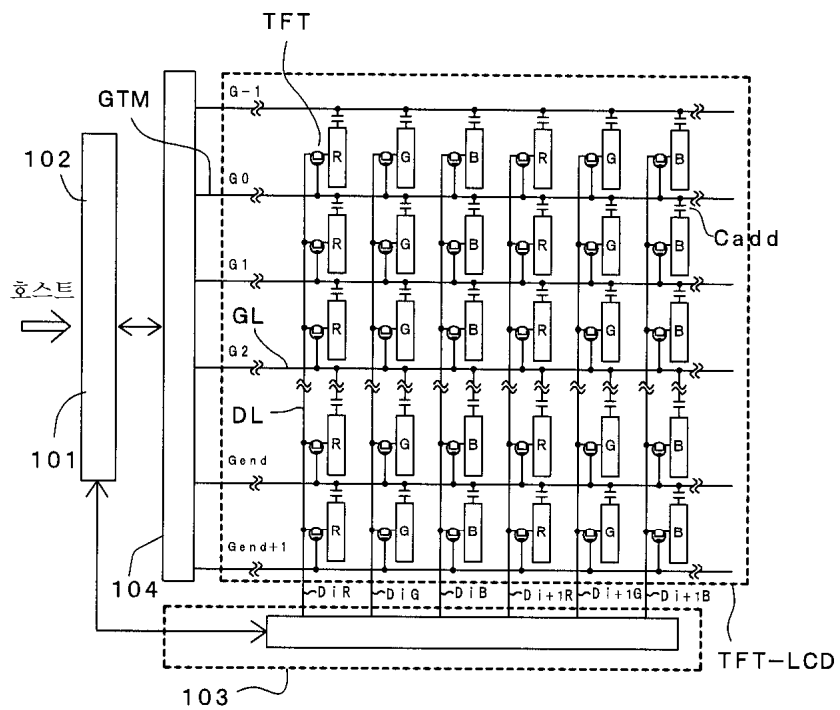
36

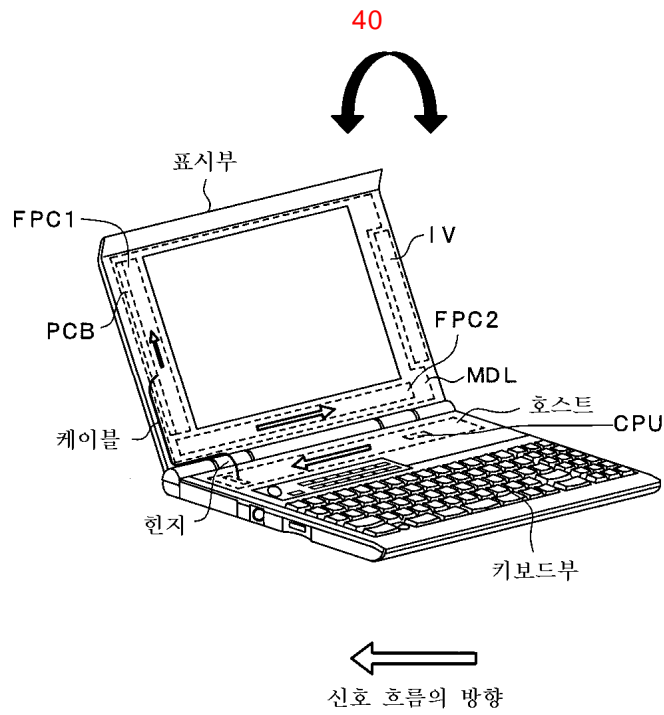
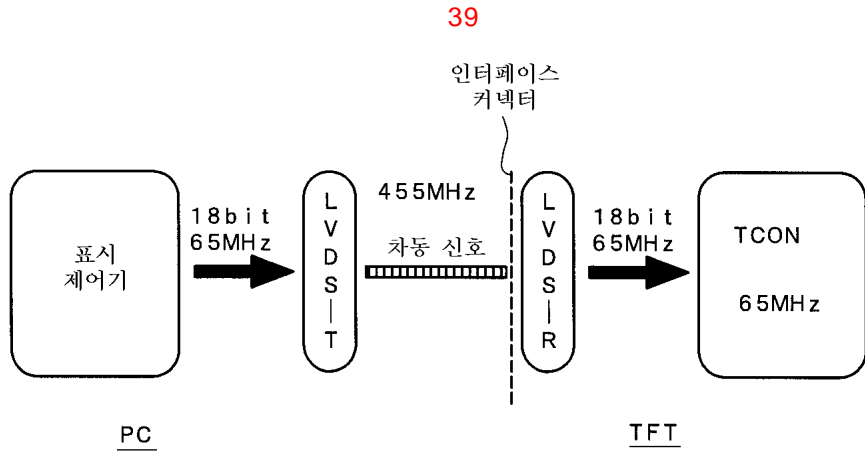


37

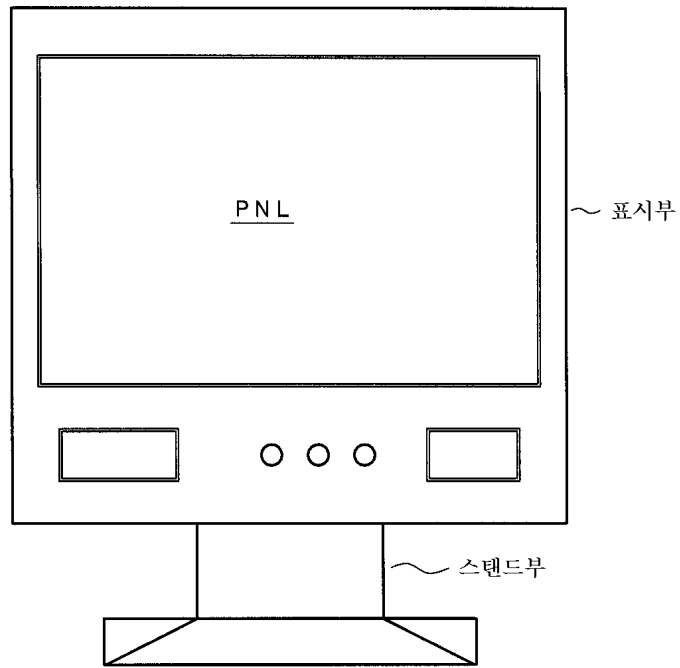


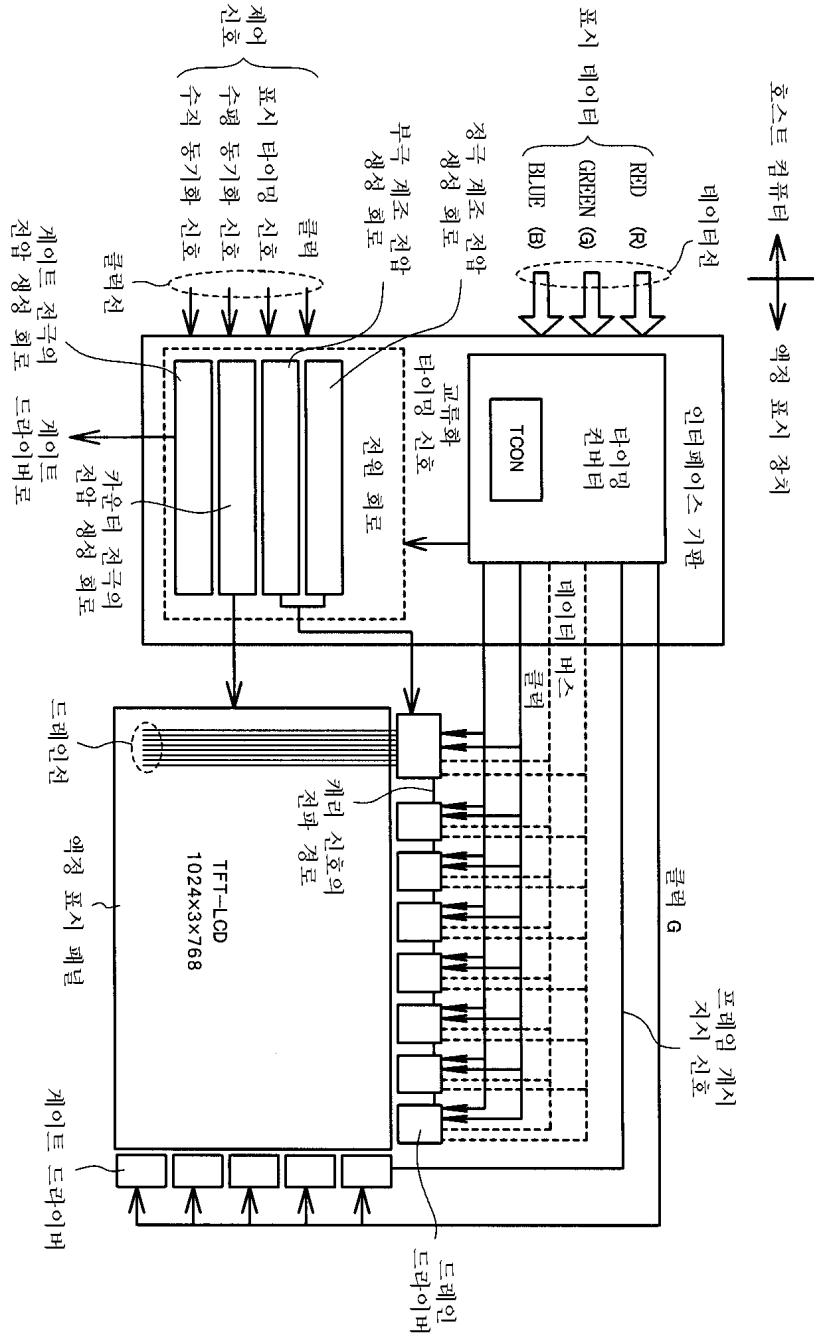
38



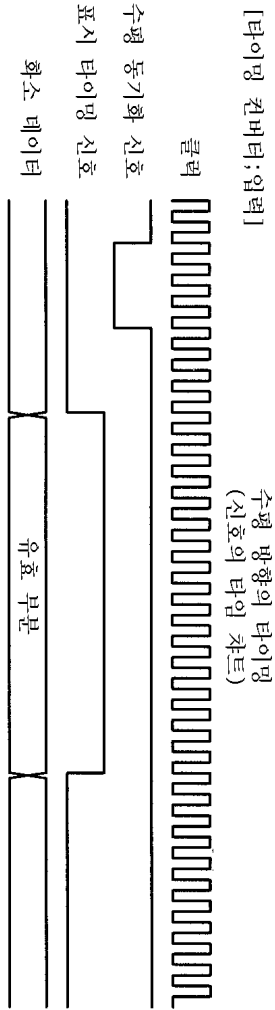


41

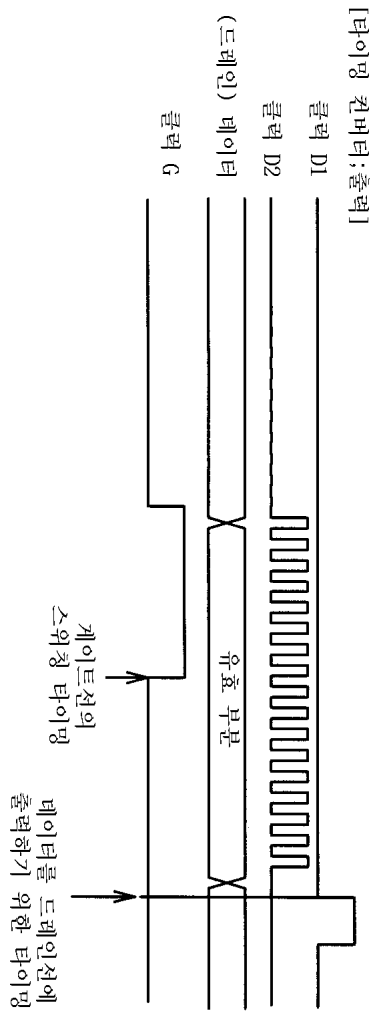




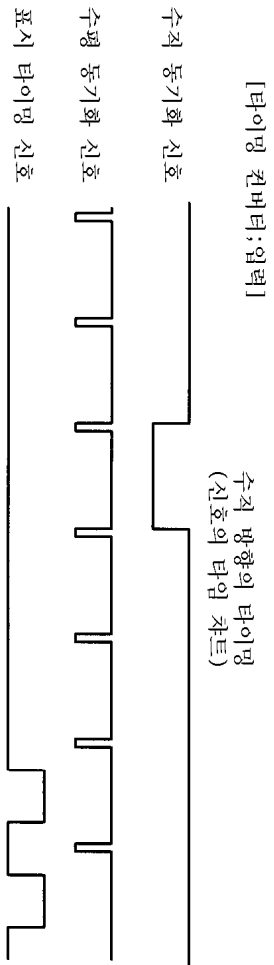
43a



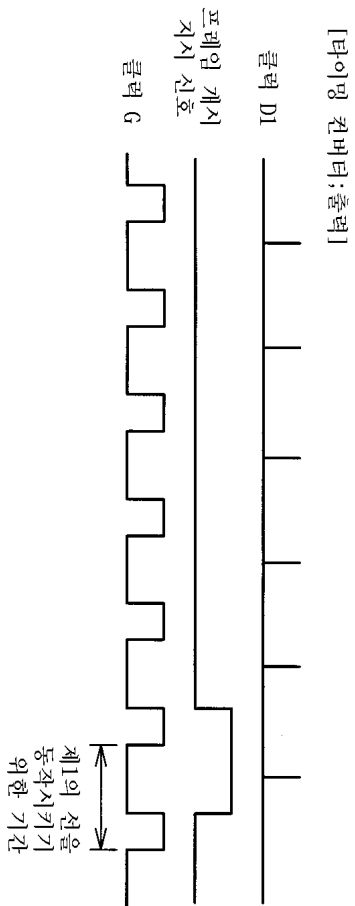
43b



44a



44b



45

