Title: METHOD FOR SYNCHRONIZING AN AUTOMATION DATA COMMUNICATIONS NETWORK

Abstract: The object of the invention is a module (1-6, 1-8, 1-10, 1-12, 2-2 ... 2-16, 3-2) for an automation data transmission network, said module (1-6, 1-8, 1-10, 1-12, 2-2 ... 2-16, 3-2) comprising an Ethernet switch (3-8). The invention is characterized in that the module comprises means (3-10, 3-12, 3-14) for receiving and transmitting a two-part time synchronization pulse in which the first and second part of the two-part time synchronization pulse jointly indicate time data so that the module (1-6, 1-8, 1-10, 1-12, 2-2 ... 2-16, 3-2) is adapted to receive time data from the first part and to convey the first part through the module's Ethernet switch (3-8), and the module (1-6, 1-8, 1-10, 1-12, 2-2 ... 2-16, 3-2) is adapted to convey the second part past the module's Ethernet switch (3-8) and, in response to the second part, to synchronize itself with the time data indicated by the first part.
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Method for synchronizing an automation data communications network

Field of technology
The invention relates to an automation data communications network, particularly to time synchronization in such a network.

Background of the invention
An automation data communications network may comprise several IEDs (Intelligent Electronic Devices), such as relays, and a switch can be arranged in a functional connection with these devices to connect the IED to said network. If the switch is integrated in the device, devices can be interconnected without an external switch. This will result in substantial benefits with regard to costs and the time for constructing the systems.

Separate IEDs measure different quantities in an electric grid, such as voltage and current. If a protective function is required in a particular grid malfunction, a precondition for the efficiency of the protection is that the protection can be enabled and that it is operational. If synchronization between the devices is not accurate, the sampling phase difference between the A/D (Analog/Digital) instrument transformers for the measured quantities, such as voltage and current, cannot be precisely calculated. Because the devices measure the samples at different times due to inaccuracy of synchronization, the designed phase difference between the measurements is no longer valid. This can lead to a situation in which grid protection does not work sufficiently or at all.

The problem with prior art LAN solutions lies in grid measurement errors arising from internal delays in switches and the unpredictability of such delays. These make it impossible to achieve accurate protocol-based time synchronization between IEDs at the microsecond level and may lead to insufficient protection of the electric grid.

Brief description of the invention
The objective of the invention is to develop a method and an apparatus implementing the method in order to solve the problems referred to above. The objective of the invention will be accomplished by a method and system characterized by the independent claims. The dependent claims describe preferred embodiments of the invention.
The invention is based on using the vacant pairs of conductors in the Ethernet cable to distribute an accurate time synchronization signal to the network devices.

The advantage of a method and system according to the invention is that no separate wiring is required for the time synchronization signal, which, together with a daisy-chaining facility, substantially reduces the need for wiring.

**Brief description of the figures**

In the following the invention will be described in more detail in connection with preferred embodiments by referring to the enclosed drawings, where

Figure 1 illustrates part of an automation data communications network according to the invention and one of its preferred embodiments;

Figure 2 illustrates daisy-chaining of a more extensive system according to the invention and one of its preferred embodiments;

Figure 3 illustrates a device according to the invention and one of its preferred embodiments;

Figure 4 illustrates synchronization signalling according to the invention and one of its preferred embodiments; and

Figure 5 illustrates the flow of data signals according to the invention and one of its preferred embodiments.

**Detailed description of the invention**

Figure 1 illustrates part of an automation data communications network 1-1. The network may comprise one or more control and data acquisition devices 1-2 such as so-called SCADA elements (Supervisory Control and Data Acquisition), which can be a computer or a relay for example. A SCADA element can be connected 1-28 to an element providing timing in the form of a synchronization signal, a clock master element 1-4. There can be one or more of these elements in the network. Furthermore, the network may comprise one or more modules for the automation data communications network, such as an IED group and/or an IED 1-6, 1-8, 1-10, 1-12, for example a protective relay.

The communications between the SCADA element and one or more IEDs, or between IEDs, can be bidirectional. For example, a SCADA element can provide control commands to an IED, and an IED can provide measurement and event data to a SCADA element or to other IEDs.
Figure 1 shows that a switch 1-7, 1-9, 1-11, 1-13 can be arranged in a functional connection with the relay to connect the IED to said network 1-1. If the switch is integrated in the device, devices can be interconnected 1-20, 1-22, 1-24 without an external switch.

In order to enable protocol-based time synchronization between IEDs at the microsecond level, the internal delays of integrated switches and the unpredictability of these delays must be taken into account when connecting IEDs to the network. According to an embodiment of the invention, this can be done, for example, by supplying one or more separate synchronization signals to one or more IEDs. Because the IEDs can be daisy-chained, another embodiment allows the synchronization signal to be conveyed from one IED to another in a LAN, for example by using the vacant pairs of conductors in a standard Ethernet cable. According to a third preferred embodiment, the synchronization signal can be communicated on a pair of conductors intended to be used for supplying power, the pair conveying the Power Over Ethernet standard signal. Vacant pairs of conductors can also be used in this case, and the synchronization signal can be modulated onto a power supply signal compliant with the IEEE 802.3af standard (IEEE, Institute of Electrical and Electronics Engineers) without the power supply signal interfering with the synchronization signal.

In addition to the synchronization signal, which is the second part of a two-part time synchronization pulse for an IED, the IEDs can be supplied with the first part of the two-part time synchronization pulse, which is a network message providing time data. The message can provide coarse time data that can be defined more precisely using the synchronization signal. The network message can be included in the synchronization signal, in which case the synchronization pulse can be called a single-phase synchronization pulse. In a certain single-phase time synchronization pulse, such as an IRIG-B signal (Inter-Range Instrumentation Group), the bit sequence can be synchronized with GPS time, for example, and the bit sequence of the synchronization signal starts at each full second.

Alternatively, the network message can be a message separate from the synchronization signal, in which case the synchronization pulse can be called a two-phase synchronization pulse. The synchronization signal and the network message can thus be conveyed in different conductors of the LAN. Therefore, the module can be adapted to receive time data from a first part,
such as a network message, and to convey the first part of the time data through the module's Ethernet switch. Furthermore, the module can be adapted to convey a second part, such as a synchronization signal, past the module's Ethernet switch and, in response to the second part, synchronize itself with the time data indicated by the first part. Alternatively, the module can be adapted to convey the entire time pulse signal past the module's Ethernet switch.

Thus the first clock signal, the synchronization pulse, which is communicated from the clock master elements) to the IEDs and is required for the synchronization of the IEDs, can comprise a synchronization signal and/or a network message. The synchronization signal, which can be daisy-chained from one device to another to achieve mutual synchronization between the devices, can be a pulse sequence signal, such as a 1 pps (pulse per second) signal, or a signal containing the time, such as an IRIG-B signal. The network message can be a SNTP network message for example.

The synchronization signal provided to the network devices according to the invention and its preferred embodiments can be directly communicated from one device to another without processing it in the device and/or without making the synchronization signal go through a LAN switch such as an Ethernet switch. Alternatively, one or more IEDs can process the synchronization signal before it is communicated to the next IED. For example, an IED can perform time and/or frequency conversion on the received synchronization pulse before forwarding it, for example if the received pulse is too coarse.

If the LAN being used is an Ethernet network, its cable structure is often prescribed. An Ethernet cable can contain 8 conductors, of which 4 conductors are used for communications in a 10/100 Mbps Ethernet. The remaining 4 conductors are vacant for other use. Therefore, separate synchronization signals can be conveyed to the network using these pairs of conductors.

When connecting devices in a LAN, such as an Ethernet, different standards allow for the use of 4-pair copper cable in which only 2 pairs are required for data transmission. Despite this, all 4 pairs are connected to an 8-pin RJ-45 connector. In different standards the numbering of the pairs can vary, but usually the following conductors constitute pairs: (1,2), (3,6), (4,5) and (7,8), which refers to the first and second conductor, the third and sixth
conductor, the fourth and fifth conductor and the seventh and eighth conductor.

In a preferred embodiment of the invention, internal delays in the integrated switches of the IEDs can be eliminated by using the cable pair (4,5) for time synchronization and the pair (7,8) for broadcast. The pairs (1,2) and (3,6) can be reserved for actual data transmission. As described above, when the pair (4,5) is connected according to the invention and its preferred embodiments, it does not break at the IED; the synchronization signal can be connected directly from the input to the output with galvanic contact, and the signal can pass directly from one Ethernet connector to another. In this case, the time synchronization signal, such as the first clock signal provided by the clock master element, is not conveyed to the Ethernet switch (Figure 3: 3-8) but from one connector to another and to an FPGA element. Therefore, the synchronization signal is not processed between the IEDs or within an IED, and no element for processing the synchronization signal is required between the ports. Instead, the synchronization signal can be received from the preceding device on a first cable and forwarded to the next device on a second cable using the same pair (4,5). The IED can have an on/off switch for connecting the synchronization signal from one Ethernet connector to another or blocking the connection of the synchronization signal from one Ethernet connector to another, as described below in connection with Figure 3.

If the synchronization signals are daisy-chained from one Ethernet port to another, in a preferred embodiment the IEDs do not modify the signal in any way. This minimises the time delay within the chain, and the daisy-chaining does not cause any substantial delays between the first and the last IED. Furthermore, the embodiment in question provides a less complex structure. In other cases, potential delays caused by hardware might cause errors at the final end of the chain.

Each IED can also forward a synchronization pulse in the chain of devices 1-20, 1-22, 1-24 regardless of whether the device in question uses synchronization or not. Furthermore, the devices 1-6 ... 1-12 can be adapted to be compatible with a standard Ethernet. In this case, the inherent synchronization feature of the devices will be unavailable however.

According to another preferred embodiment, the IED contains an element such as a correlator element for processing the synchronization signal between the synchronization input and output. According to yet another
preferred embodiment, there is an element between the IEDs for processing the synchronization signal.

The first part of the time synchronization signal can also be conveyed to all IEDs by Ethernet broadcast substantially simultaneously.

As described above, in order to synchronize the IEDs the Ethernet ports of the IEDs can receive a time synchronization signal, such as a one-second pulse, and forward it to the next IED through an on/off switch for example. However, the Ethernet switch within the IED does not receive the time synchronization signal but may receive a data signal, for example as an Ethernet network message, for the purpose of coarse time synchronization.

As described above, according to the invention and its preferred embodiment, the synchronization pulse provided by the clock master element can be, for example, the 1 pps (pulse per second) pulse from the GPS system (Global Positioning System), which allows accurate synchronization of the device’s internal clock. The actual time data can be received through SNTP (Simple Network Time Protocol) or the IEEE 1588 Ethernet protocol, for example.

The purpose of the synchronization described above is to synchronize the sampling of measured quantities and/or a real-time clock, and synchronization can be used to compensate for bus delays between two IEDs, for example. When using a real-time clock, the synchronization tolerance must be in the order of a few milliseconds if synchronization is transmitted as an SNTP message.

Both the clock master element and one or more synchronization master elements in the network can receive different synchronization signals that can either be used for direct synchronization of the element or that can assist in the synchronization of the element. Synchronization can be implemented in one, two or several phases.

The synchronization master element can be the first device 1-6 in the chain 1-20, 1-22, 1-24 of IEDs 1-6, 1-8, 1-10, 1-12. The element can forward the synchronization signal to all other devices in the chain that are to be synchronized according to the invention and its preferred embodiments. The element providing timing for the IEDs, the synchronization master 1-6, can be synchronized using the IRIG-B (Inter-Range Instrumentation Group) time code standard used by the clock master element 1-4 and the SNTP time synchronization protocol provided by the clock master element 1-4, for
example. IRIG-B refers to a time code, a presentation of synchronization, and SNTP refers to a protocol according to which the time code can be decoded. Having received the synchronization pulses transmitted by the clock master element, the synchronization master element can forward the pulses and all of the other IEDs can accurately use them to synchronize themselves with each other.

In a certain embodiment the IRIG-B code is linked from one IED to another, and all devices must route it from one port to another and to the FPGA element within the device. If a certain device does not support the IRIG-B time code, it shall be located last in the chain.

Thus the synchronization of IEDs can be performed in two phases, for example by using an IEEE network message for coarse synchronization in the first phase. In the second phase, precise synchronization of the IED’s clock can be performed using the pps signal from a GPS device, for example. The time signal can also be coarsely transmitted in an SNTP message, after which the clock synchronization signal can be used to compensate for the asynchronicity of the IED’s clock. In other words, the synchronization signal coming from the bus can be, for example, a one-second pulse that indicates a full second without actual time data. The time data, which can include the date, hour, minute and second, can be received in an SNTP message, for example.

The SNTP signal can pass through an Ethernet switch, and the switch can route the signal to the IED’s CPU element (Central Processing Unit) and/or forward it from the next Ethernet port on the basis of the recipient address. The switch can ensure that the SNTP signal goes through the chain of IEDs from end to end. However, a network message does not provide accurate synchronization between the devices; this can be achieved using a synchronization signal for example. In a preferred embodiment each IED separately requests an SNTP signal being conveyed on the Ethernet, which is only required for the purpose of initially setting the clock.

Any sequence of pulses to which the IED can synchronize itself can be used for synchronization. Several pulses of different durations or frequencies can be used for synchronization. When using a one-second pulse, it must be ensured that the device’s local oscillator is able to maintain a sufficiently small time difference between the devices. An IRIG-B signal can also be used to achieve equal intervals between the edges of the synchronization signal, for example 10 milliseconds. In this case, the time data
can also be conveyed in the sequence. Synchronization between the devices must remain sufficiently accurate for this 10-millisecond duration. If even more precise synchronization is desired, a pulse sequence of 1 MHz can be used between the devices, for example.

When several IEDs are daisy-chained, the network message intended for synchronization, such as an SNTP message, IEEE 1588 message or a message provided by some other protocol, may have to queue in one or more devices, for example in the device's Ethernet switch, before the previous message in the line-up has left the IED. Only after this can the network message leave the IED for the next IED to assist in the synchronization of that IED. For this reason, the switch within an IED can also include queuing buffers. Such queuing can cause inaccuracy in message-based synchronization used in an Ethernet.

As described above, the invention and its preferred embodiment also enable daisy-chaining of devices with protocol-based time synchronization using Ethernet switches and a vacant pair of conductors (4,5) or the power supply pair of conductors in the cable. In this case, the IEDs must support the feature in question. Connections within the network can be provided using galvanic Ethernet cable, meaning that the pair can be galvanically forwarded in a device connected to the network so that all devices can listen to the same physical pair and receive synchronization pulses substantially simultaneously. The synchronization pulses can bypass the Ethernet switch, in which case other communications on the Ethernet bus do not affect the transmission of synchronization pulses.

Figure 2 illustrates daisy-chaining of a more extensive system according to the invention and one of its preferred embodiments. In this example, IEDs 2-2, 2-4, 2-6 and 2-8 in the first group 2-70 are daisy-chained to each other 2-20, 2-22, 2-24 and further daisy-chained 2-32 to a second daisy-chained 2-26, 2-28, 2-30 group 2-80 of IEDs 2-10, 2-12, 2-14, 2-16. The IEDs can be daisy-chained to each other using a galvanic Ethernet cable, for example, which can be a standard 100Base-TX cable, also known as fast 100 Mbps cable. Instead of galvanic cable, IEDs or groups of IEDs located at a long distance can be interconnected using fibre Ethernet, for example the 100Base-FX standard, which also represents a fast 100 Mbps cable. Such interconnection can reduce interference and asynchronicity of clocks between
different devices or groups of devices, as the clock signals to each group of devices can be received from the groups' own time synchronization sources.

When connecting more extensive systems to the daisy chain between IEDs and IED groups, a connection such as an optical fibre connection 2-32 can be used. If it is necessary to ensure that an interruption of the synchronization in the optical fibre does not interfere with device synchronization, a separate clock master element can be used for the subsequent devices. Thus the network may contain one or more clock master elements that can function, for example, solely as elements providing synchronization or also as IEDs. Instead of or in addition to clock master elements, the network may contain one or more synchronization master elements for synchronizing the IEDs. Both the clock master element and the synchronization master element can be located anywhere within the network or outside the network.

Therefore, a first group of devices 2-70, for example, may receive a time synchronization signal from a first time synchronization source 2-40, and a second group of devices 2-80 may receive a time synchronization signal from a second time synchronization source 2-50; the same synchronization signal, such as a GPS signal, can be conveyed to both time synchronization sources, for example from one or more clock master elements in the network. In this case, a time synchronization receiver, such as a GPS receiver, can be arranged in connection with the time synchronization source, also known as a synchronization device. The receiver can also be integrated in the device.

In other words, the clock master element 1-4, 2-40, 2-50 and/or one or more IEDs can be adapted to receive the signal transmitted by the GPS system and generate a first clock signal 1-26, 2-34, 2-36 at least partly based on said signal.

In Figure 2, element 2-40 represents a control and data acquisition device and a time synchronization source; the data and synchronization signal 2-36 provided by the element 2-40 can be conveyed, for example, to the first IED 2-2 in the IED group 2-70.

Figure 3 illustrates an IED 3-2 according to the invention and one of its preferred embodiments. The device comprises at least two elements, such as Ethernet ports 3-10, 3-12, that receive and forward communications from and to a LAN, such as an Ethernet. The switch 3-8 can be an Ethernet switch integrated in the IED that can route Ethernet communications, Ethernet
packets, from one port to another. The switch can be used for adapting the device for daisy-chaining with other IEDs.

The IED 3-2 that is to be synchronized can be implemented using a FPGA element 3-4 (Field Programmable Gate Array) that, for example, can receive time synchronization, such as the synchronization signal of a first clock signal, and synchronize voltage and current measurements. In other words, each IED connected to the network can include a clock module implemented by an FPGA element, for example, that can synchronize itself to a synchronization signal provided by a clock master element. The time synchronization pulse 3-20, 3-21, 3-22 can be conveyed to the FPGA element and forwarded from the FPGA element using the Ethernet ports 3-10 and 3-12. For example, the FPGA element can operate so that it does not modify the signal but can decide whether to forward the synchronization signal in the chain. If the next device does not support the synchronization signal, the synchronization signal is not routed to the outgoing port. The FPGA element can provide a real-time clock, the time generated by which can be forwarded, for example to a CPU element (Central Processing Unit) 3-6.

According to the invention and its preferred embodiments, the clock master element or an IED operating as a synchronization master element can generate the first clock signal 1-26, 2-34, 2-36. The first IED 1-6, 1-8, 1-10, 1-12, 2-2 ... 2-16 in the chain can be adapted to receive the first clock signal, which can be directly transmitted to the second IED 1-6, 1-8, 1-10, 1-12, 2-2 ... 2-16 regardless of whether the first IED uses the first clock signal or not.

Within the IED, the first clock signal can be conveyed to an FPGA element. It can be adapted to receive the first clock signal, to compare the time indicated by the first clock signal with the time indicated by the device's internal clock signal, a second clock signal, and, at least partly on the basis of said comparison, to modify the device's internal clock signal.

According to an alternative embodiment, the FPGA element is adapted to receive the first clock signal and use it as the device's internal, second clock signal 3-22.

Clock processing in the FPGA element must be programmed in accordance with the synchronization signal being used. This means that the synchronization signal cannot be freely chosen unless there is enough space on the FPGA element to process all of the methods described above. When the synchronization signal is conveyed to an FPGA element, the element must
be programmed to process the signal; the FPGA requires different types of processing for different types of signals. For example, if a one-second pulse is supplied to the FPGA element, the clock's second count must be at a sharp second and the millisecond count must be zero. If a one-kilohertz pulse is supplied, synchronization must be done in one millisecond, and the microsecond values must be zero. The programming of an FPGA element requires a certain number of logical elements, and the FPGA element can be programmed for different synchronization signals.

In addition to the synchronization signal, normal Ethernet communications, a data signal 3-30, 3-31, can pass to and from the IED and can be conveyed from the Ethernet ports to a switch 3-8. The data signal can be any Ethernet message containing data and having a certain Ethernet frame. The data signal can be a network message, such as an SNTP message, that can be routed through the Ethernet switch to the CPU element 3-6. Furthermore, the signal can be separated using the switch 3-8 and conveyed to a clock implemented using a FPGA element. One of the tasks of the switch 3-8 is indeed to contribute to the implementation of daisy-chaining.

There is a switch 3-14 between the Ethernet ports 1 and 2. It can be a mechanical switch, a solid state switch or a galvanic switch, for example, and can be used to break the forward route of the synchronization pulse; it is a so-called on/off switch for opening and/or closing the synchronization line. The switch 3-14 can also be implemented using a connection arrangement internal to the FPGA element.

When the IED is started, the FPGA element can drive the IED line to a certain state and verify whether device start-up is successful. For example, if the last device on the bus generates a potential of 0 V or 5 V on the line, which is different from the set voltage, it can be concluded that the device does not support the set voltage and thus the synchronization technology or synchronization signal being used. On the other hand, if the voltages settle to be substantially identical, the device supports the set voltage. If a third-party device not supporting the set voltage is connected to the chain, the line may break.

Thus the detection mechanism can be based, for example, in an arrangement in which the synchronization lines (4,5) are connected to the ground potential in devices that do not support synchronization. This allows the FPGA element to drive the line to the "1" state through a fairly high-resistance
pull-up resistor by active or internal pull-up. If the state of the line remains zero, it is known that the external device drives the line to the "0" state and that the device does not support synchronization. In this case, the FPGA element can break the chaining of the synchronization line from one Ethernet port to another using the switch 3-14 when the FPGA element is adapted to control this switch.

In Figure 3 the reference number 3-6 refers to the IED’s CPU (Central Processing Unit), which performs actual protection functions and can use the time stamp provided by the clock module. The clock can obtain the correct time from a synchronization message. Alternatively, the rising or falling edge of the synchronization pulse can be monitored.

Furthermore, a device according to Figure 3 can be fitted with automation that detects whether a device connected to the port supports synchronization technology. This can be tested by the FPGA element in the system for example. The unit can determine whether the most recently connected device has a synchronization function or not. This can be tested, for example, by detecting the presence of a termination resistor. This makes it possible to avoid compatibility problems with other devices. If a device does not support time synchronization, the lines can be connected to ground through a termination resistor for example. A device that does not support synchronization can be connected as the last device on the line. Detection can also be carried out using a data message and/or by software and/or using an identifier in memory for example.

Figure 4 illustrates synchronization signaling according to the invention and one of its preferred embodiments. At step 4-2, the time synchronization master element can transmit a synchronization signal to a first IED. The signal can be conveyed to the first port of the device and forwarded at step 4-4 directly to the device’s second Ethernet port and at step 4-6 to the FPGA element. The synchronization signal can also progress directly from the first port of the IED to the FPGA element.

Thus the IED can fetch a clock synchronization pulse and verify the clock of its own FPGA element by comparing it with the clock signal provided by the clock synchronization pulse. Once the signal has been transmitted to the second port of the first device, it can be directly chained to a second device at step 4-8 - that is, conveyed, transferred to the first port of the second IED. Next, the synchronization signal can proceed with the same steps as in the first
IED - at step 4-10 it can be further conveyed directly to the second port of the
second IED and at step 4-12 to the FPGA element of the second IED.

According to the invention and one of its preferred embodiments, at
steps 4-3 and/or 4-9 it can be verified whether the IED uses a synchronization
signal and if it does, the synchronization signal can be conveyed to the
device's FPGA element. If this is not the case, the synchronization signal can
be conveyed directly from the first device to the first port of the second device.

Figure 5 illustrates the flow of data signals according to the
invention and one of its preferred embodiments. At step 5-2, the data signal
can be conveyed to the IED, for example, from a second, preceding or next
IED connected to the bus, from a time synchronization device, or as control
and/or monitoring data from a SCADA element. In this case, the data can be
conveyed to the first Ethernet port 3-10 of the first IED. After this, the data
signal can be transmitted at step 5-4 to the switch 3-8, which can route the
signal to the FPGA element 3-6 at step 5-6. Next, at step 5-8 it can be verified
whether the data is addressed to the CPU element of this IED. This can be
done by verifying the MAC (Medium Access Control) address of the message
for example. If this is the case, the data can then be routed to the CPU
element of the device in question at step 5-10. If not, the data can then be
routed at step 5-12 to the next IED at step 5-14.

According to an alternative embodiment, a broadcast message can
be transmitted to all devices. This allows each IED to receive an Ethernet
message substantially simultaneously - that is, a broadcast message can
propagate in an Ethernet network.

According to yet another preferred embodiment of the invention, the
switching of the synchronization signal from one Ethernet port to another is
controlled by software in the CPU element and automatic detection can be
bypassed.

The advantage of a method and system according to the invention
and its preferred embodiments is that no separate wiring is required for the
time synchronization signal, which, together with a daisy-chaining facility, will
substantially reduce the need for wiring.

A further advantage is that the sphere of use of the invention will be
extended if the power supply conductor pair is used to communicate the
synchronization signal.
It is obvious to a person skilled in the art that the progress of technology will allow the fundamental idea of the invention to be implemented in many different ways. Thus the invention and its embodiments are not limited to the examples described above but may vary within the scope of the claims.
Claims

1. A module (1-6, 1-8, 1-10, 1-12, 2-2 ... 2-16, 3-2) for an automation data communications network, said module (1-6, 1-8, 1-10, 1-12, 2-2 ... 2-16, 3-2) comprising a LAN (Local Area Network) switch (3-8) and means (3-10, 3-12, 3-14) for receiving and transmitting a two-part time synchronization pulse in which the first and second part of the two-part time synchronization pulse jointly indicate time data so that:

- the module (1-6, 1-8, 1-10, 1-12, 2-2 ... 2-16, 3-2) is adapted to receive time data from the first part; and

- the module (1-6, 1-8, 1-10, 1-12, 2-2 ... 2-16, 3-2) is adapted to convey the second part past the module's Ethernet switch (3-8) and, in response to the second part, to synchronize itself with the time data indicated by the first part.

2. A module according to claim 1, characterized in that the module (1-6, 1-8, 1-10, 1-12, 2-2 ... 2-16, 3-2) is adapted to convey the first part through the module's LAN switch (3-8).

3. A module according to claim 1, characterized in that the module (1-6, 1-8, 1-10, 1-12, 2-2 ... 2-16, 3-2) is adapted to convey the first part past the module's LAN switch (3-8).

4. A module according to any of the preceding claims 1 to 3, characterized in that the module (1-6, 1-8, 1-10, 1-12, 2-2 ... 2-16, 3-2) is adapted to detect whether it supports the first part and/or second part of the time data (1-26, 2-34, 2-36), and if it does, the module (1-6, 1-8, 1-10, 1-12, 2-2 ... 2-16, 3-2) is adapted to receive the first part and/or second part of the time data.

5. A module (1-6, 1-8, 1-10, 1-12, 2-2 ... 2-16, 3-2) according to any of the preceding claims, characterized in that the forwarding of the time synchronization pulse and/or a part thereof is controlled by software in the CPU unit (3-6) of the module (1-6, 1-8, 1-10, 1-12, 2-2 ... 2-16, 3-2).

6. A module (1-6, 1-8, 1-10, 1-12, 2-2 ... 2-16, 3-2) according to any of the preceding claims, characterized in that the module (1-6, 1-8, 1-10, 1-12, 2-2 ... 2-16, 3-2) comprises a synchronization circuit (3-4) adapted to receive a time synchronization pulse (1-26, 2-34, 2-36), to compare the time indicated by the time synchronization pulse (1-26, 2-34, 2-36) with the time indicated by the device's internal clock signal (3-22), and, at least partly on the basis of said comparison, to modify the device's internal clock signal (3-22).
7. A module (1-6, 1-8, 1-10, 1-12, 2-2 ... 2-16, 3-2) according to any of the preceding claims, characterized in that the module (1-6, 1-8, 1-10, 1-12, 2-2 ... 2-16, 3-2) comprises a synchronization circuit (3-4) adapted to receive a time synchronization pulse (1-26, 2-34, 2-36) and use it as the internal clock signal (3-22) of the module (1-6, 1-8, 1-10, 1-12, 2-2 ... 2-16, 3-2).

8. A module (1-6, 1-8, 1-10, 1-12, 2-2 ... 2-16, 3-2) according to any of the preceding claims, characterized in that the LAN switch is an Ethernet switch.

9. A module (1-6, 1-8, 1-10, 1-12, 2-2 ... 2-16, 3-2) according to any of the preceding claims, characterized in that it comprises means for transmitting and/or receiving a time synchronization pulse (1-26, 2-34, 2-36) as a separate signal.

10. A module (1-6, 1-8, 1-10, 1-12, 2-2 ... 2-16, 3-2) according to any of the preceding claims, characterized in that it comprises means for transmitting and/or receiving a time synchronization pulse (1-26, 2-34, 2-36) using the vacant pairs of conductors in a standard Ethernet cable.

11. A module (1-6, 1-8, 1-10, 1-12, 2-2 ... 2-16, 3-2) according to any of the preceding claims, characterized in that it comprises means for transmitting and/or receiving a time synchronization pulse (1-26, 2-34, 2-36) using the pairs of conductors intended for supplying power in accordance with the Power Over Ethernet standard.

12. A module (1-6, 18, 1-10, 1-12, 2-2 ... 2-16, 3-2) according to any of the preceding claims, characterized in that it comprises means for receiving the second part (1-26, 2-34, 2-36) of a time synchronization pulse (1-26, 2-34, 2-36) as a broadcast message.

13. A module (1-6, 1-8, 1-10, 1-12, 2-2 ... 2-16, 3-2) according to any of the preceding claims, characterized in that the module (1-6, 1-8, 1-10, 1-12, 2-2 ... 2-16, 3-2) is adapted to receive a signal transmitted by the GPS system and, at least partly based on said signal, to generate a time synchronization pulse (1-26, 2-34, 2-36) and/or an internal clock signal (3-22).

14. A module (1-6, 18, 1-10, 1-12, 2-2 ... 2-16, 3-2) according to any of the preceding claims, characterized in that it comprises means for receiving and/or transmitting the first part of a time synchronization pulse (1-26, 2-34, 2-36) as an SNTP message or in accordance with the IEEE 1588 Ethernet protocol.
15. A module (1-6, 18, 1-10, 1-12, 2-2 ... 2-16, 3-2) according to any of the preceding claims, characterized in that the second part (1-26, 2-34, 2-36) of the time synchronization pulse is a one-second pulse or a 1 MHz pulse sequence.

16. A module (1-6, 18, 1-10, 1-12, 2-2 ... 2-16, 3-2) according to any of the preceding claims; characterized in that the module is an IED (Integrated Electronic Device).

17. An automation data communications network, said network comprising a clock master element (1-4, 2-40, 2-50) for generating a time synchronization pulse (1-26, 2-34, 2-36), characterized in that the network further comprises at least a first and a second daisy-chained module (1-6, 1-8, 1-10, 1-12, 2-2 ... 2-16, 3-2), said module (1-6, 1-8, 1-10, 1-12, 2-2 ... 2-16, 3-2) comprising a LAN (Local Area Network) switch (3-8) and means (3-10, 3-12, 3-14) for receiving and transmitting a two-part time synchronization pulse, in which the first and second part of the two-part time synchronization pulse jointly indicate time data so that the module (1-6, 1-8, 1-10, 1-12, 2-2 ... 2-16, 3-2) is adapted to receive time data from the first part and to convey the first part through the module's LAN switch (3-8), and the module (1-6, 1-8, 1-10, 1-12, 2-2 ... 2-16, 3-2) is adapted to convey the second part past the module's LAN switch (3-8) and, in response to the second part, to synchronize itself with the time data indicated by the first part.

18. A network according to claim 17, characterized in that the first module (1-6, 1-8, 1-10, 1-12, 2-2 ... 2-16, 3-2) is adapted to transmit a time synchronization pulse (1-26, 2-34, 2-36) directly to the second module (1-6, 1-8, 1-10, 1-12, 2-2 ... 2-16, 3-2) regardless of whether the first module (1-6, 1-8, 1-10, 1-12, 2-2 ... 2-16, 3-2) uses the time synchronization pulse (1-26, 2-34, 2-36) or not.

19. A network according to claim 17 or 18, characterized in that the module (1-6, 1-8, 1-10, 1-12, 2-2 ... 2-16, 3-2) is adapted to detect whether it supports the first part and/or second part of the time synchronization pulse (1-26, 2-34, 2-36), and if it does, the module (1-6, 1-1, 1-10, 1-12, 2-2 ... 2-16, 32) is adapted to receive the first and/or second part of the time synchronization pulse (1-26, 2-34, 2-36).

20. A network according to any of the preceding claims, characterized in that the switching of the time synchronization pulse (1-26, 2-34, 2-36) or a part thereof from one module (1-6, 1-8, 1-10, 1-12, 2-2 ...
2.16, 3-2) to another is controlled by software in the CPU unit (3-6) of the module.

21. A method for synchronizing an automation data communications network, said network comprising at least a first and a second daisy-chained module (1-6, 1-8, 1-10, 1-12, 2-2 ... 2-16, 3-2) and said module (1-6, 1-8, 1-10, 1-12, 2-2 ... 2-16, 3-2) comprising a LAN switch (3-8), characterized by

- receiving and transmitting a two-part time synchronization pulse in which the first and second part of the two-part time synchronization pulse jointly indicate time data;

- receiving time data from the first part and conveying the first part through the module’s LAN (Local Area Network) switch (3-8); and

- conveying the second part past the module’s LAN switch and, in response to the second part, synchronizing the module (1-6, 1-8, 1-10, 1-12, 2-2 ... 2-16, 3-2) with the time data indicated by the first part.

22. A method according to claim 21, characterized by communicating the time synchronization pulse or a part thereof directly to the second module regardless of whether the time synchronization pulse is used to synchronize the first module or not.
INTERNATIONAL SEARCH REPORT

International application No
PCT/FI2006/050297

A. CLASSIFICATION OF SUBJECT MATTER

INV. H04J3/06 H04L7/00 H04L12/26

According to international Patent Classification (IPC) or to both national classification and IPC.

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H04L H04J

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and where practical search terms used)

EPO-Internal

C. DOCUMENTS CONSIDERED TO BE RELEVANT

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<td>WO 02/49275 A2 (IP ACCESS LTD [GB]; PIERCY NEIL PHILIP [GB]; JOHNSON NICHOLAS DOUGALL) 20 June 2002 (2002-06-20) abstract; claims 1-5,8-10,12-20; figures 1-3 page 3, line 1 - page 4, line 18 page 5, line 12 - line 25</td>
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Date of the actual completion of the international search
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**INTERNATIONAL SEARCH REPORT**

**INTERNATIONAL SEARCH REPORT**

International application No
PCT/FI2006/050297

C(Continuation)

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