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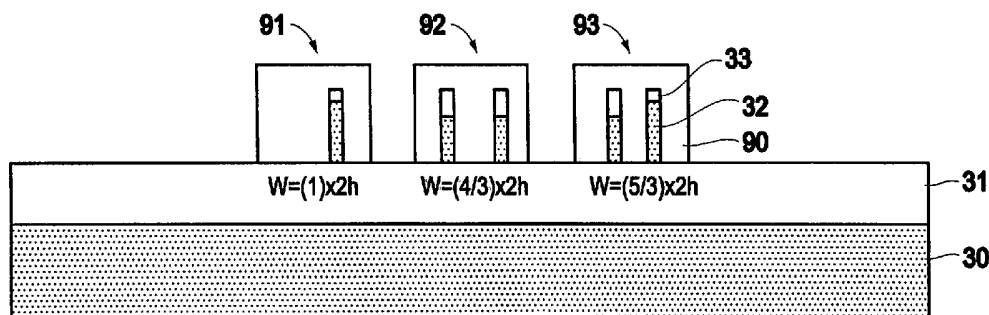
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(54) Title: MULTI-HEIGHT FINFETS



(57) Abstract: The present invention provides a FinFET device that has a first fin and a second fin. Each fin has a channel region and source and drain regions that extend from the channel region. The fins have different heights. The invention has a gate conductor positioned adjacent the fins. The gate conductor runs perpendicular to the fins and crosses the channel region of each of the first fin and second fin. The fins are parallel to one another. The ratio of the height of the first fin to the height of the second fin comprises a ratio of one to 2/3. The ratio is used to tune the performance of the transistor and determines the total channel width of the transistor.

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INTERNATIONAL SEARCH REPORT

International application No.

PCT/US04/02647

A. CLASSIFICATION OF SUBJECT MATTER

IPC(7) : H01L 21/8238, 29/772

US CL : 257/327; 438/151

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S. : 257/208, 270, 315, 316, 327, 329, 347, 348,3 49, 350, 618, 628; 438/151, 156, 157, 199, 212, 283, 286, 585

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

INSPEC; IEEE

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X, E ---	US 2004/0110331 A1 (YEO et al.) 10 June 2004 (10.06.2004), figures 5-10, paragraphs 0004-0009, 0037-0048.	1, 3-15 -----
Y, E		16-22
Y	HUANG, XEUJUE et al. Sub-50 nm P-Channel FinFET IEEE Transactions on Electron Devices, May 2001, Vol 48 No. 5 pages 881-882.	16-22
A	YU, BIN et al. FinFET Scaling to 10 nm Gate Length Electron Devices Meeting, 2002. IEDM '02 Digest. Dec. 2002.	1-22
A	KEDZIERSKI, JAKUB et al. High-performance symmetric-gate and CMOS-compatible Vt asymmetric-gate FinFET devices. Electron Devices Meeting, 2001. IEDM Technical Digest. Dec. 2001.	1-22
A	US 6,413,802 B1 (HU et al.) 02 July 2002 (02.07.2002).	1-22
A	US 4,996,574 B (SHIRASAKI) 26 February 1991 (26.02.1991).	1-22

Further documents are listed in the continuation of Box C.

See patent family annex.

* Special categories of cited documents:	"T"	later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"A" document defining the general state of the art which is not considered to be of particular relevance	"X"	document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
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"O" document referring to an oral disclosure, use, exhibition or other means		
"P" document published prior to the international filing date but later than the priority date claimed		

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C. (Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT		
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A, P	US 6,657,259 B2 (FRIED et al.) 02 December 2003 (02.12.2003).	1,2
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