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(54) Title: FABRICATION OF SOLID-STATE DEVICES HAVING THIN DIELECTRIC LAYERS (57) Abstract Certain devices require a high quality thin (< 25 nanometer) dielectric layer formed on a deposited silicon layer. Applications include capacitor dielectrics in dynamic memories and linear devices. In another application, an electrically erasable programmable read only memory (EEPROM) uses an SiO₂ layer between the write gate and the floating gate. The present technique oxidizes amorphous silicon under conditions that suppress grain growth to produce a higher quality oxide than that achieved with conventional furnace oxidation of polysilicon. Rapid thermal oxidation is one method of practicing the technique.		

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FABRICATION OF SOLID-STATE DEVICES
HAVING THIN DIELECTRIC LAYERS

Background of the Invention

1. Field of the Invention

The present invention relates to solid state devices and particularly to a method for producing such devices including a thin layer of silicon dioxide as a dielectric.

2. Description of the Prior Art

Numerous applications exist in the semiconductor art for thin layers (i.e., <25 nanometers) of silicon dioxide, e.g., as capacitor and gate electrode dielectric layers. While numerous techniques exist for producing such layers, the present invention is directed to a novel technique producing improved results.

Summary of the Invention

We have invented a technique for forming a thin silicon dioxide layer wherein amorphous silicon is oxidized under conditions that maintain at least a surface portion of the silicon amorphous as it is undergoing oxidation to form silicon dioxide. The amorphous silicon is typically formed by chemical vapor deposition at a sufficiently low temperature to ensure the amorphicity of the silicon as deposited. A conductivity-enhancing dopant, at a concentration of typically at least one weight percent, may be optionally included in the deposited material, preferably by co-deposition with the amorphous silicon.

Detailed Description

The following detailed description relates to an improved technique for growing silicon dioxide layers on deposited silicon. The inventive technique results from our discovery that grown SiO_2 layers of improved dielectric quality are obtained when the deposited silicon is amorphous, and the oxidation of the amorphous silicon is rapidly accomplished, or otherwise accomplished to prevent conversion of at least a surface portion of the amorphous silicon to polysilicon. Application of the present technique to the production of integrated circuits

and other solid state devices is possible. Silicon is considered to be amorphous when only short-range order is present at the atomic level, with any resulting grains having a size of less than 1 nanometer, as determined by x-ray or electron diffraction techniques known in the art. The effectiveness of the foregoing
5 combination of conditions is illustrated by means of the following Examples.

EXAMPLE I

In a first series of experiments, the breakdown voltage of oxidized polysilicon having various doping levels was determined. For this purpose, 400 nanometers of undoped polysilicon was deposited on a 100 nanometer thick
10 layer of SiO_2 that had been grown on each of six silicon wafers, each 5 inches in diameter. The polysilicon was deposited by a low pressure chemical vapor deposition (CVD) reaction of SiH_4 at a temperature in the range of 580 to 590 degrees C, and was in a semi-amorphous state as deposited. Two of the wafers were then exposed to PBr_3 gas at a temperature of 950 degrees C for 10
15 minutes, resulting in a doping of the polysilicon with 1.5 weight percent of phosphorus. Two other wafers were similarly exposed for 20 minutes, producing a 2 weight percent phosphorus doping, and the last two wafers were exposed for 30 minutes, producing a 2.2 weight percent doping. In all cases, the exposure to the elevated temperatures during doping caused the silicon to convert to the
20 polycrystalline state.

Three of the wafers, one at each doping level, were furnace oxidized in an atmosphere of 10% O_2 , 90% Ar, and 0.1% $\text{C}_2\text{H}_3\text{Cl}_3$ at 950 degrees C for a period of 18 minutes, producing a SiO_2 layer about 17 nanometers thick on the surface of the polysilicon layer on each wafer. Another three of the wafers, one at each
25 doping level, were rapidly oxidized by exposure to O_2 for 85 seconds at a temperature of 1000 degrees C, which was produced by a tungsten-halogen flashlamp. This produced a layer of SiO_2 about 20 nanometers thick on the polysilicon surface of each wafer. A second layer of polysilicon 340 nanometers thick, and doped with about 1 weight percent phosphorus, was deposited on the
30 foregoing 20 nanometer grown SiO_2 layer on each of the six wafers. This second polysilicon layer was patterned to form electrodes, and an electric voltage applied to each of the polysilicon layers, thereby producing an electric field across the 20 nanometer grown SiO_2 layer.

The breakdown voltage, and hence breakdown field, was determined for each grown SiO_2 layer of each wafer; the results are presented in Table 1. Note that the breakdown field did not exceed 5.5 megavolts per centimeter of film thickness, and decreased significantly at the highest dopant concentration.

5

TABLE 1

Breakdown Field for Oxidized Polysilicon

Phosphorus concentration (weight percent)		Breakdown field (MV/cm)	
		Furnace Oxidation	Rapid Oxidation
10	1.5	5.4	4.0
	2.0	5.5	5.4
	2.2	1.7	1.4

EXAMPLE II

This Example illustrates the improved dielectric films made according to one embodiment of the inventive technique. Four silicon wafers had formed thereon a 100 nanometer thick layer of silicon dioxide. Deposited on the oxide layer of each wafer was 400 nanometers of amorphous silicon that was in-situ doped with phosphorus by co-deposition of the silicon and phosphorus. The deposition was accomplished by low pressure chemical vapor deposition, using SiH_4 and PH_3 as the source gases, and a small amount of N_2 to reduce the formation of large particles. (The use of other source gases is possible.) The deposition temperature of 570 degrees C was low enough to ensure the amorphous state of the silicon as deposited. (Chemical vapor deposition temperatures below about 580 to 590 degrees C typically results in amorphous silicon.) The deposition rate, of a pressure of 1 Torr (1mm of H_g), was 6.5 nanometers/minute. This allowed a relatively short deposition period, which

prevented recrystallization of the amorphous silicon at the bottom of the film. A first two of the wafers were doped with 1.5 weight percent phosphorus, and a second two were doped with 2.4 weight percent phosphorus, by this procedure. The deposited silicon was maintained in the amorphous state following
 5 deposition.

The deposited amorphous silicon on two of the wafers, one at each doping level, was furnace oxidized as above, producing oxide thicknesses averaging about 19 nanometers. The deposited amorphous silicon on the remaining two of the wafers, one at each doping level, was rapidly oxidized as
 10 above, producing oxide thicknesses averaging about 23 nanometers. Each wafer then had a doped polysilicon top layer deposited on the grown oxide layer, and patterned to serve as an electrode as above.

The resulting breakdown fields were determined as above, and the results are shown in Table 2.

15

TABLE 2

Breakdown Field for Oxidized Amorphous Silicon

	Phosphorus concentration (weight percent)	Breakdown Field (MV/cm)	
		Furnace Oxidation	Rapid Oxidation
20	1.5	6.6	8.5
	2.5	5.8	8.8

It can be seen that the combination of rapid oxidation and amorphous silicon results in an oxide having significantly improved quality as compared to silicon dioxide films produced by the prior art technique of furnace oxidation of
 25 polysilicon, and is also superior to both rapid oxidation of polysilicon and furnace oxidation of amorphous silicon. This is due to improved surface smoothness of the rapidly oxidized amorphous silicon. Note that the improvement is especially significant at relatively high dopant concentrations;

i.e., above about 2 weight percent for phosphorus as the dopant. The deposited amorphous silicon layer may be oxidized through its entire thickness by the present technique, or alternately only a surface portion may be oxidized. During the above rapid oxidation process, the amorphous silicon material underlying
5 the surface portion became polycrystalline. If the surface portion is sufficiently oxidized before grain growth of the silicon material occurs, the improved dielectric properties are obtained largely independently of subsequent grain growth in the underlying material. Transmission electron microscope pictures of the underlying silicon show that the resulting silicon grains are much more
10 uniform when the surface of amorphous silicon is rapidly oxidized as compared to the case when the surface of polysilicon is oxidized under either of the foregoing rapid or furnace oxidation conditions. Note also that even though it is known that higher temperatures tend to promote grain growth, the "rapid oxidation" (at 1000 degrees C) was so much shorter in duration than the
15 "furnace oxidation" (at 950 degrees C) in this Example that improved dielectric quality was obtained. This is due to the rapidly oxidized surface forming a SiO_2 "cap" that maintained surface smoothness even as some grain growth in the underlying silicon occurred.

In general, "rapid oxidation" as used herein means performing the
20 oxidation in less than 5 minutes, as may be accomplished in a flashlamp heater apparatus. In accomplishing the rapid oxidation, the temperature ramp-up should provide for a heating rate that makes the transition from a relatively low temperature (e.g., 600 degrees C) to an oxidizing temperature in excess of 950 degrees C, in less than 5 minutes. A typical radiant heater (e.g., flashlamp)
25 produces this transition in less than 1 minute, and typically only a few seconds, even when starting from room temperature. This rapid transition helps avoid significant polysilicon grain growth prior to forming the oxide "cap". The time at maximum temperature is also less than 5 minutes, and in a typical case less than 2 minutes. The ramp-down of the temperature may then be relatively long
30 if desired, since the oxide "cap" will have formed, and will maintain surface smoothness even if some further polysilicon grain growth occurs during ramp-down, or in subsequent heating steps. The maximum temperature is typically in excess of 950 degrees C for a dry oxygen ambient at atmospheric pressure. However, the use of a steam oxidizing ambient and/or increased pressure may

be used to reduce the maximum temperature required. The addition of other oxidizing agents (e.g., chlorine or fluorine) may also reduce the times or temperatures required. A plasma atmosphere comprising oxygen may be used to assist the oxidation process; see, e.g., U.S. patents 4,062,747 and 4,300,989 co-

5 assigned herewith. These techniques may thus be used to reduce the oxidation temperature sufficiently so that polysilicon grain formation (from the amorphous silicon) is retarded until after the surface portion is oxidized. The oxidation times may then be longer than those used for "rapid oxidation", and still achieve improved dielectric quality as compared to oxidation of polysilicon.

10 For example, plasma assisted oxidation of silicon at temperatures below 600 degrees C is known in the art. As applied to the present technique, the use of a relatively low oxidizing temperature provides for reducing (or even eliminating) the rate of polysilicon grain formation and growth, while still allowing oxidation of the amorphous silicon to a usable thickness (e.g., greater than 5 nanometers).

15 Although deposition of amorphous silicon has been illustrated above, the amorphous silicon may be formed by other techniques. For example, a layer of deposited polysilicon may be rendered amorphous by ion beam damage. The ion species may be, for example, an inert gas (e.g., argon), or a dopant used to enhance the conductivity of the silicon. However, in some cases, only a surface

20 portion of the polysilicon need be amorphized thereby, for the reasons noted above. We recommend that the amorphous surface portion be at least 10 nanometers thick prior to the oxidizing, to help ensure the benefits noted herein. The oxidizing typically proceeds to produce a thickness of the silicon dioxide of at least 3 nanometers. The oxidizing typically is terminated before

25 oxidizing the entire thickness of the deposited silicon, but the entire thickness may be oxidized if desired. If the oxidizing is accomplished at a sufficiently low temperature (e.g., less than about 580 degrees C), than the entire thickness of the silicon layer can remain amorphous during the oxidation process, assuming it was in that state prior to oxidation. Exposure to higher temperatures (e.g.,

30 greater than about 590 degrees C) during subsequent processing operations may then cause polysilicon grain formation in the silicon underneath the oxidized surface region. For reasons as noted above, the oxidized surface "cap" results in improved surface smoothness, and increased electric breakdown field, in that case also.

It can be seen from the above Examples that the present techniques produces an oxide layer having an electric breakdown field of typically over 8 megavolts per centimeter. In a typical case, it appears that the electric breakdown field of SiO_2 formed by the inventive technique is at least 10 percent
5 greater than for an equally thick layer of SiO_2 grown on polysilicon, under comparable oxidizing conditions (e.g., the same times, temperatures, and oxidizing ambient). Other operations known in the art (e.g., growing or depositing silicon nitride on the silicon dioxide) may be used to further improve various properties of the layer formed by the present technique.

Claims

1. A method of making a solid state device by steps comprising depositing a layer of silicon and oxidizing at least a portion of said layer,
CHARACTERIZED in that
 - 5 at least a surface portion of said layer is amorphous silicon, and said oxidizing is accomplished by heating the amorphous silicon in an ambient comprising oxygen for a time sufficiently short and a temperature sufficiently low to suppress the formation of polysilicon grains in said surface portion at least during an initial portion of said oxidizing, whereby a layer of silicon
10 dioxide having an increased electric breakdown field is obtained.
 2. The method of claim 1 wherein said amorphous silicon is in the amorphous state as deposited at a temperature of less than 580 degrees C.
 3. The method of claim 1 wherein said amorphous silicon is formed by ion-beam damage of deposited polycrystalline silicon.
 - 15 4. The method of claim 1 wherein said amorphous silicon includes at least 1 weight percent of a conductivity-enhancing dopant that is co-deposited with said layer of silicon.
 5. The method of claim 1 wherein said amorphous silicon includes at least 2 weight percent of a conductivity-enhancing dopant.
 - 20 6. The method of claim 5 wherein said dopant is phosphorus.
 7. The method of claim 1 wherein the entire thickness of the deposited silicon layer is oxidized by said oxidizing.
 8. The method of claim 1 wherein only a surface portion of said layer is oxidized by said oxidizing, and the portion of said layer underlying said surface
25 portion is polysilicon following said oxidizing.
 9. The method of claim 1 wherein the oxidized portion of said layer has a thickness of less than 25 nanometers.
 10. The method of claim 1 wherein said heating occurs at a rate that increases the temperature of said layer from 600 degrees C to 950 degrees C in a
30 time of less than 5 minutes.
 11. The method of claim 10 wherein said heating maintains said layer at a temperature in excess of 950 degrees C for a time of less than 5 minutes.

12. The method of claim 1 wherein the oxidized portion of said layer has a thickness of at least 3 nanometers.

AMENDED CLAIMS

[received by the International Bureau on 21 July 1987 (21.07.87);
original claims 1-12 replaced by new claims 1-14 (2 pages)]

1. A method of making a solid state device by steps comprising depositing a layer of silicon and oxidizing at least a portion of said layer.

CHARACTERIZED in that

5 said layer is amorphous silicon, and said oxidizing is accomplished by continually increasing the temperature of the amorphous silicon from less than 600 degrees C to at least 950 degrees C in an ambient comprising oxygen for a time sufficiently short to oxidize a surface portion of said layer before the underlying portion of said amorphous silicon is converted to polysilicon, whereby a smooth
10 layer of silicon dioxide having an increased electric breakdown field is obtained on a layer of polysilicon.

2. The method of claim 1 wherein said amorphous silicon is in the amorphous state as deposited at a temperature of less than 530 degrees C.

3. The method of claim 1 wherein said amorphous silicon is formed
15 by ion-beam damage of deposited polycrystalline silicon.

4. The method of claim 1 wherein said amorphous silicon includes at least 1 weight percent of a conductivity-enhancing dopant that is co-deposited with said layer of silicon.

5. The method of claim 1 wherein said amorphous silicon includes at
20 least 2 weight percent of a conductivity-enhancing dopant.

6. The method of claim 5 wherein said dopant is phosphorus.

7. The method of claim 1 wherein the oxidized portion of said layer has a thickness of less than 25 nanometers.

8. The method of claim 1 wherein said layer as oxidized by said
25 oxidizing comprises a dielectric layer of a capacitor.

9. The method of claim 1 wherein said layer as oxidized by said oxidizing comprising a gate dielectric of an insulated gate field effect transistor.

10. The method of claim 1 wherein said heating occurs at a rate that increases the temperature of said layer from 600 degrees C to 950 degrees C in a
30 time of less than 5 minutes.

11. The method of claim 10 wherein said heating maintains said layer at a temperature in excess of 950 degrees C for a time of less than 5 minutes.

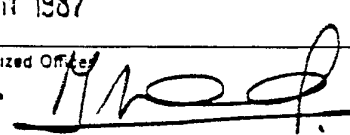
12. The method of claim 1 wherein the oxidized portion of said layer has a thickness of at least 3 nanometers.

13. The method of claim 1 wherein the electric breakdown field of said layer of silicon dioxide is at least 3 megavolts per centimeter.

14. The method of claim 1 wherein the electric breakdown field of said layer of silicon dioxide is at least 10 percent greater than the electric
5 breakdown field of a layer of silicon dioxide of the same thickness grown on polysilicon under comparable oxidizing conditions.

INTERNATIONAL SEARCH REPORT

International Application No PCT/US 87/00272

I. CLASSIFICATION OF SUBJECT MATTER (if several classification symbols apply, indicate all) *		
According to International Patent Classification (IPC) or to both National Classification and IPC		
IPC ⁴ : H 01 L 21/28; H 01 L 21/316		
II. FIELDS SEARCHED		
Minimum Documentation Searched ⁷		
Classification System	Classification Symbols	
IPC ⁴	H 01 L	
Documentation Searched other than Minimum Documentation to the Extent that such Documents are Included in the Fields Searched ⁸		
III. DOCUMENTS CONSIDERED TO BE RELEVANT ⁹		
Category *	Citation of Document, ¹¹ with indication, where appropriate, of the relevant passages ¹²	Relevant to Claim No. ¹³
A	Journal of the Electrochemical Society, volume 133, no. 2, February 1986, (Manchester, US), C.Y. Lu et al.: "Thermal oxidation of undoped LPCVD polycrystalline silicon films", pages 446-447 see page 446, column 1, paragraph 2 - page 447, column 2, paragraph 1; figure 1	1,2,10,11
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A	Proceedings of the IEEE International Conference on Circuits and Computers ICCC '80, 1-3 October 1980, IEEE, (New York, US), N. Tsubouch et al.: "The application of high pressure oxidation process to fabrication of MOS LSI", pages 461-464 see page 462, column 1, paragraph 2 - paragraph 8	1,4-6,10,11
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A	FR, A, 2536208 (RCA) 18 May 1984 see claims 1-8	1,2,4-6,8, 10,11
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	./.	
* Special categories of cited documents: ¹⁰ "A" document defining the general state of the art which is not considered to be of particular relevance "E" earlier document but published on or after the international filing date "L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified) "O" document referring to an oral disclosure, use, exhibition or other means "P" document published prior to the international filing date but later than the priority date claimed "T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention "X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step "Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art. "&" document member of the same patent family		
IV. CERTIFICATION		
Date of the Actual Completion of the International Search		Date of Mailing of this International Search Report
28th April 1987		- 3 JUN 1987
International Searching Authority		Signature of Authorized Officer
EUROPEAN PATENT OFFICE		M. VAN MOL 

III. DOCUMENTS CONSIDERED TO BE RELEVANT (CONTINUED FROM THE SECOND SHEET)		
Category *	Citation of Document, with indication, where appropriate, of the relevant passages	Relevant to Claim No
A	IEEE Transactions on Electron Devices, volume ED-32, no. 3, March 1985, (New York, US), L. Faraone et al.: "Characterization of thermally oxidized n ⁺ poly- crystalline silicon", pages 577-583 see table I; page 579, column 2, paragraph 1	1-3,5,6, 10,11
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A	Proceedings of the International Electron Devices Meeting, 1-4 December 1985, IEEE, (New York, US), T. Warabisako et al.: A 600° C process for MOSFET fabrication using micro- wave plasma-stream gate oxidation", see pages 216-219	
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A	Proceedings of the International Electron Devices Meeting, 1-4 December 1985, IEEE, (New York, US), T. Ono et al.: "Studies of thin poly Si oxides for E and E ² PROM", see pages 380-383	
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A	Extended Abstracts of the Journal of the Electrochemical Society, volume 81-1, May 1981, S.K. Lai: "Very thin gate insulators", see page 541	

ANNEX TO THE INTERNATIONAL SEARCH REPORT ON

INTERNATIONAL APPLICATION NO.

PCT/US 87/00272 (SA 16198)

This Annex lists the patent family members relating to the patent documents cited in the above-mentioned international search report. The members are as contained in the European Patent Office EDP file on 15/05/87

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Patent document cited in search report	Publication date	Patent family member(s)	Publicati date
FR-A- 2536208	18/05/84	SE-A- 8306071	13/05/84
		DE-A- 3340583	17/05/84
		JP-A- 59103347	14/06/84
		GB-A,B 2131407	20/06/84

For more details about this annex :

see Official Journal of the European Patent Office, No. 12/82