

(19) World Intellectual Property Organization
International Bureau



(43) International Publication Date
6 November 2008 (06.11.2008)

PCT

(10) International Publication Number
WO 2008/134396 A1

(51) International Patent Classification:
GI1C 16/10 (2006.01) *GI1C 16/34* (2006.01)

(21) International Application Number:
PCT/US2008/061376

(22) International Filing Date: 24 April 2008 (24.04.2008)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
11/739,732 25 April 2007 (25.04.2007) US

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(81) Designated States (unless otherwise indicated, for every kind of national protection available): AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BR, BW, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RS, RU, SC, SD, SE, SG, SK, SL, SM, SV, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States (unless otherwise indicated, for every kind of regional protection available): ARIPO (BW, GH, GM, KE, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MT, NL, NO, PL, PT, RO, SE, SI, SK, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Published:

- with international search report
- before the expiration of the time limit for amending the claims and to be republished in the event of receipt of amendments

(54) Title: PROGRAMMING AND/OR ERASING A MEMORY DEVICE IN RESPONSE TO ITS PROGRAM AND/OR ERASE HISTORY

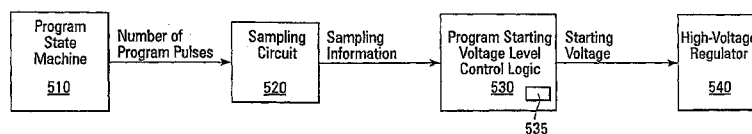


FIG. 5

(57) Abstract: For one embodiment, a program starting voltage of one or more program pulses applied to one or more memory cells (308) is in response, at least in part, to a number of program pulses previously required to program the one or more memory cells and/or an erase starting voltage of one or more erase pulses applied to one or more memory cells (308) is based on a number of erase pulses previously required to erase the one or more memory cells (308). For another embodiment, the adjustment of a program starting voltage level and/or an erase starting voltage level of one or more program and/or erase pulses applied to one or more memory cells (308) is in response, at least in part, to a number of program/erase cycles previously applied to the one or more memory cells (308).



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PROGRAMMING AND/OR ERASING A MEMORY DEVICE IN RESPONSE TO ITS PROGRAM AND/OR ERASE HISTORY

FIELD

5 The present disclosure relates generally to memory devices and in particular the present disclosure relates to programming and/or erasing a memory device in response, at least in part, to its program and/or erase history.

BACKGROUND

10 Memory devices are typically provided as internal, semiconductor, integrated circuits in computers or other electronic devices. There are many different types of memory including random-access memory (RAM), read only memory (ROM), dynamic random access memory (DRAM), synchronous dynamic random access memory (SDRAM), and flash memory.

15 Flash memory devices have developed into a popular source of non-volatile memory for a wide range of electronic applications. Flash memory devices typically use a one-transistor memory cell that allows for high memory densities, high reliability, and low power consumption. Changes in threshold voltage of the cells, through programming of charge storage or trapping layers or other physical phenomena, determine the data value of
20 each cell. Common uses for flash memory include personal computers, personal digital assistants (PDAs), digital cameras, digital media players, cellular telephones, and removable memory modules.

 A NAND flash memory device is a common type of flash memory device, so called for the logical form in which the basic memory cell configuration is arranged.
25 Typically, the array of memory cells for NAND flash memory devices is arranged such that the control gate of each memory cell of a row of the array is connected to a word line. Columns of the array include strings (often termed NAND strings) of memory cells connected together in series, source to drain, between a pair of select lines, a source select line and a drain select line. The source select line includes a source select gate at each
30 intersection between a NAND string and the source select line, and the drain select line includes a drain select gate at each intersection between a NAND string and the drain select

line. The select gates are typically field-effect transistors. Each source select gate is connected to a source line, while each drain select gate is connected to a column bit line.

The memory array is accessed by a row decoder activating a row of memory cells by selecting the word line connected to a control gate of a memory cell. In addition, the word lines connected to the control gates of unselected memory cells of each string are driven to operate the unselected memory cells of each string as pass transistors, so that they pass current in a manner that is unrestricted by their stored data values. Current then flows from the column bit line to the source line through each NAND string via the corresponding select gates, restricted only by the selected memory cells of each string. This places the current-encoded data values of the row of selected memory cells on the column bit lines.

For some applications, flash memory uses a single bit per cell. Each cell is characterized by a specific threshold voltage, which is sometimes referred to herein as a V_t level. Within each cell, two or more possible V_t levels exist. These V_t levels are controlled by the amount of charge that is stored on the floating gate. For some NAND architectures, for example, a memory cell might have a V_t level greater than zero in a programmed (or logic zero) state and a V_t level less than zero in an erase state. As used herein, a program V_t refers to a V_t level of a memory cell in a programmed state, and an erase V_t refers to a V_t level of a memory cell in an erase state.

Memory cells are typically programmed using program/erase cycles, e.g., where such a cycle might involve first erasing a memory cell and then programming the memory cell. For a NAND array, a block of memory cells is typically erased by grounding all of the word lines in the block and applying an erase voltage to a semiconductor substrate on which the memory cells are formed, and thus to the channels of the memory cells, to remove the charge from the floating gates. More specifically, the charge is removed through Fowler-Nordheim tunneling of electrons from the floating gate to the channel, resulting in an erase V_t typically less than zero.

Programming typically involves applying a programming voltage to one or more selected word lines and thus to the control gate of each memory cell in communication with (e.g., electrically coupled to) the one or more selected word lines, regardless of whether a memory cell is targeted or untargeted for programming. While the programming voltage is applied to the one or more selected word lines, a potential, such as a ground potential, is applied to the substrate, and thus to the channels of these memory cells, to charge the floating

gates. More specifically, the floating gates are charged through Fowler-Nordheim tunneling of electrons from the channel to the floating gate, resulting in a program V_t typically greater than zero.

For the reasons stated herein, and for other reasons which will become apparent to those skilled in the art upon reading and understanding the present specification, there is a need in the art for alternative program and erase schemes.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 shows an example plot of a sometimes referred to herein as program V_t of a typical flash memory cell for a given program voltage and pulse width versus the number of program/erase cycles applied to the flash memory cell and an example plot of an erase V_t of a typical flash memory cell for a given erase voltage and pulse width versus the number of program/erase cycles applied to the flash memory cell.

Figure 2A is a simplified block diagram of an embodiment of a NAND flash memory device, according to an embodiment of the disclosure.

Figure 2B illustrates an embodiment of a memory array, according to another embodiment of the disclosure.

Figure 3 illustrates an embodiment of a NAND memory array in accordance with another embodiment of the disclosure.

Figure 4 is an illustration of an embodiment of a memory module, according to another embodiment of the disclosure.

Figure 5 illustrates an embodiment of a portion of control logic of an embodiment of a memory device, according to another embodiment of the disclosure.

Figure 6 illustrates a series of program pulses typically used to program one or more memory cells.

Figure 7 illustrates an embodiment of a portion of control logic of an embodiment of a memory device, according to another embodiment of the disclosure.

Figure 8 illustrates an embodiment of a portion of control logic of an embodiment of a memory device, according to another embodiment of the disclosure.

DETAILED DESCRIPTION

In the following detailed description of the present embodiments, reference is made to the accompanying drawings that form a part hereof. These embodiments are described in sufficient detail to enable those skilled in the art to practice disclosed subject matter, and it is to be understood that other embodiments may be utilized and that process, electrical or mechanical changes may be made without departing from the scope of the claimed subject matter. The following detailed description is, therefore, not to be taken in a limiting sense, and the scope of the claimed subject matter is defined only by the appended claims and equivalents thereof.

The mechanism for both programming and erasing memory cells results in the passage of electrons through a tunnel dielectric layer, e.g., a tunnel oxide layer, interposed between the substrate on which the memory cells are formed and the floating gates of the memory cells, and therefore, electrons can become trapped in the oxide layer. As the number of program/erase cycles increases, an increasing number of electrons become trapped in the oxide layer. The trapped electrons act to increase the charge on the floating gates and thus the program V_t and the erase V_t of the memory cells. Therefore, the program V_t and the erase V_t increase as the number of program/erase cycles increases, as shown in Figure 1. As the program V_t and the erase V_t increase with the number of program/erase cycles, the erase voltage applied to the substrate for erasing the memory cells should be increased to properly erase all the memory cells, and the programming voltage applied to the word lines should be decreased to avoid over programming the memory cells.

The programming operation typically involves applying, to selected word lines, a number of programming pulses that start at a predetermined starting voltage level, typically insufficient to program all of the targeted memory cells of the selected word lines, and that are incremented until all of the targeted memory cells of the selected word lines are programmed. If the predetermined starting voltage provides for efficient programming when the memory device is new, it may lead to over-programming of some memory cells whose program V_t has increased too much through multiple program/erase cycles. However, if a predetermined starting voltage is chosen to avoid over-programming of memory cells later in the device life-cycle, it will generally lead to inefficient programming when the device is new as an excessive amount of program pulses will be required to program the memory cells.

One or more selected memory cells are typically erased by applying one or more erase pulses having the same or differing (e.g., successively incremented) voltage levels to the substrate while the word line(s) in communication with the one or more selected memory cells are grounded. However, as the number of program/erase cycles increases, it becomes more difficult to erase the memory cells in that the erase threshold voltage increases as the number of program/erase cycles increases. If the erase voltage provides for efficient erase operations when the memory device is new, it will generally lead to inefficient erase operations later in the device life-cycle. For example, an excessive amount of erase pulses will be required to erase the memory cells whose erase V_t has increased too much through multiple program/erase cycles. However, if the erase voltage is chosen to avoid excessive erase pulses later in the device life-cycle, it may lead to over-erasure of memory cells when the device is new.

Figure 2A is a simplified block diagram of a NAND flash memory device 200 in communication with a processor 230 as part of an electronic system, according to an embodiment. The processor 230 may be a memory controller or other external host device. Memory device 200 includes an array of memory cells 204 arranged in rows and columns. A row decoder 208 and a column decoder 210 are provided to decode address signals. Address signals are received and decoded to access memory array 204.

Memory device 200 also includes input/output (I/O) control circuitry 212 to manage input of commands, addresses and data to the memory device 200 as well as output of data and status information from the memory device 200. An address register 214 is in communication with I/O control circuitry 212, and row decoder 208 and column decoder 210 to latch the address signals prior to decoding. A command register 224 is in communication with I/O control circuitry 212 and control logic 216 to latch incoming commands. Control logic 216 controls access to the memory array 204 in response to the commands and generates status information for the external processor 230. The control logic 216 is in communication with row decoder 208 and column decoder 210 to control the row decoder 208 and column decoder 210 in response to the addresses.

Control logic 216 is also in communication with a cache register 218. Cache register 218 latches data, either incoming or outgoing, as directed by control logic 216 to temporarily store data while the memory array 204 is busy writing or reading, respectively, other data. For one embodiment, control logic 216 may include one or more circuits adapted

to produce a particular and predictable outcome or set of outcomes in response to one or more input events. During a write operation, data is passed from the cache register 218 to data register 220 for transfer to the memory array 204; then new data is latched in the cache register 218 from the I/O control circuitry 212. During a read operation, data is passed from the cache register 218 to the I/O control circuitry 212 for output to the external processor 230; then new data is passed from the data register 220 to the cache register 218. A status register 222 is in communication with I/O control circuitry 212 and control logic 216 to latch the status information for output to the processor 230.

In accordance with one embodiment of the disclosure, control logic 216 is configured to monitor pulse counts and/or program/erase cycles, and to adjust a program starting voltage and/or to adjust an erase starting voltage in response, at least in part, to the pulse counts and/or cycles.

Memory device 200 receives control signals at control logic 216 from processor 230 over a control link 232. The control signals may include at least chip enable CE#, a command latch enable CLE, an address latch enable ALE, and a write enable WE#. Memory device 200 receives command signals (which represent commands), address signals (which represent addresses), and data signals (which represent data) from processor 230 over a multiplexed input/output (I/O) bus 234 and outputs data to processor 230 over I/O bus 234.

For example, the commands are received over input/output (I/O) pins [0:7] of I/O bus 234 at I/O control circuitry 212 and are written into command register 224. The addresses are received over input/output (I/O) pins [0:7] of bus 234 at I/O control circuitry 212 and are written into address register 214. The data are received over input/output (I/O) pins [0:7] for an 8-bit device or input/output (I/O) pins [0:15] for a 16-bit device at I/O control circuitry 212 and are written into cache register 218. The data are subsequently written into data register 220 for programming memory array 204. For another embodiment, cache register 218 may be omitted, and the data are written directly into data register 220. Data are also output over input/output (I/O) pins [0:7] for an 8-bit device or input/output (I/O) pins [0:15] for a 16-bit device.

It will be appreciated by those skilled in the art that additional circuitry and signals can be provided, and that the memory device of Figure 2A has been simplified to help focus on the invention. It should be recognized that the functionality of the various block components described with reference to Figure 2A may not be segregated to distinct

components or component portions of an integrated circuit device. For example, a single component or component portion of an integrated circuit device could be adapted to perform the functionality of more than one block component of Figure 2A. Alternatively, one or more components or component portions of an integrated circuit device could be combined to perform the functionality of a single block component of Figure 2A.

Additionally, while specific I/O pins are described in accordance with popular conventions for receipt and output of the various signals, it is noted that other combinations or numbers of I/O pins may be used in the various embodiments.

Figure 2B illustrates memory array 204, according to another embodiment. For one embodiment, memory array 204 has a primary array 250 with primary memory blocks 255_1 to 255_K and a secondary memory array 260 with secondary memory blocks 265_1 to 265_L . For another embodiment, one or more of secondary memory blocks 265 are redundant memory blocks for replacing one or more defective primary memory blocks. One or more of secondary memory blocks 265 may store a number of program/erase cycles applied to one or more memory cells, such as a block of primary memory cells, in accordance with embodiments of the disclosure.

Figure 3 illustrates a NAND memory array 300 as a portion of memory array 204, such as a primary memory block 255 or a secondary memory block 265, in accordance with another embodiment. As shown in Figure 3, the memory array 300 includes word lines 302_1 to 302_N and intersecting local bit lines 304_1 to 304_M . For ease of addressing in the digital environment, the number of word lines 302 and the number of bit lines 304 are each some power of two, e.g., 256 word lines 302 by 4,096 bit lines 304.

Memory array 300 includes NAND strings 306_1 to 306_M . Each NAND string includes floating gate transistors 308_1 to 308_N , each located at an intersection of a word line 302 and a local bit line 304. The floating gate transistors 308 represent non-volatile memory cells for storage of data. The floating gate transistors 308 of each NAND string 306 are connected in series, source to drain, between a source select gate 310, e.g., a field effect transistor (FET), and a drain select gate 312, e.g., an FET. Each source select gate 310 is located at an intersection of a local bit line 304 and a source select line 314, while each drain select gate 312 is located at an intersection of a local bit line 304 and a drain select line 315.

A source of each source select gate 310 is connected to a common source line 316. The drain of each source select gate 310 is connected to the source of the first floating gate transistor 308 of the corresponding NAND string 306. For example, the drain of source select gate 310₁ is connected to the source of floating gate transistor 308₁ of the
5 corresponding NAND string 306₁. A control gate 320 of each source select gate 310 is connected to source select line 314. It is common for a common source line to be connected between source select gates for NAND strings of two different NAND arrays. As such, the two NAND arrays share the common source line.

The drain of each drain select gate 312 is connected to the local bit line 304 for
10 the corresponding NAND string at a drain contact 328. For example, the drain of drain select gate 312₁ is connected to the local bit line 304₁ for the corresponding NAND string 306₁ at drain contact 328₁. The source of each drain select gate 312 is connected to the drain of the last floating gate transistor 308_N of the corresponding NAND string 306. For example, the source of drain select gate 312₁ is connected to the drain of floating gate transistor 308_N of
15 the corresponding NAND string 306₁. It is common for two NAND strings to share the same drain contact.

Typical construction of floating gate transistors 308 includes a source 330 and a drain 332, a floating gate 334, and a control gate 336, as shown in Figure 3. Floating gate transistors 308 have their control gates 336 coupled to a word line 302. A column of the
20 floating gate transistors 308 is a NAND string 306 coupled to a given local bit line 304. A row of the floating gate transistors 308 are those transistors commonly coupled to a given word line 302.

Figure 4 is an illustration of a memory module 400, according to another embodiment. Memory module 400 is illustrated as a memory card, although the concepts
25 discussed with reference to memory module 400 are applicable to other types of removable or portable memory, e.g., USB flash drives, and are intended to be within the scope of “memory module” as used herein. In addition, although one example form factor is depicted in Figure 4, these concepts are applicable to other form factors as well.

In some embodiments, memory module 400 will include a housing 405 (as
30 depicted) to enclose one or more memory devices 410, though such a housing is not essential to all devices or device applications. At least one memory device 410 is a non-volatile

memory having control logic configured in accordance with embodiments of the invention, e.g., as described above in conjunction with Figure 2A for control logic 216.

Where present, the housing 405 includes one or more contacts 415 for communication with a host device. Examples of host devices include digital cameras, digital recording and playback devices, PDAs, personal computers, memory card readers, interface hubs and the like. For some embodiments, the contacts 415 are in the form of a standardized interface. For example, with a USB flash drive, the contacts 415 might be in the form of a USB Type-A male connector. In general, however, contacts 415 provide an interface for passing command, address and/or data signals between the memory module 400 and a host having compatible receptors for the contacts 415.

The memory module 400 may optionally include additional circuitry 420 which may be one or more integrated circuits and/or discrete components. For some embodiments, the additional circuitry 420 may include a memory controller for controlling access across multiple memory devices 410 and/or for providing a translation layer between an external host and a memory device 410. For example, there may not be a one-to-one correspondence between the number of contacts 415 and a number of I/O connections to the one or more memory devices 410. Thus, a memory controller could selectively couple an I/O connection (not shown in Figure 4) of a memory device 410 to receive the appropriate signal at the appropriate I/O connection at the appropriate time or to provide the appropriate signal at the appropriate contact 415 at the appropriate time. Similarly, the communication protocol between a host and the memory module 400 may be different than what is required for access of a memory device 410. A memory controller could then translate the command signal(s) received from a host into the appropriate command signal(s) to achieve the desired access to the memory device 410. Such translation may include changes in signal voltage levels and/or multiplexing or demultiplexing to command signals, for example.

The additional circuitry 420 may also include functionality unrelated to control of a memory device 410, such as logic functions as might be performed by an ASIC (application specific integrated circuit). Also, the additional circuitry 420 may include circuitry to restrict read or write access to the memory module 400, such as password protection, biometrics or the like. The additional circuitry 420 may include circuitry to indicate a status of the memory module 400. For example, the additional circuitry 420 may include functionality to determine whether power is being supplied to the memory module 400 and whether the

memory module 400 is currently being accessed, and to display an indication of its status, such as a solid light while powered and a flashing light while being accessed. The additional circuitry 420 may further include passive devices, such as decoupling capacitors to help regulate power requirements within the memory module 400.

Figure 5 illustrates a portion of control logic 216 of memory device 200 of Figure 2, according to another embodiment. A program state machine 510 controls the programming of one or more target memory cells of memory array 204. Program state machine 510 determines the number of program pulses *ppuls* (Figure 6) it takes to program one or more target memory cells, e.g., corresponding to a page of memory cells, of a selected word line, to which the program pulses *ppuls* are applied. For one embodiment, applying a program pulse *ppuls* to a selected word line includes applying a programming voltage V_{prog} to the selected word line, followed by applying a program verify voltage V_{verify} to the selected word line, as shown in Figure 6.

For one embodiment, programming starts by applying a programming voltage V_{prog} , e.g., $V_{prog,1}$, having a program starting voltage level $V_{prog,start}$ to the selected word line. If the program verify indicates that one or more of the target memory cells are programmed, the programming is completed for those memory cells. If any of the target memory cells remain unprogrammed, the programming voltage $V_{prog,1}$ is increased from the program starting voltage level $V_{prog,start}$ by a program voltage step ΔV , resulting in a programming voltage $V_{prog,2} = V_{prog,1} + \Delta V$ at the selected word line, as shown in Figure 6. These remaining unprogrammed target memory cells then receive an additional programming pulse while programmed target memory cells and other memory cells associated with the word line are inhibited from programming. If the program verify indicates that one or more of the remaining target memory cells are now programmed, the programming is completed for those memory cells. This sequence is repeated, e.g., using program pulses $V_{prog,3}$ and $V_{prog,4}$, until all of the target memory cells are programmed, i.e., until the target memory cells are at least at their desired program V_t .

Subsequently, programming may proceed to other memory cells of the selected word line that correspond to another page, or programming may proceed to another word line of the same memory block or another memory block. Note that hereinafter, unless specified otherwise, a memory block may be a primary memory block 255 (Figure 2B) or a secondary

memory block 265 that can or is being used as a redundant memory block to replace a defective primary memory block.

An erase operation is typically performed on a block of memory cells before they are programmed. An erase operation followed by a programming operation, such as described above, constitutes an exemplary program/erase cycle. Note that the program Vt , for a given program voltage and pulse width, generally increases as the number of program/erase cycles increases, as shown in Figure 1. This means that for a given program starting voltage level $V_{prog,start}$, the number of program pulses *ppuls* it takes to program one or more target memory cells may decrease as the number of program/erase cycles increases.

A sampling circuit 520 is in communication with program state machine 510, as shown in Figure 5. For one embodiment, sampling circuit 520 determines the number of program pulses *ppuls* it takes to program a certain (e.g., a predetermined) number (or a sample) of memory cells a certain number of times after power-up. For another embodiment, sampling circuit 520 may gather and hold the number of program pulses *ppuls* it takes to program this "sample." For one embodiment, this "sample" may include one or more targeted memory cells from each of a plurality of word lines, such as a memory block of word lines, a single page of memory cells, etc. For another embodiment, the number of program pulses *ppuls* it takes to program the sample may be determined each time the sample is programmed. For another embodiment, sampling circuit 520 determines the number of program pulses *ppuls* it takes to program a sample of memory cells corresponding to each page of memory cells each time that page of memory cells is programmed.

Logic 530 for controlling the program starting voltage level $V_{prog,start}$ is in communication with sampling circuit 520, as shown in Figure 5. For one embodiment, logic 530 includes a volatile or non-volatile latch 535 that stores the sampling information, e.g., the number of program pulses *ppuls* it takes to program a sample of memory cells, from sampling circuit 520. Note that for some embodiments, e.g., where each sample of memory cells corresponds to a single page of memory cells and where the pages are programmed a single page at a time, sampling circuit 520 may be omitted. For such embodiments, the number of pulses required to program that page may be stored directly in latch 535 after that page is programmed. For one embodiment, logic 530 determines the average number of program pulses *ppuls* it takes to program one or more memory cells of each selected word line of a sample, e.g., where the sample includes one or more memory cells of each of a

plurality of word lines, and stores the average in latch 535; thus, the average is an average per word line.

For one embodiment, logic 530 compares the number of program pulses *ppuls* determined by sample circuit 520, or determined by program state machine 510, or an average number of program pulses *ppuls* per word line, as determined by logic 530, to a target number of programming pulses that may be stored by or preprogrammed in logic 530. When the number of program pulses *ppuls* is different than the target number of programming pulses, logic 530 may adjust a program starting voltage level $V_{prog,start}$ so that the number of program pulses *ppuls* applied during the next program operation will tend toward the target number of programming pulses. For example, if the number of program pulses *ppuls* is greater than the target number of programming pulses, logic 530 may increase the program starting voltage level $V_{prog,start}$ to reduce the number of program pulses *ppuls* applied during the next program operation. For another embodiment, logic 530 may store the difference between the target number of programming pulses and the number of program pulses *ppuls* in latch 535, e.g., when latch 535 is a non-volatile latch. For a further embodiment, logic 530 may only adjust the program starting voltage level $V_{prog,start}$ when the number of program pulses *ppuls* exceeds the target number of programming pulses by some number greater than one.

A high-voltage regulator 540 is in communication with logic 530. For one embodiment, a trim of high-voltage regulator 540 for setting the program starting voltage is set to the program starting voltage level $V_{prog,start}$ from logic 530.

Figure 7 illustrates a portion of control logic 216 of memory device 200 of Figure 2, according to another embodiment. An erase state machine 710 controls erasing of one or more target memory cells of memory array 204. For one embodiment, erase state machine 710 erases one or more target memory cells prior to programming the one or more memory cells. For another embodiment, erase state machine 710 erases the memory cells a block at a time. Erase state machine 710 determines the number of erase pulses it takes to erase one or more target memory cells of a selected word line, e.g., to which ground is applied. For one embodiment, applying an erase pulse includes applying an erase voltage (e.g., a negative voltage), followed by an erase-verify operation that determines whether the target memory cells have been erased.

For one embodiment, erasing starts by applying an erase voltage having an erase starting voltage level to the substrate. If the erase verify indicates that each of the one or more target memory cells is erased, the erase is completed. Otherwise, the erase voltage is increased (e.g., negatively or in magnitude) from the erase starting voltage level by an erase voltage step. If the subsequent erase verify indicates that each of the one or more target memory cells is erased, the erase is completed. Otherwise, the erase voltage is again increased by the erase voltage step followed by an erase verify. This is repeated until each of the one or more target memory cells is erased, i.e., until the target memory cells are at least at their desired erase V_t .

Note that the erase V_t generally increases (e.g., becomes less negative) for a given erase voltage and pulse width as the number of program/erase cycles increases, as shown in Figure 1. This means that for a given erase starting voltage level, the number of erase pulses it takes to erase one or more target memory cells generally increases as the number of program/erase cycles increases.

A sampling circuit 720 is in communication with erase state machine 710, as shown in Figure 7. For one embodiment, sampling circuit 720 determines the number of erase pulses it takes to erase a certain number (or sample) of memory cells a certain number of times after power-up. For another embodiment, sampling circuit 720 may gather and hold the number of erase pulses it takes to program this "sample." For one embodiment, this "sample" may include one or more targeted memory cells from each of a plurality of word lines, such as a memory block of word lines. For another embodiment, the number of erase pulses it takes to erase the sample may be determined each time the sample is erased. For another embodiment, sampling circuit 720 determines the number of erase pulses it takes to erase a sample of memory cells corresponding to a block of memory cells each time that block of memory cells is erased.

Logic 730 for controlling the erase starting voltage level is in communication with sampling circuit 720, as shown in Figure 7. For one embodiment, logic 730 includes a volatile or non-volatile latch 735 that stores the sampling information, e.g., the number of erase pulses it takes to erase a sample of memory cells, from sampling circuit 720. Note that for some embodiments, e.g., where each sample of memory cells corresponds to a block of memory cells and where the blocks are erased a single block at a time, sampling circuit 720 may be omitted. For such embodiments, the number of pulses required to erase that block

may be stored directly in latch 735 after that block is erased. For one embodiment, logic 730 determines the average number of erase pulses it takes to erase one or more memory cells of each selected word line of a sample, e.g., where the sample includes one or more memory cells of each of a plurality of word lines, and stores the average in latch 735; thus, the average is an average per word line.

For one embodiment, logic 730 compares the number of erase pulses determined by sample circuit 720, or directly from erase state machine 710, or an average number of erase pulses per word line, determined by logic 730, to a target number of erase pulses that may be stored by or preprogrammed in logic 730. When the number of erase pulses is different than the target number of erase pulses, logic 730 may adjust an erase starting voltage level so that the number of erase pulses applied during the next erase operation will tend toward the target number of erase pulses. For example, if the number of erase pulses is more than the target number of erase pulses, logic 730 may increase the erase starting voltage level (e.g., negatively or the magnitude of the erase starting voltage level) to reduce the number of erase pulses applied during the next erase operation. For another embodiment, logic 730 may store the difference between the target number of programming pulses and the number of erase pulses, e.g., when latch 735 is a non-volatile latch. For a further embodiment, logic 730 may only adjust the erase starting voltage level when the number of erase pulses exceeds the target number of erase pulses by some number greater than one.

A high-voltage regulator 740 is in communication with logic 730. For one embodiment, a trim of high-voltage regulator 740 for setting the erase starting voltage is set to the erase starting voltage level from logic 730.

Figure 8 illustrates a portion of control logic 216 of memory device 200 of Figure 2, according to another embodiment. A control state machine 810 controls the programming and/or erasing of one or more target memory cells of one or more memory blocks of memory array 204. For one embodiment, control state machine 810 erases one or more target memory cells prior to programming the one or more memory cells. For another embodiment, control state machine 810 erases the memory cells a block at a time prior to programming one or more target memory cells of the corresponding erased block.

A counter 820 is in communication with control state machine 810 and a memory 830. For one embodiment, memory 830 is a portion of secondary memory array 260 of Figure 2B, such as one or more NAND strings of memory cells of one of secondary memory

blocks 265 (Figure 2B). For one embodiment, memory 830 may store the number of program/erase cycles applied to the memory cells of each memory block. For other embodiments, the number of program/erase cycles applied to the memory cells of the respective memory blocks may be substantially the same, and thus, memory 830 stores a nominal number of program/erase cycles, e.g., per memory block. For one embodiment, counter 820 is reset upon power-up and is then loaded with the number of program/erase cycles previously stored in memory 830, e.g., as part of an initialization sequence of the memory device.

Each time control state machine 810 performs a programming operation and/or erase operation, by programming and/or erasing one or more target memory cells, control state machine 810 sends a signal, indicative that a program/erase cycle has occurred, to counter 820, and counter 820 then increments the current counter value (i.e., the number of program/erase cycles) by one. For one embodiment, the signal is in the form of a clock pulse that causes counter 820 to count up by one.

Compare logic 840 is in communication with counter 820, as shown in Figure 8. Counter 820 outputs the incremented number of program/erase cycles to compare logic 840. Compare logic 840 compares the incremented number of program/erase cycles to one or more numerical values. For one embodiment, the one or more numerical values may be part of a look-up table of compare logic 840.

Compare logic 840 is in communication with starting-voltage control logic 850 for controlling the program starting voltage level $V_{prog,start}$, described above in conjunction with Figures 5 and 6, and/or the erase starting voltage level, described above in conjunction with Figure 7, as shown in Figure 8. Compare logic 840 outputs cycling stage signals to starting-voltage control logic 850 in response, at least in part, to the comparison of the determined number of program/erase cycles to the one or more numerical values. Starting-voltage control logic 850 then adjusts the program starting voltage level and/or the erase starting voltage level in response to the cycling stage signals from compare logic 840. For example, when the incremented number of program/erase cycles is less than a first numerical value, starting-voltage control logic 850 sets the program starting voltage level to a first program level and/or the erase starting voltage level to a first erase level in response to the cycling stage signals from compare logic 840. When the incremented number of program/erase cycles is greater than or equal to the first numerical value and less than a

second numerical value, starting-voltage control logic 850 sets the program starting voltage level to a second program level and/or the erase starting voltage level to a second erase level, for example, in response to the cycling stage signals from compare logic 840. The comparisons may continue until the incremented number of program/erase cycles exceeds a maximum numerical value.

For one embodiment, the program starting voltage level may be set so that a certain number of programming pulses is applied to one or more selected word lines, and/or the erase starting voltage level is set so that a certain number of erase pulses is applied to the substrate on which the memory cells are formed. For another embodiment, the program starting voltage level and/or the erase starting voltage level are adjusted so that the number of programming pulses and/or the number of erase pulses remain substantially fixed, regardless of the number of program/erase cycles. For example, the number programming pulses may correspond to the number of programming pulses required to program one or more memory cells after a large number of program/erase cycles has occurred, and/or the number of erase pulses may correspond to the number of erase pulses required to erase one or more memory cells after a large number of program/erase cycles has occurred. Therefore, since the required number of programming pulses generally decreases as the number of program/erase cycles increases and the required number of erase pulses generally increases as the number of program/erase cycles increases, the program starting voltage level would need to decrease and the erase starting voltage level would need to increase as the number of program/erase cycles increases to keep the number of programming and erase pulses fixed.

A high-voltage regulator 860 is coupled to starting-voltage control logic 850. For one embodiment, a trim of high-voltage regulator 860 for setting the program starting voltage and/or the erase starting voltage are set to the program starting voltage level and the erase starting voltage level from starting-voltage control logic 850.

The incremented number of program/erase cycles output from counter 820 is stored in memory 830, thereby updating the number of program/erase cycles stored in memory 830. For one embodiment, the output of counter 820 may be stored in memory 830 upon power-down of the memory device.

CONCLUSION

Although specific embodiments have been illustrated and described herein it is manifestly intended that the scope of the claimed subject matter be limited only by the following claims and equivalents thereof.

What is claimed is:

1. A method of operating a memory device (200), comprising:

determining a number of program pulses required for programming one or more memory cells (308) of the memory device (200) during a programming operation and/or determining a number of erase pulses required for erasing one or more memory cells (308) of the memory device (200) during an erase operation; and

adjusting a program starting voltage level of one or more program pulses applied to the one or more memory cells (308) during a subsequent programming operation in response, at least in part, to the number of program pulses determined in the prior programming operation and/or adjusting an erase starting voltage level of one or more erase pulses applied to the one or more memory cells (308) during a subsequent erase operation in response, at least in part, to the number of erase pulses determined in the prior erase operation.
2. The method of claim 1, wherein adjusting the program starting voltage level of one or more program pulses applied to the one or more memory cells (308) during a subsequent programming operation comprises adjusting the program starting voltage level so that the number of program pulses applied during the subsequent programming operation will tend toward a target number of programming pulses, and/or wherein adjusting the erase starting voltage level of one or more erase pulses applied to the one or more memory cells (308) during a subsequent erase operation comprises adjusting the erase starting voltage level so that the number of erase pulses applied during the subsequent erase operation will tend toward a target number of erase pulses.
3. The method of claim 2, wherein the target number of programming pulses is less than the number of program pulses determined in the prior programming operation and/or wherein the target number of erase pulses is less than the number of erase pulses determined in the prior erase operation.

4. The method of claim 1, 2, or 3, wherein determining a number of program pulses required for programming one or more memory cells (308) of the memory device (200) during a programming operation comprises at least one of determining an average number of program pulses it takes to program a sample of memory cells (308) and determining the number of program pulses it takes to program a sample of memory cells (308) a certain number of times after power-up, and/or wherein determining a number of erase pulses required for erasing one or more memory cells (308) of the memory device (200) during an erase operation comprises at least one of determining an average number of erase pulses it takes to erase a sample of memory cells (308) and determining the number of erase pulses it takes to erase a sample of memory cells (308) a certain number of times after power-up.
5. The method of claim 4, wherein the sample of programmed memory cells (308) may or may not include the memory cells (308) currently being programmed and/or wherein the sample of erased memory cells (308) may or may not include the memory cells (308) currently being erased.
6. The method of claim 1, wherein adjusting a program starting voltage level of one or more program pulses applied to the one or more memory cells (308) during a subsequent programming operation is in response to the number of program pulses determined in the prior programming operation exceeding a certain number of program pulses or exceeding the certain number of program pulses by more than one, and/or wherein adjusting an erase starting voltage level of one or more erase pulses applied to the one or more memory cells (308) during a subsequent erase operation is in response to the number of erase pulses determined in the prior erase operation exceeding a certain number of erase pulses or exceeding the certain number of erase pulses by more than one.

7. A method of operating a memory device (200), comprising:
determining a number of program/erase cycles applied to one or more memory cells (308) of the memory device (200); and
adjusting a program starting voltage level and/or an erase starting voltage level in response, at least in part, to the determined number of program/erase cycles.
8. The method of claim 7, wherein determining a number of program/erase cycles applied to one or more memory cells (308) comprises incrementing a count of a number of program/erase cycles previously applied to the one or more memory cells (308) of the memory device (200) by one each time a subsequent program/erase cycle is applied to the one or more memory cells (308).
9. The method of claim 8 further comprises storing the incremented count in the memory device (200).
10. The method of claim 9, wherein the incremented count is stored upon power-down of the memory device (200).
11. The method of claim 7 further comprises before adjusting the program starting voltage level and/or the erase starting voltage level, comparing the determined number of program/erase cycles applied to the one or more memory cells (308) to one or more numerical values.
12. The method of claim 11, wherein the one or more numerical values are part of a look-up table of the memory device (200).

13. The method of any one of claims 7-12, wherein adjusting a program starting voltage level and/or an erase starting voltage level further comprises:
- setting the program starting voltage level to a first program level and/or setting the erase starting voltage level to a first erase level when the determined number of program/erase cycles applied to the one or more memory cells (308) is less than a certain numerical value; and
- setting the program starting voltage level to a second program level and/or setting the erase starting voltage level to a second erase level when the determined number of program/erase cycles applied to the one or more memory cells (308) is greater than or equal to the numerical value.
14. The method of any one of claims 7-12, wherein adjusting a program starting voltage level and/or an erase starting voltage level comprises adjusting the program starting voltage level so that a number of programming pulses applied to one or more selected word lines (302) remains substantially fixed regardless of the determined number of program/erase cycles and/or adjusting the erase starting voltage level so that a number of erase pulses applied to a substrate on which the memory cells (308) are formed remains fixed regardless of the determined number of program/erase cycles.
15. A memory device (200), comprising:
- a memory array (204);
- a state machine (510, 710) configured to control program and/or erase operations on the memory array (204) and to determine of a number of program pulses required to program one or more memory cells (308) of the memory array (204) and/or a number of erase pulses required to erase one or more memory cells (308) of the memory array (204); and
- starting-voltage level control logic (530, 730) coupled to the state machine (510, 710), the starting-voltage level control logic (530, 730) configured to adjust a program starting voltage level of one or more program pulses applied to one or more memory cells (308) of the memory array (204) during a programming

operation in response, at least in part, to a number of program pulses required for programming one or more memory cells (308) during a previous programming operation and/or to adjust an erase starting voltage level of one or more erase pulses applied to one or more memory cells (308) during an erase operation in response, at least in part, to a number of erase pulses required for erasing one or more memory cells during a previous erase operation.

16. The memory device (200) of claim 15, further comprising a sampling circuit (520, 720) in communication with the starting-voltage level control logic (530, 730) and the state machine (510, 710), the sampling circuit (520, 720) configured to determine a number of program pulses it takes to program a sample of one or more memory cells (308), wherein the sample of programmed memory cells (308) includes the one or more memory cells (308) programmed during the previous programming operation, and/or to erase a sample of one or more memory cells (308), wherein the sample of erased memory cells (308) includes the one or more memory cells (308) erased during the previous erase operation.
17. The memory device (200) of claim 16, wherein the starting-voltage level control logic (530, 730) is configured to determine an average number of program pulses it takes to program the sample of programmed memory cells (308) and/or to determine an average number of erase pulses it takes to erase the sample of erased memory cells (308).
18. The memory device (200) of claim 16, wherein the starting-voltage level control logic (530, 730) comprises a latch (535, 735) configured to store the number of program pulses required for programming the one or more memory cells (308) programmed during the previous programming operation and/or to store the number of erase pulses required for erasing the one or more memory cells (308) erased during the previous erase operation.

19. The memory device (200) of claim 15, wherein the one or more memory cells (308) programmed during the previous programming operation include the one or more memory cells (308) to which the one or more program pulses with the adjusted program starting voltage level are being applied and/or the one or more memory cells (308) erased during the previous erase operation include the one or more memory cells (308) to which the one or more erase pulses with the adjusted erase starting voltage level are being applied.
20. The memory device (200) of claim 15, wherein the one or more memory cells (308) programmed during the previous programming operation do not include the one or more memory cells (308) to which the one or more program pulses with the adjusted program starting voltage level are being applied and/or the one or more memory cells (308) erased during the previous erase operation do not include the one or more memory cells (308) to which the one or more erase pulses with the adjusted erase starting voltage level are being applied.
21. The memory device (200) of claim 15, wherein the starting-voltage level control logic (530, 730) is further configured to compare the number of program pulses required for programming the one or more memory cells (308) programmed during the previous programming operation to a target number of programming pulses and/or to compare the number of erase pulses required for erasing the one or more memory cells (308) erased during the previous erase operation to a target number of erase pulses.
22. The memory device (200) of claim 21, wherein the starting-voltage level control logic (530, 730) is further configured to adjust the program starting voltage level of the one or more program pulses when the number of program pulses required for programming the one or more memory cells (308) programmed during the previous programming operation exceeds the target number of programming pulses by some number greater than one and/or to adjust the erase starting voltage level of the one or more erase pulses when the number of erase pulses required for erasing the one or

more memory cells (308) erased during the previous erase operation exceeds the target number of erase pulses by some number greater than one.

23. A memory device (200), comprising:
- an array (204) of memory cells (308);
 - control logic (216) in communication with the array (204) of memory cells (308), the control logic (216) comprising:
 - a control state machine (810) configured to control program and/or erase operations on the array (204) of memory cells (308);
 - a counter (820) in communication with the control state machine (810);
 - a memory (830) in communication with the counter (820);
 - compare logic (840) coupled to the counter (820); and
 - starting-voltage level control logic (850) coupled to the compare logic (840);
 - wherein the counter (820) is configured to receive, from the memory (830), a number of program/erase cycles applied to one or more memory cells (308) of the array (204) of memory cells (308) and to increment that number of program/erase cycles each time a program/erase cycle is applied to the one or more memory cells (308);
 - wherein the compare logic (840) is configured to compare the incremented number of program/erase cycles to one or more numerical values; and
 - wherein the starting-voltage level control logic (850) is configured to adjust a program starting voltage level and/or an erase starting voltage level based on the comparison of the incremented number of program/erase cycles to the one or more numerical values.
24. The memory device (200) of claim 23, wherein the counter (820) is further configured to update the memory (830) by sending the incremented number of program/erase cycles to the memory (830).

25. The memory device (200) of claim 23 or 24, wherein the memory (830) is a portion of the array (204) of memory cells (308).

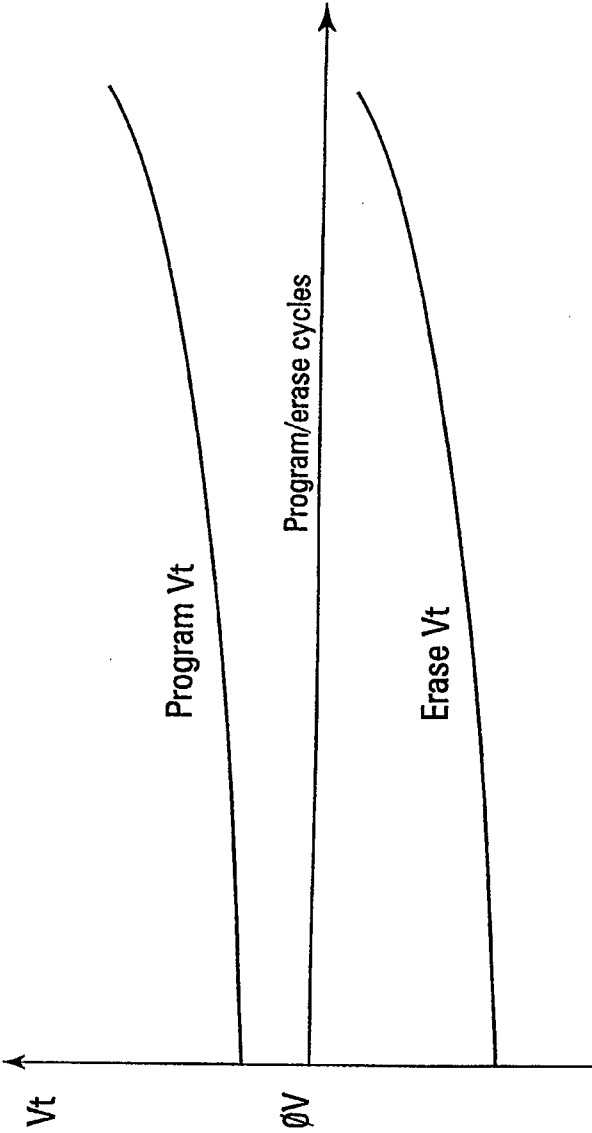


FIG. 1

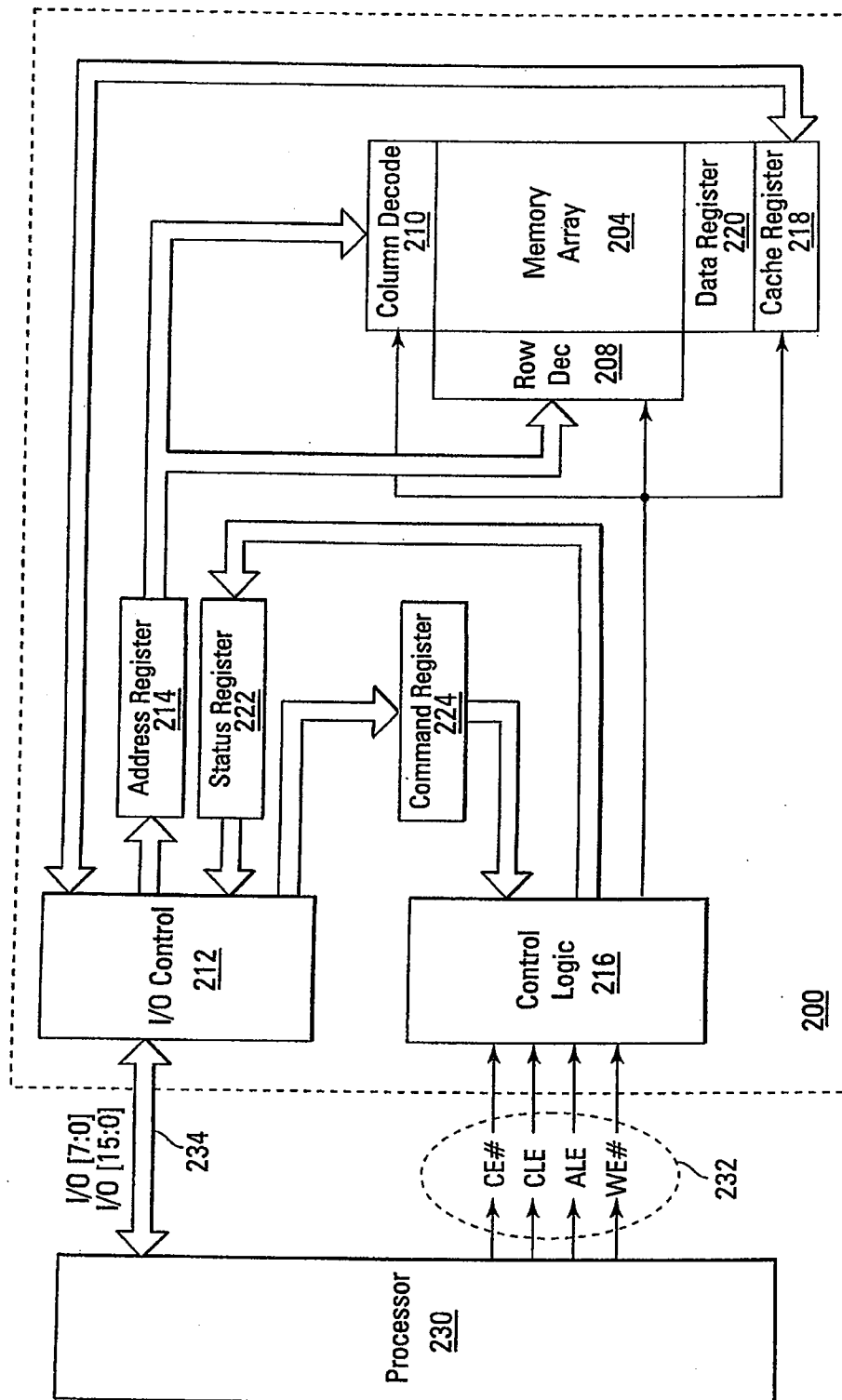


FIG. 2A

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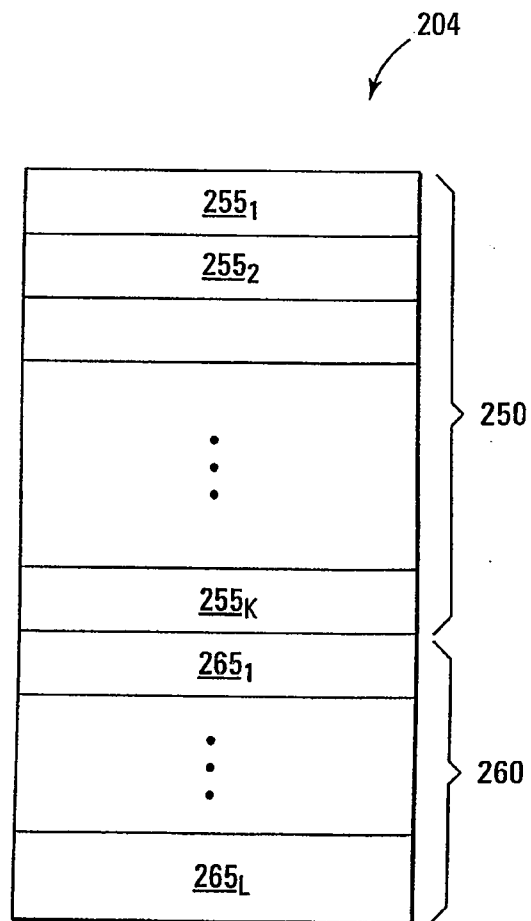


FIG. 2B

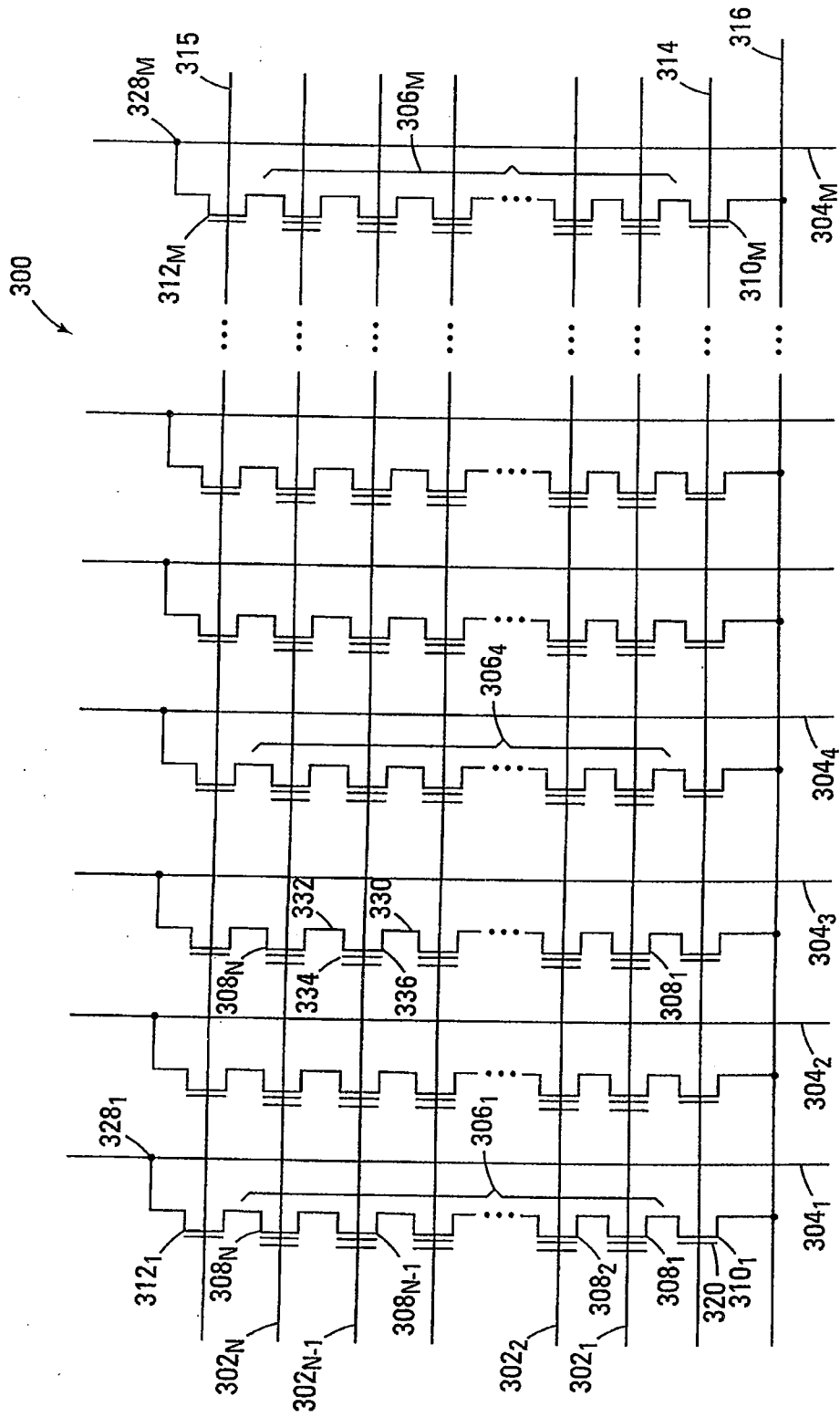


FIG. 3

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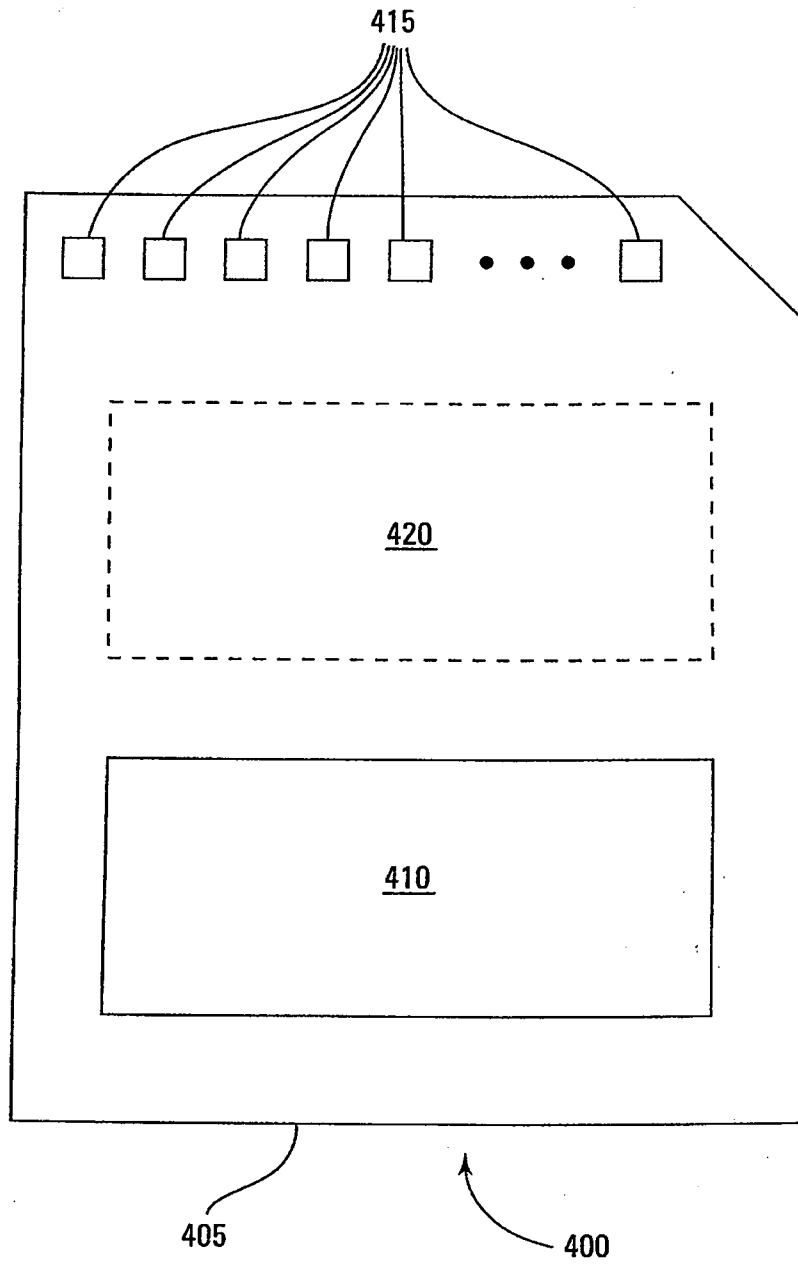


FIG. 4

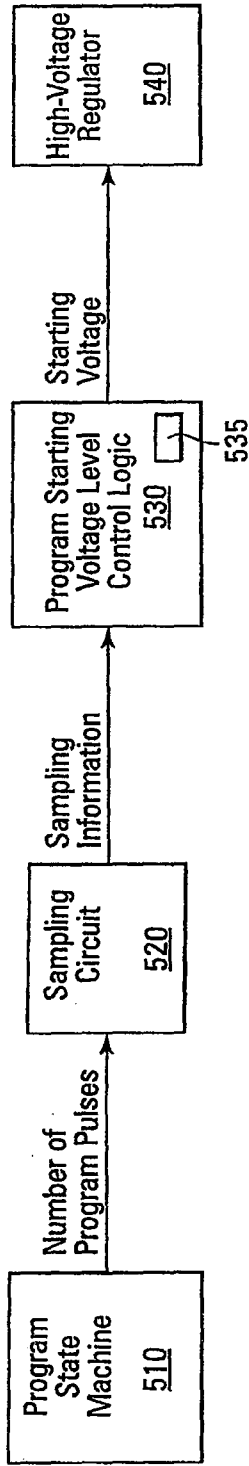


FIG. 5

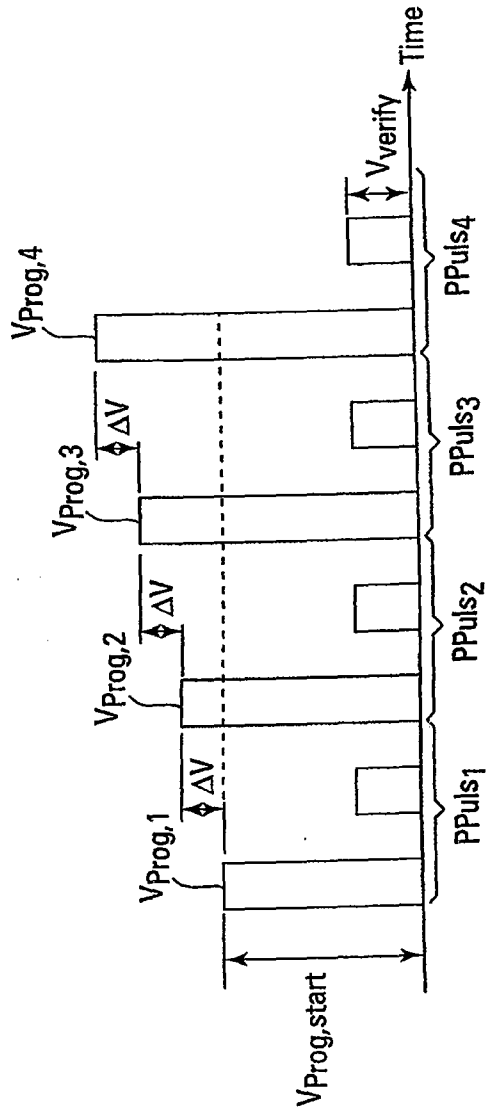
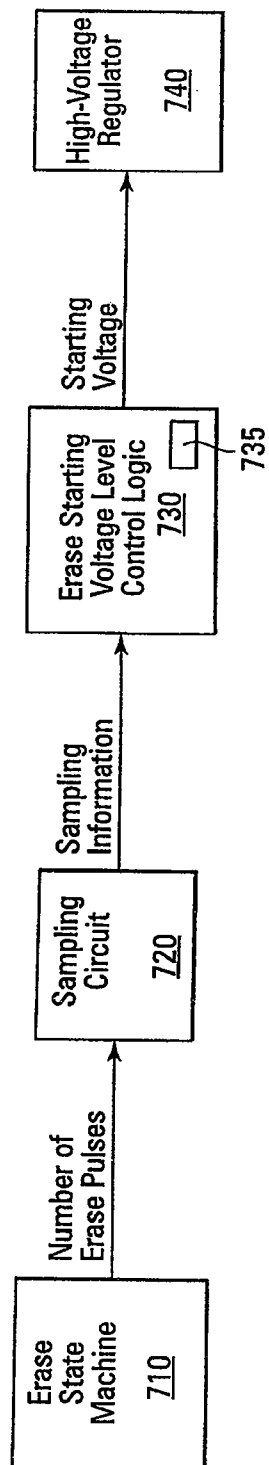


FIG. 6
Prior Art

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**FIG. 7**

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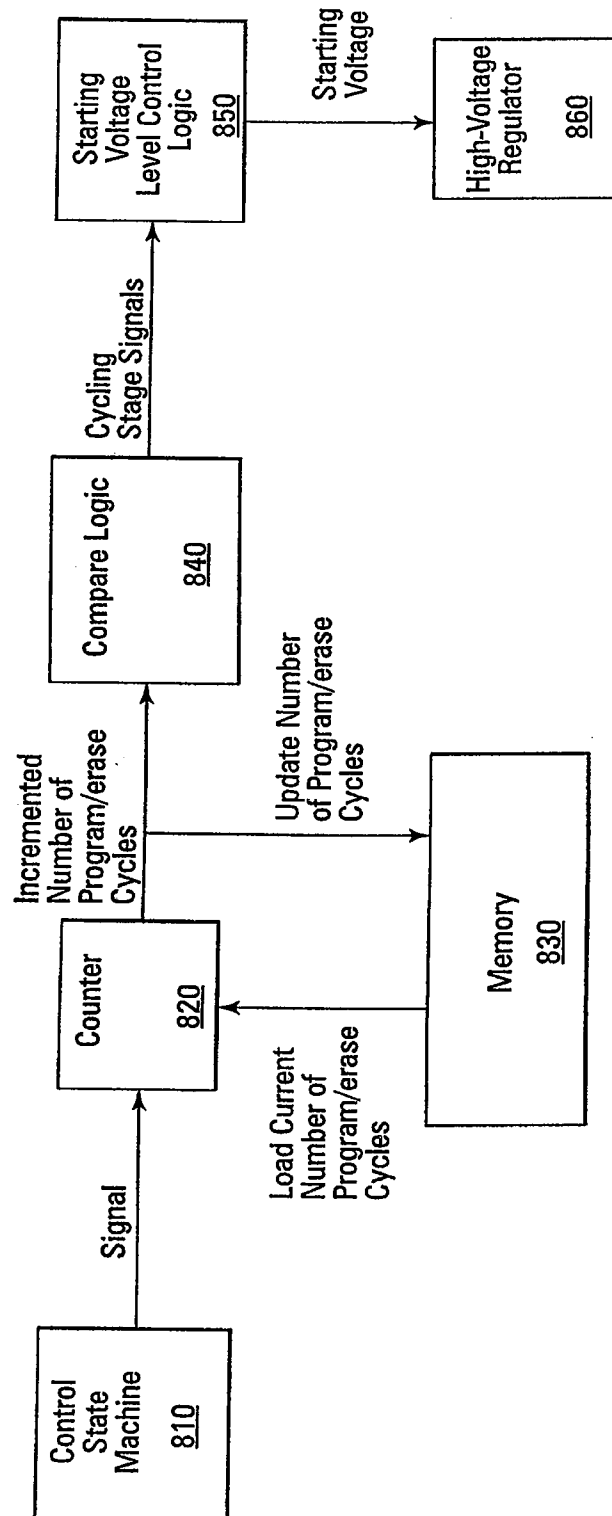


FIG. 8

INTERNATIONAL SEARCH REPORT

International application No

PCT/US2008/061376

A. CLASSIFICATION OF SUBJECT MATTER

INV. G11C16/10 G11C16/34

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
G11C

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal, WPI Data, INSPEC, IBM-TDB

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 6 327 183 B1 (PAWLETKO JOSEPH G [US] ET AL) 4 December 2001 (2001-12-04) columns 8-12; figures 3,10A-B	1-6, 15-22
X	US 6 278 633 B1 (WONG SAU C [US] ET AL) 21 August 2001 (2001-08-21) column 6, line 36 - column 10, line 18; figures 1,2A column 12, line 30 - line 59	1,2,4,5, 15-21
X	US 7 200 708 B1 (KREIFELS JERRY A [US]) 3 April 2007 (2007-04-03) column 2, line 20 - column 6, line 10; figures 1,2	1-3,6, 15,16, 19,21,22



Further documents are listed in the continuation of Box C.



See patent family annex.

* Special categories of cited documents:

- *A* document defining the general state of the art which is not considered to be of particular relevance
- *E* earlier document but published on or after the international filing date
- *L* document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
- *O* document referring to an oral disclosure, use, exhibition or other means
- *P* document published prior to the international filing date but later than the priority date claimed

T later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

X document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

Y document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

G document member of the same patent family

Date of the actual completion of the international search

16 July 2008

Date of mailing of the international search report

08/10/2008

Name and mailing address of the ISA/

European Patent Office, P.B. 5818 Patentlaan 2
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Havard, Corinne

INTERNATIONAL SEARCH REPORT

International application No

PCT/US2008/061376

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 6 205 055 B1 (PARKER ALLAN [US]) 20 March 2001 (2001-03-20) column 2, line 24 - column 3, line 38; figure 3	1-3, 6, 15, 16, 19, 21, 22

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2008/061376

Box No. II Observations where certain claims were found unsearchable (Continuation of item 2 of first sheet)

This international search report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. ☐ Claims Nos.:
because they relate to subject matter not required to be searched by this Authority, namely:
2. ☐ Claims Nos.:
because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out, specifically:
3. ☐ Claims Nos.:
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

Box No. III Observations where unity of invention is lacking (Continuation of item 3 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:

see additional sheet

1. ☐ As all required additional search fees were timely paid by the applicant, this international search report covers allsearchable claims.
2. ☐ As all searchable claims could be searched without effort justifying an additional fees, this Authority did not invite payment of additional fees.
3. ☐ As only some of the required additional search fees were timely paid by the applicant, this international search reportcovers only those claims for which fees were paid, specifically claims Nos.:
4. ☒ No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:

1-6, 15-22

Remark on Protest

- ☐ The additional search fees were accompanied by the applicant's protest and, where applicable, the payment of a protest fee.
- ☐ The additional search fees were accompanied by the applicant's protest but the applicable protest fee was not paid within the time limit specified in the invitation.
- ☐ No protest accompanied the payment of additional search fees.

FURTHER INFORMATION CONTINUED FROM PCT/ISA/ 210

This International Searching Authority found multiple (groups of) inventions in this international application, as follows:

1. claims: 1-6,15-22

Method of adjusting of a program/erase starting voltage level in function of the needed number of program/erase pulses

2. claims: 7-14,23-25

Method of triggering adjusting of the program/erase starting voltage level in function of the number of rewrite cycles

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No

PCT/US2008/061376

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 6327183	B1	04-12-2001	NONE
US 6278633	B1	21-08-2001	US 6330185 B1 11-12-2001
US 7200708	B1	03-04-2007	NONE
US 6205055	B1	20-03-2001	NONE