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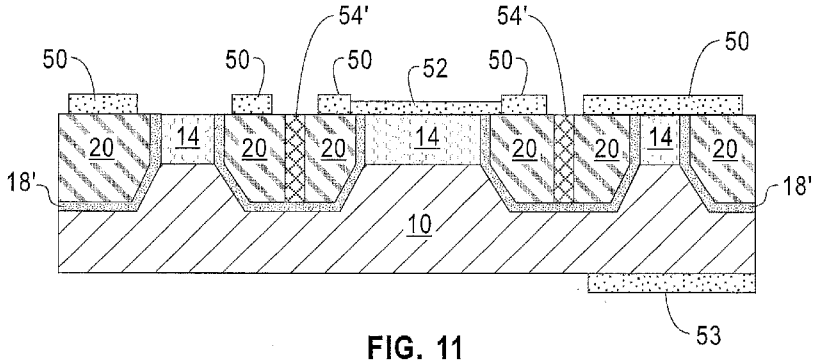


FIG. 11

(57) Abstract: A method for selective formation of a gallium nitride material on a (100) silicon substrate. The method includes forming a blanket layer of dielectric material on a surface of a (100) silicon substrate. The blanket layer of dielectric material is then patterned forming a plurality of patterned dielectric material structures on silicon substrate. An etch is employed that selectively removes exposed portions of the silicon substrate. The etch forms openings within the silicon substrate that expose a surface of the silicon substrate having a (111) crystal plane. A contiguous A1N buffer layer is then formed on exposed surfaces of each patterned dielectric material structure and on exposed surfaces of the silicon substrate. A gallium mtride material is then formed on a portion of the contiguous A1N buffer layer and surrounding each sidewall of each patterned dielectric material structure.

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# SELECTIVE GALLIUM NITRIDE REGROWTH ON (100) SILICON

## BACKGROUND

**[0001]** The present disclosure generally relates to a method for integrating Group III nitrides (e.g., GaAlInN) with silicon and more particularly to a method of selectively forming a gallium nitride material on a (100) silicon substrate. The present disclosure also relates to a semiconductor structure including a gallium nitride material surrounding sidewalls of a patterned dielectric material structure and located adjacent a surface of the (100) silicon substrate having a (111) crystal plane.

**[0002]** Group III nitride materials are a unique group of semiconductor materials which can be used in a wide variety of applications including, for example, optoelectronics, photovoltaics and lighting. Group III nitride materials are composed of nitrogen and at least one element from Group III, i.e., aluminum (Al), gallium (Ga) and indium (In), of the Periodic Table of Elements. Illustrative examples of some common gallium nitrides are GaN, GaAIN, and GaAlInN. By changing the composition of Al, Ga and/or In within a Group III nitride material, the Group III nitride material can be tuned along the electromagnetic spectrum; mainly from 210 nm to 1770 nm. This spectrum includes the visible light emitting diode (LED), which is more than a 10 billion dollar industry with a forecasted double digit yearly growth rate. This continuous growth in LED demand enables the infrastructural build-up for the growth and fabrication of Group III nitride based semiconductor devices.

**[0003]** One of the bottlenecks for Group III nitride based semiconductor devices is a lack of a latticed matched substrate. Some of the conventional substrates are sapphire ($A1_20_3$), silicon carbide (SiC), silicon (Si), and zinc oxide (ZnO) that have about 13%, 3%, 17% and 2%, respectively, lattice mismatch with GaN. Currently, lattice matched freestanding GaN and A1N substrates are being developed. However, lattice matched substrates suffer from availability and cost.

**[0004]** Most of the Group III nitride consumer-targeted devices are conventionally grown on sapphire substrates. There is, however, a need for the development of Group III nitride technology on more available and cheaper substrates such as silicon. The integration between Group III nitrides and silicon substrates are difficult because of the different crystal structure and lattice constant of those materials. As such, a method is needed which can be used to easily integrate Group III nitride materials with silicon substrates.

SUMMARY

**[0005]** In one aspect of the present disclosure, a method for selectively forming a gallium nitride material on a silicon substrate is provided. The method of the present disclosure includes first forming a blanket layer of dielectric material on an uppermost surface of a (100) silicon substrate. Next, the blanket layer of dielectric material is patterned forming a plurality of patterned dielectric material structures on portions of the uppermost surface of the (100) silicon substrate and exposing other portions of the uppermost surface of the (100) silicon substrate. The exposed other portions of the uppermost surface of the (100) silicon substrate are then etched to expose a surface within the (100) silicon substrate having a (111) crystal plane, A contiguous A1N buffer layer is then formed on exposed surfaces of each patterned dielectric material structure and on exposed surfaces of the silicon substrate. A gallium nitride material is then formed on a portion of the contiguous A1N buffer layer and suiTounding each sidewall of each patterned dielectric material structure.

**[0006]** In another aspect of the present disclosure, a semiconductor structure is provided. The semiconductor structure of the present disclosure includes a (100) silicon substrate having a plurality of patterned dielectric material structures located on an uppermost surface of the silicon substrate and a plurality of openings located within the silicon substrate and beneath the plurality of patterned dielectric material structures, wherein each opening exposes a surface of the silicon substrate having a (111) crystal plane. The structure of the present disclosure further includes a gallium nitride material surrounding each sidewall of each patterned dielectric material structure and located adjacent to the surface of the silicon substrate having the (111) crystal plane. A semiconductor device can be positioned upon and within the gallium nitride material.

**[0007]** In a further aspect of the present disclosure, a semiconductor structure is provided that includes a (100) silicon substrate having a plurality openings located within the silicon substrate, wherein each opening exposes a surface of the silicon substrate having a (111) crystal plane.

This structure further includes an epitaxial semiconductor material located on an uppermost surface of the (100) silicon substrate, and a gallium nitride material located adjacent to the surface of the silicon substrate having the (111) crystal plane and adjacent a portion of the epitaxial semiconductor material. The structure also includes at least one semiconductor device located upon and within the gallium nitride material and at least one other semiconductor device located upon and within the epitaxial semiconductor material.

## BRIEF DESCRIPTION OF THE DRAWINGS

**[0008]** FIG. 1 is a pictorial representation (through a cross sectional view) illustrating a (100) silicon substrate that can be employed in one embodiment of the present disclosure.

**[0009]** FIG. 2 is a pictorial representation (through a cross sectional view) illustrating the silicon substrate illustrated in FIG. 1 after forming a blanket layer of dielectric material on an uppermost surface of the silicon substrate.

**[0010]** FIG. 3 is a pictorial representation (through a cross sectional view) illustrating the structure of FIG. 2 after forming patterned dielectric material structures from the blanket layer of dielectric material.

**[0011]** FIG. 4 is a pictorial representation (through a cross sectional view) illustrating the structure of FIG. 3 after etching exposed surfaces of the silicon substrate to form openings in the silicon substrate that expose a surface of the silicon substrate having a (111) crystal plane.

**[0012]** FIG. 5 is a pictorial representation (through a cross sectional view) of the structure of FIG. 4 after forming a contiguous A1N buffer layer on exposed surfaces of each patterned

dielectric material structure and on exposed surfaces of the silicon substrate within each opening.

**[0013]** FIG. 6 is a pictorial representation (through a cross sectional view) illustrating the structure of FIG. 5 after forming a gallium nitride material on a portion of the contiguous AIN buffer layer and surrounding each sidewall of each patterned dielectric material structure.

**[0014]** FIGS. 7A, 7B and 7C are scanning electron micrographs (SEMs) of a structure including GaN integrated on a (100) silicon substrate that is formed using the method of the present disclosure.

**[0015]** FIG. 8 is a pictorial representation (through a cross sectional view) illustrating the structure of FIG. 6 after semiconductor device fabrication.

**[0016]** FIG. 9 is a pictorial representation (through a cross sectional view) illustrating the structure of FIG. 6 after formation of another dielectric material.

**[0017]** FIG. 10 is a pictorial representation (through a cross sectional view) illustrating the structure of FIG. 9 after planarization which provides a planar structure.

**[0018]** FIG. 11 is a pictorial representation (through a cross sectional view) illustrating the structure of FIG. 10 after semiconductor device fabrication.

**[0019]** FIG. 12 is a pictorial representation (through a cross sectional view) illustrating the structure of FIG. 6 after removing an uppermost portion of the contiguous AIN buffer layer that lies atop each patterned dielectric material structure.

**[0020]** FIG. 13 is a pictorial representation (through a cross sectional view) illustrating the structure of FIG. 12 after removing each patterned dielectric material structure.

**[0021]** FIG. 14 is a pictorial representation (through a cross sectional view) illustrating the structure of FIG. 13 after epitaxially growth of a semiconductor material on an exposed portion of the uppermost surface of the (100) silicon substrate and planarization.

**[0022]** FIG. 15 is a pictorial representation (through a cross sectional view) illustrating the structure of FIG. 14 after semiconductor device fabrication.

**[0023]** FIG. 16 is a pictorial representation (through a cross sectional view) illustrating the structure of FIG. 13 after removing sidewall portions of the remaining A1N buffer layer.

**[0024]** FIG. 17 is a pictorial representation (through a cross sectional view) illustrating the structure of FIG. 16 after epitaxially growth of a semiconductor material on an exposed portion of the uppermost surface of the (100) silicon substrate and planarization.

**[0025]** FIG. 18 is a pictorial representation (through a cross sectional view) illustrating the structure of FIG. 17 after device fabrication.

**[0026]** FIG. 19 is a pictorial representation (through a cross sectional view) illustrating the structure of FIG. 16 after forming a dielectric material liner.

**[0027]** FIG. 20 is a pictorial representation (through a cross sectional view) illustrating the structure of FIG. 19 after removing portions of the dielectric material liner and forming dielectric spacers.

**[0028]** FIG. 21 is a pictorial representation (through a cross sectional view) illustrating the structure of FIG. 20 after epitaxially growth of a semiconductor material on an exposed portion of the uppermost surface of the (100) silicon substrate and planarization.

**[0029]** FIG. 22 is a pictorial representation (through a cross sectional view) illustrating the structure of FIG. 21 after semiconductor device fabrication.

DETAILED DESCRIPTION

**[0030]** The present disclosure, which provides a method of selectively forming a gallium nitride material on a (100) silicon substrate, and a semiconductor structure including a gallium nitride material surrounding sidewalls of a patterned dielectric material structure and present on a (111) crystal plane of a (100) silicon substrate, will now be described in greater detail by referring to the following discussion and drawings that accompany the present disclosure. It is noted that the drawings are provided for illustrative purposes only and are not drawn to scale.

**[0031]** In the following description, numerous specific details are set forth, such as particular structures, components, materials, dimensions, processing steps and techniques, in order to illustrate the present disclosure. However, it will be appreciated by one of ordinary skill in the art that various embodiments of the present disclosure may be practiced without these, or with other, specific details. In other instances, well-known structures or processing steps have not been described in detail in order to avoid obscuring the various embodiments of the present disclosure.

**[0032]** It will be understood that when an element as a layer, region or substrate is referred to as being "on" or "over" another element, it can be directly on the other element or intervening elements may also be present. In contrast, when an element is referred to as being "directly on" or "directly over" another element, there are no intervening elements present. It will also be understood that when an element is referred to as being "connected" or "coupled" to another element, it can be directly connected or coupled to the other element or intervening elements may be present. In contrast, when an element is referred to as being "directly connected" or "directly coupled" to another element, there are no intervening elements present.

**[0033]** Metalorganic chemical vapor deposition (MOCVD) has been the backbone of the Group Ill-nitrides growth and an industry standard for epitaxial growth of compound semiconductors on a crystalline substrate. There has been a sustained improvement in wafer

throughput by MOCVD making it cost-effective in mass-production. For GaN-based transistors to be competitive: epitaxial process and substrate cost must be < $ 2/cm$^2$ as well as current power device material demand (> $10^7$ 6-inch wafers per year) must be fulfilled through mature process platform.

**[0034]** MOCVD technology is the most mature and scalable to volume production. All commercial electronics have so far been produced with MOCVD systems (especially LED). Silicon substrates are the most scalable and cost effective for volume production. Adequate epitaxial film uniformity, defect levels, device reliability and process cost structure must be achieved to permit the use of gallium nitride (GaN) on Si based devices to achieve widespread use in power electronics. Device processing should be CMOS compatible to achieve commercially viability. Thus, there is a need for the integration of GaN devices on silicon substrates that benefits the MOCVD growth capabilities. Particularly, silicon (100) is of interest due to integration of GaN-based devices with CMOS technology.

**[0035]** Currently, for the MOCVD growth of GaN onto silicon substrates, silicon (111) substrates are employed. Si (111) is preferred for GaN epitaxy due to the three fold symmetry of Si 111 plane and hexagonal structure (six-fold symmetry) of GaN. Si (100) is another substrate of interest due to possible integration of GaN devices with Si (i.e., CMOS) electronics. However, GaN on Si (001) leads to polycrystalline structures or very rough surfaces consisting of many grains. The reason for this is the fourfold symmetry and the possibility for GaN with its sixfold symmetry to grow with two preferred rotational alignments on this surface. For such c-axis oriented material, the lattice mismatch is anisotropic and yields approximately 15% for <112bar0> || Si<lbar00> and 0.7% for <101bar0> || Si <lbar00>. While these mismatch values are lower than for Si (111), the material quality is low due to twist boundaries. Thus, off cut-oriented Si (100) substrates (typically 4° to 7° towards (110)) are preferred for single crystalline GaN epitaxy. However, for true integration with silicon electronics, it is essential to develop GaN epitaxy on non-off cut Si (100) substrates as off cut substrates lead to anisotropy and performance issue in silicon electronic devices.

**[0036]** Although the lattice mismatch between (0001) GaN and (111) Si is -16.8%, the main bottleneck for GaN-on-Silicon epitaxy is the thermal lattice mismatch (approximately -53%) that leads to cracking. The present disclosure provides a method to reconcile the issue of lattice and thermal mismatch of the direct epitaxy growth and thus allow for facile integration of a gallium nitride material and a (100) silicon material. The term "gallium nitride material" as used throughout the present disclosure denotes pure gallium nitride, or gallium nitride that may include other Group III elements such as, for example, Al and/or In. As such, the term "gallium nitride material" as used throughout the present disclosure includes gallium nitride-containing materials such as, for example, GaN, GaAIN, GalnN and GaAlInN.

**[0037]** The method of the present disclosure includes forming a blanket layer of dielectric material on a surface of a (100) silicon substrate. The blanket layer of dielectric material is then patterned forming a plurality of patterned dielectric material structures on the silicon substrate. An etch is employed that selectively removes exposed portions of the silicon substrate. The etch forms openings within the silicon substrate that expose a surface of the silicon substrate having a (111) crystal plane. A contiguous A1N buffer layer is then formed on exposed surfaces of each patterned dielectric material structure and on exposed surfaces of the silicon substrate. A gallium nitride material is then formed on a portion of the contiguous A1N buffer layer and surrounding each sidewall of each patterned dielectric material structure. This method will now be described in greater detail by referring to FIGS. 1-6.

**[0038]** Referring first to FIG. 1, there is illustrated a silicon substrate 10 which has a (100) crystallographic surface orientation that can be employed in one embodiment of the present disclosure. The silicon substrate 10 having the (100) crystallographic surface orientation may also be referred to herein as "a (100) silicon substrate". In one embodiment, and as illustrated in the drawings, the (100) silicon substrate 10 may be a bulk semiconductor material having silicon located between a planar uppermost surface and a planar bottommost surface. In another embodiment, the (100) silicon substrate 10 may be a topmost layer of a silicon-on-insulator substrate. In such an embodiment, an insulator material such as, for example, a dielectric material, can be located between the planar uppermost surface and a planar bottommost surface of the silicon-on-insulator substrate, and the (100) silicon substrate 10 is located on an uppermost surface of the insulator material. A semiconductor material such as,

for example, silicon, germanium, silicon germanium, a III-V compound semiconductor material or a II-V semiconductor material can be located beneath the insulator material of the silicon-on-insulator substrate. In yet another embodiment, the (100) silicon substrate 10 can be a topmost layer of a multilayered stack of semiconductor materials. In still yet another embodiment, the (100) silicon substrate can be a topmost layer of a silicon-on-sapphire substrate.

**[0039]** The (100) silicon substrate 10 that can be employed in the present disclosure is typically a single crystalline material and may be doped, undoped or contain regions that are doped and other regions that are non-doped. The dopant may be an n-type dopant selected from an Element from Group VA of the Periodic Table of Elements (i.e., P, As and/or Sb) or a p-type dopant selected from an Element from Group IIIA of the Periodic Table of Elements (i.e., B, Al, Ga and/or In). The (100) silicon substrate 10 may contain one region that is doped with a p-type dopant and other region that is doped with an n-type dopant. The thickness of the (100) silicon substrate 10 can be from 50 microns to 2 cm, although lesser and greater thickness can also be employed.

**[0040]** Referring now to FIG. 2, there is illustrated the (100) silicon substrate 10 of FIG. 1 after forming a blanket layer of dielectric material 12 on an uppermost surface of the (100) silicon substrate 10. As shown, the blanket layer of dielectric material 12 is a contiguous layer that covers the entire uppermost surface of the (100) silicon substrate 10. In some embodiments, the blanket layer of dielectric material 12 can be comprised of silicon dioxide, silicon nitride, or silicon oxynitride.

**[0041]** In one embodiment of the present disclosure, the blanket layer of dielectric material 12 can be formed using a thermal process including, for example, thermal oxidation, thermal nitridation and thermal oxynitridation. In such an embodiment, the (100) silicon substrate 10 is heated in an oxidizing and/or nitriding ambient at a temperature of 700°C or greater. In another embodiment of the present disclosure, the blanket layer of dielectric material 12 can be formed onto the uppermost surface of the (100) silicon substrate 10 by utilizing a deposition process such as, for example, chemical vapor deposition, and plasma enhanced chemical vapor deposition. Notwithstanding which technique is used in forming the blanket

layer of dielectric material 12, the blanket layer of dielectric material 12 typically has a thickness a few monolayers to as thick as a couple of microns or more.

**[0042]** Referring to FIG. 3, there is illustrated the structure of FIG. 2 after forming a plurality of patterned dielectric material structures (hereinafter patterned dielectric material structures 14) from the blanket layer of dielectric material 12. As shown, the patterned dielectric material structures 14 are located on portions of the uppermost surface of the (100) silicon substrate 10, while other portions of the (100) silicon substrate are exposed.

**[0043]** The patterned dielectric material structures 14 can be formed by lithography and etching. The lithographic step used in forming the patterned dielectric material structures 14 includes applying a blanket layer of a photoresist material on the uppermost surface of the blanket layer of dielectric material, exposing the photoresist material to radiation and developing the exposed photoresist material. The etching step used in forming the patterned dielectric material structures 14 may include a dry etching process or a chemical wet etching process. When a dry etching process is employed, one of reactive ion etching, plasma etching, and ion beam etching can be used. When a chemical wet etch process is employed, a chemical etchant that selectively removes exposed portions of the blanket layer of dielectric material is used. After the etching process has been performed, the patterned photoresist material is stripped from the structure utilizing a conventional resist stripping process such as, for example, ashing.

**[0044]** Each patterned dielectric material structure 14 that is formed has four sides, i.e., four vertical sidewalls, and thus is in the shape of a parallelogram. In one embodiment, each patterned dielectric material structure 14 is a square. In another embodiment, each patterned dielectric material structure 14 is a rectangle.

**[0045]** Each patterned dielectric material structure 14 has a length and width. In some embodiments, the length can equal the width. In other embodiments, the length can be different (greater than or less than) from the width. The length of each patterned dielectric material structure 14 can be within a range from 10 nm to 100 μm, while the width can be from 10 nm to 100 μm. Other width and length values are possible with the upper limit being

application dependent. In the present application, the width of each patterned dielectric material structure 14 runs parallel to the cross section shown in FIG. 3, while the length of each patterned dielectric material structure 14 runs into and out of the cross section shown in FIG. 3.

**[0046]** Referring now to FIG. 4, there is illustrated the structure of FIG. 3 after etching exposed surfaces of the (100) silicon substrate 10 using each patterned dielectric material structures 14 as an etch mask to form openings 17 in the (100) silicon substrate 10 that expose a surface (designated as "A" in FIG. 4) of the (100) silicon substrate 10 within each opening 17 that has a (111) crystal plane. By "(1 11) crystal plane" it is meant any plane within the (111) crystal plane family including, but not limited to, 111, lbarl 1, and 1lbarl. In the drawing, the designation "B" denotes a planar surface of the (100) silicon substrate 10 that has a (100) crystal plane which is located beneath the uppermost surface of the (100) silicon substrate 10. By "(100) crystal plane" it is meant any plane within the (100) crystal plane family.

**[0047]** The etching of the exposed surfaces of the (100) silicon substrate can be performed utilizing a crystallographic wet etch; the crystallographic wet etch may also be referred to as an anisotropic wet etch that is orientation dependent. In one embodiment of the present disclosure, the crystallographic wet etch that is employed includes using KOH as a chemical etchant. Other chemical etchants can be used in the crystallographic wet etch as long as the chemical etchant that is selected is capable of exposing a surface of the (100) silicon substrate 10 having the (111) crystal plane. Examples of other chemical etchants that can be used in the crystallographic wet etch of the present disclosure, include, but are not limited to, an aqueous solution of ethylene diamine and pyrocatechol or tetramethylammonium hydroxide.

**[0048]** In accordance with an aspect of the present disclosure, each opening 17 that is formed within the (100) silicon substrate 10 has an upper portion having a width (wl) that is larger than a width (w2) of a lower portion. In some embodiments of the present disclosure, the width (wl) of the upper portion of each opening 17 is from 250 nm to 10,000 μιη, while the width (w2) of the lower portion of each opening 17 is from 200 nm to 10,000 μτη. In some

embodiments, an upper portion of each opening 17 can extend beneath each of the patterned dielectric material structures 14.

**[0049]** The structure that is shown in FIG. 4 is then heated in a hydrogen atmosphere and then a prealuminization process is performed which stabilizes the surfaces of the silicon substrate. These steps are performed prior to forming the A1N buffer layer, and prior to forming the gallium nitride material. The heating of the structure shown in FIG. 4 in a hydrogen atmosphere includes placing the structure shown in FIG. 4 into a reactor chamber of a metalorganic chemical vapor deposition (MOCVD) apparatus. In some embodiments, and prior to placing the structure shown in FIG. 4 into the MOCVD reactor chamber, the structure can be cleaned using an HF cleaning process. The MOCVD reactor chamber including the structure shown in FIG. 4 is then evacuated to a pressure of about 50-100 mbar or less and then a hydrogen atmosphere is introduced into the reactor chamber. In some embodiments, the pressure within the MOCVD reactor is at atmospheric, i.e., 760 mbar. The hydrogen atmosphere may include pure hydrogen or hydrogen admixed with an inert carrier gas such as, for example, helium and/or argon. When an admixture is employed, hydrogen comprises at least 25 % or greater of the admixture, the remainder of the admixture (up to 100%) is comprised of the inert carrier gas. With the hydrogen atmosphere present in the reactor chamber, the structure is heated to a temperature of about 900°C or less. In one embodiment, the temperature in which the structure shown in FIG. 4 is heated under the hydrogen atmosphere is from 500°C to 600°C. In another embodiment, the temperature in which the structure shown in FIG. 4 is heated under the hydrogen atmosphere is from 600°C to 900°C. Notwithstanding the temperature in which the structure of FIG. 4 is heated under the hydrogen atmosphere, the heating is performed for a time period of 5 minutes to 20 minutes. This step of the present disclosure is believed to clean the surfaces and hydrogenate the exposed surfaces of the (100) silicon substrate. In some embodiments, the heating under hydrogen can be replaced with heating under an inert gas.

**[0050]** Since gallium will react directly with silicon, a prealuminization step is performed to stabilize the silicon nucleation sites prior to forming the gallium nitride material; no Al layer is formed during this step of the present disclosure. If the prealuminization step is not performed, gallium nitride material will not be selectively deposited around the patterned

dielectric material structures. The prealuminization step is performed by introducing an organoaluminum precursor such as, for example, a trialkylaluminum compound, wherein the alkyl contains from 1 to 6 carbon atoms, into the reactor chamber. Examples of trialkylaluminum compounds that can be employed in the present disclosure, include, but are not limited to, trimethylaluminum, triethylaluminum, and tributylaluminum. The organoaluminum precursor can be introduced in the reactor chamber of the MOCVD apparatus neat, or it can be admixed with an inert carrier gas. The prealuminization step is typically performed at a temperature of 450°C or greater. In one embodiment, the introducing of the organoaluminum precursor typically occurs at a temperature from 500°C to 600°C. In another embodiment, the introduction of the organoaluminum precursor occurs at a temperature from 600°C to 900°C. Notwithstanding the temperature in which the organoaluminum precursor is introduced into the reactor chamber, the prealuminization is performed for a time period of 5 seconds to 120 seconds.

**[0051]** After heating the structure shown in FIG. 4 in hydrogen and performing the above mentioned prealuminization step, a contiguous AIN buffer layer 18 is formed on exposed surfaces of each patterned dielectric material structure 14 and on exposed surfaces (A,B) of the (100) silicon substrate 10. The resultant structure including the contiguous AIN buffer layer 18 is shown, for example, in FIG. 5.

**[0052]** The contiguous AIN buffer layer 18 is formed by introducing an organoaluminum precursor (i.e., a trialkylaluminum compound as mentioned above) and a nitride precursor such as, for example, ammonium nitride into the reactor chamber of the MOCVD apparatus. An inert earner gas may be present with one of the precursors used in forming the contiguous AIN buffer layer 18, or an inert carrier gas can be present with both the precursors used in forming the contiguous AIN buffer layer 18. The contiguous AIN buffer layer 18 is typically formed at a temperature of 600°C or greater. In one embodiment, the deposition of the contiguous AIN buffer layer 18 typically occurs at a temperature from 650°C to 850°C. In another embodiment, the deposition of the contiguous AIN buffer layer 18 typically occurs at a temperature from 850°C to 1050°C. Notwithstanding the temperature in which the contiguous AIN buffer layer 18 is formed, the deposition of the contiguous AIN buffer layer 18 is performed for a time period of 1 minute to 20 minutes. The contiguous AIN buffer

layer 18 that is formed typically has a thickness from 10 nm to 250 nm, with a thickness from 60 nm to 80 nm being even more typical. The Applicant of the present application has found that when the contiguous A1N buffer layer 18 is within the above described ranges, the selectivity of gallium nitride material deposition can be improved when a thicker A1N buffer layer is formed. For example, a 64 nm A1N buffer layer provides higher selectivity for gallium nitride material deposition as compared to a 32 nm A1N buffer layer. The 32 nm A1N buffer layer provides higher selectivity for gallium nitride material deposition as compared to a 10 nm A1N buffer layer.

**[0053]** Referring now to FIG. 6, there is illustrated the structure of FIG. 5 after selectively forming a gallium nitride material 20 surrounding each sidewall of each patterned dielectric material structure 14 and located adjacent the surface (i.e., surface A) of the silicon substrate having the (111) crystal plane. In some embodiments, and as illustrated in FIG. 6, a bottommost surface of the gallium nitride material 20 may extend above the planar surface (designated previously as B) of the (100) silicon substrate 10 that has a (100) crystal plane.

**[0054]** The gallium nitride material 20 that is formed at this point of the present disclosure is a contiguous material layer. In one embodiment of the present disclosure, the gallium nitride material 20 located adjoining corners of each patterned dielectric material structure 14 has a first thickness and the gallium nitride material 20 located adjoining sidewalls of each patterned dielectric material structure 14 has a second thickness, wherein the second thickness is greater than the first thickness. This aspect of the present disclosure can also be seen more clearly within the SEMs shown in FIGS. 7B and 7C of the present disclosure.

**[0055]** In some embodiments of the present disclosure, and as illustrated in FIG. 6, a space 21 is present between the gallium nitride material 20 that is located around different patterned dielectric material structures 14. In other embodiments (not shown), no space is present between the gallium nitride material 20 that is surrounding different patterned dielectric material structures. In some embodiments, the gallium nitride material 20 may have an uppermost surface that is coplanar with the uppermost surface of each patterned dielectric material structure 14. In other embodiments the gallium nitride material 20 may have an uppermost surface that is vertically offset, either above or below, the uppermost surface of

each patterned dielectric material structure 14.

**[0056]** In one embodiment of the present disclosure, the gallium nitride material 20 is pure gallium nitride. In another embodiment of the present disclosure, the gallium nitride material 20 comprises gallium nitride that includes at least one other Group III element such as, for example, Al and/or In. In such an embodiment, the gallium nitride material 20 may comprise GaAIN, GalnN or GaAlInN.

**[0057]** Notwithstanding the composition of the gallium nitride material 20, the gallium nitride material 20 is single crystal. Also, the gallium nitride material 20 that is formed is a single phase material. By "single phase material" it is meant wurtzite phase: c-direction of GaN is aligned with (111) direction of the original (100) silicon substrate.

**[0058]** The deposition of the gallium nitride material 20 includes introducing an organogallium precursor and a nitride precursor such as, for example, ammonium nitride into the reactor chamber of the MOCVD apparatus. In some embodiments, an optional organoaluminum precursor (such as described above) and/or an optional organoindium precursor (such as, for example, a trialkylindium compound, e.g., trimethylindium) can also be used. Examples of organogallium precursors that can be employed in the present disclosure include trialkylgallium compounds such as, for example, trimethylgallium and triethlygallium. An inert carrier gas may be present with one of the precursors used in forming the gallium nitride material 20, or an inert carrier gas can be present with both the precursors used in forming the gallium nitride material 20. The deposition of the gallium nitride material is typically performed at a temperature of 850°C or greater. In one embodiment, the deposition of the gallium nitride material 20 typically occurs at a temperature from 900°C to 1200°C. In another embodiment, the deposition of the gallium nitride material 20 typically occurs at a temperature from 1200°C to 1400°C. Notwithstanding the temperature in which the gallium nitride material 20 is formed, the deposition of the gallium nitride material 20 is performed for a time period of 1 minute to 2 hours. The gallium nitride material 20 that is formed typically has a thickness from 100 nm to 5000 nm, with a thickness from 500 nm to 1000 nm being even more typical.

**[0059]** Referring now to FIGS. 7A (large area of a bulk (100) silicon substrate processed in accordance with the present disclosure), 7B (top down view of Structure 1 highlighted in FIG. 7A) and 7C (bird's eye view at the area near Structure 1 highlighted in FIG. 7B), there are illustrated actual scanning electron micrographs (SEMs) of a structure that is formed using the method of the present disclosure. As can been seen from these SEMs, the method of the present disclosure provides selective and control growth of a gallium nitride material around the patterned dielectric material structures and square patterns can be achieved. Also, the method of the present disclosure proves a highly uniform and controlled distribution of gallium nitride material around the patterned dielectric material structures.

**[0060]** After forming the structure shown in FIG. 6, semiconductor devices such as, for example, field effect transistors (FET), photonic devices (i.e., light emitting diodes or laser diodes) and combinations thereof, can be formed using conventional process that are well known to those skilled in the art. In some embodiments, the semiconductor devices can be formed upon and within the gallium nitride material 20. In other embodiments, the semiconductor devices can be formed upon and within the gallium nitride material 20 and on an epitaxial semiconductor material that can be grown adjacent the gallium nitride material 20 and on an exposed uppermost surface of the original (100) silicon substrate 10. When FETs are formed upon and within the gallium nitride material 20, a portion of the gallium nitride material 20 can serve as a device channel and a gate stack including at least a gate dielectric material and gate electrode can be formed above the device channel utilizing conventional silicon complementary metal oxide semiconductor (CMOS)-like processes. In some embodiments, the FETs built atop the gallium nitride material 20 can be interconnected with existing silicon CMOS circuits to form a hybrid system. Some examples of fabricating semiconductor devices are now described. In some embodiments, a photonic device can be sandwiched between a topmost and bottommost surface of the (100) silicon substrate 10.

**[0061]** Reference is first made to the structure shown in FIG. 8 which shows the structure of FIG. 6 after forming semiconductor devices 50 upon and within the gallium nitride material 20. In some embodiments, an interconnect 52 can be present above a patterned dielectric material structure 14 that connects one of the semiconductor devices 50 to a neighboring semiconductor device 50. In this embodiment, the semiconductor devices 50 can be FETs

that are formed upon and within the gallium nitride material 20, and interconnect 52 can be a conductive material.

**[0062]** Reference is now made to FIGS. 9-11 which illustrate another embodiment of the present disclosure in which the structure shown in FIG. 6 can be used as a template for forming semiconductor devices thereon. Specifically, FIG. 9 illustrates the structure of FIG. 6 after formation of another dielectric material 54. The another dielectric material 54 may include one of the dielectric materials mentioned above, or the another dielectric material 54 may include a planarizing dielectric material such as, for example, a photoresist, a silicate glass, or an oxide such as silicon dioxide. As shown, the another dielectric material 54 can fill the space between neighboring gallium nitride material 20 which is located on different patterned dielectric material structures 14. Also, and as shown, the another dielectric material 54 can be present atop the gallium nitride material 20 and atop a portion of the contiguous AlN buffer layer 18 that is present on uppermost surfaces of each of the patterned dielectric material structures 14.

**[0063]** The another dielectric material 54 can be formed by a deposition process including, but not limited to, chemical vapor deposition, plasma chemical vapor deposition, chemical solution deposition, evaporation and spin-on coating. The thickness of the another dielectric material 54 is typically from 100 nm to 10,000 nm, with a thickness from 2000 nm to 4000 nm being more typical for chemical-mechanical polishing purposes. Other thickness can be employed so long as the uppermost surface of the another dielectric material 54 is above a horizontal portion of the contiguous AIN buffer layer 18 that is present on the uppermost surface of each of the patterned dielectric material structures 14.

**[0064]** Referring now to FIG. 10, there is illustrated the structure of FIG. 9 after performing planarization which removes a portion of the another dielectric material 54 and the horizontal portion of the contiguous AIN buffer layer 18 that is present on uppermost surface of each of the patterned dielectric material structures 14 stopping on an uppermost surface of the gallium nitride material 20 and an uppermost surface of each patterned dielectric material structure 14. A planar structure is provided in which remaining portions of the another dielectric material 54', vertical portions of the AIN buffer layer 18', gallium nitride material

20, and each patterned dielectric material structure 14 have uppermost surfaces that are coplanar with each other. The planarization process that is used in the present disclosure may include chemical mechanical polishing and/or grinding.

**[0065]** Referring now to FIG. 11, there is illustrated the structure of FIG. 10 after semiconductor device fabrication. In this embodiment, semiconductor devices 50, e.g., FETs, and interconnects 52 can be formed on one side of the structure including the exposed gallium nitride material 20, photonic devices 53 such as light emitting diodes or laser diodes, and their other contacts can be formed on the opposite side of the structure and on an exposed surface of the original (100) silicon substrate.

**[0066]** Reference is now made to FIGS. 12-15 which illustrate yet another embodiment of the present disclosure in which semiconductor devices can be formed using the structure shown in FIG. 6. Specifically, FIG. 12 illustrates the structure of FIG. 6 after removing an uppermost horizontal portion of the contiguous A1N buffer layer 18 that lies atop each patterned dielectric material structure 14. The removal of the uppermost horizontal portion of the contiguous A1N buffer layer 18 that lies atop each patterned dielectric material structure 14 can be performed by planarization. The remaining portion of the A1N buffer layer is labeled as 18'. As shown in the drawing, each of the patterned dielectric material structures 14 is exposed.

**[0067]** Referring now to FIG. 13, there is illustrated the structure of FIG. 12 after removing each patterned dielectric material structure 14 so as to expose a portion of the uppermost surface of the original (100) silicon substrate 10. The removal of each of the exposed patterned dielectric material structure 14 can be performed utilizing an etching process that selectively removes the dielectric material that constitutes the patterned dielectric material structures 14 from the structure. Examples of such an etching process that can be used at this point of the present disclosure include, but are not limited to, hydrofluoric acid.

**[0068]** Referring now to FIG. 14, there is illustrated the structure of FIG. 13 after epitaxially growth of a semiconductor material 56 (the semiconductor material 56 may also be referred to as an epitaxial semiconductor material since it is formed utilizing an epitaxial process) on

the exposed portion of the uppermost surface of the (100) silicon substrate 10 and planarization. As shown, sidewall surfaces of the semiconductor material 56 contact pillar portions of the remaining portion of the A1N buffer layer 18', and a bottommost surface of the semiconductor material 56 contacts the uppermost surface of the (100) silicon substrate 10.

**[0069]** Epitaxially growing, epitaxial growth and/or deposition" mean the growth of a semiconductor material on a deposition surface of a semiconductor material, in which the semiconductor material being grown has the same crystalline characteristics as the semiconductor material of the deposition surface. In the present embodiment, the semiconductor material 56 has the same crystalline characteristics as that of the physically exposed uppermost surface of the (100) silicon substrate 10. When the chemical reactants are controlled and the system parameters set correctly, the depositing atoms arrive at the deposition surface with sufficient energy to move around on the surface and orient themselves to the crystal arrangement of the atoms of the deposition surface. Thus, an epitaxial film deposited on a {100} crystal surface will take on a {100} orientation. In some embodiments, the epitaxial deposition process is a selective deposition process.

**[0070]** The semiconductor material 56 that can be epitaxially deposited includes any semiconductor material such as, for example, silicon (Si), germanium (Ge), and silicon germanium (SiGe). In one embodiment, the semiconductor material 56 includes a same semiconductor material as that of the silicon substrate 10. In another embodiment, the semiconductor material 56 includes a different semiconductor material as that of the silicon substrate 10. It is noted that the specific material compositions for the semiconductor material 56 are provided for illustrative purposes only, and are not intended to limit the present disclosure, as any semiconductor material that may be formed using an epitaxial growth process.

**[0071]** A number of different sources may be used for the deposition of semiconductor material 56. In some embodiments, in which the semiconductor material 56 is composed of silicon, the silicon gas source for epitaxial deposition may be selected from the group consisting of hexachlorodisilane ($Si_2Cl_6$), tetrachlorosilane ($SiCl_4$), dichlorosilane ($Cl_2SiH_2$),

trichlorosilane ($Cl_3SiH$), methylsilane ($(CH_3)SiH_3$), dimethylsilane ($(CH_3)_2SiH_2$), ethylsilane ($(CH_3CH_2)Si¾$), methyldisilane ($(CH_3)Si_2H_5$), dimethyldisilane ($(CH_3)_2Si_2H_4$), hexamethyldisilane ($(CH_3)_6Si_2$) and combinations thereof. In some embodiments, in which semiconductor material 56 is composed of germanium, the germanium gas source for epitaxial deposition may be selected from the group consisting of germane ($GeH_4$), digermane ($Ge_2H_6$), halogermane, dichlorogermane, trichlorogermane, tetrachloro germane and combinations thereof. In some embodiments, in which the semiconductor material 56 is composed of silicon germanium, the silicon sources for epitaxial deposition may be selected from the group consisting of silane, disilane, trisilane, tetrasilane, hexachlorodisilane, tetrachlorosilane, dichlorosilane, trichlorosilane, methylsilane, dimethylsilane, ethylsilane, methyldisilane, dimethyldisilane, hexamethyldisilane and combinations thereof, and the germanium gas sources may be selected from the group consisting of germane, digermane, halogermane, dichlorogermane, trichlorogermane, tetrachloro germane and combinations thereof.

**[0072]** The temperature for epitaxial semiconductor deposition typically ranges from 550°C to 900°C. Although higher temperature typically results in faster deposition, the faster deposition may result in crystal defects and film cracking. The apparatus for performing the epitaxial growth may include a chemical vapor deposition (CVD) apparatus, such as atmospheric pressure CVD (APCVD), low pressure CVD (LPCVD), plasma enhanced CVD (PECVD), metal-organic CVD (MOCVD) and others. The epitaxial semiconductor material 56 that is deposited can be doped or undoped. By "undoped" it is meant that the maximum dopant concentration of p-type or n-type dopants that are present in the epitaxial semiconductor material is less than $5x10^{17}$ atoms/$cm^3$.

**[0073]** Following the epitaxial growth of semiconductor material 56, a planarization process such as chemical mechanical polishing and/or grinding can be used to provide the planar structure shown in FIG. 14.

**[0074]** Referring now to FIG. 15, there is illustrated the structure of FIG. 14 after semiconductor device fabrication, In this embodiment, semiconductor devices 50, e.g., FETs,

are formed upon and within both the gallium nitride material 20 and the semiconductor material 56.

**[0075]** Reference is now made to FIGS. 16- 18 which illustrate a further embodiment of the present disclosure which employs the structure shown in FIG. 6 as a template structure for forming semiconductor devices. Specifically, FIG. 16 illustrates the structure of FIG. 13 after removing sidewall portions, i.e., pillar portions, of the remaining AIN buffer layer so as to expose a potion of a sidewall of each gallium nitride material. The removal of the pillar portions of the remaining AIN buffer layer can be performed utilizing an etching process that selectively removes the exposed sidewall portions of the remaining AIN buffer layer. In one embodiment of the present disclosure, the etching process that can be used to selectively remove the exposed sidewall portions of the remaining AIN buffer layer comprises potassium hydroxide (KOH) or sulfuric acid ($H_2S0_4$). As shown, a portion of the AIN buffer layer (labeled as 18") remains within each of the openings that were formed into the (100) silicon substrate, and a topmost surface of element 18" is coplanar with an uppermost surface of the original (100) silicon substrate.

**[0076]** Referring now to FIG. 17, there is illustrated the structure of FIG. 16 after epitaxially growth of a semiconductor material 56 on an exposed portion of the uppermost surface of the (100) silicon substrate and planarization. The material of semiconductor material 56, epitaxial growth process, and planarization process used in this embodiment is the same as that mentioned above for forming the structure shown in FIG. 14. In this embodiment of the present disclosure a gap 55 is present between the semiconductor material 56 and the gallium nitride material 20.

**[0077]** Referring now to FIG. 18, there is illustrated the structure of FIG. 17 after semiconductor device fabrication. In this embodiment, semiconductor devices 50, e.g., FETs, are formed upon and within both the gallium nitride material 20 and the semiconductor material 56. An interconnect 52 can be present which can connect semiconductor devices located on the gallium nitride material to semiconductor devices located on the semiconductor material 56.

**[0078]** Reference is now made to FIGS. 19-22 which illustrate a yet further embodiment of the present disclosure which employs the structure shown in FIG. 6 as a template structure for forming semiconductor devices. Specifically, FIG. 19 illustrates the structure of FIG. 16 after forming a dielectric material liner 58. The dielectric material liner 58 may comprise a dielectric oxide, dielectric nitride, and/or dielectric oxynitride. In one embodiment of the present disclosure, the dielectric material liner 58 comprises silicon dioxide or silicon nitride. The dielectric material liner 58 can be formed utilizing a conformal deposition process such as, for example, chemical vapor deposition, plasma enhanced chemical vapor deposition or atomic layer deposition. By "conformal" it is meant that the deposition provides a film that defines a morphologically uneven interface with another body and has a thickness that is substantially the same (i.e., ± 10 Angstroms) everywhere along the interface. The thickness of the dielectric material liner 58 can be from 2 nm to 5 nm, although lesser and greater thicknesses can also be employed.

**[0079]** Referring now to FIG. 20, there is illustrated the structure of FIG. 19 after removing portions of the dielectric material liner 58 and forming dielectric spacers 60. The removal of portions of the dielectric material liner 58 can be performed utilizing an etching process such as, for example, reactive ion etching (RIE). As shown, the portions of the dielectric material liner 58 that are removed are located on horizontal surfaces of the structure shown in FIG. 19.

**[0080]** Referring now FIG. 21, there is illustrated the structure of FIG. 20 after epitaxially growth of a semiconductor material 56 on an exposed portion of the uppermost surface of the (100) silicon substrate and planarization. The material of semiconductor material 56, epitaxial growth process, and planarization process used in this embodiment is the same as that mentioned above for forming the structure shown in FIG, 14. It is noted that during the epitaxial grown of the semiconductor material 56, polycrystalline semiconductor material 62 forms in the space that is present between different portions of gallium nitride material 20.

**[0081]** FIG. 22 is a pictorial representation (through a cross sectional view) illustrating the structure of FIG. 21 after semiconductor device fabrication. In this embodiment, semiconductor devices 50, e.g., FETs, are formed upon and within both the gallium nitride material 20 and the semiconductor material 56. An interconnect 52 can be present which can

connect semiconductor devices located on the gallium nitride material to semiconductor devices located on the semiconductor material 56.

**[0082]** While the present disclosure has been particularly shown and described with respect to various embodiments thereof, it will be understood by those skilled in the art that the foregoing and other changes in forms and details may be made without departing from the spirit and scope of the present disclosure. It is therefore intended that the present disclosure not be limited to the exact forms and details described and illustrated, but fall within the scope of the appended claims.

CLAIMS

What is claimed is:

1. A method for selectively forming a gallium nitride material (20) on a silicon substrate (10), said method comprising:

forming a blanket layer of dielectric material (12) on an uppermost surface of a (100) silicon substrate (10);

patterning said blanket layer of dielectric material (12) forming a plurality of patterned dielectric material structures (14) on portions of the uppermost surface of the (100) silicon substrate (10) and exposing other portions of the uppermost surface of the (100) silicon substrate (10);

etching said exposed other portions of the uppermost surface of the (100) silicon substrate to expose a surface having a (111) crystal plane within the (100) silicon substrate (10);

forming a contiguous A1N buffer layer (18) on exposed surfaces of each patterned dielectric material structure (14) and on exposed surfaces of the silicon substrate (10); and

forming a gallium nitride material (20) on a portion of the contiguous A1N buffer layer (18) and surrounding each sidewall of each patterned dielectric material structure (14).

2. The method of Claim 1, wherein the blanket layer of dielectric material (12) is formed by a thermal process.

3. The method of Claim 1, wherein said patterning of said blanket layer of dielectric material (12) comprises forming a blanket layer of photoresist material on said blanket layer of dielectric material (12), exposing said blanket layer of photoresist material to radiation, developing the exposed photoresist material, and etching exposed portions of the blanket layer of dielectric material (12).

4. The method of Claim 1, wherein each patterned dielectric material structure(14) has four sidewalls.

5. The method of Claim 1, wherein said etching the exposed other portions of the uppermost surface of the (100) silicon substrate (10) comprises a crystallographic wet etch.

6. The method of Claim 1, further comprising heating the etched silicon substrate (10) including said plurality of patterned dielectric material stractures (14) in an atmosphere of hydrogen and prealuminizing the exposed surfaces of the silicon substrate (10).

7. The method of Claim 6, wherein said heating in the atmosphere of hydrogen is performed at a temperature of about 900°C or less.

8. The method of Claim 6, wherein said prealuminizing comprises introducing an organoaluminum precursor to said etched silicon substrate for a time period from 5 second to 120 seconds.

9. The method of Claim 1, wherein said forming the contiguous A1N buffer layer (18) comprises introducing an organoaluminum precursor and a nitride precursor and depositing said precursors at a temperature of 600°C or greater.

10. The method of Claim 9, wherein said organoaluminum precursor comprises a trialkylaluminum compound, and said nitride precursor comprises ammonium nitride.

11. The method of Claim 1, wherein said contiguous A1N buffer layer (18) has a thickness from 10 nm to 250 nm.

12. The method of Claim 1, wherein said forming said gallium nitride material (20) comprises metalorganic chemical vapor deposition (MOCVD), and said MOCVD is performed at a temperature from 850°C or greater.

13. The method of Claim 1, wherein said gallium nitride material (20) is selected from GaN, GaAIN, GalnN and GaAlInN.

14. The method of Claim 1, wherein said gallium nitride material (20) is single crystal and is of a single phase, wherein said single phase is a wurtzite phase.

15. The method of Claim 1, wherein said etching the exposed other portions of the uppermost surface of the (100) silicon substrate (10) forms a plurality of openings (17) within the (100) silicon substrate (10), wherein each opening of said plurality of openings (17) has an upper portion having a width that is larger than a width of a lower portion.

16. The method of Claim 1, further comprising forming at least one semiconductor device (50) upon and within said gallium nitride material (20).

17. The method of Claim 1, further comprising:

forming another dielectric material (54) on exposed surfaces of the contiguous A1N buffer layer (18), exposed surfaces of the gallium nitride material (20) and exposed surfaces of the (100) silicon substrate (10);

planarizing the another dielectric material (54) to provide a planar structure in which uppermost surfaces of the gallium nitride material (20), remaining A1N buffer layer (18), remaining portion of the another dielectric material (54) and the patterned dielectric structures (14) are coplanar with each other; and

forming at least one semiconductor device (50) upon and within said gallium nitride material (20).

18. The method of Claim 17, further comprising forming a photonic device (53) via placing contacts on an exposed bottommost surface of the (100) silicon substrate (10).

19. The method of Claim 1, further comprising:

removing a horizontal portion of said contiguous A1N buffer layer (18) from atop each of the patterned dielectric material structures (14), wherein an uppermost surface of each patterned dielectric structure (14) is exposed;

removing each patterned dielectric material structure (14) to expose a portion of the uppermost surface of the (100) silicon substrate (10);

epitaxially growing a semiconductor material (56) on said exposed portion of the uppermost surface of the (100) silicon substrate (10); and

forming semiconductor devices (50) upon and within the gallium nitride material (20) and upon within said semiconductor material (56).

20. The method of Claim 1, further comprising:

removing a horizontal portion of said contiguous A1N buffer layer (18) from atop each of the patterned dielectric material structures (14), wherein an uppermost surface of each patterned dielectric structure (14) is exposed;

removing each patterned dielectric material structure (14) to expose a portion of the uppermost surface of the (100) silicon substrate (10);

removing exposed portions of a remaining portion of the contiguous A1N buffer layer (18) exposing a portion of a sidewall surface of said gallium nitride material (20);

epitaxially growing a semiconductor material (56) on said exposed portion of the uppermost surface of the (100) silicon substrate (10), wherein a gap is present between the semiconductor material (56) and the exposed portion of the sidewall surface of said gallium nitride material (20); and

forming semiconductor devices (50) upon and within the gallium nitride material (20) and upon within said semiconductor material (56).

21. The method of Claim 1,

removing a horizontal portion of said contiguous A1N buffer layer (18) from atop each of the patterned dielectric material structures (14), wherein an uppermost surface of each patterned dielectric structure (14) is exposed;

removing each patterned dielectric material structure (14) to expose a portion of the uppermost surface of the (100) silicon substrate (10);

removing exposed portions of a remaining portion of the contiguous A1N buffer layer (18) exposing a portion of a sidewall surface of said gallium nitride material (20);

forming a dielectric spacer (60) on each exposed sidewall surface of said gallium nitride material (20);

epitaxially growing a semiconductor material (56) on said exposed portion of the uppermost surface of the (100) silicon substrate (10); and

forming semiconductor devices (50) upon and within the gallium nitride material (20) and upon within said semiconductor material (56).

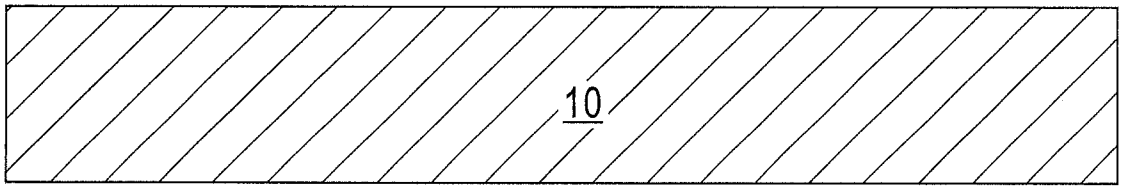


FIG. 1

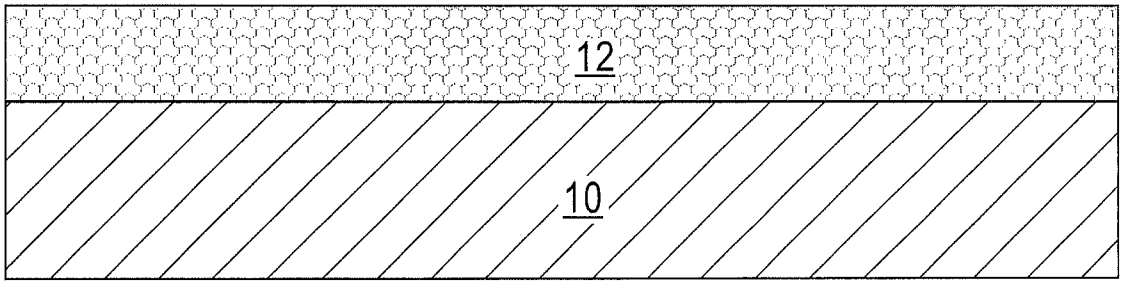


FIG. 2

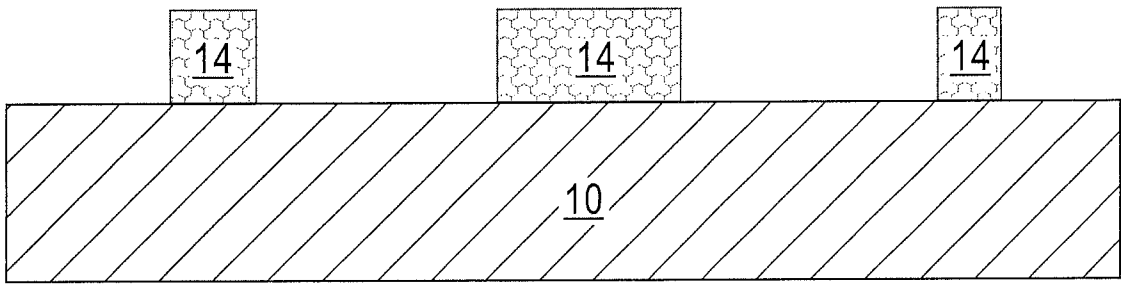


FIG. 3

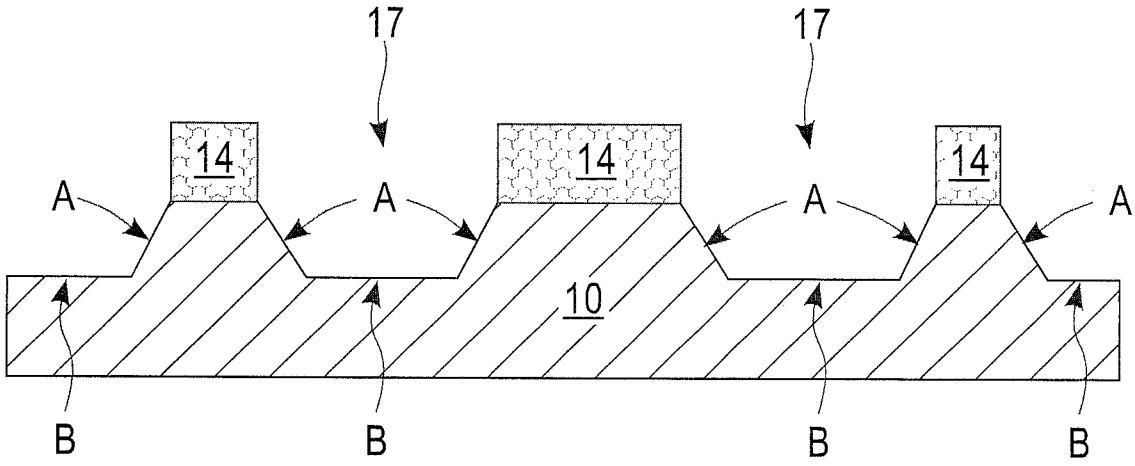


FIG. 4

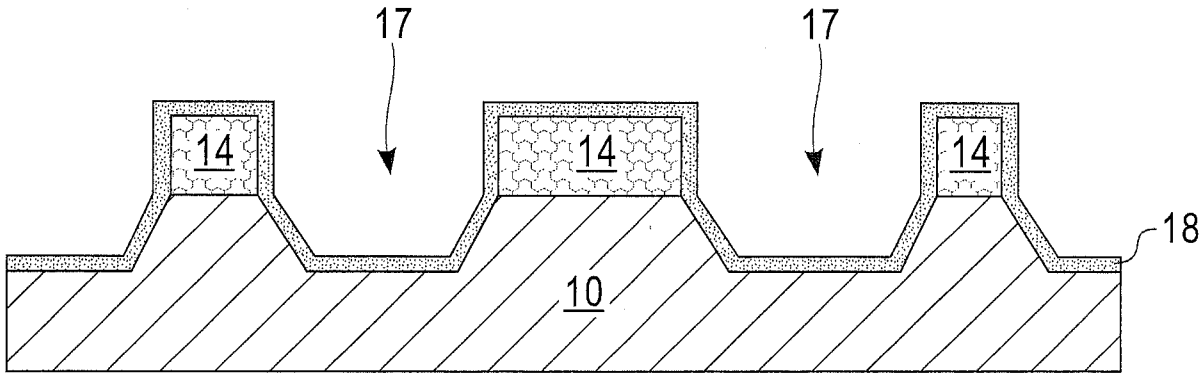


FIG. 5

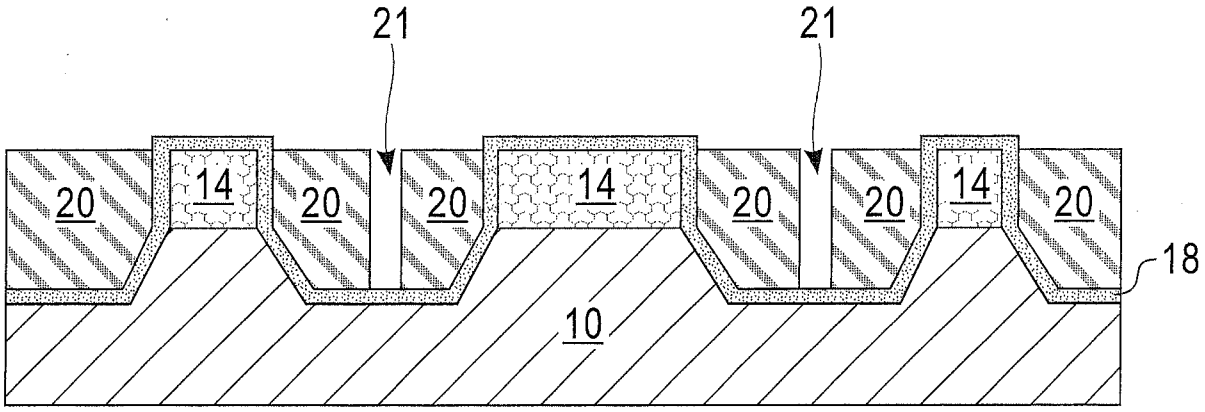


FIG. 6

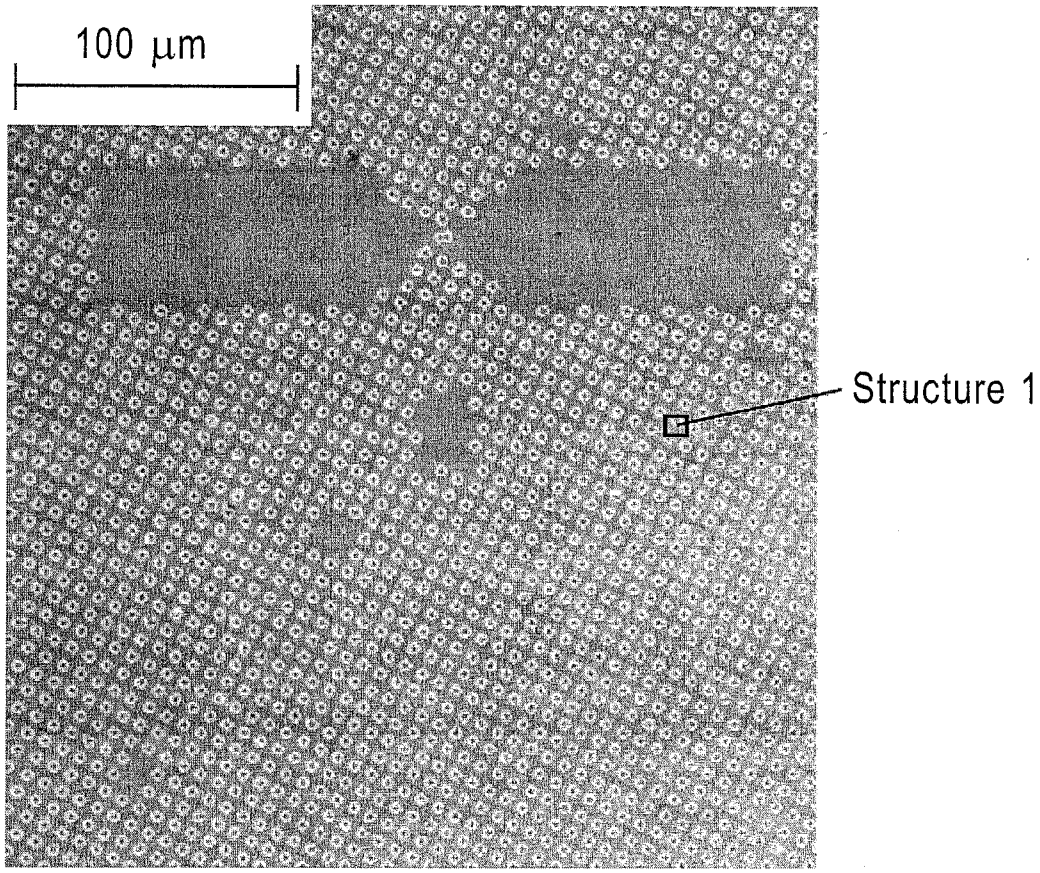


FIG. 7A

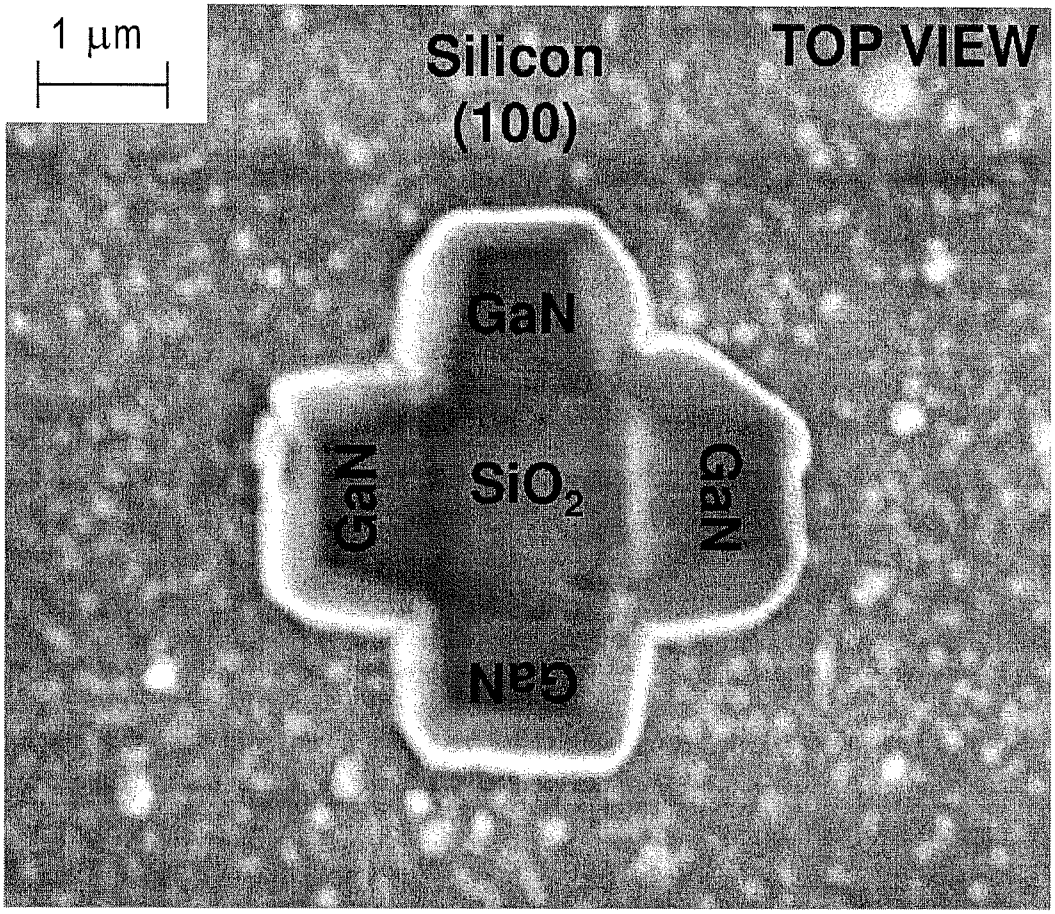


FIG. 7B

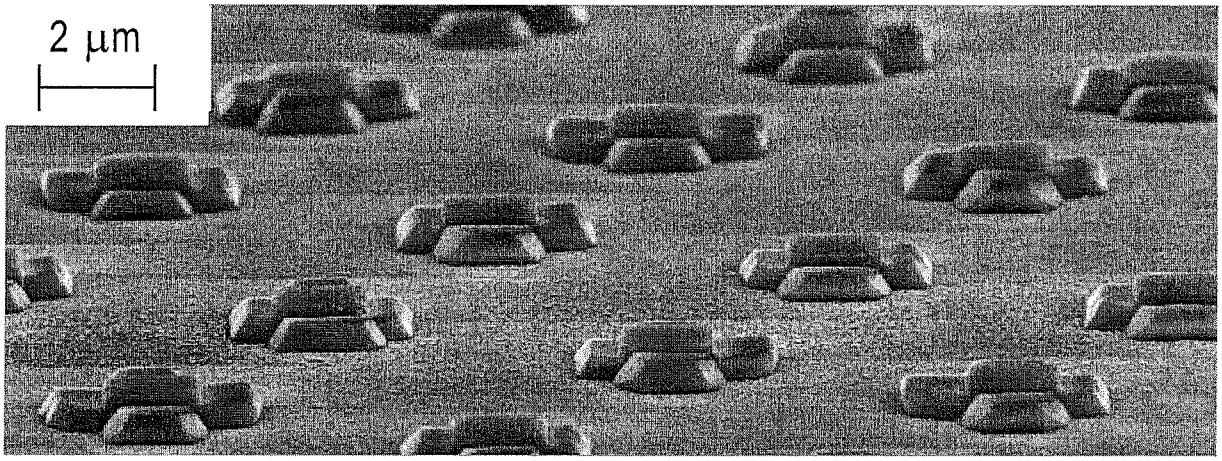


FIG. 7C

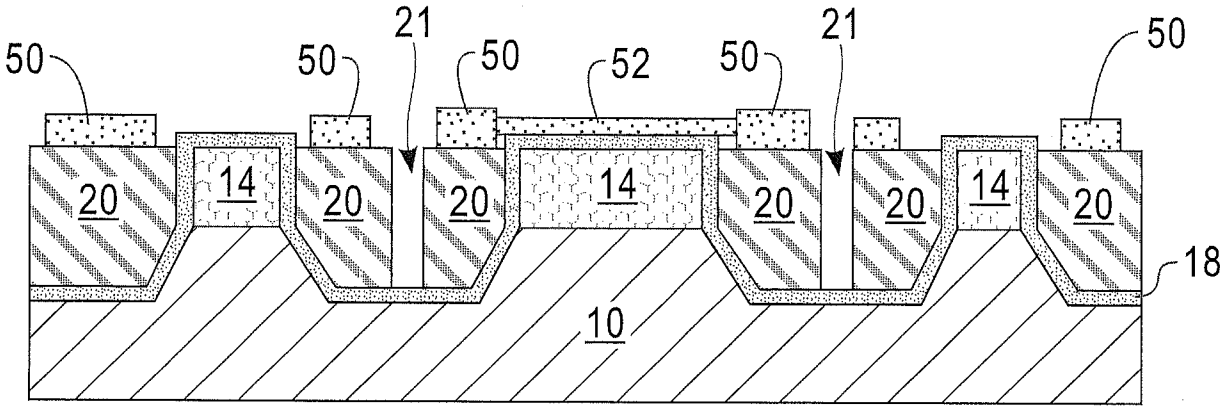


FIG. 8

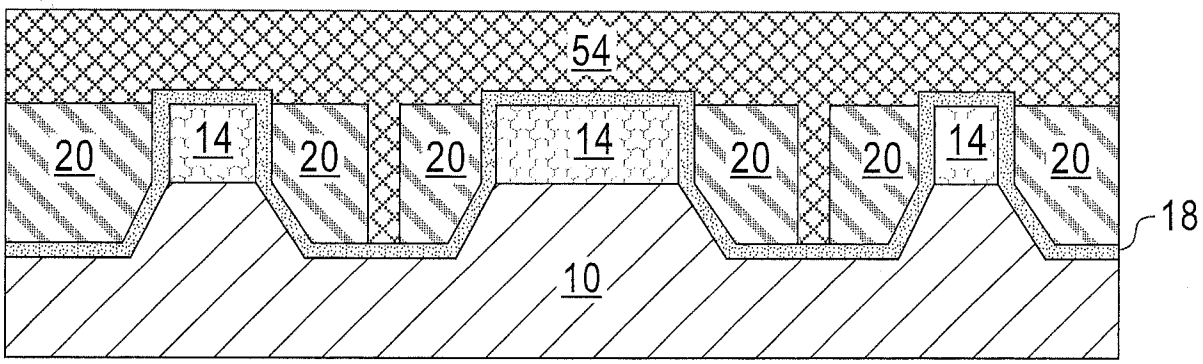


FIG. 9

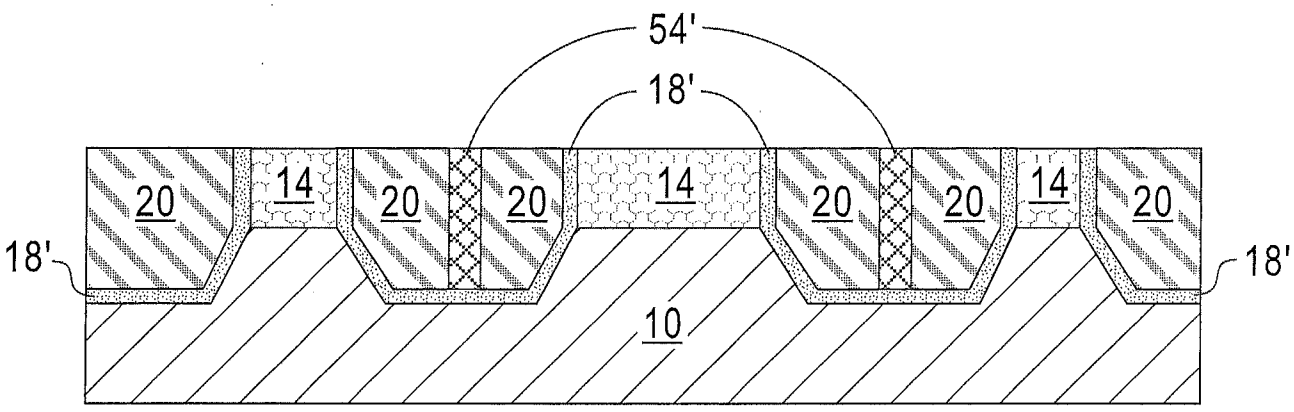


FIG. 10

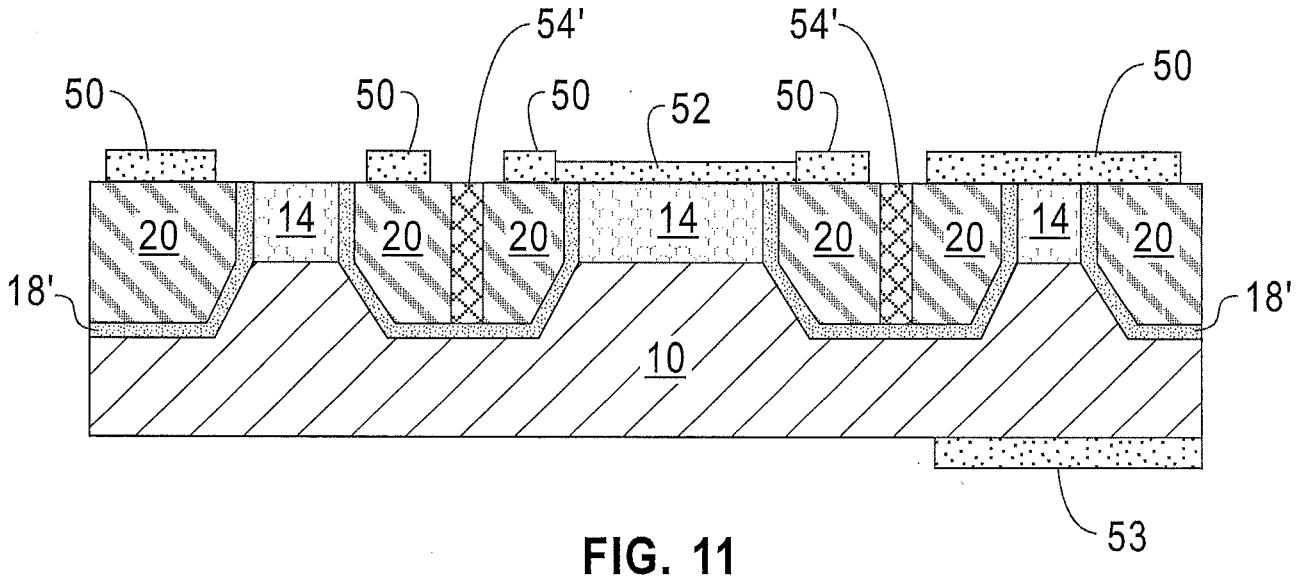


FIG. 11

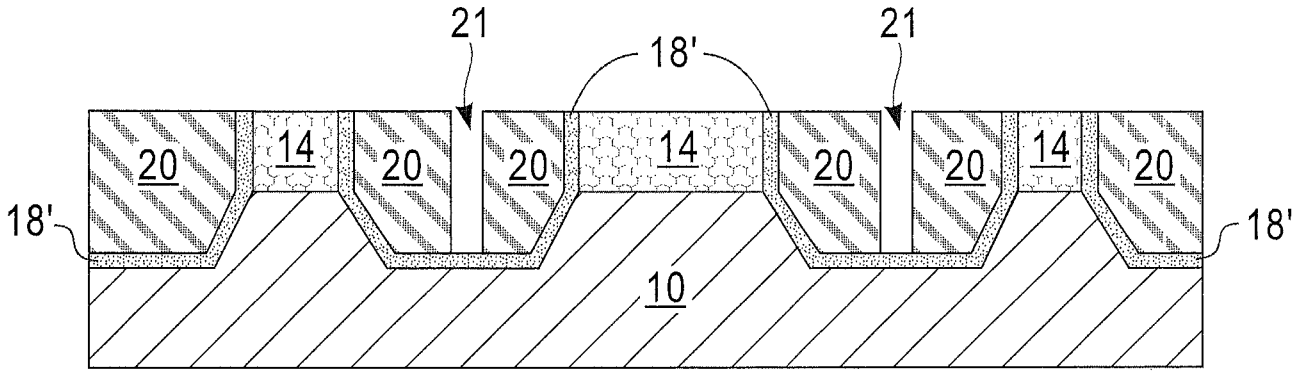


FIG. 12

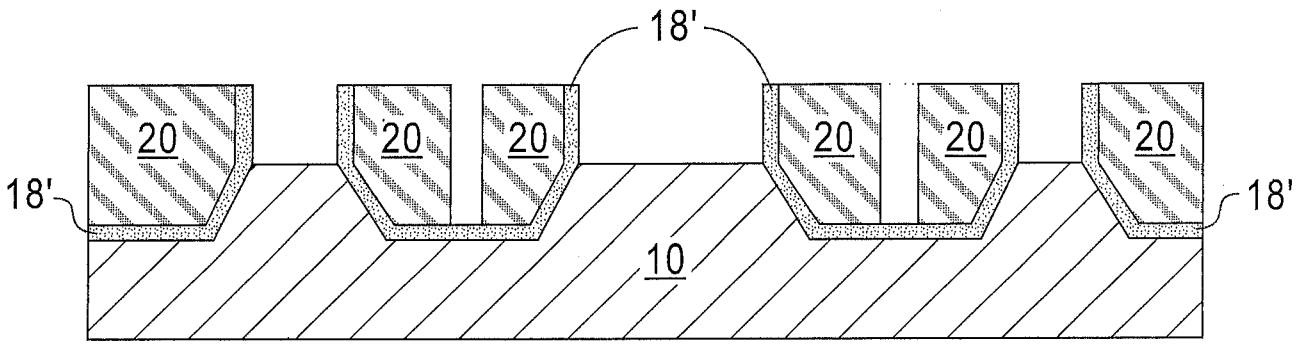


FIG. 13

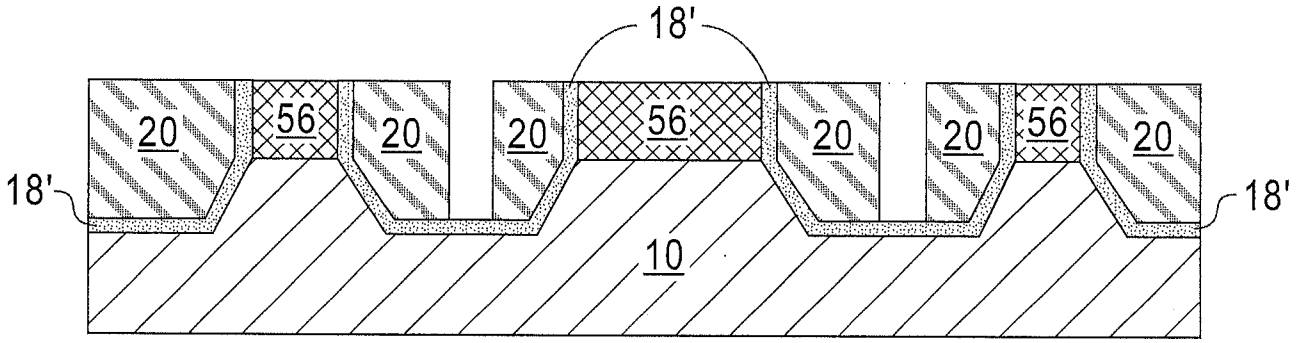


FIG. 14

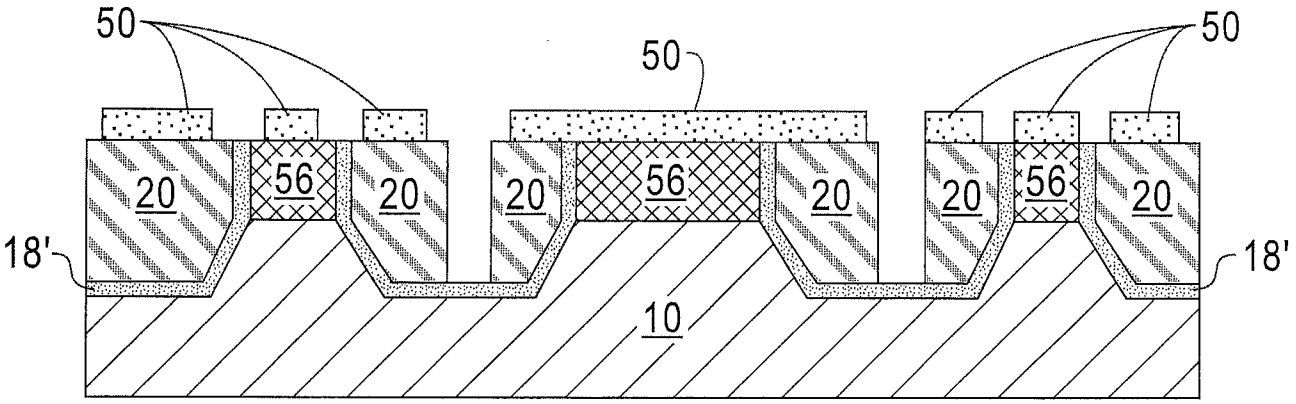


FIG. 15

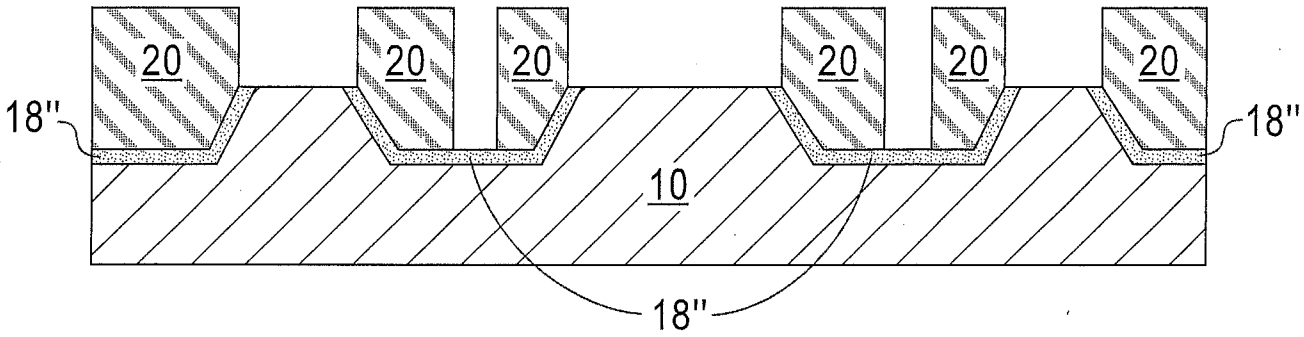


FIG. 16

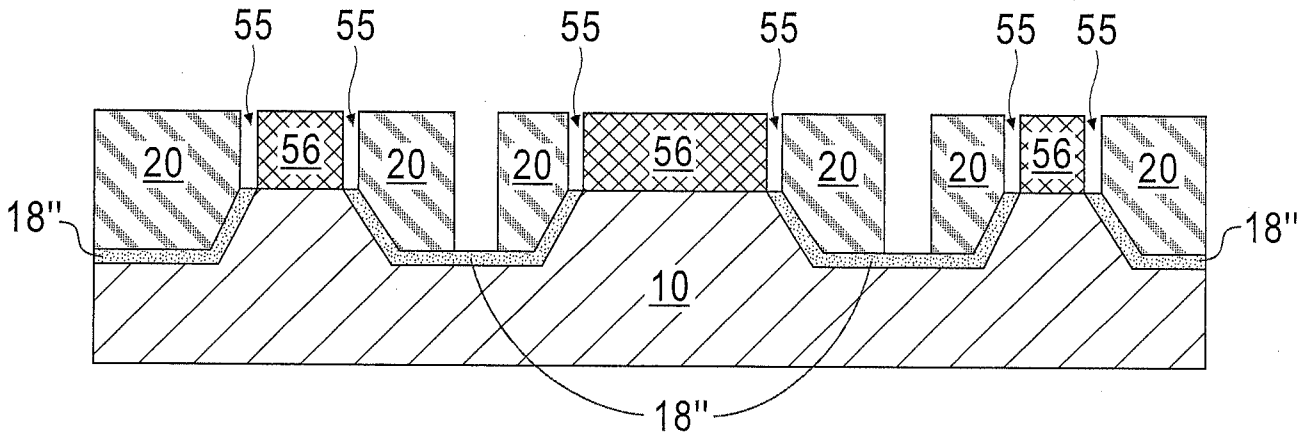


FIG. 17

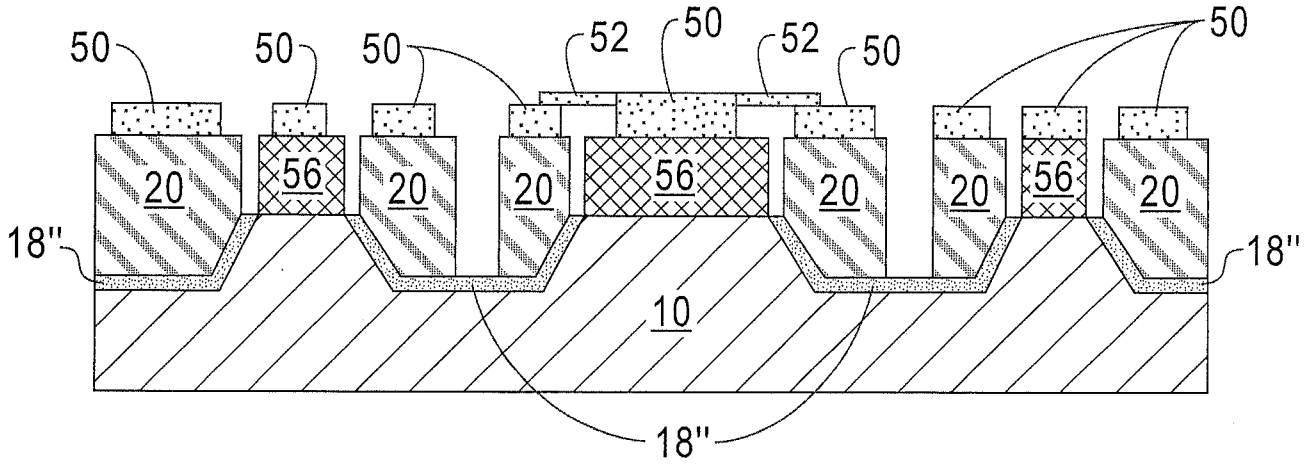


FIG. 18

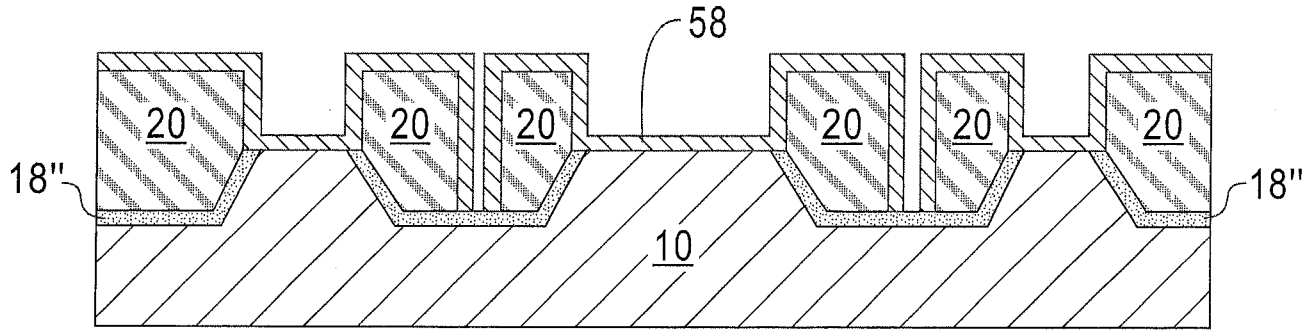


FIG. 19

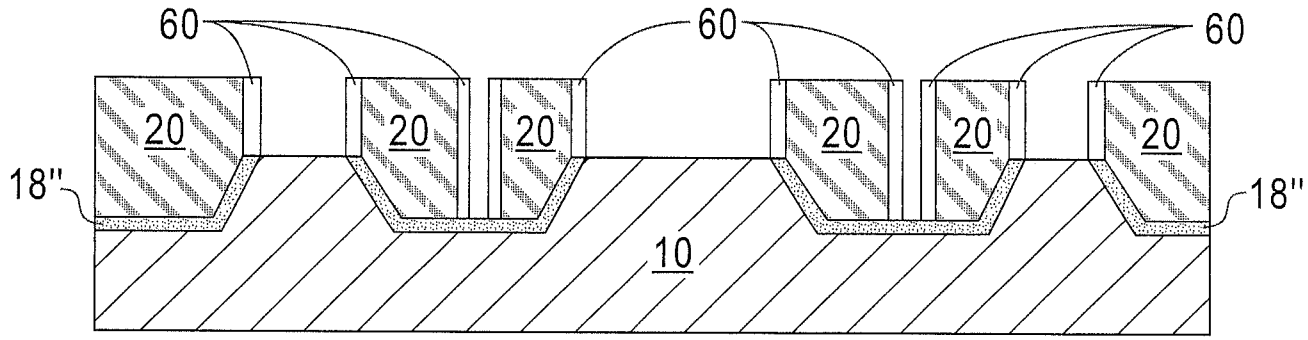


FIG. 20

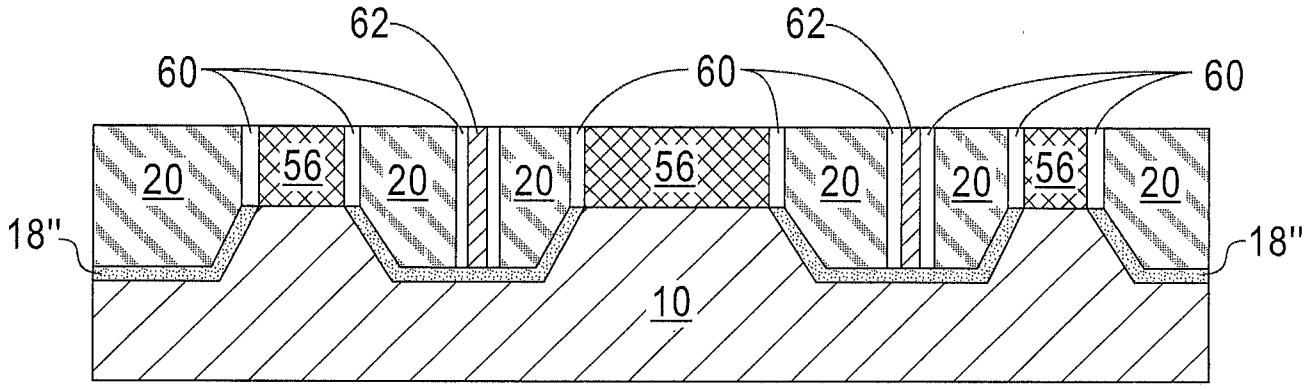


FIG. 21

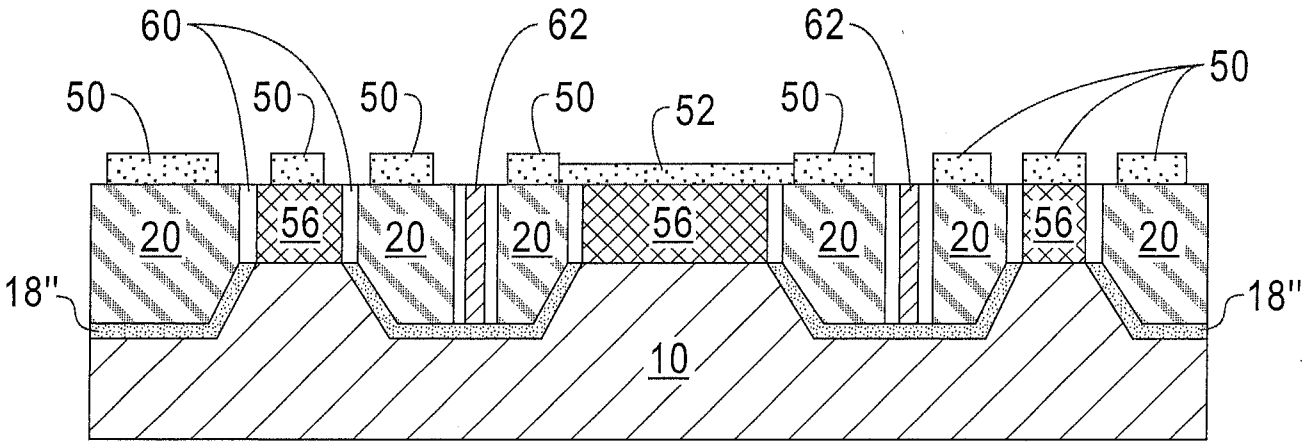


FIG. 22

**INTERNATIONAL SEARCH REPORT**

International application No.
PCT/US 13/59120

A. CLASSIFICATION OF SUBJECT MATTER
**IPC(8) - C30B 25/18 (2014.01)**
**USPC - 257/76**
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
USPC: 257/76
IPC(8): C30B 25/18 (2014.01)

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
USPC: 257/76; 257/E21 .09; 257/E29.089; 438/478 (text search - see terms below)

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
PatBase; PubWEST; Google
Search Terms Used: gallium nitride, GaN, GaAIN, GaAlinN, crystal, silicon, substrate, AIN, aluminum nitride, dielectric, etch, wet, plane, 11 1, 100, hydrogen, atmosphere, wurtzite

C. DOCUMENTS CONSIDERED TO BE RELEVANT

| Category* | Citation of document, with indication, where appropriate, of the relevant passages | Relevant to claim No. |
|---|---|---|
| Y | US 201 1/0049681 A1 (VIELEMEYER) 03 March 201 1 (03.03.201 1), Figs 4-5; paras [0046], [0049], [0054], [0057], [0058] | 1-21 |
| Y | US 2010/0025730 A1 (HEIKMAN et al.) 04 February 2010 (04.02.2010), Fig 2; paras [0055], [0075] | 1-21 |
| Y | US 201 1/01 80806 A1 (HEBERT) 28 July 201 1 (28.07.201 1), para [001 6] | 2 |
| Y | US 201 1/0108850 A1 (CHENG et al.) 12 May 201 1 (12.05.201 1), paras [0056], [0067], [0071] | 5, 18 |
| Y | US 2012/0003770 A1 (HASHIMOTO et al.) 05 January 2012 (05.01.2012), para [0073] | 6-8 |
| Y | US 2009/0149008 A1 (KRYLIOUK et al.) 11 June 2009 (11 .06.2009), entire document especially para [0010] | 6-10 |
| A | US 2003/0136333 A1 (SEMOND et al.) 24 July 2003 (24.07.2003), entire document | 1-21 |
| A | US 2010/0032696 A1 (YU et al.) 11 February 2010 (11.02.2010), entire document | 1-21 |
| A | US 2012/0270378 A1 (KITTLER et al.) 25 October 2012 (25.10.2012), entire document | 1-21 |
| A | US 2008/0023710 A1 (PARK et al.) 31 January 2008 (31 .01 .2008), entire document | 1-21 |
| A | US 2012/021 1759 A1 (LIU et al.) 23 August 2012 (23.08.2012) entire document | 1-21 |

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"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search
07 January 2014 (07.01.2014)

Date of mailing of the international search report
**24 JAN 2014**

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Form PCT/ISA/210 (second sheet) (July 2009)