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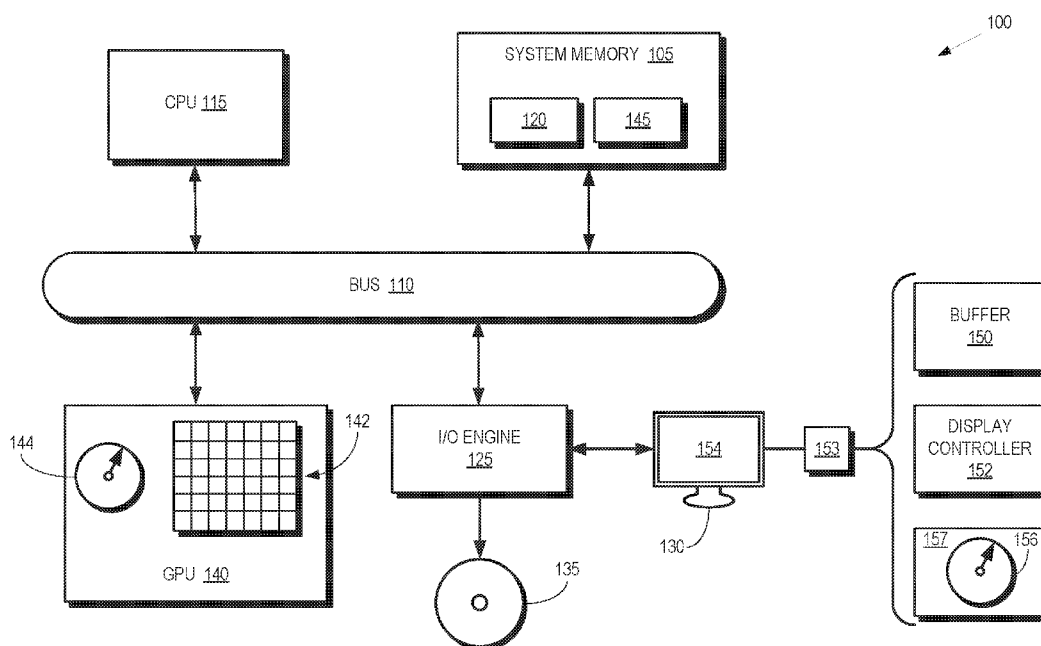


FIG. 1

(57) Abstract: A system includes a timing reference and one or more processors configured to generate and provide, based on the timing reference, frames to a display system that supports variable refresh rates. The frames include a vertical blanking region having a first duration. The display system transmits information indicating an operation to be performed by the display system during the vertical blanking region of one or more subsequent frames. The one or more processors are configured to increase the first duration to a second duration in response to receiving the information indicating an operation to be performed by the display system during the vertical blanking region of at least one subsequent frame. In some cases, the first duration of the vertical blanking region is a minimum duration that corresponds to a maximum refresh rate supported by the display system.



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REDUCED VERTICAL BLANKING REGIONS FOR DISPLAY SYSTEMS THAT SUPPORT VARIABLE REFRESH RATES

BACKGROUND

[0001] A display system includes a screen that displays video rendered by a processor such as a graphics processing unit (GPU) and provided to the display system in a stream of frames. The display video timing is determined by a frame rate (or refresh rate), a number of pixels per line in the frame (HTotal), a number of lines per frame (VTotal), and a pixel clock rate (PClk) that is equal to the product of the refresh rate, the number of pixels per line, and the number of lines per frame. The number of pixels per line includes a horizontal active region that includes pixel values used to generate images and a horizontal blanking region that conveys other information such as digital audio or metadata. Thus, the total number of pixels per line is equal to a sum of the pixels in the horizontal active region and the pixels in the horizontal blanking region. The number of lines per frame includes a vertical active region that includes pixel values and a vertical blanking region that conveys other information such as digital audio or metadata. Thus, the total number of lines per frame is equal to a sum of the lines in the vertical active region and the lines in the vertical blanking region. For example, a high definition frame can represent an image using 1080 active vertical lines that include values of the pixels and 45 vertical blanking lines. A line rate for the frame is defined as the pixel clock rate divided by the number of pixels per line or, equivalently, as the product of the refresh rate and the number of lines per frame.

SUMMARY OF EMBODIMENTS

[0002] In accordance with one aspect, an apparatus includes a timing reference and at least one processor configured to provide, based on the timing reference, frames to a display system that supports variable refresh rates, wherein the frames comprise a vertical blanking region having a first duration, and wherein the at least one processor is configured to increase the first duration to a second duration in response to receiving information indicating an operation to be performed by the display system during the vertical blanking region of at least one subsequent frame.

[0003] In some embodiments, the first duration of the vertical blanking region is a minimum duration that corresponds to a maximum refresh rate supported by the display system, the at least one processor is configured to increase the first duration to the second duration while maintaining durations of active regions of the frames and pixel clock rates of the frames, the operation to be performed by the display system during the vertical blanking region of the at least one subsequent frame comprises at least one of changing a power state of the display system or adjusting a clock frequency of the display system, the at least one processor is configured to defer transmitting a request to a display a frame to the display system until receiving an indication that the operation is complete and the at least one processor is configured to decrease the second duration in response to receiving the indication that the operation is complete, the at least one processor is configured to determine whether the display system supports variable refresh rates in response to the at least one processor being connected to the display system, and/or the at least one processor is configured to selectively enable or disable modifications to durations of the vertical blanking region based on whether the display system supports variable refresh rates.

[0004] In accordance with another aspect, a method includes: generating frames comprising a vertical blanking region having a first duration, providing the frames to a display system that supports variable refresh rates, receiving information indicating an operation to be performed by the display system during the vertical blanking region of at least one subsequent frame, and increasing the first duration to a second duration in response to receiving the information.

[0005] In some embodiments, the first duration of the vertical blanking region is a minimum duration that corresponds to a maximum refresh rate supported by the display system, increasing the first duration comprises increasing the first duration to the second duration while maintaining durations of active regions of the frames and pixel clock rates of the frames, receiving the information indicating the operation to be performed by the display system comprises receiving information indicating at least one of changing a power state of the display system or adjusting a clock frequency of the display system, the method further includes deferring transmission of a request to a display a frame to the display system until receiving an indication that the operation is complete and decreasing the second duration in response to receiving the indication that the operation is complete, the method includes determining whether

the display system supports variable refresh rates in response to at least one processor being connected to the display system, and/or the method further includes selectively enabling or disabling modifications to durations of the vertical blanking region based on whether the display system supports variable refresh rates.

[0006] In yet another aspect, a display system that supports variable refresh rates includes a timing reference, a display interface configured to couple to a display screen, and a display controller coupled to the timing reference and the display interface and configured to present, based on the timing reference, frames to the display interface that comprise a vertical blanking region having a first duration, and wherein the first duration is increased to a second duration in response to the display system transmitting information indicating an operation to be performed by the display system during the vertical blanking region of at least one subsequent frame.

[0007] In some embodiments, the first duration of the vertical blanking region is a minimum duration that corresponds to a maximum refresh rate supported by the display system, the first duration is increased to the second duration while maintaining durations of active regions of the frames and pixel clock rates of the frames, the operation comprises at least one of changing a power state of the display system or adjusting a clock frequency of the display system, the display system is configured to transmit an indication that the operation is complete, and/or the second duration is decreased in response to transmitting the indication that the operation is complete.

[0008] In yet another aspect, a method includes receiving frames for presentation on a display screen in a display system that supports variable refresh rates, wherein the frames comprise a vertical blanking region having a first duration, transmitting information indicating an operation to be performed by the display system during the vertical blanking region of at least one subsequent frame, receiving frames having a second duration for the vertical blanking region that is longer than the first duration in response to transmitting the information, and performing the operation during the vertical blanking region of the received frames having the second duration.

[0009] In some embodiments, the first duration of the vertical blanking region is a minimum duration that corresponds to a maximum refresh rate supported by the display system, the operation comprises at least one of changing a power state of the

display system or adjusting a clock frequency of the display system, the method further includes transmitting an indication that the operation is complete, and/or the second duration is decreased in response to transmitting the indication that the operation is complete.

BRIEF DESCRIPTION OF THE DRAWINGS

[0010] The present disclosure may be better understood, and its numerous features and advantages made apparent to those skilled in the art by referencing the accompanying drawings. The use of the same reference symbols in different drawings indicates similar or identical items.

[0011] FIG. 1 is a block diagram of a processing system that selectively reduces a vertical blanking region for frames provided to a display system that supports variable refresh rates according to some embodiments.

[0012] FIG. 2 is a block diagram of a frame that is generated by a GPU and provided to a display system according to some embodiments.

[0013] FIG. 3 is a flow diagram of a method of selectively enabling reduced or variable vertical blanking regions according to some embodiments.

[0014] FIG. 4 is a flow diagram of a method of modifying durations of vertical blanking regions in frames generated by a source processor and provided to a display system according to some embodiments.

DETAILED DESCRIPTION

[0015] A minimum duration of a vertical blanking region in a frame is determined by standards that are implemented in a processor (such as a GPU) and a display system. For example, the Harmonized Video Timing (HVT) standard sets a minimum duration of the vertical blanking time at about 300 microseconds (μ s) and the Coordinated Video Timing (CVT) standard sets the minimum duration of the vertical blanking time at 460 μ s. The frame refresh rates used by applications such as video games have increased from frequencies on the order of 120 Hz to frequencies of 240 Hz, 480 Hz, and perhaps higher as the graphics requirements of the applications continue to increase. Consequently, the percentage of each frame that is reserved

for the vertical blanking region increases as the duration of the frame decreases, which requires an increase in the line rate and the pixel rate because the size of the active regions, *e.g.*, the number of pixels per frame, remains the same. For example, at 480 Hz, the duration of the frame is 2.08 microseconds and the percentage of the frame consumed by the vertical blanking region is 14.4% for the 300 μ s vertical blanking region in HVT and 22.1% for the 460 μ s vertical blanking region in CVT. In order to reduce the percentage of the frame consumed by the vertical blanking region and improve the line and pixel rates, some displays implement a shorter, non-standardized vertical blanking region, *e.g.*, 100 or 150 μ s.

[0016] The processor performs different tasks during the active and blanking regions. While processing the horizontal and vertical active regions, the processor accesses the data used to display images from a memory via one or more memory interfaces and data fabric interfaces. In contrast, during some or all the vertical blanking regions there can be periods when no data is transferred over the memory/fabric interfaces. The processor can utilize these gaps in display processing during vertical blanking regions to perform other operations such as modifying a clock speed, retraining clocks used by the interfaces, modifying a power state of the processor, and other operations that require a gap in memory access/fabric delivery and that may cause interruptions in memory reads and fabric traffic. For example, the clock used by a memory interface can be retrained in response to a transition from a high frequency/high power state to a low frequency/low power state during the minimum vertical blanking times defined by HVT and CVT. However, the operations that the processor typically performs during the vertical blanking regions are difficult (or impossible) to complete within the reduced duration vertical blanking region. For example, a clock that drives a memory interface cannot be retrained in 100 μ s.

[0017] FIGs 1-4 disclose techniques for reducing a fraction of a frame that is consumed by a vertical blanking region for most frames, while also preserving the processor's ability to perform other operations such as changing power states and adjusting clock frequencies, by constraining the use of shorter vertical blanking regions to display systems that implement variable refresh rates. Some embodiments of the display system implement variable refresh rates to dynamically adapt the display refresh rate to variable frame rates received from a source, *e.g.*, the frames associated with an irregular load produced when a processor is rendering

complex gaming content. The refresh rate is varied by modifying vertical blanking regions of the frames while maintaining the size of the active regions and the pixel clock rate. In operation, the processor is initially providing frames having a reduced duration vertical blanking region such as 100 μ s or 150 μ s. The processor increases the duration of the vertical blanking region, *e.g.*, in response to the signaling indicating that an operation such as a changing power state or clock frequency adjustment should be (or will be) performed in one or more subsequent frames. In some embodiments, the processor defers transmitting a request to display a frame until the triggering operation is complete, thereby increasing the duration of the vertical blanking region of the frame. Modifying the frame rate to provide time to complete the operation does not cause visual artifacts such as stuttering because the display system is required to implement variable refresh rates to compensate for the processor's changing frame rate. Subsequent frames return to the minimum vertical blanking region if no further time needed.

[0018] FIG. 1 is a block diagram of a processing system 100 that selectively reduces a vertical blanking region for frames provided to a display system that supports variable refresh rates according to some embodiments. The processing system 100 includes or has access to a system memory 105 or other storage component that is implemented using a non-transitory computer readable medium such as a dynamic random-access memory (DRAM). However, some embodiments of the memory 105 are implemented using other types of memory including static RAM (SRAM), nonvolatile RAM, and the like. The processing system 100 also includes a bus 110 to support communication between entities implemented in the processing system 100, such as the memory 105. Some embodiments of the processing system 100 include other buses, bridges, switches, routers, and the like, which are not shown in FIG. 1 in the interest of clarity.

[0019] The processing system 100 includes at least one central processing unit (CPU) 115. Some embodiments of the CPU 115 include multiple processing elements (not shown in FIG. 1 in the interest of clarity) that execute instructions concurrently or in parallel. The processing elements are referred to as processor cores, compute units, or using other terms. The CPU 115 is connected to the bus 110 and communicates with the memory 105 via the bus 110. The CPU 115 executes instructions such as program code 120 stored in the memory 105 and the

CPU 115 stores information in the memory 105 such as the results of the executed instructions. The CPU 115 is also able to initiate graphics processing by issuing draw calls.

[0020] An input/output (I/O) engine 125 handles input or output operations associated with a display system 130, as well as other elements of the processing system 100 such as keyboards, mice, printers, external disks, and the like. The I/O engine 125 is coupled to the bus 110 so that the I/O engine 125 communicates with the memory 105, the CPU 115, or other entities that are connected to the bus 110. In the illustrated embodiment, the I/O engine 125 reads information stored on an external storage component 135, which is implemented using a non-transitory computer readable medium such as a compact disk (CD), a digital video disc (DVD), and the like. The I/O engine 125 also writes information to the external storage component 135, such as the results of processing by the CPU 115.

[0021] The display system 130 supports a variable refresh rate so that the display system 130 can present frames at refresh rates within a range up to a maximum refresh rate. For example, the display system 130 can support refresh rates of 24 Hz, 25 Hz, 30 Hz, 50 Hz, 60 Hz, 100 Hz, and 120 Hz. The variable refresh rate corresponds to a variable vertical blanking region, which is within a range beginning at a minimum vertical blanking region that corresponds to the maximum refresh rate of the display system 130. In some embodiments, the refresh rates are determined by querying the display system 130 for its Enhanced Extended Display Identification Data (E-EDID) and determining the refresh rates from the E-EDID reply.

[0022] The processing system 100 includes at least one GPU 140 that renders images for presentation by the display system 130. For example, the GPU 140 renders objects to produce values of pixels that are provided to the display system 130, which uses the pixel values to display an image that represents the rendered objects. The GPU 140 includes one or more processing elements such as an array 142 of compute units that execute instructions concurrently or in parallel. Some embodiments of the GPU 140 are used for general purpose computing. In the illustrated embodiment, the GPU 140 communicates with the memory 105 (and other entities that are connected to the bus 110) over the bus 110. However, some embodiments of the GPU 140 communicate with the memory 105 over a direct

connection or via other buses, bridges, switches, routers, and the like. The GPU 140 executes instructions stored in the memory 105 and the GPU 140 stores information in the memory 105 such as the results of the executed instructions. For example, the memory 105 stores a copy 145 of instructions that represent a program code that is to be executed by the GPU 140. The GPU 140 also includes a timing reference 144.

[0023] The GPU 140 generates a stream of frames that is provided to the display system 130. The GPU 140 renders frames at different refresh rates to match the variable refresh rates supported by the display system 130. For example, the GPU 140 renders frames and provides them to the display system 130 at 50 Hz in response to determining that the display system 130 is presenting frames at 50 Hz. For another example, the GPU 140 renders frames and provides them to the display system at 60 Hz in response to determining that the display system 130 is presenting frames at 60 Hz. Some embodiments of the display system 130 include a buffer 150 that stores the frames in the stream received from the GPU 140. The display system 130 also includes a display controller 152 that reads out the pixel values in the frames from the buffer 150 and uses the values to display an image on (or present an image to) a screen 154. The display controller 152 provides the frames via a display interface 153 (such as an HDMI or DisplayPort interface) configured to couple to the screen 154. The display system 130 also includes a timing reference 156, which is synchronized to the GPU timing reference 144 during normal operation. Some embodiments of the timing reference 156 are implemented in a timing controller (TCON) chip 157, *e.g.*, as an application-specific integrated circuit (ASIC) or other circuit, which also performs timing and synchronization operations for the display system 130, as discussed herein.

[0024] The frames generated by the GPU 140 and displayed by the display system 130 are characterized by a number of pixels per line in the frame (HTotal), a number of lines per frame (VTotal), and a pixel clock rate (PClk) that is equal to the product of the refresh rate, the number of pixels per line, and the number of lines per frame. In some embodiments, the GPU 140 provides frames to the display system 130 at a relatively high refresh rate (corresponding to a reduced duration of a vertical blanking region) if the display system 130 supports a variable refresh rate. In some embodiments, the initial duration of the vertical blanking region is a minimum duration that corresponds to a maximum refresh rate supported by the display system. The

reduced duration of the vertical blanking region is likely to be insufficient to perform some necessary operations at the display system 130. Consequently, if the display system 130 is going to perform one or more of these operations, the display system 130 transmits information indicating that the display system 130 is going to perform the operation(s) during the vertical blanking region of one or more subsequent frames. In response to receiving the information, the GPU 140 modifies a refresh rate for the frames by increasing the duration of the vertical blanking region in subsequent frames. The GPU 140 can also increase the refresh rate for the frames by decreasing the duration of the vertical blanking region in response to receiving an indication that the display system 130 has completed performing the operation and no longer requires the increase duration of the vertical blanking region.

[0025] FIG. 2 is a block diagram of a frame 200 that is generated by a GPU and provided to a display system according to some embodiments. The frame 200 is generated (e.g., rendered) by some embodiments of the GPU 140 shown in FIG. 1 and displayed or presented by some embodiments of the display system 130 shown in FIG. 1.

[0026] The frame 200 is partitioned into lines 201 (only one indicated by a reference numeral in the interest of clarity) of pixels 202 (only one indicated by a reference numeral in the interest of clarity). Each line 201 includes a number 205 of pixels per line (HTotal). The number 205 of pixels per line includes a horizontal active region 210 that includes pixel values used to generate images (as indicated by the open boxes) and a horizontal blanking region 215 that conveys other information such as digital audio or metadata (as indicated by the hatched boxes). The frame 200 also includes a number 220 of lines per frame (VTTotal). The number 220 of lines per frame includes a vertical active region 225 that includes pixel values (as indicated by the open boxes) and a vertical blanking region 230 that conveys other information such as digital audio or metadata (as indicated by the hatched boxes). Thus, the total number 220 of lines per frame is equal to a sum of the lines in the vertical active region 225 and the lines in the vertical blanking region 230. For example, a high definition frame can represent an image using 1080 active vertical lines that include values of the pixels and 45 vertical blanking lines.

[0027] The GPU provides the frame 200 (and the display system presents the frame 200) at a refresh rate. The frame 200 is therefore characterized by a pixel clock rate (PClk) that is equal to the product of the refresh rate, the number 205 of pixels per line, and the number 220 of lines per frame. A line rate for the frame 200 is defined as the pixel clock rate divided by the number 205 of pixels per line or, equivalently, as the product of the refresh rate and the number 220 of lines per frame. As discussed herein, the GPU modifies a duration of the vertical blanking region 230 based on requirements at the display system that is presenting the frame 200. The GPU initially generates frames having a reduced duration of the vertical blanking region 230 (corresponding to a higher refresh rate) such as a minimum duration of the vertical blanking region 230 determined by one or more standards implemented in the GPU and the display system. The GPU can increase the duration of the vertical blanking region 230 in response to an indication that the display system requires a longer duration, *e.g.*, to perform one or more operations during the vertical blanking region 230.

[0028] FIG. 3 is a flow diagram of a method 300 of selectively enabling reduced or variable vertical blanking regions according to some embodiments. The method 300 is implemented in some embodiments of the processing system 100 shown in FIG. 1.

[0029] At block 305, a source processor (such as a GPU) is associated with a display system. As used herein, the term “associate” refers to providing information to the source processor that configures the source processor (or causes the source processor to be configured) to render and provide frames to the display system using parameters that are determined based on one or more characteristics of the display system. In some embodiments, the source processor and the display system are associated by forming a physical (*e.g.*, wired or wireless) connection between the source processor and the display processor. The physical connection is then used to convey information between the devices, *e.g.*, the source processor can query the display system for its E-EDID and generate configuration parameters based on information in the E-EDID reply received from the display system. In some embodiments, the source processor is configured based on characteristics of the display system that are provided to the source processor without necessarily connecting the source processor and the display system. For example, the characteristics of the display system can be provided to the source processor, and

the source processor can be configured based on the characteristics, prior to connecting the source processor and the display system.

[0030] At decision block 310, the source processor determines whether the display system supports short (or variable) vertical blanking regions and variable refresh rates. In some embodiments, the determination is made based upon information received in an E-EDID reply from the display system. If the display system supports short (or variable) vertical blanking regions and variable refresh rates, the method 300 flows to the block 315. If the display system does not support short (or variable) vertical blanking regions and variable refresh rates, the method flows to the block 320.

[0031] At block 315, the display system supports short vertical blanking regions and variable refresh rates, which allows the display system to transition to longer vertical blanking regions that are used to configure the display system to support features including power optimizations. Use of the power optimizations is therefore enabled at block 315. In some embodiments, the source processor is configured to render and provide frames at a relatively high refresh rate using vertical blanking regions of a relatively short duration in most instances. However, in response to receiving signaling from the display system indicating a request for a longer duration of the vertical blanking region that is utilized by an additional feature such as power optimization, the source processor is configured to modify the duration of the vertical blanking region, *e.g.*, by increasing the duration.

[0032] At block 320, the display system does not support short vertical blanking regions and variable refresh rates. In that case, the display system is not able to transition to longer vertical blanking regions that are used to configure the display system to support features including power optimizations. The use of additional features such as power optimization are therefore disabled at block 320. Instead, the source processor uses a fixed duration of the vertical blanking region that corresponds to the refresh rate supported by the display system.

[0033] FIG. 4 is a flow diagram of a method 400 of modifying durations of vertical blanking regions in frames generated by a source processor and provided to a display system according to some embodiments. The method 400 is implemented in some embodiments of the processing system 100 shown in FIG. 1.

[0034] At block 405, the source processor is rendering frames with a reduced vertical blanking region and providing the rendered frames to the display system for display on a screen.

[0035] At decision block 410, the source processor determines whether the display system will require a longer vertical blanking region. Some embodiments of the display system provide an indication or a request for the longer vertical blanking region, e.g., to provide additional time to perform one or more operations at the display system. If a longer vertical blanking region has been requested, the method 400 flows to the block 415. Otherwise, the method 400 returns to block 405.

[0036] At block 415, the source processor increases the vertical blanking region and begins rendering frames with the increased vertical blanking region. The frames are provided to the display system, which displays images based on information in the active region of the frame and performs one or more operations concurrently with the vertical blanking region. In some embodiments, the source processor defers transmitting a request to display a frame to the display system until the display system indicates that it is completed performing the one or more operations, thereby increasing the duration of the vertical blanking region of the frame.

[0037] At decision block 420, the source processor determines whether the display system still requires the longer vertical blanking region. Some embodiments of the display system provide an indication that the one or more operations are complete, which indicates that the display system no longer needs the longer vertical blanking region. If the display system no longer requires the longer vertical blanking region because the operation is complete, the method 400 flows to block 405 and the source processor reduces the duration of the vertical blanking region. If the display system still requires the longer vertical blanking region because the operation is not complete, the method 400 flows to the block 415.

[0038] A computer readable storage medium may include any non-transitory storage medium, or combination of non-transitory storage media, accessible by a computer system during use to provide instructions and/or data to the computer system. Such storage media can include, but is not limited to, optical media (e.g., compact disc (CD), digital versatile disc (DVD), Blu-Ray disc), magnetic media (e.g., floppy disc, magnetic tape, or magnetic hard drive), volatile memory (e.g., random access

memory (RAM) or cache), non-volatile memory (e.g., read-only memory (ROM) or Flash memory), or microelectromechanical systems (MEMS)-based storage media. The computer readable storage medium may be embedded in the computing system (e.g., system RAM or ROM), fixedly attached to the computing system (e.g., a magnetic hard drive), removably attached to the computing system (e.g., an optical disc or Universal Serial Bus (USB)-based Flash memory), or coupled to the computer system via a wired or wireless network (e.g., network accessible storage (NAS)).

[0039] In some embodiments, certain aspects of the techniques described above may be implemented by one or more processors of a processing system executing software. The software includes one or more sets of executable instructions stored or otherwise tangibly embodied on a non-transitory computer readable storage medium. The software can include the instructions and certain data that, when executed by the one or more processors, manipulate the one or more processors to perform one or more aspects of the techniques described above. The non-transitory computer readable storage medium can include, for example, a magnetic or optical disk storage device, solid state storage devices such as Flash memory, a cache, random access memory (RAM) or other non-volatile memory device or devices, and the like. The executable instructions stored on the non-transitory computer readable storage medium may be in source code, assembly language code, object code, or other instruction format that is interpreted or otherwise executable by one or more processors.

[0040] Note that not all of the activities or elements described above in the general description are required, that a portion of a specific activity or device may not be required, and that one or more further activities may be performed, or elements included, in addition to those described. Still further, the order in which activities are listed are not necessarily the order in which they are performed. Also, the concepts have been described with reference to specific embodiments. However, one of ordinary skill in the art appreciates that various modifications and changes can be made without departing from the scope of the present disclosure as set forth in the claims below. Accordingly, the specification and figures are to be regarded in an illustrative rather than a restrictive sense, and all such modifications are intended to be included within the scope of the present disclosure.

[0041] Benefits, other advantages, and solutions to problems have been described above with regard to specific embodiments. However, the benefits, advantages, solutions to problems, and any feature(s) that may cause any benefit, advantage, or solution to occur or become more pronounced are not to be construed as a critical, required, or essential feature of any or all the claims. Moreover, the particular embodiments disclosed above are illustrative only, as the disclosed subject matter may be modified and practiced in different but equivalent manners apparent to those skilled in the art having the benefit of the teachings herein. No limitations are intended to the details of construction or design herein shown, other than as described in the claims below. It is therefore evident that the particular embodiments disclosed above may be altered or modified and all such variations are considered within the scope of the disclosed subject matter. Accordingly, the protection sought herein is as set forth in the claims below.

WHAT IS CLAIMED IS:

1. An apparatus, comprising:
 - a timing reference; and
 - at least one processor configured to provide, based on the timing reference, frames to a display system that supports variable refresh rates, wherein the frames comprise a vertical blanking region having a first duration, and wherein the at least one processor is configured to increase the first duration to a second duration in response to receiving information indicating an operation to be performed by the display system during the vertical blanking region of at least one subsequent frame.
2. The apparatus of claim 1, wherein the first duration of the vertical blanking region is a minimum duration that corresponds to a maximum refresh rate supported by the display system.
3. The apparatus of claim 1 or 2, wherein the at least one processor is configured to increase the first duration to the second duration while maintaining durations of active regions of the frames and pixel clock rates of the frames.
4. The apparatus of any of claims 1 to 3, wherein the operation to be performed by the display system during the vertical blanking region of the at least one subsequent frame comprises at least one of changing a power state of the display system or adjusting a clock frequency of the display system.
5. The apparatus of any of claims 1 to 4, wherein the at least one processor is configured to defer transmitting a request to a display a frame to the display system until receiving an indication that the operation is complete.
6. The apparatus of claim 5, wherein the at least one processor is configured to decrease the second duration in response to receiving the indication that the operation is complete.
7. The apparatus of any preceding claim, wherein the at least one processor is configured to determine whether the display system supports variable refresh rates in response to the at least one processor being connected to the display system.

8. The apparatus of claim 7, wherein the at least one processor is configured to selectively enable or disable modifications to durations of the vertical blanking region based on whether the display system supports variable refresh rates.
9. A method comprising:
- generating frames comprising a vertical blanking region having a first duration;
 - providing the frames to a display system that supports variable refresh rates;
 - receiving information indicating an operation to be performed by the display system during the vertical blanking region of at least one subsequent frame; and
 - increasing the first duration to a second duration in response to receiving the information.
10. The method of claim 9, wherein the first duration of the vertical blanking region is a minimum duration that corresponds to a maximum refresh rate supported by the display system.
11. The method of claim 9 or claim 10, wherein increasing the first duration comprises increasing the first duration to the second duration while maintaining durations of active regions of the frames and pixel clock rates of the frames.
12. The method of any of claims 9 to 11, wherein receiving the information indicating the operation to be performed by the display system comprises receiving information indicating at least one of changing a power state of the display system or adjusting a clock frequency of the display system.
13. The method of any of claims 9 to 12, further comprising:
- deferring transmission of a request to a display a frame to the display system until receiving an indication that the operation is complete.
14. The method of claim 13, further comprising:
- decreasing the second duration in response to receiving the indication that the operation is complete.
15. The method of any of claims 9 to 14, further comprising:

determining whether the display system supports variable refresh rates in response to at least one processor being connected to the display system.

16. The method of claim 15, further comprising:

selectively enabling or disabling modifications to durations of the vertical blanking region based on whether the display system supports variable refresh rates.

17. A display system that supports variable refresh rates, the display system comprising:

a timing reference;

a display interface configured to couple to a display screen; and

a display controller coupled to the timing reference and the display interface and configured to present, based on the timing reference, frames to the display interface that comprise a vertical blanking region having a first duration, and wherein the first duration is increased to a second duration in response to the display system transmitting information indicating an operation to be performed by the display system during the vertical blanking region of at least one subsequent frame.

18. The display system of claim 17, wherein the first duration of the vertical blanking region is a minimum duration that corresponds to a maximum refresh rate supported by the display system.

19. The display system of claim 17 or 18, wherein the first duration is increased to the second duration while maintaining durations of active regions of the frames and pixel clock rates of the frames.

20. The display system of any of claims 17 to 19, wherein the operation comprises at least one of changing a power state of the display system or adjusting a clock frequency of the display system.

21. The display system of any of claims 17 to 21, wherein the display system is configured to transmit an indication that the operation is complete.

22. The display system of claim 21, wherein the second duration is decreased in response to transmitting the indication that the operation is complete.

23. A method comprising:

receiving frames for presentation on a display screen in a display system that supports variable refresh rates, wherein the frames comprise a vertical blanking region having a first duration;

transmitting information indicating an operation to be performed by the display system during the vertical blanking region of at least one subsequent frame;

receiving frames having a second duration for the vertical blanking region that is longer than the first duration in response to transmitting the information; and

performing the operation during the vertical blanking region of the received frames having the second duration.

24. The method of claim 23, wherein the first duration of the vertical blanking region is a minimum duration that corresponds to a maximum refresh rate supported by the display system.

25. The method of claim 23 or 24, wherein the operation comprises at least one of changing a power state of the display system or adjusting a clock frequency of the display system.

26. The method of any of claims 23 to 25, further comprising:

transmitting an indication that the operation is complete.

27. The method of claim 26, wherein the second duration is decreased in response to transmitting the indication that the operation is complete.

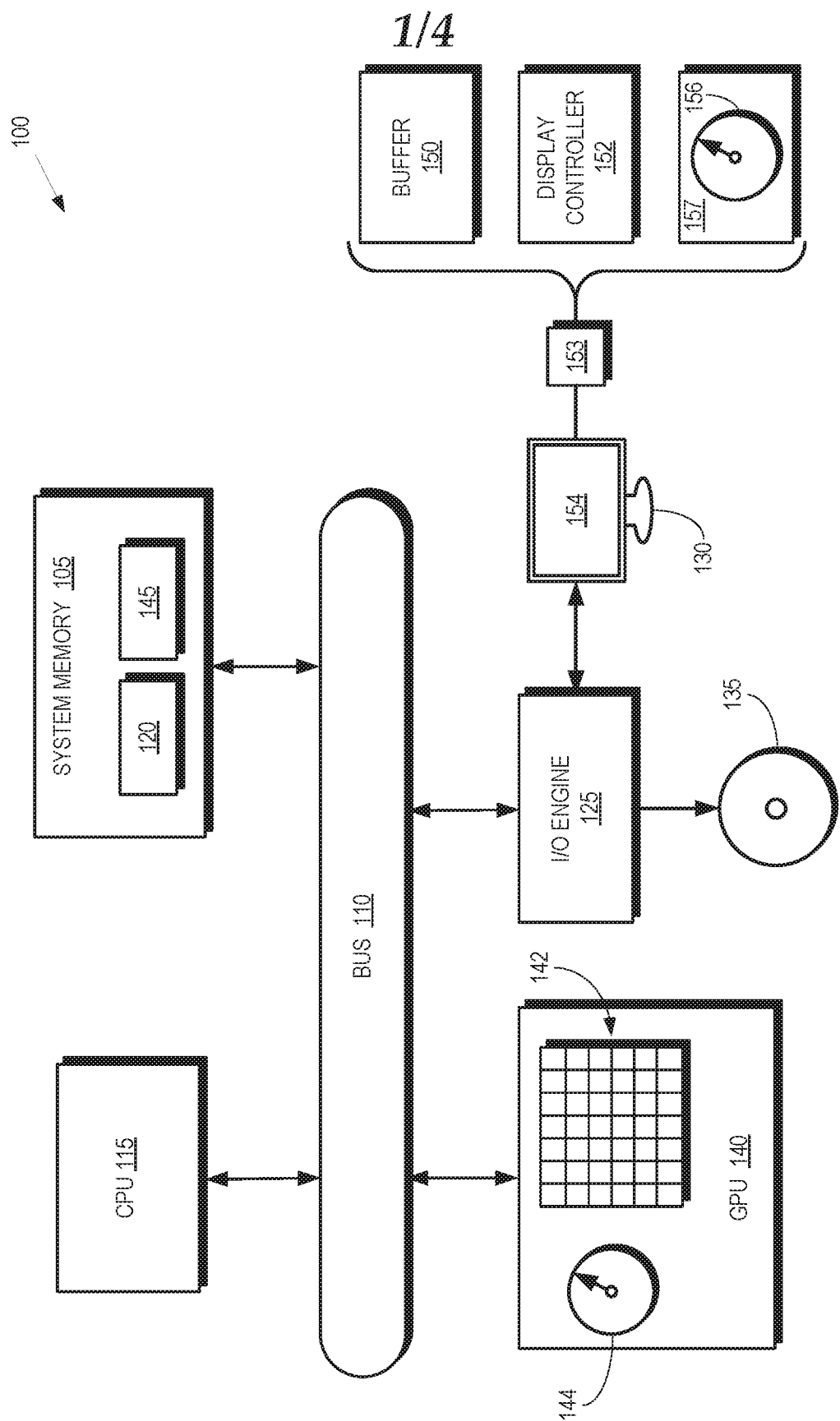


FIG. 1

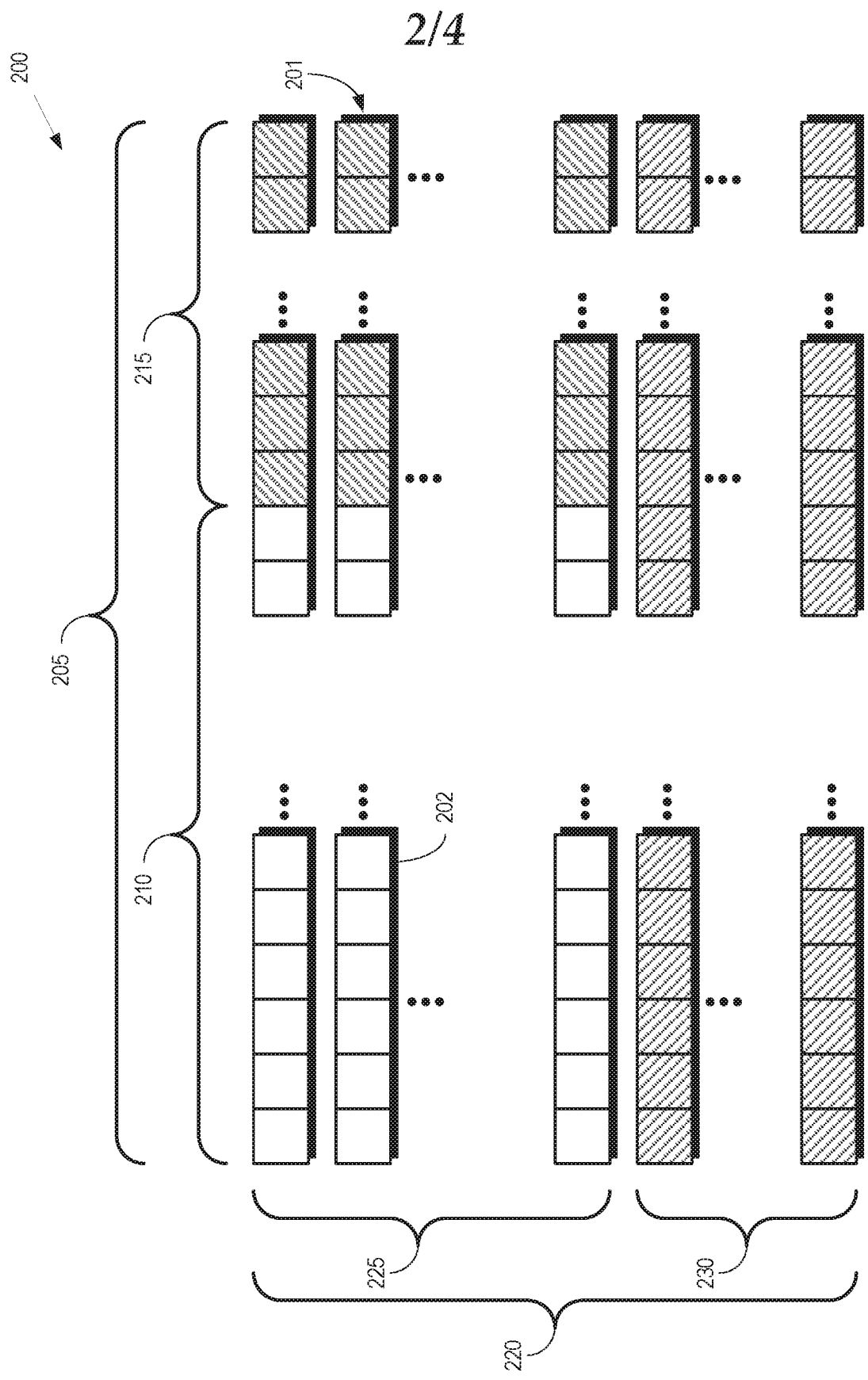
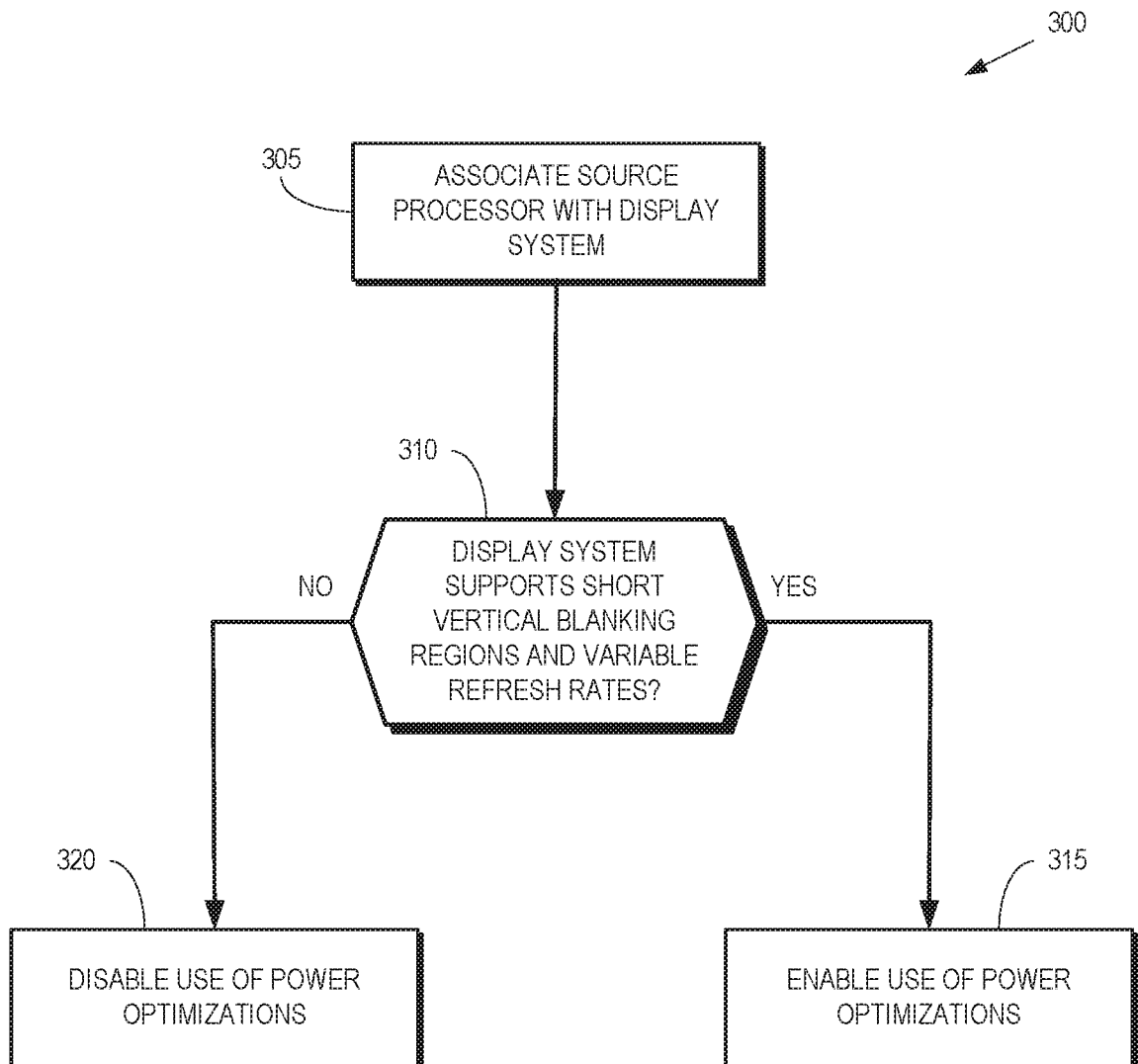
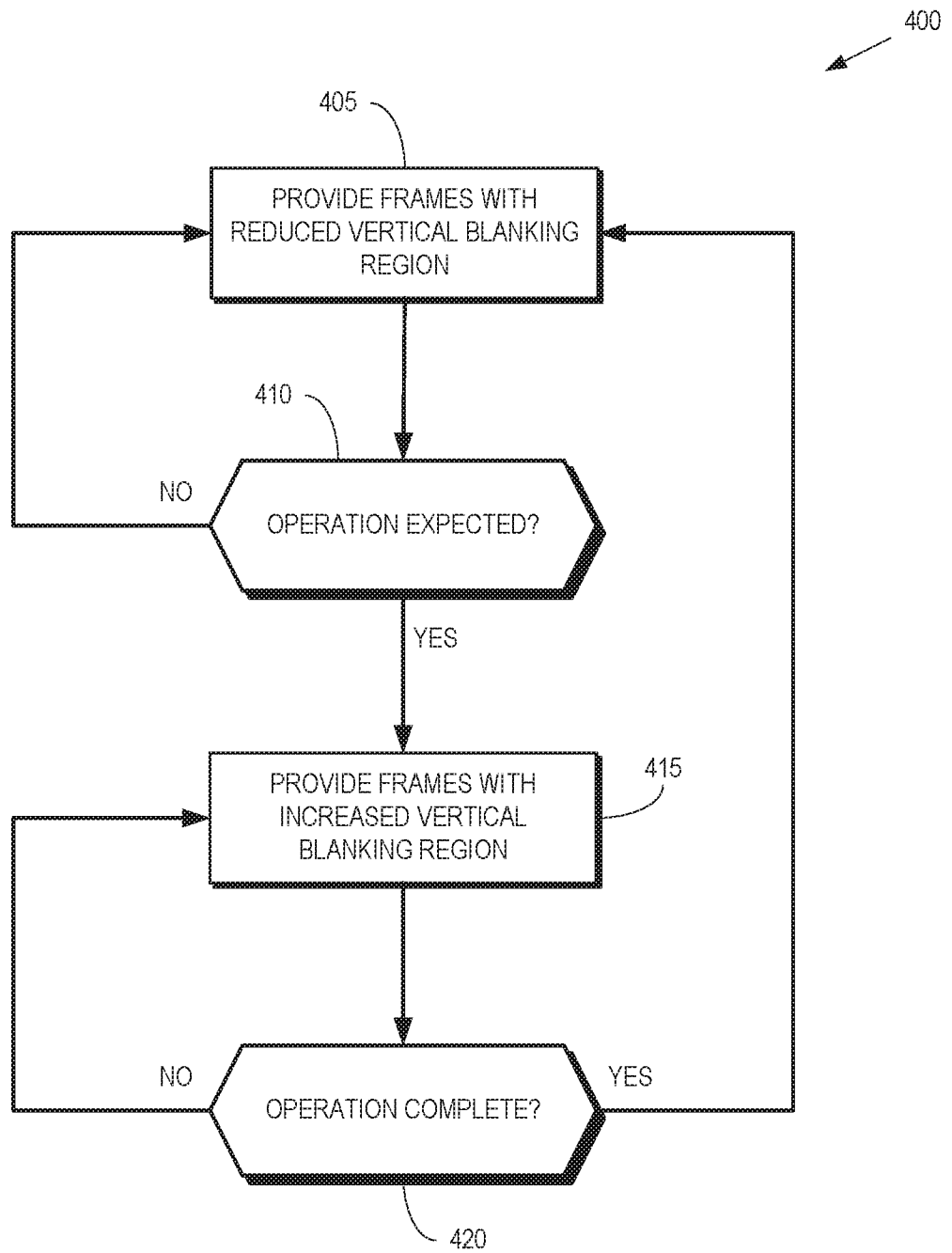


FIG. 2

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**FIG. 3**

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**FIG. 4**

INTERNATIONAL SEARCH REPORT

International application No.

PCT/IB2021/058694

A. CLASSIFICATION OF SUBJECT MATTER

IPC: **G09G 5/18** (2006.01) , **H04N 7/088** (2006.01)

CPC:

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC: **G09G 5/18** (2006.01) , **H04N 7/088** (2006.01)

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic database(s) consulted during the international search (name of database(s) and, where practicable, search terms used)

Database: Canadian Patent Database, Questel Orbit

Keywords: timing reference, variable refresh rate, vertical, blank, pixel, clock rate, duration, minimum, maximum

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X, Y	US2008100598A1, Juenger, 01 May 2008 (01-05-2008) See the whole document	1, 9, 17, 23 2-8, 10-16, 18-22, 24-27
Y	US20080055318A1, Glen, 06 March 2008 (06-03-2018) See the whole document	2-8, 10-16, 18-22, 24-27
A	WO2012079148A1, Hussain et al., 21 June 2012 (21-06-2012) See the whole document	1-27
A	US2012169930A1, Carter, 05 July 2012 (05-07-2012) See the whole document	1-27

☐ Further documents are listed in the continuation of Box C.☒ See patent family annex.

* "A" "D" "E" "L" "O" "P"	Special categories of cited documents: document defining the general state of the art which is not considered to be of particular relevance document cited by the applicant in the international application earlier application or patent but published on or after the international filing date document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified) document referring to an oral disclosure, use, exhibition or other means document published prior to the international filing date but later than the priority date claimed	"T" "X" "Y" "&"	later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art document member of the same patent family
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Date of the actual completion of the international search
29 December 2021 (29-12-2021)Date of mailing of the international search report
29 December 2021 (29-12-2021)Name and mailing address of the ISA/CA
Canadian Intellectual Property Office
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INTERNATIONAL SEARCH REPORT
Information on patent family members

International application No.
PCT/IB2021/058694

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US2008055318A1	06 March 2008 (06-03-2008)	EP2070072A2 EP2293272A1 EP2293272B1 US2014307166A1 US9924134B2 WO2008026070A2 WO2008026070A3	17 June 2009 (17-06-2009) 09 March 2011 (09-03-2011) 21 September 2016 (21-09-2016) 16 October 2014 (16-10-2014) 20 March 2018 (20-03-2018) 06 March 2008 (06-03-2008) 02 May 2008 (02-05-2008)
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US2012169930A1	05 July 2012 (05-07-2012)	US8599310B2	03 December 2013 (03-12-2013)

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IPC:

CPC: