United States Patent

[11] 3,619,798

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[54] **THREE-PORT ELECTRICAL NETWORK**
4 Claims, 8 Drawing Figs.

[52] **U.S. Cl.** **330/19,** 330/22, 330/30
[51] **Int. Cl.** **H03f 3/42**
[50] **Field of Search** ..... 330/19, 22, 30 D, 32, 69

[56] **References Cited**

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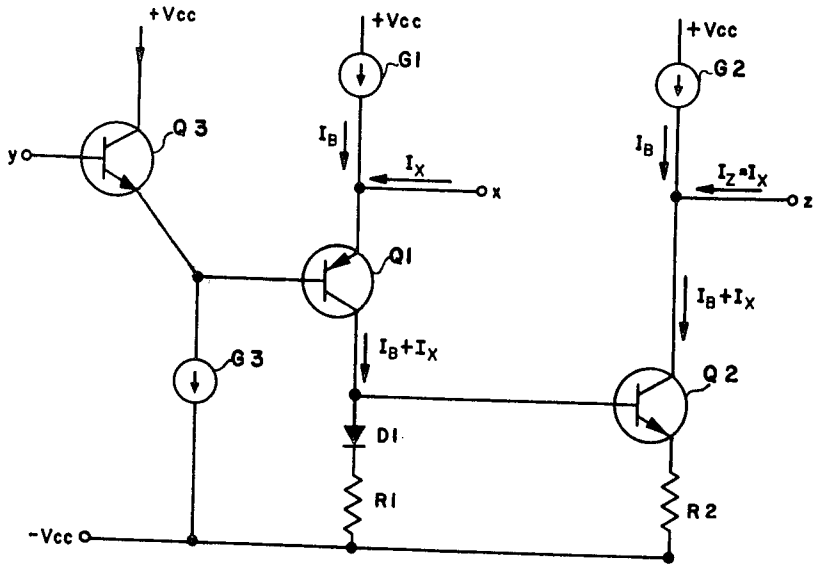
ABSTRACT: A three-port electrical network that has a first port whose impedance is high and whose voltage controls the potential of a second port which has low or zero impedance and through which an independent current flows to reappear at a third port at high impedance which consists of a unity gain amplifier having high input impedance and low output impedance and means for deriving a current related to the current flowing in the output port of the amplifier and means for conveying this current to a third port. The latter two means are current followers energized from constant current sources.



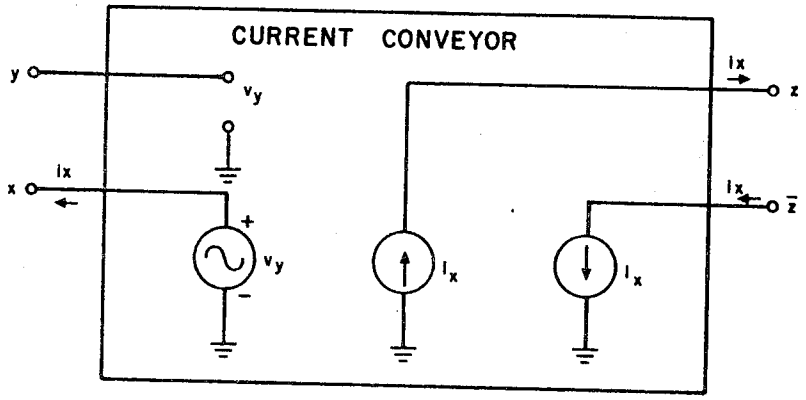


FIG. 1

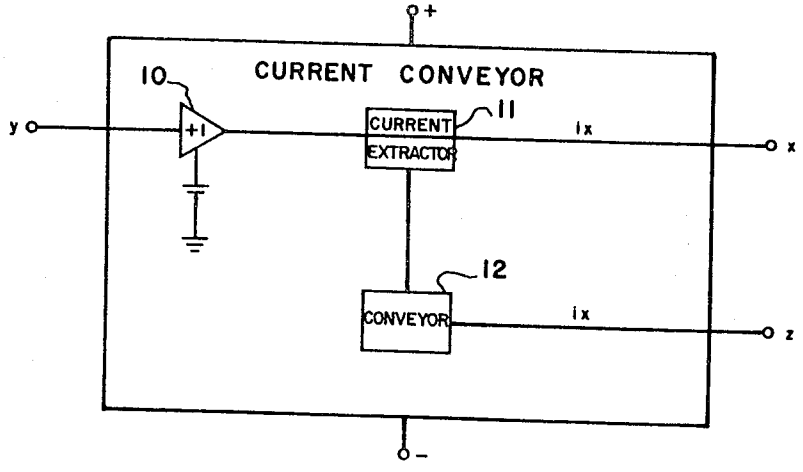


FIG. 2

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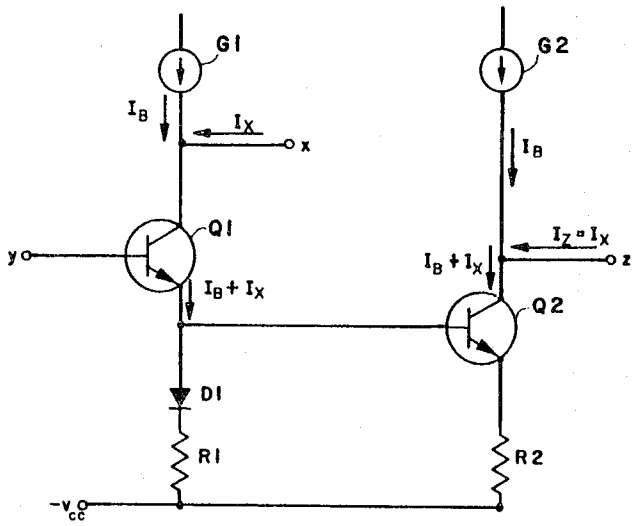

FIG. 3

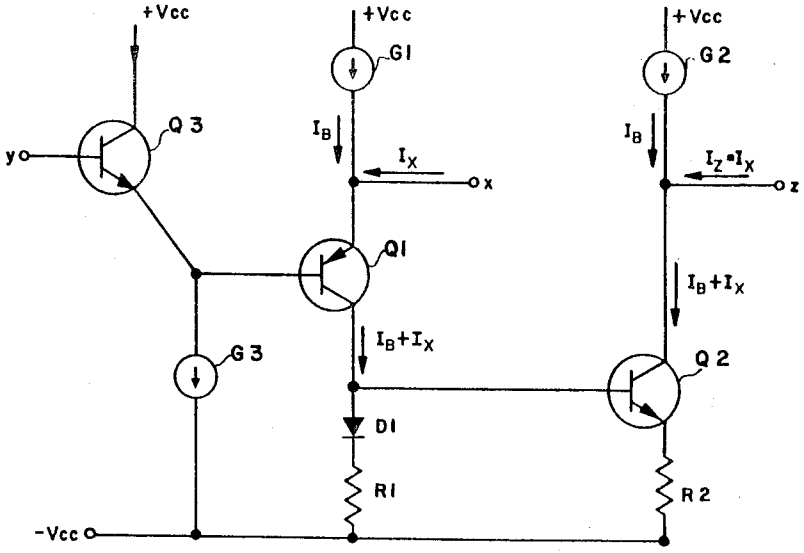

FIG. 4

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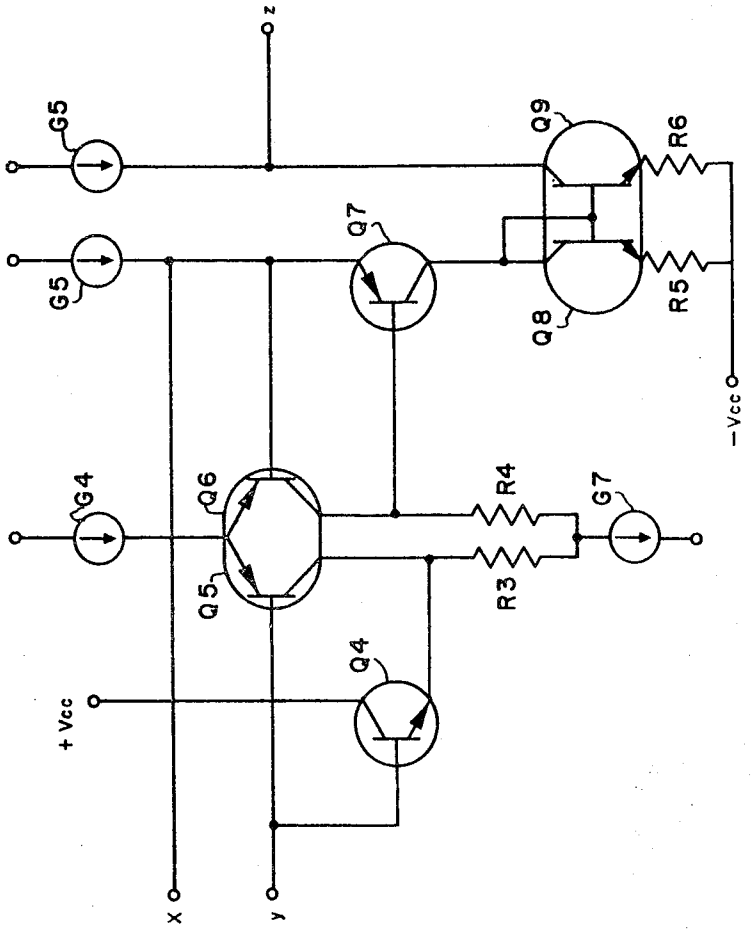

FIG. 5

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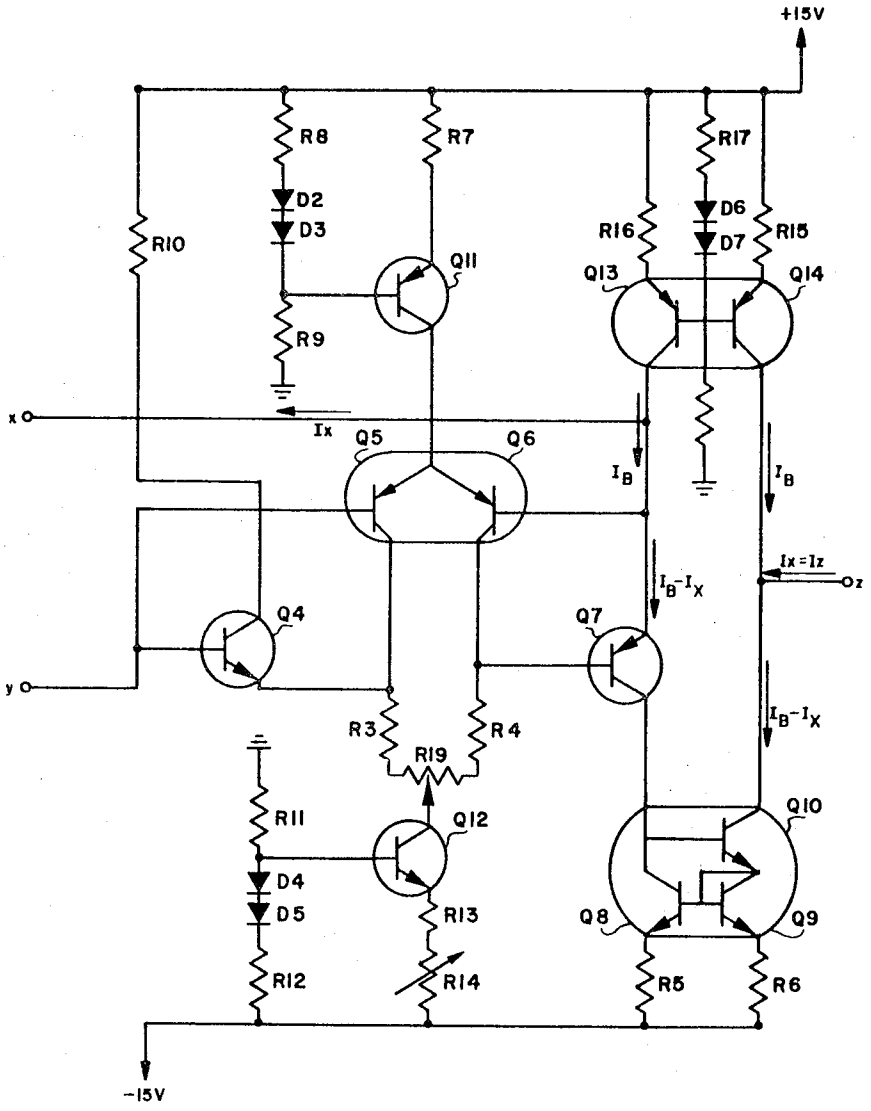

FIG. 6

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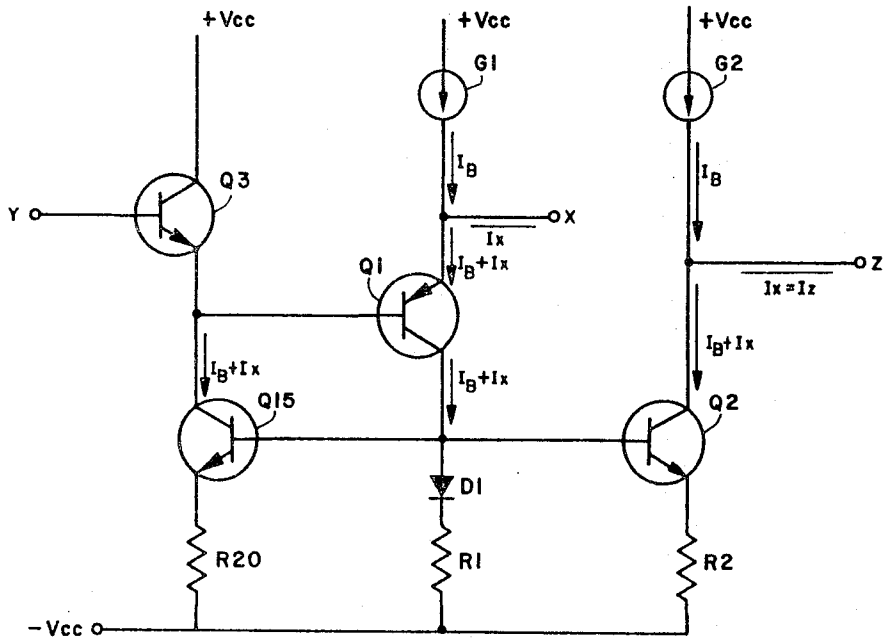

FIG. 7

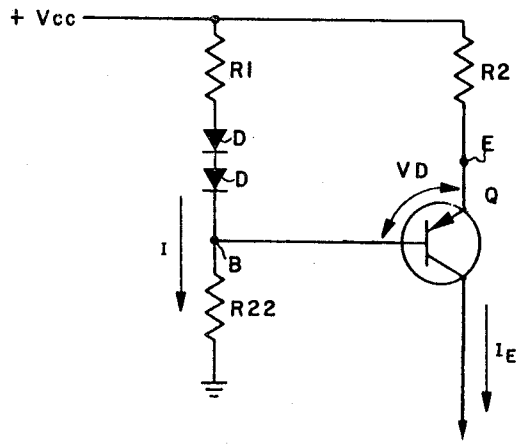

FIG. 8

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THREE-PORT ELECTRICAL NETWORK

This invention relates to an electronic three-port network and more particularly to a circuit that possesses a first port whose input impedance is infinite and whose voltage controls the potential of a second port exhibiting zero impedance and through which an independent current flows to reappear at a third port where the impedance is infinite.

In an earlier patent application, Ser. No. 769,798 , filed in the U.S. Pat. Office on Oct. 23, 1968, and in a paper "The Current Conveyor—a new circuit building block" published in the Proceedings of the IEEE Vol. 56, No. 8 in Aug. 1968, we disclosed the concept of Current Conveying and an implementation in the form of a circuit building block for the Current Conveyor. This circuit building block has been found to be useful in many communication and instrumentation applications. The Current Conveyor disclosed is a three-port network with the three ports termed for convenience x, y, and z. Its terminal characteristics can be best represented by a hybrid matrix giving the outputs of the three ports in terms of their corresponding inputs. This can be stated or represented as:

$$\begin{bmatrix} i_y \\ v_x \\ i_z \end{bmatrix} = \begin{bmatrix} 0 & 1 & 0 \\ 1 & 0 & 0 \\ 0 & \pm 1 & 0 \end{bmatrix} \begin{bmatrix} v_y \\ i_x \\ v_z \end{bmatrix} \quad (1)$$

All currents (i) and voltages (v) are total instantaneous quantities rather than incremental values. This property requires that any implementation of the Current Conveyor should be direct-coupled, should have no offset and should ensure linear ideal operation over a wide signal range.

The present disclosure is concerned with a new building block circuit embodying the Current Conveying concept but with different and more versatile terminal characteristics. The terminal characteristics of this circuit which is a three-port network with the ports termed x, y, and z can also be represented by a hybrid matrix giving the outputs of the three ports in terms of their corresponding inputs as follows:

$$\begin{bmatrix} i_y \\ v_x \\ i_z \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 1 & 0 & 0 \\ 0 & \pm 1 & 0 \end{bmatrix} \begin{bmatrix} v_y \\ i_x \\ v_z \end{bmatrix} \quad (2)$$

A practical circuit realization of a Current Conveyor having these three-port will consist of an ideal voltage buffer stage with input at y and output x and means for accepting or supplying current at x and conveying an equal current to z where the impedance level will be high.

It is an object of the present invention to provide a three-port network that has a first port whose input impedance is very high and whose voltage controls the potential of a second port exhibiting substantially zero impedance and through which an independent current flows to reappear at a third port where the impedance is very high.

This and other objects of the invention are achieved by a unity gain close-to-ideal amplifier (perfect buffer having very high input impedance and low output impedance), means for extracting the output current and conveying it to a third free terminal having infinite impedance, and means for supplying suitable biasing currents to the amplifier and the extraction means.

In drawings which illustrate the embodiments of the invention,

FIG. 1 is an idealized circuit diagram of a Current Conveyor with the required properties,

FIG. 2 is a block diagram of the Current Conveyor showing elements necessary to achieve the characteristics of the idealized circuit of FIG. 1,

FIG. 3 is a first approximation circuit realization of a Current Conveyor which has characteristics approaching the idealized form of FIG. 1,

FIG. 4 is a further circuit realization which has characteristics more nearly approaching those of FIG. 1,

FIG. 5 is the circuit of FIG. 4 but with arrangement for negative feedback to the input transistor,

FIG. 6 is a complete circuit diagram of an actual Current Conveyor that closely approaches the idealized version of FIG. 1,

FIG. 7 is a variant form of the circuit of FIG. 4, and

FIG. 8 shows a constant current source generator that may be used in the Current Conveyor.

Referring to FIG. 1, a Current Conveyor that will produce the characteristics of matrix equation (2) given above is shown. The input port y is at a voltage to ground of v_y, with an infinite input impedance. Port x is made to have a voltage to ground of v_y also and in this respect is a voltage follower. A current i_x flowing out of port x is regenerated and "conveyed" to port z at infinite output impedance. A fourth terminal or port z may be employed to provide an output current opposite in direction to port z. It is realized of course that the essential problem is to achieve an actualized circuit conformation that closely approaches the characteristics of FIG. 1.

FIG. 2 illustrates the principle requirements of an actualized circuit. Input port y is connected to a unity gain, ideal (perfect buffer) amplifier **10** having infinite input impedance and providing little or no voltage offset. The output current i_x of the amplifier is extracted by suitable current extractor means **11** and taken to a conveyor **12** that "conveys" it to output port z at infinite impedance. The impedance looking into port x is low. Suitable biasing currents will have to be provided for operation of the various components.

FIG. 3 is an actualization of the circuit and has input port y connected to the base of transistor Q1 which is fed by a biasing current I_B provided by constant current generator G1 and a current I_x flowing into port x . Assuming a high impedance looking into port y (no current flowing into Q1 from y), a current $I_B + I_x$ flows out of the collector of Q1. Transistor Q2, diode D1 and resistors R1 and R2 act as a current extractor and a current $I_B + I_x$ is duplicated in the collector of Q2. If Q2 is biased by a current I_B by constant current generator G2, then a current $I_z = I_x$ will flow into port z, the impedance looking into port z being very high (infinite). This current suffers certain deficiencies in that Q1 does not provide sufficiently high input impedance and gives a voltage offset between ports y and x. The current I_x is however conveyed to port z which has a very high output impedance.

The circuit of FIG. 3 can be improved by the addition of an input transistor Q3 giving much higher input impedance. Suitable biasing current is provided by current source G3. The offset voltage between ports x and y is approximately cancelled and the output impedance at port z remains high. A further improvement is achieved in FIG. 5 in which negative feedback is provided by transistors Q5 and Q6 resulting in a very high input impedance at port y. Transistor pair Q5 and Q6 biased by a current from constant current source G4 acts as a difference amplifier and gives a current output that controls transistors Q4 and Q7 such that the voltage at the input (port x) will be identical to that at port y (zero voltage offset). Transistors Q4, Q5, Q6, and Q7 acts as a unity gain amplifier giving idealized, perfect buffer operation. Transistor Q7 also acts as the current extractor and the current flowing in it (I_B from current source G5 plus I_x drawn from port x) is applied to transistors Q8 and Q9 and bias resistors R5 and R6 (which would be equal in value) which act as a Current Conveyor. An identical current $I_B + I_x$ appears at the the collector of Q9. Constant current source G5 is arranged to provide a biasing current I_B such that the current at port z will be $-I_x$ as required.

FIG. 6 is a complete circuit of the FIG. 5 version of the Current Conveyor with a suitable type of biasing current supply that may be used shown. All operating elements are the same as shown in FIG. 5. Transistor Q11 in conjunction with diodes D2 and D3 and resistors R7, R8, and R9 form a constant current source, the operation of which will be described below in conjunction with FIG. 8. Transistor Q12 in conjunction with diodes D4 and D5 and resistors R11, R12, and R13 with R14 also operate in the same way. Transistors Q13 and Q14 in relation to diodes D6 and D7 and related resistors R15, R16, R17, and R18 also act as bias current sources. Transistor Q10 is in-

serted to balance the effect of Q8. Resistors R3 and R4 and also R5 and R6 should be equal resistance, matched sets. Resistors R19 and R14 are potentiometers and are used to adjust out imbalances in the circuit.

In an actual circuit built and operated the following circuit components and values were used:

Q4, Q12—2N3642
Q7, Q11—2N3638
Q5, Q 6—MD5000
Q8, Q9, Q10—CA3018
Q13, Q14—FSP24
R3, R 4—91 OHMS
R5, R 6—510 OHMS
R 7—7.5 K
R8, R 9—6.8 K
R11, R12, R13—4.7 K
R14—1 K
R15, R16, R17, R18—1 K
R19—500 OHMS
R10—820 OHMS

FIG. 7 is a variant form of circuit to that of FIG. 4 and is similar to that circuit except that the biasing current to input transistor Q3 is supplied via a transistor Q15 and a resistor R20. Resistor R20 should be equal in value and matched with resistors R1 and R2. Because of matching of transistors and resistors, identical currents flow in Q15 and Q2 and these will be equal to that in Q1. This circuit provides voltage offset compensation, and generally high input impedance at *y*. The input is really an emitter follower circuit. The output impedance at *x* is low but that at *y* is not as high as in FIG. 4 and therefore the circuit is probably not as useful as that of FIGS. 5 and 6.

Referring now to FIG. 8, a useful biasing current source is shown and this is the type used in the FIG. 6 version of the circuit. This circuit is particularly useful in that it provides a current output that can be precisely known and which depends solely on the supply voltage (V_{cc}) and a resistor (R23) in the circuit. Assuming the voltage drop across each diode and from base to emitter of transistor Q to be equal (not difficult to achieve in practice) and represented by V_D, then

$$I=\frac{V_{cc}-2V_D}{R21+R22}$$

$$\text{The voltage at point B}=V_B=IR22=\frac{V_{cc}-2V_D}{R21+R22}R22$$

$$\text{The voltage at point E}=V_E=\frac{V_{cc}-2V_D}{R21+R22}R22+V_D$$

$$\text{The current through resistor R23}=I_E$$

$$=\frac{V_{cc}-V_E}{R23}=\frac{V_{cc}-\frac{V_{cc}-2V_D}{R21+R22}R22-V_D}{R23}$$

If R21, R22, and R23 are made equal and equal to *R* then

$$I=\frac{V_{cc}-\frac{V_{cc}-2V_D}{2R}R-V_D}{R}$$

$$I_E=\frac{V_{cc}-\frac{V_{cc}}{2}+V_D-V_D}{R}$$

$$I_E=\frac{V_{cc}}{2R}$$

From this it will be seen that the biasing current I_E is dependent only on the supply voltage and a resistor. Referring to FIG. 6 it will be seen that as a common supply is used and resistors can readily be matched that bias currents of precisely equal magnitude are engendered as required.

The Current COnveyor described here has many possible applications as a circuit building block. Some of these include a voltage-controlled voltage-source, a negative impedance converter, a negative-impedance inverter, and an analog computing element. The device will have many additional applications and it is envisaged that it may prove as versatile a building block as the operational amplifier for example. Applications of the device are described in some detail in a paper entitled "A Second Generator Current Conveyor and its Applications" given by the inventors at the 1968 IEEE International Symposium on Circuit Theory in Miami, Fla. on Dec. 4, 1968.

We claim:

1. A three-port electrical network that has a first port whose impedance is high and whose voltage controls the potential of a second port exhibiting substantially zero impedance and through which an independent current flows to reappear at a third port where impedance is high comprising a unity gain transistorized amplifying stage whose control electrode is connected to the said first port of the network, whose output is connected to the said second port and also to a first source of constant biasing current and whose input is connected to a voltage bias source through an impedance, a current follower comprising a transistor whose output is connected to a second source of constant biasing current equal in magnitude to the biasing current form the first source, whose input is connected to the said voltage bias source through an impedance, and whose control electrode is connected to the input of the said amplifying stage such that the current follower provides at its output a current related in magnitude to the current flowing into the said second port, and means comprising a connection to said current follower transistor at its output which is adapted to be a high impedance point for conveying this current to the said third port.

2. A three-port electrical network as in claim 1 in which the amplifying stage is a transistor operating as an emitter follower.

3. A three-port electrical network comprising:

1. a unity gain buffer amplifier having an input port at high impedance and an output port at low impedance and including a first transistor connected as an emitter follower amplifier whose control electrode is connected to said input port, a difference amplifier comprising second and third transistors connected in parallel and connected at their inputs to a first common bias current source and at their outputs to a second common bias current source via a bias resistance network, the control electrode of the first transistor being connected to the control electrode of the second transistor, the output of the first transistor being connected to the output of said second transistor, and a fourth transistor whose input is connected to a third bias current source, the said output port, and the control electrode of said third transistor and whose control electrode is connected to the output of the third transistor, the said bias resistances being of such value that the ratio of the two bias currents flowing through the second and third transistors will be such that the input current to the first port of the buffer amplifier becomes almost zero and the voltages at the input and output ports are almost equal,
2. means for extracting a current equal to the current flowing in the said output port of the buffer amplifier including the said fourth transistor which provides at its output a current equal to the current flowing in the said output port plus the current obtained from the third bias current source.
3. current follower means including a fifth transistor connected to the output of the fourth transistor and a sixth, diode-connected transistor energized by a fourth source

of bias current equal to the third, the control electrodes of said fifth and sixth transistors being interconnected such that a current flows in the sixth transistor equal to the current in the fifth transistor, and

4. mans comprising a connection to the sixth transistor at its output which is adapted to be a high impedance point for conveying this current to the said third port.

4. A three-port network as in claim 3 wherein the constant bias current sources comprise a transistor whose input is connected via a first resistor of known resistance value to a constant voltage supply and whose control input is connected via two diodes and a second resistor equal in value to the first resistor to an equal constant voltage supply and to a fixed voltage reference via a third resistor equal in value to said first and second resistors, said transistor providing at its output a current having a value related only to the supply voltage and the resistors.

* * * * *