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(54) Title: GENERATING THE UNDER VOLTAGE PROTECTION THRESHOLD

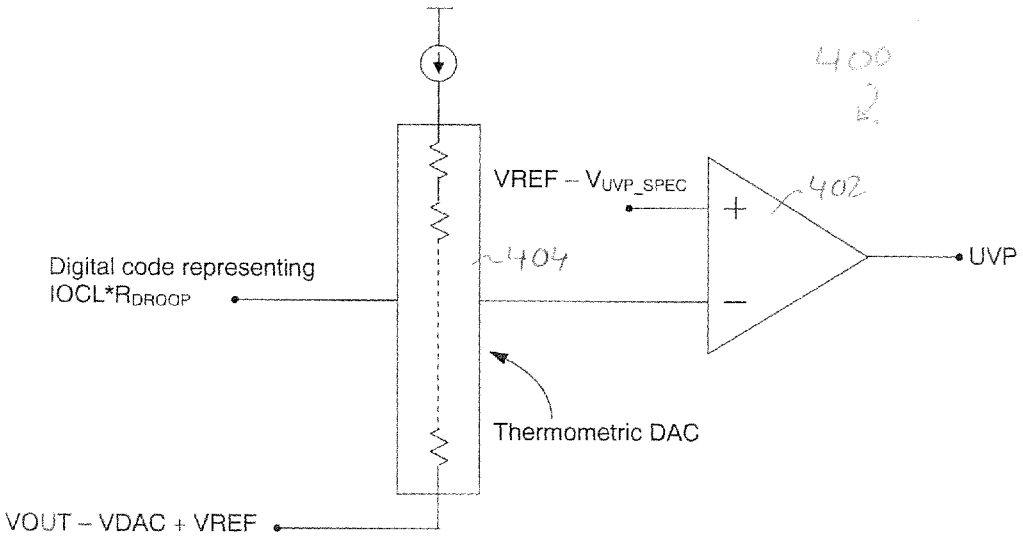

FIG. 4

(57) Abstract: In described examples of a voltage regulator (300) having a regulated output voltage that droops down from a reference voltage (VDAC), an improvement includes generating a droop voltage portion of an under voltage protection threshold (IOCL*DROOP) by using a realization that an under voltage condition only occurs when an overcurrent condition (IOCL) exists, so that the droop portion includes the overcurrent limit value multiplied by droop resistance.

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[Continued on next page]

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— *as to applicant's entitlement to apply for and be granted a patent (Rule 4.17(ii))*

— *as to the applicant's entitlement to claim the priority of the earlier application (Rule 4.17(iii))*

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GENERATING THE UNDER VOLTAGE PROTECTION THRESHOLD

BACKGROUND

[0001] Under voltage protection is a feature of voltage regulators where the regulator takes an action such as raising an alarm or shutting itself down when its output voltage is pulled too low by an external load. The protection kicks in when the output voltage falls below a certain threshold. In non-droop voltage regulators, generating the under voltage (UV) threshold is straightforward. However, in finite-droop voltage regulators, the droop voltage needs to be added to the UV threshold. Generating droop voltage needs additional circuitry that adds to silicon area and complexity.

SUMMARY

[0002] In described examples of a controller for a voltage regulator having a regulated output voltage that droops down from a reference voltage, the controller includes means for generating a droop voltage portion of an under voltage protection threshold by using a realization that an under voltage condition only occurs when an overcurrent condition exists, so that the droop portion comprises the overcurrent limit value multiplied by droop resistance.

[0003] In described examples of a controller for a voltage regulator having a regulated output voltage that droops down from a reference voltage, and having an under voltage limit circuit, the controller includes: a signal generator to generate a voltage representative of a droop voltage at a constant current output; a circuit to add the droop voltage at a constant current output to a user-determined under voltage specification voltage to create a voltage representative of the sum; and a comparator to compare an output voltage of the regulator with the sum voltage to establish a new under voltage protection threshold.

[0004] In further described examples of a controller for a voltage regulator having a regulated output voltage that droops down from a reference voltage, and having an under voltage limit circuit, the controller includes: a circuit to apply a digital representation of a droop voltage at a constant output current to a first input of a digital to analog converter; a circuit to apply a signal representing output voltage of the voltage regulator minus the reference voltage to a second input

of the digital to analog converter; and a circuit to apply an output of the digital to analog converter to a first input of a comparator. A second input of the comparator is coupled to a signal representing the reference voltage minus a user-determined under voltage specification voltage to create a voltage representative of the difference. The comparator is to compare the signals at the first and second inputs of the comparator to establish a new under voltage protection threshold.

BRIEF DESCRIPTION OF THE DRAWINGS

[0005] FIG. 1 shows a principle of output voltage droop.

[0006] FIG. 2 shows a control principle for a controller for a voltage regulator.

[0007] FIG. 3 shows an embodiment of a control circuit for a voltage regulator in accordance with principles of example embodiments.

[0008] FIG. 4 shows an alternate embodiment of the control circuit for a voltage regulator in accordance with principles of example embodiments.

DETAILED DESCRIPTION OF EXAMPLE EMBODIMENTS

[0009] This solution eliminates additional circuitry by generating the droop voltage and the UV threshold in a simpler manner, exploiting the fact that (in this example) an under voltage condition only occurs when an over-current condition exists.

[0010] The droop voltage is described with reference to a graph 100 in FIG. 1. In this example, the voltage regulator is required to regulate and output voltage that droops down from the reference voltage (VDAC) by an amount proportional to the load current:

$$VOUT = VDAC - R_{DROOP} * IOUT$$

where VOUT is the output voltage of the regulator, VDAC is a voltage reference to which the output of the voltage regulator is regulated, R_{droop} is an effective resistance to voltage regulator, and IOUT is the output current of the voltage regulator.

[0011] A fault condition (such as excessive load or a short) can cause the output voltage to be lower than its expected value. An excursion equal to the UVP threshold in the output voltage can be tolerated. Beyond such threshold, the voltage regulator must take some action, such as raising a flag or turning off the output.

[0012] The voltage regulator can have an over-current-limit feature, where it does not allow load currents higher than the overcurrent limit (OCL) threshold to flow out of its output.

[0013] In this type of example, whenever a UVP condition exists, an OCL condition also

exists. Referring to the graph 200 in FIG. 2, because the voltage regulator maintains a constant output current (equal to the OCL threshold, IOCL) during the OCL condition, the droop value in the UVP condition is R_{DROOP}*IOCL. This equation gets modified based on linear regulator or switching regulator. If linear IOCL is the same as the current limit in the system, in case of switching regulator depending on the implementation of OCL, the value of IOCL will modify into either IOCL (average current limit), IOCL+Rippe/2 if valley mode OCL, or IOCL-Ripple/2 if peak mode control.

[0014] In this type of example, the UVP threshold is required to be the UVP threshold spec (user selected) plus the droop voltage, where the UVP threshold spec is a fixed voltage. Thus, the actual UVP threshold at which the UVP condition is detected is:

$$VOUT = VDAC - IOUT*R_{DROOP} - UVP\_SPEC$$

where UVP_SPEC is a user supplied fixed voltage.

[0015] Accordingly, it is the same as:

$$VOUT = VDAC - IOCL*R_{DROOP} - UVP\_SPEC \text{ (since IOUT = IOCL in UVP condition)}$$

[0016] If the output current IOUT is used to generate the UVP threshold, it would involve sensing the output current and converting it into a voltage proportional to R_{DROOP} before adding it to the UVP_SPEC voltage. This would need at least one amplifier and a few resistors. However, because IOCL can be used in place of IOUT and IOCL threshold and R_{DROOP} are fixed numbers, the sensed IOUT is not required to be converted to a droop voltage, and an amplifier can be eliminated. The implementation is a constant voltage threshold generation (e.g., a fixed current flowing through a fixed resistance). The circuit 300 in FIG. 3 includes comparator 302, resistor 306 and current source 304.

[0017] The inequality realized by the circuit is:

$$VOUT < VDAC - (IOCL\_R_{DROOP} + V_{UVP\_SPEC})$$

where $IOCL\_R_{DROOP}$ is the droop voltage at constant output current.

[0018] In a second embodiment, instead of sensing the VOUT directly, a more accurate signal represents VOUT in the form of VOUT – VDAC + VREF, where VREF is a fixed reference voltage to ensure the signal Vout-VDAC has swing on both sides. Vref is internally generated or externally provided and used as common mode for all the blocks. It can take a value of zero if a negative value case is not required.

[0019] To limit the input common mode of the comparator, a UVP threshold spec signal is

referred to the same VREF.

$$(VREF - V_{UVP\_SPEC})$$

where V_{UVP_SPEC} is a user-determined voltage.

[0020] The circuit 400 in FIG. 4 includes comparator 402 and thermometric DAC 404.

[0021] The inequality realized by the circuit is still the same:

$$VOUT < VDAC - (IOCL\_R_{DROOP} + V_{UVP\_SPEC})$$

where V_{UVP_SPEC} is a user-determined voltage.

[0022] This technique can be used with linear or switching regulators.

[0023] Modifications are possible in the described embodiments, and other embodiments are possible, within the scope of the claims.

CLAIMS

What is claimed is:

1. A controller for a voltage regulator having a regulated output voltage that droops down from a reference voltage, the controller comprising:

means for generating a droop voltage portion of an under voltage protection threshold by using a realization that an under voltage condition only occurs when an overcurrent condition exists, so that the droop portion comprises the overcurrent limit value multiplied by droop resistance.

2. The controller of claim 1, further comprising an under voltage limit circuit to realize an inequality of:

$VOUT < VDAC - (IOCL\_RDROOP + V_{UVP\_SPEC})$,

wherein IOCL_RDROOP is the droop voltage at constant output current, VOUT is the output voltage of the regulator, VDAC is the reference voltage, and V_{UVP_SPEC} is a user-determined fixed voltage.

3. The controller of claim 1, wherein the reference voltage is applied to a first input of a comparator through a resistor, the first input also being coupled by a current source to a reference voltage to generate the voltage $IOCL\_RDROOP + V_{UVP\_SPEC}$,

wherein IOCL_RDROOP is the droop voltage at constant output current, and V_{UVP_SPEC} is a user-determined voltage; and

a second input of the comparator being coupled to VOUT to generate the under voltage protection threshold.

4. A controller for a voltage regulator having a regulated output voltage that droops down from a reference voltage, and having an under voltage limit circuit, the controller comprising:

a signal generator to generate a voltage representative of a droop voltage at a constant current output;

a circuit to add the droop voltage at a constant current output to a user-determined under voltage specification voltage to create a voltage representative of the sum; and

a comparator to compare an output voltage of the regulator with the sum voltage to establish a new under voltage protection threshold.

5. The controller of claim 4, wherein the under voltage limit circuit realizes an inequality of:

$VOUT < VDAC - (IOCL\_RDROOP + V_{UVP\_SPEC})$,

wherein IOCL_RDROOP is the droop voltage at constant output current, VOUT is the output voltage of the regulator, VDAC is the reference voltage, and V_{UVP_SPEC} is a user-determined fixed voltage.

6. The controller of claim 5, wherein the reference voltage is applied to a first input of a comparator through a resistor, the first input also being coupled by a current source to a reference voltage to generate the voltage $IOCL\_RDROOP + V_{UVP\_SPEC}$,

wherein IOCL_RDROOP is the droop voltage at constant output current, and V_{UVP_SPEC} is a user-determined voltage; and

a second input of the comparator being coupled to VOUT to generate the under voltage protection threshold.

7. A controller for a voltage regulator having a regulated output voltage that droops down from a reference voltage, and having an under voltage limit circuit, the controller comprising:

a circuit to apply a digital representation of a droop voltage at a constant output current to a first input of a digital to analog converter;

a circuit to apply a signal representing output voltage of the voltage regulator minus the reference voltage to a second input of the digital to analog converter; and

a circuit to apply an output of the digital to analog converter to a first input of a comparator, wherein a second input of the comparator is coupled to a signal representing the reference voltage minus a user-determined under voltage specification voltage to create a voltage representative of the difference;

the comparator being to compare the signals at the first and second inputs of the comparator to establish a new under voltage protection threshold.

8. The controller of claim 7, wherein the under voltage limit circuit realizes an inequality of:

$VOUT < VDAC - (IOCL\_RDROOP + V_{UVP\_SPEC})$,

wherein IOCL_RDROOP is the droop voltage at constant output current, VOUT is the output voltage of the regulator, VDAC is the reference voltage, and V_{UVP_SPEC} is a user-determined fixed voltage.

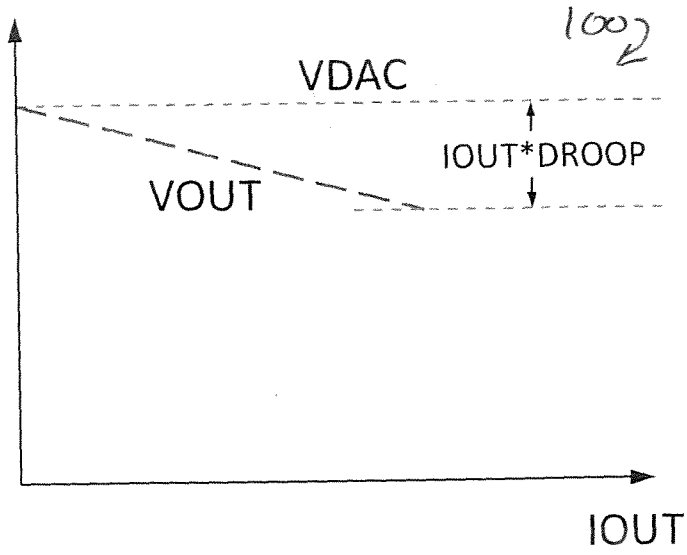
100
VDAC
IOUT*DROOP
VOUT
IOUT

FIG. 1

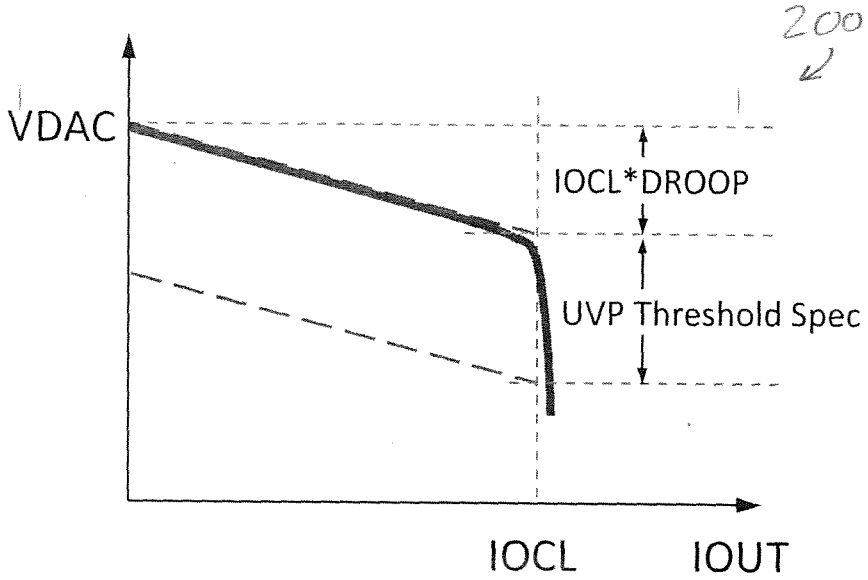
200
VDAC
IOCL*DROOP
UVP Threshold Spec
IOCL
IOUT

FIG. 2

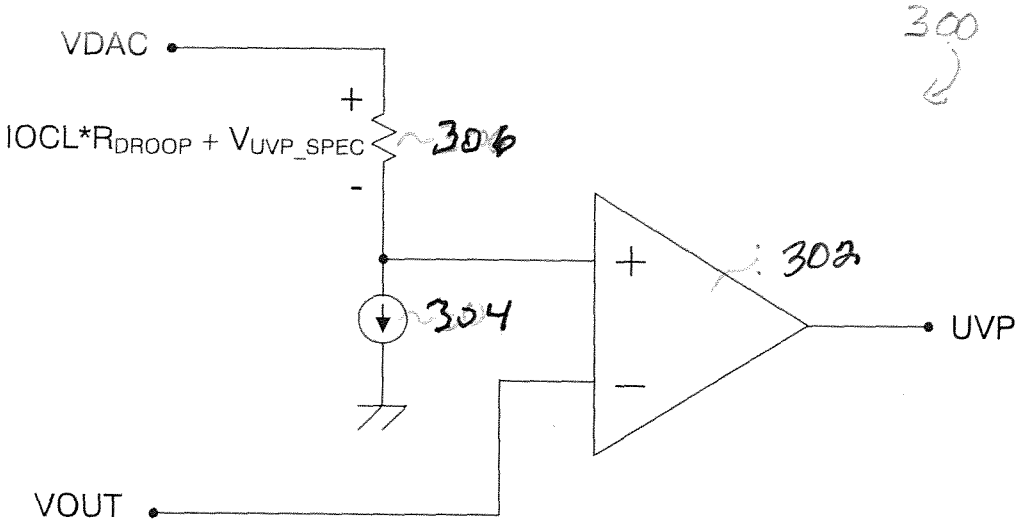

FIG. 3

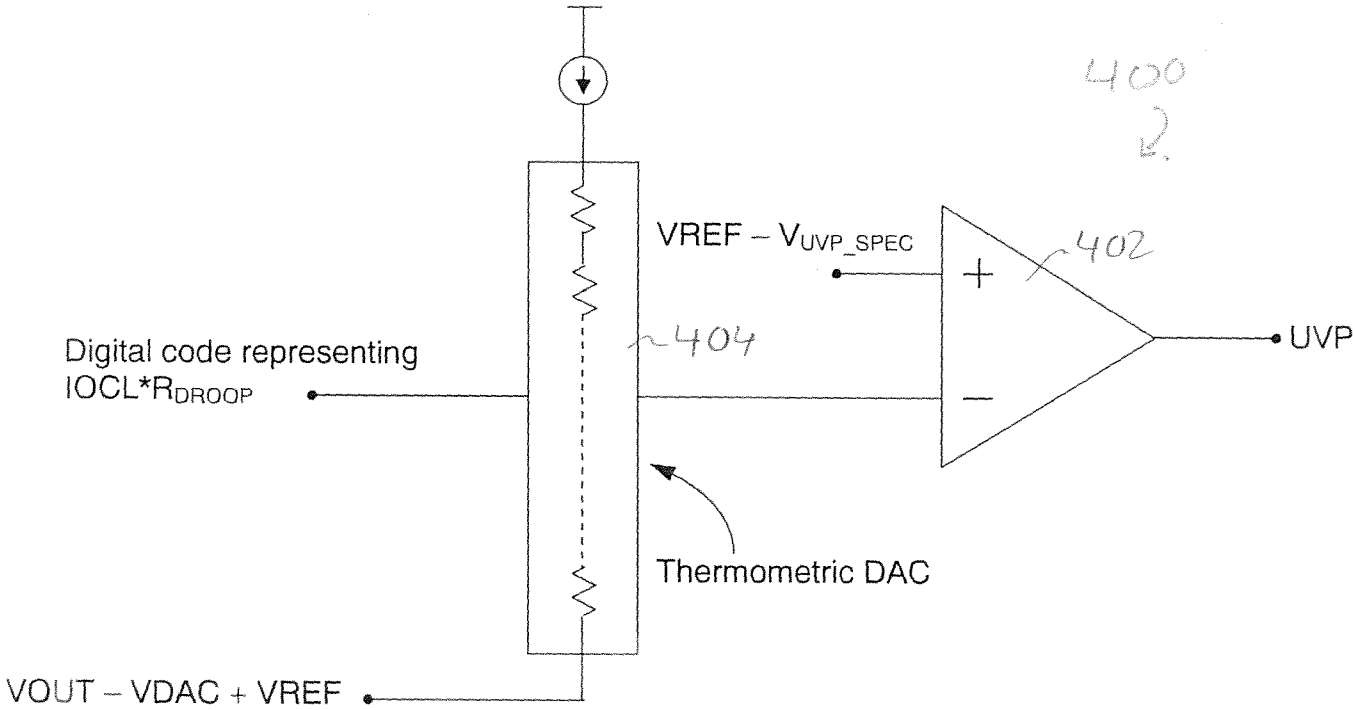
400
VREF – V_{UVP_SPEC}
402
404
Digital code representing
IOCL*R_{DROOP}
UVP
Thermometric DAC
VOUT – VDAC + VREF

FIG. 4

INTERNATIONAL SEARCH REPORT

International application No.

PCT/US 2017/033193

A. CLASSIFICATION OF SUBJECT MATTER

H02H 3/24 *(2006.01)*

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H02H 3/24; G05F 1/565, 5/08

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

PatSearch (RUPTO internal), USPTO, PAJ, Esp@cenet, DWPI, EAPATIS, PATENTSCOPE

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US2015/0015215 A1 (UNIVERSAL GLOBAL SCIENTIFIC INDUSTIAL CO,LTD) 15.01.2015	1-8
A	US5666044 A (CHERRY SEMICONDUCTOR CORPORATION) 09.09.1997	1-8
A	CN104283472 A (UNIVERSAL SCIENTIFIC INDUSTRIAL CO., LTD) 14.01.2015	1-8
A	FR2476927 A (LABORATORES D'ELECTRONICUE ET DE PHISICUE APPLIOUEE LEP) 28.08.1981	1-8

☐ Further documents are listed in the continuation of Box C.

☐ See patent family annex.

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Date of the actual completion of the international search	Date of mailing of the international search report
07 August 2017 (07.08.2017)	17 August 2017 (17.08.2017)

Name and mailing address of the ISA/RU:	Authorized officer
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