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(54) SEMICONDUCTOR CIRCUIT ARRANGEMENTS

(71) We, INTERNATIONAL BUSINESS MACHINES CORPORATION, a corporation organized and existing under the laws of the State of New York in the United States of America, of Armonk, New York 10504, United States of America do hereby declare the invention for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

This invention relates to semiconductor circuit arrangements including an integrated circuit comprising a bipolar inverting transistor and a charge injection zone close to the base-emitter junction of the inverting transistor.

According to one aspect of the invention, a circuit arrangement includes (1) an integrated semiconductor circuit comprising a bipolar inverting transistor and a charge injection zone sufficiently close to the base-emitter junction of the inverting transistor to supply power to the inverting transistor by charge carrier injection and (2) sensing circuit means connected between the charge injection zone and a terminal for the supply of current to the charge injection zone, to detect a reduction in current supplied via the terminal to the charge injection zone when the inverting transistor is rendered conductive by the application of a suitable potential to its base, the reduction in current being due to the reinjection of current into the charge injection zone by the inverting transistor.

According to another aspect of the invention, a data storage circuit arrangement includes an integrated semiconductor circuit comprising a pair of cross-coupled bipolar inverting transistors and a pair of charge injection zones each sufficiently close to the base-emitter junction of an associated one of the inverting transistors to supply power to that transistor by charge carrier injection; a pair of bit lines, a different one of the pair being

connected to each of the charge injection zones; and sensing circuit means connected to the pair of bit lines to detect reinjection of current into one of the injection zones by the inverting transistor with which that zone is associated, the reinjection of current being due to the conductive state of that transistor.

In the past few years the field of logic networks with bipolar transistors has seen some major improvements which have attracted the attention of the experts and which under the term MTL (Merged Transistor Logic) or I<sup>2</sup>L (Integrated Injection Logic) have gained entry to a great number of technical publications. Attention is drawn, for example, to the articles in IEEE Journal of Solid-State Circuits, Vol. SC-7, No. 5, October 1972, pp. 340 ff and 346 ff and to the relevant patent literature, such as UK Patent Specification No. 1284257. This injection logic concept is essentially based on inverting single or multiple collector transistors which are powered by direct minority carrier injection, i.e., by minority carrier injection inside the semiconductor body, close to (order of magnitude one diffusion length) their emitter-base junctions.

This bipolar logic concept has short switching times. In addition, it is suitable for the manufacture of extremely highly integrated large-scale logic circuits with a great number of logic elements on one single semiconductor chip. In order to produce logic circuits in highly integrated technology, essentially three requirements have to be met. The basic circuits must be simple and require little space, so that as great a number of them as possible can be arranged on one semiconductor chip. In addition, the layout of the circuits must be such that an adequate speed does not excessively increase the power dissipation on the chip, which is tantamount to the requirement that the product of the factors delay time and power dissipation per logic function should be low. Finally, to achieve a

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good yield and thus for technological and economical reasons, the manufacturing process required must be simple and easy to master. All these requirements are basically met by the logic concept described, particularly in comparison with other existing logic concepts (e.g. TTL logic).

One basic structure of this logic concept, as described in the above-mentioned UK patent specification, consists in that the emitter and collector zones of a lateral transistor structure are arranged, suitably spaced from each other, in a semiconductor basic material of a first conductivity type. The collector zone of the lateral transistor structure comprises at least one further zone of the opposite conductivity type to serve as a collector zone of an inversely operated vertical transistor structure. The collector zone of the lateral transistor structure simultaneously forms the base zone of the vertical transistor structure. The base zone of the lateral transistor and the emitter zone of the inversely operated vertical transistor structure are formed by the semiconductor basic material of the first conductivity type. For operating this semiconductor structure as a basic logic circuit, a current is impressed into the emitter zone of the lateral transistor structure. As a function of the input signal applied to the base zone of the vertical transistor, this current controls the output signal current through the vertical transistor structure. By merging the identically doped zones connected to the same potential, a structure is obtained offering an optimum degree of integration and requiring in the embodiment considered only two diffusion processes.

Other known embodiments of this basic circuit consist of a layer structure with four zones of different conductivity types which comprise two vertical monolithically merged transistor structures and which are suitably operated. The minority carriers are again injected via the emitter zone of one transistor, which causes the basic circuit to be powered, while the necessary signal inversion is effected via the other transistor structure.

The logic networks required can be realized by suitably combining such inverting logic circuits.

For determining the conductive or the switching state of individual inverting transistors of the basic circuits as a result of a logic function, the signal path must comprise suitable sensing circuits. These sensing circuits generally load the signal paths, causing additional undesired increases in the switching times. Therefore, it is desirable to reduce such loading of the signal path to a minimum.

The inverting basic logic circuits

described are not only excellently suited to building logic networks but they can also be used to advantage as a component for monolithically integrated storage cells. Such storage cells are used in particular in digital data processing systems. The cells are arranged in the form of an array, so that each cell can be addressed via suitable selection means, while data are written into or read from it.

It is known that inverting logic circuits require two stages to obtain storage cells in the form of bistable circuits or flip-flops. A storage cell thus consists of two such basic circuits which are symmetrically designed, the output of one circuit being connected to the input of the other to fulfil the feedback condition. In this manner the usual flip-flop cross-coupling is obtained.

U.K. Patent Specification No. 1374058 describes a storage cell which consists of two of the logic circuits referred to above, the collector of the inverting transistor of one circuit being cross-coupled to the base of the inverting transistor of the other circuit. The two inverting transistors are again inversely operated, forming the actual flip-flop transistors. The complementary transistor of each basic circuit serves as a load element for the two flip-flop transistors. This complementary transistor, via which the minority carrier injection, i.e., the power supply, is effected, is connected by means of a separate line. For addressing, i.e., for writing into and reading from a storage cell, the base of each flip-flop transistor is additionally connected to the emitter of an associated additional complementary addressing transistor, whose collector is connected to the associated bit line and whose base is connected to the address line. Thus in addition to the injecting transistor forming the load element, a further addressing transistor is required which is again formed by a lateral transistor structure.

The simple semiconductor structure required is obtained by laterally arranging the two circuits forming one storage cell each and by merging the zones connected to the same potential. This known storage cell permits building up a storage array in which the storage cells are arranged in at least two horizontal rows and in at least four vertical columns. A first vertical address line is associated with the first and the second column and a second vertical address line is associated with the third and the fourth column. In addition, a first horizontal address line is associated with the first row and a second horizontal address line with the second row. Finally, a first bit line pair is associated with the first column, a second bit line pair with the second and the third column and a third bit line pair with the

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fourth column, whereby each bit line pair extends preferably in a vertical direction between the associated columns.

The bit lines are connected in each case to the collectors of the addressing transistors, the first address line is connected to the emitters of the transistors forming the load elements, and the second addressing line is connected to the bases of the addressing transistors.

How the invention can be carried into effect will now be described by way of example, with reference to the accompanying drawings, in which:—

Fig. 1A represents, in section, an inverting logic circuit structure embodying the invention;

Fig. 1B is an equivalent circuit diagram of the structure represented in Fig. 1A showing the operation of the circuit;

Fig. 2A is an equivalent circuit diagram of a storage cell embodying the invention consisting of two cross-coupled basic circuits as shown in Fig. 1A and Fig. 1B;

Fig. 2B represents a plan of part of an integrated storage array with storage cells embodying the invention; and

Figs. 2C and 2D are sectional views of the storage array represented in Fig. 2B.

A semiconductor structure (Fig. 1A) forms the basic structure of the logic known under the term "Integrated Injection Logic".

The layout and the operation of this structure are described in detail in the literature mentioned at the beginning of the present specification, so that subsequently only a summary need be given. The designations chosen are such that they simultaneously indicate the conductivity type of the individual zones.

As a basic material a lightly doped semiconductor substrate of a first conductivity type, for example, of the P-conductivity type, is used. On the semiconductor substrate a highly doped buried  $N^+$  zone of the opposite conductivity type is arranged. The buried  $N^+$  zone is followed by an N-doped epitaxial layer N1. Two oppositely doped zones P1 and P2 are embedded spaced from each other in the epitaxial layer N1. In the zone P2 a further zone N2 doped oppositely thereto is arranged. The equivalent circuit diagram of this structure is shown in Fig. 1B, the identical designation of the individual identical zones permitting a direct comparison between the structure and the equivalent circuit diagram.

Thus the inverting logic basic circuit essentially consists of an inverting transistor with the zone sequence N2 P2 N1, which is fed by the direct injection of minority carriers. The inverting transistor is designed as an inversely operated, vertical transistor.

For the purpose of injecting minority carriers, a complementary transistor with a P1 N1 P2 zone sequence is provided, which is arranged laterally in the structure considered. The two transistors are jointly integrated, utilizing common semiconductor zones and thus permitting the highest degree of integration. The epitaxial layer N1 simultaneously serves as the base zone of the lateral transistor P1 N1 P2 and as the emitter of the vertical transistor N2 P2 N1. Zone P1 forms the emitter of the lateral transistor. Zone P2 simultaneously forms the base of the vertical, inverting transistor and the collector of the injecting lateral transistor. Zone N2 forms the collector of the inverting transistor. An injector terminal I, via which a current is externally provided in the direction of the arrow, is arranged on zone P1 forming the emitter of the injecting transistor. This current supplies the operating current for the inverting transistor N2 P2 N1. A control terminal C, via which the conductive state of the inverting transistor is switched, connected to zone P2 forming the base of this transistor. The collector terminal O which simultaneously forms the output of the inverting basic circuit is arranged on zone N2.

To embody the invention, the basic circuit is extended by a sensing circuit S connected in the injection current path, i.e., to the power supply. The conductive state of the inverting transistor, determined by the control signal on control terminal C, can be sensed by the sensing circuits. For this purpose advantage is taken of the fact that with a conductive inverting transistor N2 P2 N1, base zone P2 simultaneously acts as an emitter reinjecting into zone P1 of the lateral transistor structure a current opposite to the normal injection or supply current. Thus when the inverting transistor is conducting, the current flowing through injector terminal I has a lower value than with a non-conductive transistor (assuming the same VBE). This current difference can be sensed by means of a standard sensing circuit. For this purpose the sensing circuit can be designed in such a manner that it senses either the current difference or a corresponding voltage difference. For this reason the sensing circuit S is shown merely as a block circuit in Figs. 1A and 1B. In the equivalent circuit diagram of Fig. 1B current from the transistor structure marked by broken lines is reinjected when the inverting transistor is conductive. This transistor structure is identical to the injecting transistor structure P1 N1 P2, the emitter and the collector functions being merely exchanged. In this manner means are obtained for sensing the conductive state of the inverting transistor without the need for additional lines or additional

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semiconductor zones in the basic structure.

Two of the basic circuits shown in Figs. 1A and 1B can be merged to form a highly integrated storage cell, as shown in the equivalent circuit diagram of Fig. 2A. The individual semiconductor zones bear the same reference symbols as in Figs. 1A and 1B, the designations of one of the two basic circuits being provided with superscripts for ready distinction.

The storage cell is designed in the form of a flip-flop. The two inverting transistors T3 and T4 form the actual flip-flop transistors. The collector of the inverting transistor of one basic circuit is cross-coupled to the base of the inverting transistor of the other basic circuit. In this manner the required mutual feed-back of the two inverting basic circuits is achieved. The transistors T1 and T6 of one and the transistors T2 and T5 of the other basic circuit form the injecting reinjecting transistor structure for the associated complementary, inverting transistor. The injector terminal I (see Figs. 1A and 1B) of each basic circuit is connected to a respective bit line B01, B11 of a bit line pair. The emitters of the two flip-flop transistors T3 and T4 are connected to a common address line X.

A plan view and partial sectional views of the structural layout of a storage array consisting of such storage cells are shown in Fig. 2B and Figs. 2C and 2D, respectively.

A section of a storage array comprising six storage cells is shown in Fig. 2D. The storage cells are arranged in a known manner in rows and columns (Fig. 2B). The individual rows are electrically insulated from each other by means of isolation zones P3, P4 embedded in zone N1 common to all the storage cells. One bit line pair B01—B11, B02—B12 and B03—B13, respectively, is associated with each vertical column of storage cells. Thus each storage cell is made up of two zones P1, P2, N2 and P1', P2', N2' common to all storage cells of the array and arranged in an epitaxial layer N1 on a P- substrate. The functions of said zones will be described by means of Figs. 1 and 2A. The bit lines B0X of each pair are connected in each case to the injecting zones P1 and the bit lines B1X are connected to the injecting zones P1' of each storage cell of the associated column. The cross-coupling between zones N2 and N2' of each storage cell, which form the collectors of the two inverting transistors and the flip-flop transistors T3, T4, consists of two conductors M1 and M2 extending across an insulating layer D (Figs. 2C and 2D). The address line X1, X2, etc., of each row of storage cells is formed by the highly doped, buried N<sup>+</sup> zoned arranged in each row.

Adjacent storage cells of a row can be separated from each other either by a

suitable inhibitor zone or by a suitably selected mutual spacing.

This description gives an idea of the degree of integration, the simple layout, and the easy manufacturing process of the storage cell structure and the whole storage array.

Only one bit line pair per column and one address line X in the form of a buried N<sup>+</sup> zone per row are required for operating the storage array.

The operation of a storage cell embodying the invention will now be described in detail with reference to Fig. 2A. In the standby state all address lines X have the same potential. This potential may be, for example, 0.5 volt. The two bit lines B01 and B11 are each connected to a potential about 0.7 volt higher than that of the address line X. The potential of the bit lines is controlled in such a manner that the same current  $IE_1 = IE_2$  flows in the injecting transistors T1 and T2 (which simultaneously form the load transistors) of all the cells. This holds for base emitter voltages  $V_{BE1} = V_{BE2}$ . If the current amplification of transistors T3 and T4 in common emitter configuration is greater than 1, the flip-flop adopts a stable state in which the standby current of the cell can be chosen to be very low.

For addressing the storage cell, the potential of the address line X is lowered by several hundred millivolts, for example, to 0 volt.

For reading there are two different operating modes.

A read operation consists in that the same potential is impressed onto both bit lines, so that the two injecting and load transistors T1 and T2, respectively, carry the same current  $IE_1 = IE_2$ . This current is preferably chosen higher than that in the standby state, in order to achieve a higher speed. The non-selected cells connected to the same bit line pair are practically cut off from the power supply during this process, since the emitter-base voltage of the load transistors T1 and T2 is several hundred millivolts lower than the emitter-base voltage of the flip-flop transistors T3 and T4 of the selected address line X. However, in comparison with the read time, the information of the non-selected storage cells is maintained for a long time by the stored load in the flip-flop transistor capacities. If the flip-flop transistor T3 is conductive and the flip-flop transistor T4 is non-conductive, an emitter current  $IE_6$  flows in transistor T6, while no such current flows in transistor T5. In accordance with the current amplification  $\alpha_6$  of transistor T6, a current  $\alpha_6 \times IE_6$  flows back into bit line B0, so that the current  $I_0 = IE_1 - \alpha_6 \times IE_6$  flows in said bit line. The current

flowing in bit line B1 is  $I_1 = I_{E2}$ . As with the same bit line potentials the currents  $I_{E1}$  and  $I_{E2}$  have the same magnitude, the current difference obtained is  $\Delta I = I_1 - I_0 = \alpha_6 \times I_{E6} \approx \alpha_1 \times \alpha_6 \times I_{E1}$ . This current difference  $\Delta I$  can be measured by means of a sensing circuit in the form of a low-resistivity amplifier and is indicative of the switching or storage state of the storage cell.

The second mode suitable for reading consists in that the impressed voltages are replaced by impressed currents on the bit lines. In this case  $I_0 = I_1$ , so that the emitter currents  $I_{E1}$  and  $I_{E2}$  of the injecting transistors assume the values  $I_{E1} = I_0 + \alpha_6 \times I_{E6} \approx I_0 + \alpha_1 \times \alpha_6 \times I_{E1}$  and  $I_{E2} = I_1 = I_0$ .

From this  $I_{E2}/I_{E1} \approx 1 - \alpha_1 \times \alpha_6$  is obtained for the ratio of the two currents. On the basis of the known diode equation  $I_E = I_S \times \exp V_{BE}/26\text{mV}$  (reverse saturation current  $I_S$ ) a voltage difference  $\Delta V \times V_{BE2} - V_{BE1} = 26 \text{ mV} \times \ln(1 + \alpha_1 \times \alpha_6)$  is obtained. For  $\alpha_1 = 0.7$  and  $\alpha_2 = 0.7$  the voltage difference obtained is, for example,  $\Delta V \approx 10 \text{ mV}$ .

This voltage difference can be amplified by means of a differential amplifier connected to the bit lines and thus supplies a signal characterizing the storage state of the cell.

A write operation is extraordinary simple. As in the case of a read operation, the address line X is lowered by several hundred mV. A current is applied to one of the two bit lines. If, for example, flip-flop transistor T4 is to be made conductive, then a current  $I_1$  is applied to bit line B11 only. A large part of the current  $I_1$  flows into the base of flip-flop transistor T4, switching this transistor. This determines the storage state of the cell.

The schematic structural layout illustrated in Figs. 2B, 2C and 2D shows that the storage cell requires only a very small semiconductor area. All cells of an array with a common X-address are arranged in a strip-shaped isolation region (row), the low-resistivity  $N^+$  zone simultaneously serving as a subcollector for the flip-flop transistors and as an address line.

In the standby state the zones P1 and P1' act as emitters and the zones P2 and P2' as collectors. During writing, Zone P1 or zone P1' acts as an emitter and zone P2 or zone P2' as a collector. During reading, zone P2 or zone P2' acts as an emitter and zone P1 or zone P1' as a collector. The two zones P1 and P2' are connected to bit lines B01 and B11. Thus only these two lines are required for wiring the storage cell in a storage array.

Apart from the simple operation, only very small voltage swings are necessary for operating the storage cell. Thus, only simple peripheral circuits are necessary.

#### WHAT WE CLAIM IS:—

1. A circuit arrangement including (1) an integrated semiconductor circuit comprising a bipolar inverting transistor and a charge injection zone sufficiently close to the base-emitter junction of the inverting transistor to supply power to the inverting transistor by charge carrier injection and (2) sensing circuit means connected between the charge injection zone and a terminal for the supply of current to the charge injection zone, to detect a reduction in current supplied via the terminal to the charge injection zone when the inverting transistor is rendered conductive by the application of a suitable potential to its base, the reduction in current being due to the reinjection of current into the charge injection zone by the inverting transistor.

2. A circuit arrangement as claimed in claim 1, in which the integrated circuit is formed on a lightly doped semiconductor substrate of one conductivity type, the collector zone of the transistor is part of an epitaxial layer of the opposite conductivity type, the base zone of the transistor is a zone of said one conductivity type formed in the epitaxial layer and the emitter zone of the transistor is a zone of the opposite conductivity type formed in the emitter zone, and the charge injection zone is a further zone of said one conductivity type formed in the epitaxial layer on one side of the base zone of the transistor.

3. A circuit arrangement as claimed in claim 2, in which the substrate is of P-conductivity type.

4. A data storage circuit comprising a pair of circuit arrangements as claimed in claim 2 or claim 3, the collector of the inverting transistor of one arrangement being cross-connected to the base of the inverting transistor of the other arrangement and *vice versa* and a pair of bit lines, a different one of the pair being connected to each of the charge injection zones, to apply an operating potential and read/write signals to the charge injection zones.

5. A data storage circuit as claimed in claim 4, further comprising an address line connected to the emitters of the inverting transistors.

6. A data storage circuit as claimed in claim 5, in which the address line comprises a highly doped zone of the opposite conductivity type buried in the epitaxial layer beneath the zones of the one conductivity type.

7. A data storage circuit as claimed in any of claims 3 to 6, in which the pair of circuit arrangements are integrated side-by-side in a semiconductor body and the cross-connections are made by conductors

disposed on an insulating layer on the semiconductor body.

5 8. A circuit arrangement substantially as described with reference to Figs. 1A and 1B of the accompanying drawings.

9. A data storage circuit arrangement including an integrated semiconductor circuit comprising a pair of cross-coupled bipolar inverting transistors and a pair of charge injection zones each sufficiently close to the base-emitter junction of an associated one of the inverting transistors to supply power to that transistor by charge carrier injection; a pair of bit lines, a different one of the pair being connected to each of the charge injection zones; and sensing circuit means connected to the pair of bit lines to detect reinjection of current into one of the injection zones by the inverting transistor with which that zone is associated, the reinjection of current being due to the conductive state of that transistor.

10. An arrangement as claimed in claim 9, in which the integrated circuit is formed on a lightly doped substrate of one conductivity type, the collector zone of each transistor is part of an epitaxial layer of the opposite conductivity type, the base zone of each transistor is a zone of said one conductivity type formed in the epitaxial layer and the emitter zone of each transistor is a zone of the opposite conductivity type formed in its emitter zone and each of the charge injection zones is a further zone of said one conductivity type formed in the epitaxial layer on one side of the base zone of the transistor with which it is associated.

11. A data storage circuit arrangement as

claimed in claim 9 or claim 10, further comprising an address line connected to the emitters of the inverting transistors. 40

12. A data storage circuit arrangement as claimed in claim 11, in which the address line comprises a highly doped zone of the opposite conductivity type buried in the epitaxial layer beneath the zones of the one conductivity type. 45

13. A data storage circuit arrangement as claimed in claim 12, in which the integrated circuit comprises a matrix of storage cells each comprising a pair of cross-coupled bipolar inverting transistors and a pair of charge injection zones each sufficiently close to the base-emitter junction of an associated one of the inverting transistors to supply power to that transistor by charge carrier injection, and the integrated circuit is formed so that the emitter zones of all the inverting transistors are comprised in a common epitaxial layer, the rows of storage cells are isolated from each other by isolation strips in the semiconductor body, a common buried address line serves each row of cells and there is a corresponding pair of bit lines connected to the charge injection zones of all the cells in each column. 50 55 60 65

14. A data storage circuit arrangement as claimed in claim 7, substantially as described with reference to Figs. 2A to 2D of the accompanying drawings. 70

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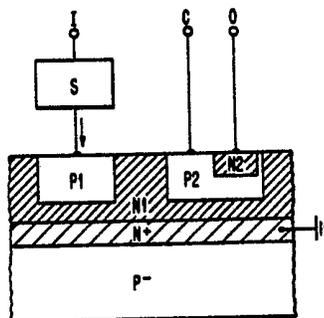


FIG. 1A

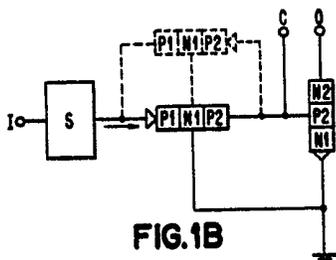


FIG. 1B

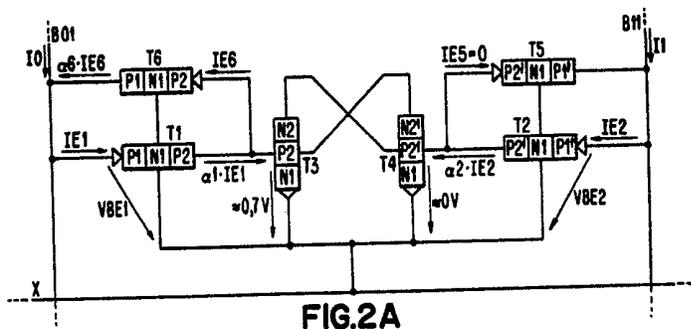


FIG. 2A

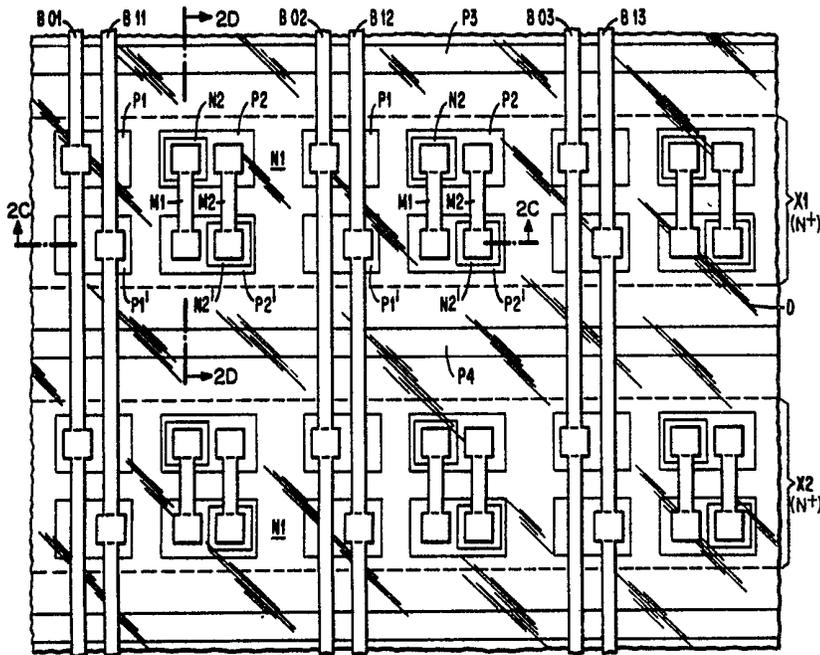


FIG. 2B

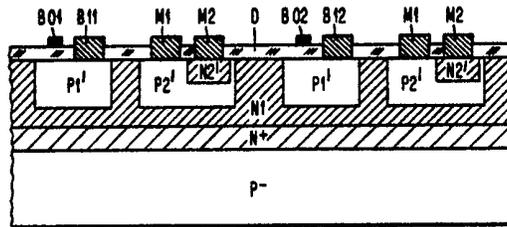


FIG. 2C

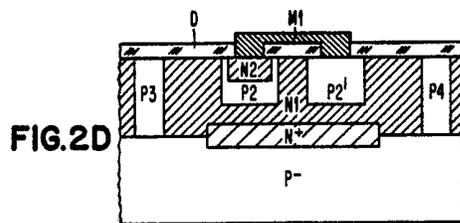


FIG. 2D