A processor architecture which permits the registers (1024, 1026) and control latches (1072-1090) of the processor to be easily accessed without using instructions to achieve such access. The architecture provides for an internal access (IA) function which is enabled by applying an IA Request signal to an IA terminal (1039) of the processor. During the IA function, normal program execution in the processor is suspended and the registers (1024, 1026) and control latches (1072-1090) may be accessed as if they were storage locations in a random-access memory. After the IA function is enabled, the address of a register or control latch selected for access is applied to the Address/Data port (1001) of the processor, and an IA Control Code specifying the strobing of the Address/Data port is applied to the Status terminals (1035-1038) of the processor. After strobing of the address, a second IA Control Code specifying either reading or writing of the selected register or control latch is applied to the Status terminals (1035-1038). If the second Control Code specifies reading, the contents of the selected register (1024, 1026) or control latch (1072-1090) is provided at the Address/Data port (1001). If the second Control Code specifies writing, data received at the Address/Data port (1001) is stored in the selected register.
<table>
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</tr>
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MICROPROCESSOR ARCHITECTURE HAVING INTERNAL ACCESS MEANS

This invention relates to a processor for executing a program of instructions, the processor comprising input/output terminals for receiving instructions for normal operation of the processor, input/output buffers for forwarding the instructions, for normal operations of the processor, a plurality of internal registers for storing data for normal operations of the processors, status terminals for delivering output status information from the processor, a control circuit responsive to a present instruction for the normal operation, for providing normal control signals governing the execution of a normal processor operation specified by the present instruction, including register control signals governing the reading and/or writing of the internal registers.

Integrated circuits capable of performing the functions of a processing unit of a digital computer are known in the art. Such circuits, termed microprocessors, are now widely used in a variety of relatively low-cost data processing applications such as, stored program controlled telephone equipment, data terminals, electric appliance controls, and home computers. Normally, microprocessors are combined with other components, such as memory circuits and input/output circuits, to form microcomputers. Some of the more recently developed microprocessors and microcomputers are fabricated entirely on a single integrated circuit chip.

In general, a microprocessor is designed to execute a sequence of instructions called a program and includes means for fetching instructions from a program store, an instruction register for storing a present instruction being executed, a plurality of internal registers for storing operands, addresses, and intermediate
data, and a control unit for decoding the current instruction and providing control signals to govern the execution of a processor operation specified by the current instruction. Since most processor operations involve the reading and/or writing of certain internal registers, the control unit provides register control signals for controlling such reading and writing operations when required for the execution of the current instruction.

Recent advances in integrated circuit technology in the areas known as very-large-scale-integration (VLSI) have made feasible the design of single-chip microprocessors and microcomputers having more complex architectures than was previously possible. For example, such advances have made possible microprocessor architectures having wider and more numerous internal busses, "pipeline" arrangements which allow the overlapping of fetch and execute operations, and wider and more numerous internal registers. However, such increases in the architectural complexity of microprocessors impinge upon both the testing of and the development of programs in such microprocessors.

In general, program development in a microprocessor becomes more difficult as the complexity of the microprocessor increases. In order to detect and diagnose program "bugs" efficiently, a programmer should monitor and analyze the contents of the internal registers of the microprocessor during program execution. As the complexity of the microprocessor increases, the number of internal registers to be monitored by the programmer also increase. Furthermore, in prior art microprocessors the available means for monitoring the contents of internal registers are inconvenient and some internal registers cannot be directly monitored at all.

Typically, the internal registers of a microprocessor fall into two categories, namely a user and a nonuser category. The user category includes those internal registers which can be directly accessed (i.e.,
read and/or written) through the execution of appropriate instructions, while the nonuser category includes those internal registers, such as the temporary data registers, temporary address registers, program counter and control latches, which cannot be directly accessed through instructions. Because in prior art microprocessors the only available means for observing the contents of internal registers is through the execution of appropriate instructions, only those registers in the user category are available for monitoring during program development, and such monitoring requires the insertion of appropriate additional instructions in predetermined locations in a program under development. Thus, microprocessors of the prior art have the problems of not permitting a programmer to directly observe the contents of registers in the nonuser category and inconveniently requires the programmer to alter the program under development by the insertion of additional instructions whenever monitoring of internal registers is desired at particular program locations. Therefore, from the standpoint of facilitating program development it would be advantageous to have a microprocessor architecture which would permit a programmer to monitor the contents of internal registers in both the user and nonuser categories without having to use program instructions for such monitoring.

Functional testing of a microprocessor also becomes more difficult as the complexity of the microprocessor increases. Because tests on an integrated circuit chip can only be made from the terminals (i.e., the bonding pads or package pins) of the chip, and because the internal conductors of the chip are, as a practical matter, not accessible for either the application of test signals or the observation of circuit responses, therefore the individual functional components of a microprocessor, such as the control unit, the arithmetic unit, etc., cannot be tested independently but only as part of signal paths between input and output terminals. Consequently, not all
of the potential logical faults in the various functional components are detectable using tests made only from the terminals of the chip. The number of undetectable logical faults tend to increase as the complexity of the microprocessor increases.

Functional testing of a digital integrated circuit chip is typically performed by applying a sequence of binary logic signals called test vectors to the input terminals of a chip being tested and by observing the response signals called output vectors at the output terminals of the chip. Logical faults in the chip are detected by comparing the observed output vectors with those which would be expected from a properly functioning chip, a disagreement in the comparison indicating the existence of one or more logical faults in the chip. Both the application of the test vectors and the comparison of the output vectors are typically performed by automatic test equipment.

A test vector sequence is normally designed to minimize the number of logical faults which are undetectable in a functional test while using the shortest possible sequence. The undetectable faults are undesirable since chips having such faults would pass the functional test. An excessively lengthy test vector sequence is also undesirable since such a sequence would require a long testing time and therefore lead to a high testing cost. A figure of merit for a test vector sequence, commonly referred to as the fault coverage, is the percentage of all potential logical faults of the chip being tested which are detectable in a functional test using that test vector sequence. In general, the maximum achievable fault coverage for a test vector sequence for functional testing of a prior art microprocessor is less than one hundred percent and decreases as the complexity of the microprocessor increases. Moreover, the length of a test vector sequence required to achieve maximum fault coverage increases as the complexity of the microprocessor being
tested increases.

It is known that the maximum achievable fault coverage in the functional testing of a microprocessor can be increased and the length of the test vector sequence for achieving maximum fault coverage can be decreased by increasing the access to the internal circuit nodes of the microprocessor for the purpose of applying of test signals and of detecting circuit responses. Access to many of the internal circuit nodes of a microprocessor can be achieved by providing direct access to the internal registers of the microprocessor. However, to derive optimal testing benefits from such access, the means which are used to provide access to the internal registers must not themselves introduce a significant number of undetectable logical faults. Therefore, such means should be simple and should be largely independent of the other functional components of the microprocessor, particularly the control unit. Therefore, such means should not be under the control of microprocessor instruction.

In a copending United States patent application having Serial No. 61,741, entitled "Microprocessor Architecture for Improved Chip Testability" and filed on July 30, 1979 in the name of M. Shoji, a co-inventor in the present application, it was disclosed that a substantial number of the undetectable logical faults in a microprocessor are situated in the control unit and that a significant improvement in the functional testing of a microprocessor can be achieved by making the control signals from the control unit directly observable at the terminals of the microprocessor chip. According to the Shoji application, observability of the control signals is achieved by providing the microprocessor with means for directly coupling the control lines of the microprocessor to its terminals. However, where the control unit of a microprocessor includes control latches for storing control signals, observability of the control signals may also be achieved by providing means for directly reading the
control latches.

In view of the above-discussed problems in functional testing and in program development, a need clearly exists for a microprocessor architecture which provides random access to the internal registers of the microprocessor including the control latches by independent means which are not under the control of instructions.

**Summary of the Invention**

The problem is solved in accordance with the invention in which the processor further comprises a first circuit for receiving a test command signal from an external source and for generating a test enable signal to enable the processor to execute a test operation, a timing generator responsive to the test enable signal for suspending the execution of the normal operations, the input/output buffers for receiving and forwarding test addresses of a specified internal register during the test operation, a second circuit comprising a decoder responsive to the present test address for providing during test operation a selection signal corresponding to the specified internal register, the status terminals being connected for receiving test control codes, and a control block responsive to the test control codes for generating test control signals, third circuitry connected for receiving the register control signals during normal operation and the test control signals during test operation and responsive both to the selection signal and to the test enable signal for providing appropriate ones of the test control signals to the specified internal register during test operation and for providing the register control signals to the specified internal register during normal operation, whereby during test operation the input/output buffer receives data from the input/output terminals, which data are to be stored in the specified internal register when writing is specified by the present test control code, but delivers data to the input/output terminals from the specified internal register when reading is specified by
the present test control code.

**Brief Description of the Drawings**

- FIGS. 1 and 2 form a block diagram of a processor unit according to a preferred embodiment of the present invention, the relative positions of FIGS. 1 and 2 being shown in FIG. 25.

- FIG. 3 is a timing diagram illustrating the timing signals of the processor unit;

- FIG. 4 is a timing diagram illustrating the principal signals of the IA function;

- FIG. 5 is a logic diagram of a preferred embodiment of the IA Request Enable Circuit;

- FIG. 6 is a logic diagram of a preferred embodiment of the IA Input Latches and the IA Control Block;

- FIG. 7 is a logic diagram of a preferred embodiment of the Timing Generator;

- FIG. 8 is a logic diagram of the Reset circuit;

- FIG. 9 is a logic diagram of preferred embodiments of the IA A-BUS Latch and the Temporary A-BUS Register Address Decoder;

- FIG. 10 is a logic diagram of one of the Temporary A-BUS Registers (R-latch), and a preferred embodiment of its associated Control Multiplexers;

- FIG. 11 is a logic diagram of another one of the Temporary A-BUS Registers (Q-latch), and a preferred embodiment of its Control Multiplexers;

- FIG. 12 is a logic diagram of another one of the Temporary A-BUS Registers (Address Latch), and a preferred embodiment of its associated Control Multiplexers;

- FIG. 13 is a logic diagram of a preferred embodiment of the IA User Register Address Multiplexers;

- FIG. 14 is a logic diagram of the User Register Array Address Decoder;

- FIG. 15 is a logic diagram of the User Register Array;
FIG. 16 is a logic diagram of a preferred embodiment of the User Register Array Control Multiplexers;
FIG. 17 is a logic diagram of preferred embodiments of the IA Control Latch Address Latch and the Control Latch Address Decoder;
FIG. 18 is a logic diagram of the BUS Multiplexer and a preferred embodiment of the BUS Control Multiplexers;
FIG. 19 is a logic diagram of a preferred embodiment of the IA C-BUS Latch and the Temporary C-BUS Register Address Decoder;
FIG. 20 is a logic diagram of one of the Temporary C-BUS Registers (TA) and a preferred embodiment of its associated Control Multiplexers;
FIG. 21 is a logic diagram of the I/O Buffers;
FIG. 22 is a logic diagram of a preferred embodiment of the I/O Buffer Control Multiplexers;
FIG. 23 is a logic diagram of the State Vector Latches and a preferred embodiment of the State Vector Initialization circuit; and
FIG. 24 is a logic diagram of a preferred embodiment of the Status Generation Logic;
FIG. 25 shown on the same sheet with FIG. 3 illustrates the relative positions of FIGS. 1 and 2.

Detailed Description

Referring now to FIGS. 1 and 2 there is shown a block diagram of a processor unit 1000 according to a preferred embodiment of the present invention. The relative positions of FIGS. 1 and 2 in the block diagram are shown in FIG. 25. Only those functional components of the processor unit which are needed to explain the invention are depicted in FIGS. 1 and 2. For simplicity the other functional components such as Arithmetic Logic Unit and the Address Arithmetic Unit which are necessary to form a complete processing unit have been omitted from the figures. The processor unit is designed to execute a sequence of instructions which are received at the Input/Output (I/O) terminals 1001. In general, an
instruction consists of an op-code which specifies a processor operation to be performed by the processor unit and an operand descriptor which specifies the operands, if any, to be used for the processor operation. The operand descriptor typically includes an address mode code specifying one of several modes for fetching operands. The operand descriptor also includes either operand address data or, in the case of the immediate data mode, one or more actual operands. The op-code and the address mode code of an instruction which is presently being executed by the processor unit are stored in an Op-code Latch 1002 of a Control Unit 1006. The main function of the Control Unit is to decode the contents of the Op-code Latch and to provide control signals governing the execution of the processor operation specified by the op-code of the present instruction, including the fetching of operands required for that processor operation. The Control Unit also receives the contents of a Control Status Latch 1004, an External Signal Latch 1003, and a State Vector Latch 1005. The Control Status Latch contains the status flags of the processing unit, while the External Signal Latch contains those externally received signals, such as the INTERRUPT, RESET, DIRECT MEMORY ACCESS REQUEST, and EXTERNAL FAULT, which modify normal program execution. The State Vector Latch contains the feedback signals from the Control Unit which determine the next state of the Control Unit. The control signals from the Control Unit are stored in nineteen byte-width Control Latches 1072 to 1090 (not all are shown), the control signals being distributed from the Control Latches to the various functional components of the processing unit along control lines which are not shown.

The processing unit has two separate 32-bit busses, designated the A-BUS and the C-BUS, which communicate through a BUS Multiplexer (MUX) 1028. During normal operation of the processor unit, the operation of the BUS Multiplexer 1028 is governed by BUS Multiplexer Control signals from the Control Unit. The use of separate
busses permits arithmetic and logic operations to take place on the C-BUS simultaneously with operand fetch or instruction fetch operations on the A-BUS. The A-BUS is coupled to the I/O Buffers 1023 which during normal operation are governed by I/O buffer Control signals from the Control Unit.

The registers of the processor unit fall into three groups, namely the Temporary A-BUS Registers 1024, the User Register Array 1025, and the Temporary C-BUS Registers 1026. The Temporary A-BUS Registers include a Q-latch and a R-latch for storing data to be used for operand address formation, an Address Latch for storing the address of the next operand to be fetched and a Program Counter for storing the address of the next instruction to be fetched. During normal operation, the reading and writing operations of the Temporary A-BUS Registers are governed by the Temporary A-BUS Register Control signals from the Control Unit.

The User Register Array includes fifteen 32-bit registers used for local storage of frequently used data and addresses. The array is implemented with a 15x32 bit Random Access Memory (RAM) (FIG. 15) having its own User Register Array Address Decoder 1027 which during normal operation decodes User Register Array Address signals provided by an Instruction Buffer (not shown in FIGS. 1 and 2) to select a register in the Array specified by the Address signals. During normal operation the reading or writing of the selected register is governed by User Register Control signals provided by the Control Unit. The User Register Array is coupled to provide data to and to receive data from the C-BUS and also to provide data directly to the R-Latch.

The Temporary C-BUS Registers include five 32-bit registers for storing operands and intermediate data for arithmetic and logic operations. The reading and writing of these registers during normal operation are governed by Temporary C-BUS Register Control signals provided by the
Control Unit. The four groups of registers 1024, 1025, 1026 and the Control Latches 1072 to 1090 comprise the internal registers of the processor unit.

The timing signals for the processor unit are provided by the Timing Generator 1029 which receives external clock signals CK34 and CK23 at respective terminals 1030 and 1031 and provides internal clock signals CK1, CK2, CK3, CK4, CK23, CK34, and CK1-IA and their respective complements CK1, CK2, CK3, CK4, CK23, CK34, and CK1-IA. The relationship of the timing signals CK1 to CK4, CK23 and CK34 is illustrated in Fig. 3. The timing signals CK1 through CK4 mark the four phases $\phi_1$ through $\phi_4$ of a machine cycle of the processor unit. An instruction cycle for the processor unit may have from 2 to 391 machine cycles depending on the instruction being executed. Timing signal CK23 overlaps $\phi_2$ and $\phi_3$ while timing signal CK34 overlaps $\phi_3$ and $\phi_4$. The signals CK1-IA and CK1-IA will be explained below, in connection with the Internal Access function of the processor unit.

Referring again to Figs. 1 and 2, a Reset circuit 1032 receives an externally provided RESET signal at terminal 1033 and provides an appropriately timed internal reset signal RESET and its complement RESET1.

The Status Generation Logic 1034 provides a 4-bit Status Code on the STATUS 0 to STATUS 3 terminals 1035 to 1038. The Status Code provides information concerning the type of memory access operation, such as instruction fetch, operand fetch, address fetch, memory write and no operation which is to take place during the next machine cycle.

During normal operation of the processor unit only the registers of the User Register Array are directly accessible for reading and writing from the I/O terminals 1001. Such access is achieved through appropriate instructions and must, therefore, involve those functional components in the instruction execution path, such as the Operator Latch 1002, the Control Unit 1006, the Control Latches 1072 to 1090, the Temporary A-BUS
Registers 1024, and the Address Arithmetic Unit (not shown in FIG. 1 and 2). However, the processor unit of FIGS. 1 and 2 is provided with a special function called Internal Access in which the internal registers of the processor unit may be randomly accessed for reading and/or writing from the I/O terminals without involving the functional components of the instruction execution path.

The Internal Access (IA) function is enabled by the application of a logic "0" level IA signal to the IA terminal 1039. A logic "0" level signal will hereafter be referred to as "0". The IA signal is sampled by an IA Request Enable circuit 1040 at the beginning of $\phi3$ following its application. There are available in the processor unit two modes for the IA function, namely a Diagnostic Mode and Instruction Mode. In the Diagnostic Mode the IA function starts at the beginning of $\phi1$ following the sampling of a "0" IA signal. In the Instruction Mode, the IA function starts at the beginning of the second machine cycle of the instruction cycle following the one in which the IA signal is sampled. The selection of the IA mode will be explained below.

At the start of the IA function, the IA Request Enable circuit 1040 provides a IAREQ signal and its complement IAREQ. The IAREQ signal enables the IA circuitry and causes the Timing Generator 1029 to inhibit the CK1-IA and CK2-IA clock signals which control the Input Latches 1002 to 1005 of the Control Unit, the slave sections (designated by $S$) of the Control Latches 1072 to 1090, and the precharge circuitry of the Arithmetic Logic Unit (not shown in FIGS. 1 and 2), and the Address Arithmetic Unit (not shown in FIGS. 1 and 2). Thus, during the IA function, all input signals to the Control Unit and all control signals provided by the Control Unit are "frozen", and all arithmetic logic operation and address computations are halted. In this manner the normal operation of the processor unit is suspended.
In addition, the IAREQ signal causes the Status Generation Logic 1034 to provide an IA Acknowledge Status Code on the Status terminals 1035 to 1038 indicating the start of the IA function. At the beginning of §4 following the appearance of the IA Acknowledge Status Code, the outputs of the Status Generation Logic go to a high impedance state, and the Status Terminals 1035 to 1038 become input terminals for IA Control Codes. By using the Status terminals as both output terminals for the status codes and as input terminals for the IA Control Codes, the number of additional terminals needed for implementation of the IA function is reduced.

During the IA function, the Status terminals are sampled at the beginning of §4 of each machine cycle by IA Input Latches 1041. The contents of the IA Input Latches are decoded by an IA Control Block 1042 to provide IA control signals IAR, IAW, IAL, IASTIN, IASTB and their complements IAR, IAW and IAL. The IA Control Codes and their corresponding functions are listed in Table I.
TABLE I

IA Control Codes

<table>
<thead>
<tr>
<th>Function</th>
<th>Hex Code</th>
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<td>ADDRESS STROBE</td>
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<tr>
<td>READ</td>
<td>6,</td>
</tr>
<tr>
<td>WRITE</td>
<td>7</td>
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Each of the internal registers of the processor unit which is to be accessible during IA function is assigned an IA Address. The registers of the User Register Array which have already been assigned addresses for reference by an instruction are assigned the same addresses for the IA function. A list of the internal registers of the processor unit, their assigned IA Addresses, and their operation during the IA function is provided in Table II.

TABLE II

<table>
<thead>
<tr>
<th>INTERNAL REGISTER</th>
<th>IA ADDRESS</th>
<th>IA FUNCTION</th>
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<tbody>
<tr>
<td>QLATCH (Temp. A-BUS Regs.)</td>
<td>0x00000000</td>
<td>Read, Write</td>
</tr>
<tr>
<td>ADDRESS LATCH</td>
<td>0x00000004</td>
<td>Read</td>
</tr>
<tr>
<td>RLATCH</td>
<td>0x00000008</td>
<td>Write</td>
</tr>
<tr>
<td>PROGRAM COUNTER</td>
<td>0x0000000C</td>
<td>Write</td>
</tr>
<tr>
<td>IAEN FLIP FLOP</td>
<td>0x0000001C</td>
<td>Read, Write</td>
</tr>
<tr>
<td>TA (Temp. C-BUS Regs.)</td>
<td>0x00000020</td>
<td>Read, Write</td>
</tr>
<tr>
<td>TB</td>
<td>0x00000024</td>
<td>Read, Write</td>
</tr>
<tr>
<td>TC</td>
<td>0x00000028</td>
<td>Read</td>
</tr>
<tr>
<td>TE</td>
<td>0x0000002C</td>
<td>Write</td>
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<tr>
<td>TF</td>
<td>Ox00000030</td>
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<td>URO0</td>
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<td>UROL</td>
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<td>URO2</td>
<td>Ox00000048</td>
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<td>URO3</td>
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<td>UR10</td>
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<td>UROE</td>
<td>Ox00000074</td>
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<tr>
<td>UART</td>
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<tr>
<td>PLA00</td>
<td>Ox00000080</td>
<td>Read</td>
</tr>
<tr>
<td>PLA01</td>
<td>Ox00000084</td>
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<tr>
<td>PLA02</td>
<td>Ox00000088</td>
<td>Read</td>
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<tr>
<td>PLA03</td>
<td>Ox0000008C</td>
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<td>Read</td>
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<td>PLA08</td>
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<tr>
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<td>Ox000000A4</td>
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<tr>
<td>PLA11</td>
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<td>PLA12</td>
<td>Ox000000B0</td>
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<tr>
<td>PLA17</td>
<td>Ox000000C4</td>
<td>Read</td>
</tr>
<tr>
<td>PLA18</td>
<td>Ox000000C8</td>
<td>Read</td>
</tr>
</tbody>
</table>
After the start of the IA function a 6-bit IA Address specifying an internal register to be accessed is applied to six of the I/O terminals, and an IA Control Code specifying ADDRESS STROBE is applied to the Status terminals 1035 to 1038. The ADDRESS STROBE IA Control Code is then decoded by the IA Control Block 1042 to provide corresponding IA Control signals IASTIN, IAL and IĂL. I/O Buffer Control Multiplexers (MUX) 1043 provide appropriate IA control signals to control the I/O Buffers during the IA function. Thus, the IASTIN signal causes the I/O Buffers to strobe the IA Address at the I/O terminals, while the IAL signal causes the present IA Address in the I/O Buffers to be transferred via the A-BUS to the IA A-BUS Address Latch 1044. The contents of the IA A-BUS Address Latch are decoded by a Temporary A-BUS Register Decoder 1046. If the present IA Address selects one of the Temporary A-BUS Registers, corresponding selection signals are provided to a Temporary A-BUS Register Control Multiplexer 1051 causing an appropriate IA control signal (IAR or IAW) to be provided to the selected register. During normal operation, the Temporary A-BUS Register Control Multiplexers provide the Temporary A-BUS Register Control signals to the Temporary A-BUS Registers. If the present IA Address selects one of the Temporary C-BUS Registers, the Temporary A-BUS Register Decoder provides an IACBUS signal to BUS Control Multiplexers 1051 causing the three most significant bits of the present IA Address on the A-BUS to be transferred via the BUS Multiplexer 1028 and the C-BUS to a IA C-BUS Address Latch 1048. During the IA function the BUS Control Multiplexer provides appropriate IA control signals and the IACBUS signal to govern the operation of the BUS Multiplexer. However, during normal operation, the BUS Control Multiplexer provides the BUS Multiplexer Control signals from the Control Unit to govern the operation of the BUS Multiplexer.
The contents of the IA C-BUS Latch are decoded by a temporary C-BUS Register Decoder 1049 which provides corresponding selection signals to Temporary C-BUS Register Control Multiplexers 1052 which in turn provides an appropriate IA Control signal (IAR or IAW) to the selected register. During normal operation the Temporary C-BUS Registers Control Multiplexer provide the Temporary C-BUS Register Control signals to govern the Temporary C-BUS Registers.

The least significant four bits of the present IA Address are also provided to User Register Address Multiplexers 1050. During the IA function, the User Register Address Multiplexers provide those bits to a User Register Address Decoder 1027, but during normal operation, the User Register Address Multiplexers provide the User Register Address signals from the Instruction Buffer (not shown) to the User Register Decoder. If during the IA function the present IA Address specifies one of the User Registers, the User Register Address Decoder provides a selection signal corresponding to the selected register to the User Register Array.

During the IA function, User Register Array Control Multiplexers 1007 provide an appropriate IA control signal (IAR or IAw) to the User Register Array, but during normal operation, the User Register Array Control Multiplexer provides the User Register Control signals.

The five least significant bits of the present IA Address are also provided to an IA Control Latch Address Latch 1045, the contents of which are decoded by a Control Latch Decoder 1047. If the present IA Address selects one of the Control Latches 1072 to 1090, the Control Latch Address Decoder provides a corresponding selection signal to enable one of nineteen groups of Tri-state Inverters 1091 to 1109 associated with the selected Control Latch.

Following the application of the ADDRESS STROBE IA Control Code, a second IA Control Code specifying either
a read or a write operation is applied to the Status terminals 1035 to 1038. The second Control Code is strobed into the IA Input Latches 1041 and decoded by the IA Control Block 1042. If the second IA Control Code specifies a read operation, the IA Control Block provides the IAR signal and its complement IAR to cause the contents of the selected internal register to be transferred via the A-BUS and the I/O buffers to the I/O terminals.

If the selected register is one of the Temporary A-BUS Registers, its contents are transferred directly to the A-BUS. If the selected register is one in the User Register Array or one of the Temporary C-BUS Registers, its contents are first transferred to the C-BUS and is then transferred to the A-BUS via the BUS Multiplexer, the IAR and IACBUS signals causing data on the C-BUS to be transferred to the A-BUS. If the selected register is one of the Control Latches, its contents are first transferred through its associated group of Tri-state Inverters to a T-BUS. The data on the T-BUS is then transferred to the A-BUS through eight Tri-state Inverters 1069 which are controlled by the output of a 2-input AND gate 1070. The AND gate receives the IAR signal and the fifth bit, IASL, of the current IA Address.

If the second IA control code specifies a write operation, input data to be written into the selected internal register must be applied to the I/O terminals. The IA Control Block first provides the IASTIN signal to cause the input data on the I/O terminals to be strobed into the I/O Buffers. The IA Control Block then provides the IAW signal and its complement IAW to cause the current input data in the I/O Buffers to be transferred to the selected register.

If the selected register is one of the Temporary A-BUS Registers, the input data is transferred directly from the A-BUS to the selected register. If the selected register is in the User Register Array or is one of the Temporary C-BUS Registers, the input data is transferred to
the C-BUS via the BUS Multiplexer.

The IA function in the processor unit is terminated by the removal of the "0" IA signal. The removal of the IA signal is sampled at the beginning of $\phi 3$ and terminates the IAREQ and IAREQ signals at the beginning of the following $\phi 1$. Termination of the IAREQ and IAREQ signals disables all of the IA circuitry and restores the CK1-IA and CK1-IA clock signals to allow the processor unit to resume its normal operation. If the terminated IA function was performed in the Instruction Mode, the processing unit resumes normal operation by fetching and executing the next instruction, the State Vector Latch 1005 having been initialized to the first state of a new instruction cycle by a State Vector Initialize Circuit 1071.

If the terminated IA function was performed in the Diagnostic Mode, the State Vector Latch is not initialized and the processor unit attempts to resume normal operation from where it left off when IA function was started. However, if data which is essential to an operation being performed by the processor unit prior to the IA function is lost during the IA function, that operation cannot be successfully resumed after termination of the IA function. In that case the processor unit must be restarted. If the Program Counter is written during the IA function, it must be restored with the address of the next instruction before termination of the IA function.

Referring now to FIG. 4, there is shown a timing diagram of the principal signals related to the IA function. Shown in FIG. 4 are the external signals on the CK34, IA, STATUS, and I/O terminals of the processor unit, the internal signals BOI3DL, IAREQ, IASTIN, IAL, IAR, IAW, and the signals on the A-BUS. As discussed above, the IA function is enabled when the external IA signal makes a logic "1" to logic "0" (1-0) transition. The IA signal is sampled at the beginning of $\phi 3$, and depending upon whether the Diagnostic Mode or the Instruction Mode has been
selected, the IA function starts at the beginning of the next machine cycle after sampling or at the beginning of the second machine cycle of the next instruction cycle, respectively. FIG. 4 illustrates the IA function in the Instruction Mode. Therefore, the IAREQ signal which controls the start of the IA function makes a logic "0" to logic "1" (0-1) transition at the beginning of $\psi 1$ of the second machine cycle of the instruction cycle following the one in which the IA function is enabled. The beginning of an instruction cycle is indicated by the BOI3DL signal which makes a 1-0 transition at the beginning of $\psi 3$ of the first machine cycle of a new instruction cycle and remains at "0" for four clock phases. The logic "1" level IAREQ signal causes the IA Acknowledge Code to appear at STATUS terminals for three clock phases after which the STATUS terminals become input terminals for the IA Control Codes. The logic "1" level will hereafter be referred to as "1". The ADDRESS STROBE Control Code may be applied to the STATUS terminals at any time after a minimum waiting period of three clock phases after the termination of the IA Acknowledge Status Code but must remain valid for a minimum period of five clock phases. The ADDRESS STROBE IA Control Code is sampled at the beginning of $\psi 3$ to cause a 0-1 transition of the IASTIN signal after a delay of two clock phases and a similar transition of the IAL signal after a delay of four clock phases. The IA Address for selecting an internal register to the access may be applied to the I/O terminals at any time after the start of the IA function but must be valid no later than three clock phase after the ADDRESS STROBE Control Code is valid. The IA Address which must remain valid for at least three clock phases is strobed into the Input Buffers by the 0-1 transition of IASTIN and is thereafter transferred to the A-BUS at the beginning of $\psi 1$ following the 0-1 transition of IAL. While the IAL signal is a "1", the various IA Address Latches are enabled to receive the IA Address. The IAL signal returns to a "0" at the beginning of $\psi 4$
following the removal of the ADDRESS STROBE Control Code from the STATUS terminals, at which time the IA Address Latches are disabled. The IA Address in the various IA Address Latches specifies the internal register being accessed until a new IA Address is transferred to the IA Address Latches.

A READ Control Code may be applied to the STATUS terminals at any time after a minimum waiting period of two clock phases following the removal of the previous IA Control Code and must remain valid for at least six clock phases. Upon being sampled at the beginning of $\phi 3$, the READ IA Control Code causes the IAR signal to go to a "1" at the beginning of the next $\phi 4$. The 0-1 transition of IAR causes the data stored in the selected internal register to be transferred to the A-BUS. This data appears at the I/O terminals five clock phases after the 0-1 transition of IAR. The IAR signal returns to a "0" at the beginning of $\phi 4$ following the removal of the READ Control Code, and the output data on the I/O terminals remain valid for one clock phase thereafter.

A WRITE Control Code may be applied to the STATUS terminals at any time after a minimum waiting period of two clock phases following the removal of the previous IA Control Code and must remain valid for at least six clock phases. Upon being sampled at the beginning of $\phi 3$, the WRITE IA Control Code causes both the IASTIN and IAW signals to go to a "1" after respective delays of two and four clock phases. The input data which is to be stored in the selected internal register is applied to the I/O terminals and must be valid no later than three clock phases after the WRITE IA Control code is valid. The input data is strobed into the I/O buffers by the 0-1 transition of IASTIN and is subsequently transferred to the A-BUS at the beginning of $\phi 1$ after IAW goes to a "1". The IAW signal returns to a "0" at the beginning of $\phi 4$ following the removal of the WRITE IA Control Code, at which time the WRITE function is completed.
The IA function is terminated when the IA signal is brought to a "1". Upon being sampled at the beginning of φ3, the "1" level of IA causes IAREQ to return to a "0" at the beginning of the following φ1, at which time all IA circuitry are disabled and the processor unit returns to normal operation.

Turning now to FIG. 5, there is shown a logic diagram of a preferred embodiment of the IA Request Enable circuit 4000. The IA signal received at the IA terminal 1039 is clocked by clock signal CK34 into a first D-type flip-flop 4002 to provide a TD signal. The TD signal is clocked by clock signals CK4 and ĊK4 into a second D-type flip-flop 4003 to provide a TDO signal and its complement TD0. The TDO signal is clocked by an ACKCK signal and its complement ĀCKCK into a third D-type flip-flop 4004 which provides the IAREQ and IA REQ signals. The ACKCK and ĀCKCK signals are provided by the IA Control Block. The IAREQ signal can be forced to a "0" by a RESETH signal from the RESET circuit.

Referring now to FIG. 6, there is shown a logic diagram of a preferred embodiment of the IA Input Latches 5000 and the IA Control Block 5100. The IA Input Latches comprise four D-type latches 5001 to 5004 which are respectively coupled to the STATUS terminals 1035 to 1038. The latches are clocked by the output of a NAND gate 5005 which receives clock signal CK34 and an IASTB signal. The IASTB signal is provided by a D-type flip-flop 5016 which receives IAREQ and is clocked by signals CK4, and ĊK4. The flip-flop has an inverted reset input which also receives IAREQ.

The contents of the latches 5001 to 5004 are decoded by a circuit comprising three Inverters 5006 to 5008 and three 4-input NOR gates 5009 to 5011, respectively, providing TD2, TD3 and TD4 signals. These signals are respectively clocked into D-type flip-flops 5012 to 5014 by clock signals CK4 and ĊK4. The flip-flops 5012 to 5014 provide IAW-PP, IAR (and IAR) and IAX-PP.
signals, respectively. The IASTIN signal is provided by a NOR gate 5016 which receives clock signal CK34, the output of a S-R flip-flop 5017, and the output of a NOR gate 5015 which received IAX-PP and IAW-PP as inputs. The flip-flop 5017 has a set input coupled to the output of a NOR gate 5018, which receives IASTIN and ČK3 signals and an inverted reset input coupled to the output of an Inverter 5019, which receives the output of NOR gate 5015.

The IAW signal is provided by a NAND gate 5020 which receives IAW-PP and the output of flip-flop 5017. The IAW signal is derived from IAW signal by an Inverter 5021. Similarly, the IAL signal is derived from IAX-PP and the output of flip-flop 5017 by a NAND gate 5022, and the IAL signal is derived from IAL signal by an inverter 5023. The IAR, IAW, IAL, and IASTIN signals are all forced to "0" when IASTB goes to a "0".

The ACKCK signal is provided by a 3-1 AND-OR-Invert (AOI) gate 5024 in which one of the AND gates receives BOI3DL, IAREQ and the output of an IAEN flip-flop 5025, and the other AND gate receives clock signal ČK1. The state of the IAEN flip-flop determines whether the IA functions is performed in the Diagnostic Mode or the Instruction Mode. If the IAEN flip-flop is in the "1" state, the IA function is performed in the Instruction Mode, and ACKCK signal goes to a "1" when signals BOI3DL and ČK1 are both at "1" levels. However, if the IAEN flip-flop is in the "0" state, the IA function is performed in the Diagnostic Mode, and ACKCK goes to a "1" whenever ČK1 signal goes to a "1". The ACKCK signal is derived from ACKCK signal by an Inverter 5026.

The IAEN flip-flop has a set input coupled to the output of NOR gate 5027 which receives TDO, ČK1 and RESET signal. The IAEN signal is forced to a "1" when all three signals received by the NOR gate 5027 are at "0" levels. Ordinarily, the IAEN flip-flop is set by applying a "1" signal on the RESET terminal of the processor unit for at least two machine cycles while a "1" signal is applied to
the IA terminal.

The IAEN flip-flop has a reset input coupled to the output of a NAND gate 5028 which receives TDO, CK1 and RESETH signals. The IAEN signal is forced to a "0" when all three signals received by the NAND gate 5028 are at "1" levels. Ordinarily, the IAEN flip-flop is reset by applying a "1" signal to the RESET terminal for a minimum duration of two machine cycles while a "0" signal is being applied to the IA terminal.

The IAEN flip-flop has been assigned an address and may be read or written during the IA function as one of the internal registers of the processor unit. When the IA Address assigned to the IAEN flip-flop is decoded by the Temporary A-BUS Register Decoder, a "1" level IAENSELH selection signal is provided to enable NAND gates 5029 and 5030. Thereafter, if an READ IA Control Code is applied to the STATUS terminals, a "1" level IAEN signal is provided to the NAND gate 5030 causing the output of this IAEN flip-flop to be transferred through a Tri-state Inverter 5031 to the least significant conductor A-BUS00 of the A-BUS. If the WRITE IA Control Code is applied after the IAEN flip-flop is selected, a "1" level IAEN signal is provided to the NAND gate 5029 causing the data on the A-BUS00 conductor of the A-BUS to be clocked into the IAEN flip-flop.

Referring now to FIG. 7 there is shown a logic diagram of a preferred embodiment of the Timing Generator 6000. The Timing Generator receives external clock signals CK34 and CK23 at respective terminals 1030 and 1031 and through respective Input Buffers 6001 and 6002 and provides CK34, CK23, CK1 to CK4 signals and their complements CK34, CK23, CK1 to CK4. The CK34 and CK23 signals are derived from the outputs of the input buffers by Inverters 6003 and 6004, respectively. The CK1 to CK4 are derived from CK34, CK23 and their complements by NAND gates 6007 to 6010, respectively. The complements CK1 and CK4 are provided by Inverters 6011 to 6014, respectively.
The Timing Generator also provides the CKI-IA signal and its complement CKI-IA. During normal operation signals CKI-IA and CKI-IA are respectively the same as CKI and CKI signals, but during the IA function CKI-IA and CKI-IA signals are forced to a "0" and a "1", respectively. The CKI-IA signal is provided by a NAND gate 6015 which receives CK34, CK23 signals and the output of a 2-1 OR-AND-Invert (OAI) gate 6017 in which one of the OR gates receives a BOI3D signal (the complement of BOI3DL) and IAREQ signal and the other OR gate receives TDO. During normal operation when TDO is a "0", the OAI gate provides a "1" signal to enable the NAND gate 6015. However, during the IA function when TDO is a "1", the OAI gate provides a "0" signal to disable the NAND gate 6015 when either BOI3D or IAREQ signal is a "1". Thus, the output of the NAND gate 6015 is forced to a "1" and the output of the Inverter 6016 is forced to a "0".

Turning now to FIG. 8, there is shown a logic diagram of a preferred embodiment of the RESET circuit 7000 which receives an externally applied RESET signal at terminal 1033 and provides a RESETH signal and its complement RESETL. The RESET signal is clocked into a D-type latch 7001 by clock signal CK34. The output of the latch is provided to the input of a Tri-state Inverter 7002 controlled by signals CK3 and CK3. The Tri-state Inverter, which is used as a dynamic latch, is enabled when CK3 is a "1" to provide its output to the input of a D-type flip-flop 7003. The D-type flip-flop, which is clocked by signals CK4 and CK4, provides the RESTL and RESETH signals.

Referring now to FIG. 9, there is shown a logic diagram of a preferred embodiment of the IA A-BUS Address Latch 8000 and the Temporary A-BUS Register Decoder 8100. The IA A-BUS Address Latch comprises six D-type flip-flops 8001 to 8006 each receiving data from one of the A-BUS conductors A-BUS02 to BUS07. The flip-flops are all clocked by the IAL and IAL signals. The Temporary A-BUS Register Decoder, which comprises NOR gates 8007 to 8011
and NAND gates 8012 to 8015, receives the normal and inverted output signals from the IA A-BUS Address Latch and provides selection signals IAPC, IARL, IAAL, IAQL and IAENSELH corresponding to the Program Counter, the R-Latch, the Address Latch, the Q-Latch and the IAEN flip-flop, respectively. In addition, the IA A-BUS Register Decoder also provides the TREG signal for enabling the Temporary C-BUS Register Decoder, the IACBUS signal for controlling the transfer of an IA Address from the A-BUS to the C-BUS, and the USREG signal for enabling the USER Register Control Multiplexer.

Referring now to FIG. 10, there is shown a logic diagram of the R-Latch 9000 and of a preferred embodiment of the Control Multiplexer 9100 associated with the R-Latch. The R-Latch is a 32-bit D-type register which is clocked by a RCLK signal and its complement RCLK. During normal operation, the R-Latch receives data from the User Register Array through Tri-state Inverters 9001 and provides data to the AAU. The Tri-state Inverters 9001 are controlled by a RIN signal and its complement RIN. During the IA function, the R-Latch may be written with data from the A-BUS received through Tri-state Inverters 9002 which are controlled by an ALIN signal and its complement ALIN. The Control Multiplexers associated with the R-Latch comprise a 4-3 AOI gate 9003 which provides the RCLK signal, a 2-2 AOI gate 9004 which provides the ALIN (RIN) signal, and Inverters 9005, 9006 and 9007 which provide the RCLK, ALIN and RIN signals, respectively. One of the AND gates of the AOI gate 9003 receives IARL, IAW, CK3, and IAREQ signals while the other AND gate receives IAREQ, CK3 signals and a write control signal RCK provided by the Control Unit. During normal operation, when IAREQ signal is a "0" and IAREQ signal is a "1", RCLK signals goes to a "1" to clock the R-Latch when CK3 and RCK signals are both at "1" levels. However, during the IA function, when IAREQ signal is a "1" and IAREQ signal is a "0", RCLK goes to a "1" when CK3, IARL, and IAW signals are all at "1"
levels. One of the AND gates of the 2-2 AOI gate 9004 receives IAREQ signal and a selection signal RL provided by the Control Unit while the other AND gate receives IAREQ and IARL signals. During normal operation, ALIN and RIN signals both follow RL. However, during the IA function, ALIN and RIN signals both follow IARL signal.

Referring now to FIG. 11 there is shown a logic diagram of the Q-Latch 10000 and of a preferred embodiment of the Control Multiplexers 10100 associated with the Q-Latch. The Q-Latch is clocked by a QCLK signal and its complement QCLK. During normal operation, the Q-Latch receives data from the Instruction Buffer through Tri-state Inverters 10001 and provides data directly to the AAÜ. The Tri-state Inverters 10001 are controlled by a QIN signal and its complement QIN. During the IA function, the Q-Latch may receive data from the A-BUS through Tri-state Inverters 10002 and may provide data to the A-BUS through Tri-state Inverters 10003. The Tri-state Inverters 10002 are controlled by a AQLIN signal and its complement AQLIN, and the Tri-state Inverters 10003 are controlled by a QUOT signal and its complement QUOT.

The Control Multiplexers associated with the Q-Latch include a 3-2 AOI gate 10009 providing a QUOT signal, a 3-3 AOI gate 10004 providing a QCLK signal, and a 3-input NAND gate 1005 providing a AQLIN signal. Also included are Inverters 10006, 10007, and 10008 providing QUOT, QCLK, and AQLIN signals, respectively. The AOI gate 10009 has one AND gate receiving IAR, IAQL and IAREQ signals and the other AND gate receiving a QL read control signal from the Control Unit and IAREQ signal. During normal operation the Tri-state inverters 10003 are enabled to transfer data to the A-BUS by a "1" level QOUT signal when the QL signal goes to a "1". During the IA function QOUT signal goes to a "1" when IAQL and IAR signals are both at the "1" level.

The AOI gate 10004 has one AND gate receiving IAW, IAQL and IAREQ signals and the other AND gate receiving a IQCK write control signal from the Control
Unit, CK4 and IAREQ signals. During normal operation the data is clocked into the Q-Latch by a "1" QCLK signal when IQCLK and CK4 signals are both at "1" levels. During the IA function, the QCLK signal goes to a "1" when IAW and IAQL signals are both at "1" levels.

The NAND gate 10005 receives IAREQ, IAW, and IAQL signals. During normal operation, the NAND gate provides a "0" level AQLIN signal to disable the Tri-state Inverters 10002, but during the IA function, the NAND gate provides a "1" level AQLIN signal to enable the Tri-state Inverters 10002 when IAW and IAQL signals are both at "1" levels.

Turning now to FIG. 12, there is shown a logic diagram of the Address Latch 11000 and a preferred embodiment of its associated Control Multiplexers 11100. During normal operation, the Address Latch receives data from the AAU and provides data to the A-BUS through Tri-state Inverters 11001 controlled by an AOUT signal and its complement ALOG. During the IA function, the Address Latch may provide data to the A-BUS through Tri-state inverters 11001. Data is clocked into the Address Latch by an ACLK signal and its complement ACLK.

The Control Multiplexers associated with the Address Latch comprise a 3-2 AOI gate 11002 providing the AOUT signal and an Inverter 11003 providing the AOUT signal. The AOI gate 11002 has one AND gate receiving IAREQ, IAAL, and IAR signals and the other AND gate receiving an AL write control signal provided by the Control Unit and IAREQ signal. During normal operation, AOUT signal goes to a "1" to enable the Tri-state Inverter 11001 when AL goes to a "1". During the IA function, AOUT signal goes to a "1" when IAAL and IAR signals are both at "1" levels.

Referring now to FIG. 13, there is shown a logic diagram of a preferred embodiment of the User Register Address Multiplexer 12000. The multiplexer comprises four pairs of Tri-state Inverters 12001 to 12004.
Each pair has one Tri-state Inverter receiving a respective bit of a User Register Address M0 to M3 from the Instruction Buffer the other Tri-state Inverter receiving a respective one of the least significant four bits of the current IA Address from the IA A-SUS Address Latch. The outputs of the Tri-state Inverters in each pair are both coupled to the input of a respective one of four D-type flip-flops 12009 to 12012. The Tri-state Inverters in each pair are controlled by signals IAREQ and IAREQ in a manner such that during normal operation, the Inverter receiving the IA Address bit is disabled and the one receiving the User Register Address bit is enabled to provide its output to the respective flip-flop. But during the IA function, the Inverter receiving the User Register Address bit is disabled and the one receiving the IA Address bit is enabled to provide its output to the respective flip-flop.

Referring now to FIG. 14 there is shown a logic diagram of a preferred embodiment of the User Register Decoder 13000. The Decoder comprises Inverters 13001 to 13004, 4-input NOR gates 13005 to 13019, Tri-state Inverters 13020 to 13034, and 2-input NAND gates 13035 to 13049. The Inverters respectively receive address bits A0 to A3 and provide the complements of the address bits. The NOR gates each receive different combinations of the address bits and their complements. The Tri-state Inverters, which are used as dynamic latches, receive the outputs of respective NOR gates and are controlled by CK1 and CK1 signals, the Inverters being enabled when signal CK1 is a "1". The NAND gates each receive the output of a respective Tri-state Inverter and signal CK23, the NAND gates providing the register select signals RS00 to RS14.

Turning now to FIG. 15, there is shown the User Register Array 14000 which includes an array of memory cells 14001 having fifteen rows and thirty-two columns.

Each row of memory cells has an associated word line coupled to all cells in that row. The wordlines of the array are coupled to receive respective register select
signals RS00 to RS14 from the User Register Decoder. Each row of the array serves as a register, and is selected when a "1" level register select signal is applied to its associated wordline. Data stored in the memory cells of a selected row and the complement of that data are provided at the BL and BL bitlines, respectively. The data in the memory cells of the selected row may be overwritten with new data received at the BL and BL bitlines. Timing signals for the array are derived from CK23 and CK34 signals by a NOR gate 14002 and an inverter 14003. The array may be read during $\phi_2$ to $\phi_4$ and may be written during $\phi_2$ and $\phi_3$. Data from the array is provided to the C-BUS through Tri-state Inverters 14004 which are controlled by an R signal and its complement $\bar{R}$, the Tri-state inverters being enabled when R is a "1". Data from the array is also provided directly to the R-Latch. The array receives data to be written into a selected row from the C-BUS through Inverters 14005 and 14006 and Transmission Gates 14007 and 14008, the latter being controlled by a W signal and its complement $\bar{W}$. The Transmission Gates go to their conducting states when signal $W$ is a "1".

Referring now to FIG. 16, there is shown a preferred embodiment of the User Register Control Multiplexers 15000. The Multiplexers include a read control section having a first pair of Tri-state Inverters 15001 and 15002 controlled by signals IAREQ and IARQ and having their outputs tied in common to provide the R signal. One of the pair 15001 receives the output of a NOR gate 15003 which receives signals IAR and $\bar{US}REG$ while the other of the pair 15002 receives a SRCREG read control signal provided by the Control Unit. During normal operation, the Inverter 15001 is disabled while Inverter 15002 is enabled, and R goes to a "1" when signal SRCREG goes to a "0". However, during the IA function, Inverter 15001 is enabled while Tri-state inverter 15002 is disabled, and R goes to a "1" when signals IAR and $\bar{US}REG$ both at "0" levels. The $\bar{R}$ signal is derived from the R
signal by an Inverter 15004.

The Multiplexers also include a write control section having a second pair of Tri-state Inverters 15005 and 15006 controlled by signals IA_REQ and IA_REQ and having their outputs tied in common, the common output being received together with signal CK23 by a NOR gate 15008 which provides the \( \bar{W} \) signal. The \( \bar{W} \) signal is derived from the \( \bar{W} \) signal by an inverter 15009. One of the pair of Tri-state Inverters 15005 receives the output of a NOR gate 15007 while the other of the pair 15006 receives a REGD write control signal provided by the Control Unit. The NOR gate 15007 receives IA_W and US_REQ signals. During normal operation, Inverter 15006 is enabled while Inverter 15005 is disabled, and \( W \) goes to a "1" when signals REGD and CK23 are both at "0" levels. However, during the IA function, Inverter 15005 is enabled while Inverter 15006 is disabled, and \( W \) goes to a "1" signal when IA_W, US_REQ and CK23 signals are all at "0" levels.

Referring now to FIG. 17, there is shown a logic diagram of preferred embodiments of the IA Control Latch Address Latch 16000 and the Control Latch Decoder 16100. The Control Latch Address Latch includes five D-type flip-flops 16001 to 16005, each one receiving data from a respective one of five conductors ABUS02 to ABUS06 of the A-BUS. The data is clocked into each flip-flop by signals IAL and IAL. The outputs PA0H to PA4H and the inverted outputs PA0L to PA4L of the flip-flops are provided to the Control Latch Decoder which comprises sixteen 2-input NAND gates 16006 to 16021 and nineteen 2-input NOR gates 16022 to 16040. The Decoder provides nineteen control latch selection signals PLA00 to PLA18.

Referring now to FIG. 18, there is shown a logic diagram of the BUS Multiplexer 17000 and a preferred embodiment of the BUS Control Multiplexers 17100. The Bus Multiplexers include Inverters 17001 and Tri-state Inverters 17002 for transferring data from the C-BUS to the A-BUS. The Tri-state Inverters 17002 are all controlled by
a CTOAH signal and its complement CTOAL and are enabled when signal CTOAH goes to a "1". The BUS Multiplexer also includes Inverters 17003 and Tri-state inverters 17004 for transferring data from the A-BUS to the C-BUS. The Tri-state Inverters 17004 are controlled by an ATOCH signal and its complement ATOCL and are enabled when ATOCH signal goes to a "1".

The BUS Control Multiplexers include a 3-2 AOI gate 17005 in which one AND gate receives IAR, IACBUS, and IAREQ signals and the other AND gate receives a CBUSS control signal provided by the Control Unit and signal $\overline{IAREQ}$. The AOI gate 17005 provides the CTOAL signal from which is derived the CTOAH signal through an inverter 17006. During normal operation, CTOAH signal goes to a "1" when CBUSS signal goes to a "1". However, during the IA function, CTOAH signal goes to a "1" only when both IAR and IACBUS signals are at "1" levels. The BUS Control Multiplexer also includes a 2-2-2 AOI gate 17007 in which a first AND gate receives IAREQ signal and the output of a NOR gate 17008, a second AND gate receives IAREQ and the inverted IACBUS signal provided by an inverter 17009, and a third AND gate receiving an $\overline{AC}$ control signal provided by the Control Unit and signal $\overline{IAREQ}$. The NOR gate 17008 receives IAW and IAL signals. The AOI gate 17007 provides the ATOCH signal from which is derived the ATOCL signal by an inverter 17009. During normal operation, ATOCH signal goes to a "1" when signal $\overline{AC}$ goes to a "0". However, during the IA function, ATOCH signal goes to a "1" when signal IACBUS and either of IAW and IAL signals are at a "1" level.

Referring now to FIG. 19, there is shown a logic diagram of a preferred embodiment of the IA C-BUS Latch 18000 and the Temporary C-BUS Register Decoder 18100. The IA C-BUS Latch comprises three D-type flip-flops 18001 to 18003 which receive data from respective conductors C-BUS02 to C-BUS04 of the C-BUS. The flip-flops are clocked by signals IAL and $\overline{IAL}$. The outputs ICBOH to ICBO2L and the
inverted outputs ICB0H to ICB2H of the flip-flops are provided to the Temporary C-BUS Register Decoder which comprises five 4-input NOR gates 18004 to 18008. The NOR gates 18004 to 18008, respectively, provide IATA, IATB, IATC, IATE, and IATF selection signals corresponding to the TA, TB, TC, TE, and TF Temporary C-BUS Registers, respectively. Each of the NOR gates 18004 to 18008 receives a different combination of the outputs and inverted outputs of the flip-flops and the TREQ signal.

Turning now to FIG. 20, there is shown a logic diagram of a representative Temporary C-BUS Register (TA) 19000 and a preferred embodiment of its associated Control Multiplexers 19100. The TA register receives data from the C-BUS, provides data directly to the ALU and provides data to the C-BUS through a Tri-state Inverter 19001 controlled by a TAOUTH signal and its complement TAOUTL. The Tri-state Inverter is enabled when TAOUTH signal goes to a "1". Data is clocked into TA by a TACKLH signal and its complement TACLKL.

The Associated Control Multiplexers include a 3-4 AOI gate in which one AND gate receives IAREQ, CK23 and a LTAH write control signal provided by the Control Unit and the other AND gate receives CK23, IAW, IATA, and IAREQ signals. The AOI gate 19002 provides the TACLKL signal from which the TACLKH signal is derived by an Inverter 19003. During normal operation, the TACLKH signal goes to a "1" whenever LTAH and CK23 signals are both at "1" levels. However, during the IA function, TACLKH signal goes to a "1" only when IAW, IATA, and CK23 signals are all at "1" levels. The Associated Control Multiplexers further include a 2-3 AOI gate 19004 in which one AND gate receives IAREQ and a LTAOUTH read control signal provided by the Control Unit and the other AND gate receives IATA, IAR, and IAREQ signals. The AOI gate 19004 provides the TAOUTL signal from which the TAOUTH signal is derived by an Inverter 19005. During normal operation, the TAOUTH signal goes to a "1" whenever LTAOUTH signal goes to a "1".
However, during the IA function, TAUTH signal goes to a "1" when IAR and IATA signals are both at "1" levels.

Referring now to FIG. 21, the I/O Buffer 20000 includes an input latch comprising thirty-two D-type flip-flops 20001 coupled to receive data from the I/O terminals 1001, the data being clocked into the flip-flops by a STIN signal and its complement STIÅN. The contents of the input latch are transferred to the A-BUS through Tri-state Inverters 20002 controlled by a SIN signal and its complement SIÅN, the Tri-state inverters being enabled when SIN is a "1". The I/O Buffer also includes an output latch comprising thirty-two D-type flip-flops 20003 coupled to receive data from the A-BUS, the data being clocked into the flip-flops by a LM signal and its complement LÅM. The contents of the output latch are transferred to the I/O terminals through Tri-state Inverters 20004 controlled by a ST0 signal and its complement ST0, the Tri-state inverters 20004 being enabled when the ST0 signal is a "1".

Turning now to FIG. 22, there is shown a logic diagram of a preferred embodiment of the I/O Buffer Control Multiplexers 21000, 21100, 21200, and a circuit for providing the STQ and STÅQ signals 21300. The Multiplexer 21000 includes a 2-1-2 AOI gate 21001 in which a first AND gate receives IASTIN and IAREQ signals, a second AND gate receives a WAITH signal derived from an externally provided WAIT signal, and a third AND gate receives a STIL control signal provided by the Control Unit and IÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅÅå


and its complement WAITL are derived from an externally applied WAIT signal in the same manner as the RESETH and RESETL signals are derived from the externally provided RESET signal.

The Multiplexer 21100 includes a 2-2 AOI gate 21004 in which one AND gate receives IAREQ signal and the output of a NOR gate 21012 and the other AND gate receives an İRABÜS control signal provided the Control Unit and İAŘEQ signal. The NOR gate 21012 receives IAL and IAW.

The output of the AOI gate 21004 is received by a Tri-state Inverter 21005 which provides the SIN signal. The Tri-state Inverter 21005, which is used as a dynamic latch, is controlled by CK1 and ĆKI signals and is enabled when CK1 signal goes to a "1". The SIN signal is derived from SIN signal by an Inverter 21006. During normal operation, the SIN signal goes to a "1" when İR_ABÜS signal is a "1". However, during the IA function, SIN signal goes to a "1" when either IAW or IAL signal is a "1".

The Multiplexer 21200 comprises a 2-2-2 AOI gates 21007 in which a first AND gate receives an OR control signal provided by the Control Unit and İAŘEQ signal, a second AND gate receives a DMAWT signal provided by the Control Unit and İAŘEQ signal, and the remaining AND gate receives İAŘ and IAREQ Signals. The output of the AOI gate 21007 is provided to a NAND gate 21010 through an Inverter 21008 and a Tri-state Inverter 21009. The NAND gate which also receives CK3 signal provides the LM signal. The Tri-state Inverter 21009, which is used as a dynamic latch, is controlled by the CKL and ĆKLI signals and is enabled when CK1 signal goes to a "1". The LM signal is derived from the LM signal by an Inverter 21011. During normal operation, the LM signal goes to a "1" whenever OR and DMAWT signals are both at "0" levels and CK3 signal is a "1". But during the IA function, the LM signal goes to a "1" whenever İAŘ signal is a "0" and CK3 signal is a "1".

The circuit for providing the STO and ĂTO signals includes a Wait State Generation Logic circuit 21012 which
receives the WAITH and WAITL signals and provides an STP
signal to a Tri-state Inverter 21013 controlled by signals
CK1 and ČŘI. The Tri-state Inverter 21013, which is used
as a dynamic latch, is enabled when CK1 signal goes to a
"1". The circuit further includes a NOR gate 21014 which
receives CK23 signal and the complement of STIL provided by
an Inverter 21015. The outputs of the NOR gate 21014 and
of the Tri-state Inverter 21013 are received by another NOR
gate 21016 which provides the STO signal. The STO signal
is derived from the STO signal by an Inverter 21017. When
the processor unit is in a wait state, the Wait State
Generation Logic circuit provides a "0" which forces the
STO signal to a "0". Otherwise, the STO signal goes to a
"1" whenever STIL is a "0" or whenever CK23 signal is a
"1".

Referring now to FIG. 23 there is shown a logic
diagram of the least significant five bits of the State
Vector Latch 22000 and a preferred embodiment of the State
Vector Initialization circuit 22100. The portion of the
State Vector Latch shown comprises five D-type flip-
flops 22001 to 22004 and 22007 which receive respective
feedback signals (next state signals) NXTSTO to NXTST4 from
the Control Unit and provide state vector input signals
STATE 0 to STATE 4 to the Control Unit. The feedback
signals are clocked into the flip-flops by CK1-IA and ČŘI-
ĪA.

The State Vector Initialization Circuit includes
a first D-type flip-flop 22005 receiving a XFERPCS control
signal and being clocked by CK1 and ČŘI signals. The first
flip-flop provides a BOI signal to a second D-type flip-
flop 22006 which is clocked by CK3 and ČŘ3 signals and
which provides an output BOI3D signal to a NAND gate 22007.
The NAND gate which also receives TDO and CK1 signals
provides its output to the inverted reset inputs of flip-
flops 22002 to 22004 and 22007 and to the set input of
flip-flop 22001 through an Inverter 22008. The flip-
flop 22006 also provides the BOI3DL signal. When the
IA function in the Instruction Mode is enabled, the TDO signal goes to a "1" but the processor unit continues normal operation until after the end of the instruction cycle in which the IA function is enabled. During the last machine cycle of that instruction cycle, the XFERPCS signal goes to a "1" causing the Program Counter to transfer the state of its master section to its slave section in preparation for an instruction fetch. When the "1" level XFERPCS signal is clocked into flip-flop 22005 by CK1 signal, the BOI signal goes to a "1" signaling the beginning of a new instruction cycle. When the "1" level BOI signal is clocked into flip-flop 22006 by CK3 signal, a "1" level BOI3D signal and a "0" level BOI3DL signal are provided to start the IA function. Thereafter, when CK1 signal goes to "1" at the beginning of the second machine cycle of the new instruction cycle, the NAND gate 22007 provides a "0" level signal to initialize the least significant five bits of the state vector to the 000001 state.

Turning now to FIG. 24, there is shown a logic diagram of a preferred embodiment of the Status Generation Logic circuit 23000. The circuit includes a status word latch comprising D-type flip-flops 23001 to 23004 which are clocked by signals CK1 and CK1. The contents of the status latch are provided to the STATUS terminals through Tri-state Inverters 23005 to 23008 controlled by IASTB and IA3STB signals. The Tri-state Inverters 23005 to 23008 are enabled when IASTB signal is a "0" but are disabled when IASTB is a "1". The circuit also includes Tri-state Inverters T1, T2, T3, and T4 which receive the outputs of Inverters 23009 to 23011 and the output of a NOR gate 23012, respectively. The Inverters 23009 to 23011, respectively, receive status signals STAT0, STAT1 and STAT2 provided by the Control Unit and the NOR gate 23012 receives signals STAT1, STAT2 and the complement of STAT0 signal provided by the Inverters 23009. The Tri-state Inverters T1, T2, T3, and T4 are controlled by IAREQ and
signals to be enabled when IAREQ signal is a "0" and
disabled when IAREQ signal is a "1". The outputs of T1,
T2, T3, and T4 are coupled to the inputs of respective
flip-flops of the status word latch. In addition, the
circuit includes Tri-state Inverters T5, T6, T7, and T8
having outputs coupled to the inputs of respective flip-
flops of the status word latch and being controlled by
IAREQ and IAREQ signals to be enabled when IAREQ signal is
a "1" and disabled when IAREQ signal is a "0". The inputs
of T5, T6, and T8 are allowed to float "1" levels while the
input of T7 receives IAREQ signal. During normal operation
when IAREQ signal is a "0", T5, T6, T7, and T8 are disabled
while T1, T2, T3, and T4 are enabled to provide a status
code derived from STAT0, STAT1, and STAT2 signals to the
status word latch. At the start of the IA function when
IAREQ signal goes to a "1", T1, T2, T3, and T4 are disabled
while T5, T6, T7, and T8 are enabled to provide a 0010 IA
acknowledge status code to the inputs of the status word
latch. The code is clocked into the status word latch and
transferred to the STATUS terminals when CK1 signal goes to
a "1". Thereafter, the Tri-state Inverters 23005 to 23008
are disabled when the IASTB signal goes a "1".

While the invention has been described with
reference to a presently preferred embodiment thereof, it
will be understood by those skilled in the art that
modifications and variations may be made to the described
embodiment without departing from the spirit and scope of
the present invention. For example, the latches for
storing the current IA Address, the decoders for the
current IA Address and the Control Multiplexers for the
various internal registers may be partitioned differently
to suit different bus structure and register arrangements.
In some instances it may be desirable to provide access to
only a subset of the internal registers of the processor
unit. Also, the type of access (i.e., read only, write
only, read and write) for individual internal registers may
be varied to suit different requirements. Furthermore,
other logic implementations may be used for the IA circuitry. In particular, many parts of the IA circuitry such as the IA Control Block, the various Control Multiplexers and the various Register Decoders may be implemented with one or more programmable-logic-arrays (PLAs). Moreover, where PLAs are used in the Control Unit of the microprocessor, it may be desirable to locate a PLA of the IA circuitry adjacent to and contiguous with a PLA of the Control Unit.
Claims

1. A processor for executing a program of instructions, the processor comprising:
   input/output terminals (1001) for receiving instructions for normal operation of the processor;
   input/output buffers for forwarding the instructions, for normal operations of the processor;
   a plurality of internal registers for storing data for normal operations of the processors;
   status terminals (1035-1038) for delivering output status information from the processor;
   a control circuit responsive to a present instruction for the normal operation, for providing normal control signals governing the execution of a normal processor operation specified by the present instruction, including register control signals governing the reading and/or writing of the internal registers;

   CHARACTERIZED IN THAT the processor further comprises:
   a first circuit (1039, 1040) for receiving a test command signal from an external source and for generating a test enable signal (IAREQ) to enable the processor to execute a test operation;
   a timing generator (1029) responsive to the test enable signal for suspending the execution of the normal operations;
   the input/output buffers (1023) for receiving and forwarding test addresses of a specified internal register during the test operation;
   a second circuit comprising:
   a decoder (1046) responsive to the present test address for providing during test operation a selection signal corresponding to the specified internal register, the status terminals (1035-1038) being connected for receiving test control codes; and
   a control block (1042) responsive to the test control codes for generating test control signals (IAR,
IAW);

third circuitry (1051) connected for receiving
the register control signals during normal operation and
the test control signals (IAR, IAW) during test operation
and responsive both to the selection signal and to the test
enable signal (IAREQ) for providing appropriate ones of the
test control signals (IAR, IAW) to the specified internal
register during test operation and for providing the
register control signals to the specified internal register
during normal operation;

whereby during test operation the input/output
buffer (1023) receives data from the input/output terminals
(1001), which data are to be stored in the specified
internal register when writing is specified by the present
test control code, but delivers data to the input/output
terminals (1001) from the specified internal register when
reading is specified by the present test control code.

2. A processor in accordance with claim 1
the processor further comprises:
clock circuitry for providing a plurality of
clock signals including a first clock signal,
CHARACTERIZED IN THAT
the timing generator (1029) includes apparatus
responsive to the test enable signal (IAREQ) for holding
the first clock signal at a fixed level.

3. A processor in accordance with claim 2
wherein the instructions are executed one at a time in a
series of instruction cycles
CHARACTERIZED IN THAT
the first circuit (1039, 1040) comprises:
apparatus for detecting the test command signal
at regular intervals during each instruction cycle; and
a bistable circuit having a first and a second
state,
the test enable signal (IAREQ, IÄREQ) being
provided after a fixed delay following the detection of the
test command signal if the bistable circuit is in the first
state but the test enable signal being provided during a fixed interval in the instruction cycle following the one in which the test command signal is detected if the bistable circuit is in the second state.

4. A processor in accordance with claim 3 wherein the means for storing the control signals comprise one or more control latches

CHARACTERIZED IN THAT
the internal registers which are assigned test addresses comprise:
the control latches;
registers which are directly accessible by instructions; and:
registers which are not directly accessible by instructions.

5. A processor in accordance with claim 4 CHARACTERIZED IN THAT the bistable circuit comprises:
a flip-flop and the internal registers which are assigned test addresses include the flip-flop.

6. A processor in accordance with claim 5 comprising:
a first bus (A-Bus), a second bus (C-Bus), bus multiplexor (1028) responsive to appropriate control signals for controllably transferring data between the first and second busses;
the control circuit provides bus control signals for governing the transfer of data between the first and second busses,

a first group of the internal registers being coupled to receive data from and/or to provide data to the first bus; and

a second group of the internal registers being coupled to receive data from and/or to provide data to the second bus,

CHARACTERIZED IN THAT
the second bus (C-Bus) is coupled to input/output
terminal (1001) receiving test addresses, for receiving
data and for providing data,
the input/output buffer responsive to a test
address identifying s specified one of the internal
registers of the first group for providing a group
selection signal; and
bus control multiplexor (1051) receiving the
bus control signals and responsive to (1) the test enable
signal, (2) the group selection signal and (3) the test
control signals for providing appropriate control signals
derived from the test control signals to the bus
multiplexor (1028), the bus control multiplexor (1051)
otherwise for providing the bus control signals to the bus
multiplexor (1028).

7. A processor in accordance with claim 6
comprising:
a third bus

CHARACTERIZED IN THAT
the control latches are coupled to provide the
control signals stored therein to the third bus; and

circuitry responsive to a test address specifying
one of the control latches and an appropriate test control
signal governing the reading of the specified internal
register for transferring the control signals on the third
bus to the second bus.

8. A processor in accordance with claim 7 the
input/output terminal (1001) includes bidirectional
input/output buffers being responsive to appropriate
control signals for transferring data and test addresses
between the input/output terminals (1001) and the second
bus, and the control circuit (1006) providing buffer
control signals governing the operation of the input/output
buffers (1023),

CHARACTERIZED IN THAT
a input/output buffer control multiplexor (1043)
receiving the buffer control signals and responsive to the
test enable signal and the test control signals for providing appropriate control signals derived from the test control signals to the input/output buffers, the input/output buffer control multiplexor (1043) otherwise providing the buffer control signals to the input/output buffers.
MICROPROCESSOR ARCHITECTURE HAVING INTERNAL ACCESS MEANS

Abstract of the Disclosure

A processor architecture is disclosed which permits the registers (1024,1026) and control latches (1072-1090) of the processor to be easily accessed without using instructions to achieve such access. The architecture provides for an internal access (IA) function which is enabled by applying an IA Request signal to an IA terminal (1039) of the processor. During the IA function, normal program execution in the processor is suspended and the registers (1024,1026) and control latches (1072-1090) may be accessed as if they were storage locations in a random-access memory. After the IA function is enabled, the address of a register or control latch selected for access is applied to the Address/Data port (1001) of the processor, and an IA Control Code specifying the strobing of the Address/Data port is applied to the Status terminals (1035-1038) of the processor. After strobing of the address, a second IA Control Code specifying either reading or writing of the selected register or control latch is applied to the Status terminals (1035-1038). If the second Control Code specifies reading, the contents of the selected register (1024,1026) or control latch (1072-1090) is provided at the Address/Data port (1001). If the second Control Code specifies writing, data received at the Address/Data port (1001) is stored in the selected register.

FIG. 1
### I. Classification of Subject Matter

According to International Patent Classification (IPC) or to both National Classification and IPC

- **Int. Cl.** G06F 11/28
- **U.S. Cl.** 364/200; 371/16

### II. Fields Searched

Minimum Documentation Searched

<table>
<thead>
<tr>
<th>Classification System</th>
<th>Classification Symbols</th>
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</thead>
<tbody>
<tr>
<td>U.S.</td>
<td>364/200 MS File, 371/16, 371/20</td>
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Documentation Searched other than Minimum Documentation to the extent that such Documents are Included in the Fields Searched

### III. Documents Considered to be Relevant

<table>
<thead>
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<th>Category</th>
<th>Citation of Document, with indication, where appropriate, of the relevant passages</th>
<th>Relevant to Claim No.</th>
</tr>
</thead>
<tbody>
<tr>
<td>X</td>
<td>US, A, 4,128,873, (LAMIAUX) 05 December 1978</td>
<td>1-8</td>
</tr>
<tr>
<td>A</td>
<td>US, A, 4,074,851, (EICHELBERGER ET AL.) 21 February 1978</td>
<td>1-8</td>
</tr>
<tr>
<td>A</td>
<td>US, A, 3,898,621, (ZELINSKI ET AL.) 5 August 1975</td>
<td>1-8</td>
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### IV. Certification

- **Date of the Actual Completion of the International Search:** 27 October 1982
- **Date of Mailing of this International Search Report:** 05 Nov 1982
- **International Searching Authority:** ISA/US

Gareth D. Shaw
### V. OBSERVATIONS WHERE CERTAIN CLAIMS WERE FOUND UNSEARCHABLE

This international search report has not been established in respect of certain claims under Article 17(2) (a) for the following reasons:

1. Claim numbers __________, because they relate to subject matter not required to be searched by this Authority, namely:

2. Claim numbers __________, because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out, specifically:

### VI. OBSERVATIONS WHERE UNITY OF INVENTION IS LACKING

This International Searching Authority found multiple inventions in this international application as follows:

1. As all required additional search fees were timely paid by the applicant, this international search report covers all searchable claims of the international application.

2. As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims of the international application for which fees were paid, specifically claims:

3. No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claim numbers:

4. As all searchable claims could be searched without effort justifying an additional fee, the International Searching Authority did not invite payment of any additional fee.

#### Remark on Protest

- The additional search fees were accompanied by applicant's protest.
- No protest accompanied the payment of additional search fees.