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(54) **DUAL REGULATOR SYSTEMS**

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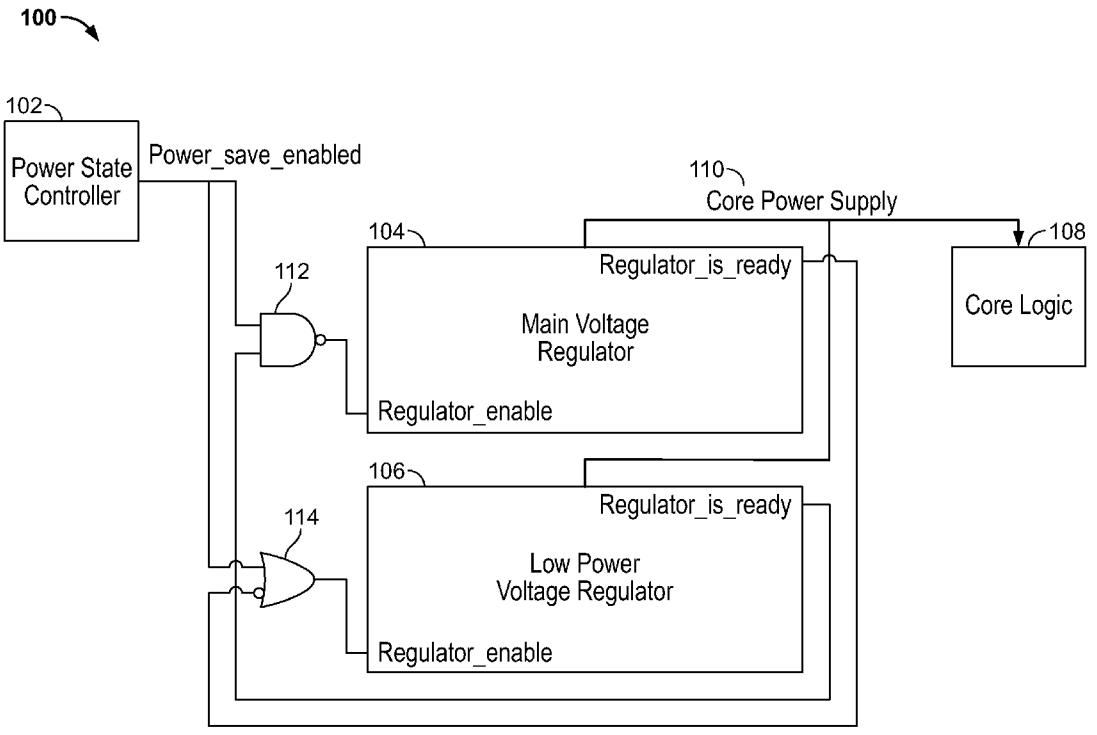
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(57) **ABSTRACT**

A microcontroller system includes a main voltage regulator and a low power voltage regulator having a static current consumption less than the static current consumption of the main voltage regulator. A power state controller enables the low power voltage regulator during a power saving mode. On exiting the power saving mode, the power state controller enables the main voltage regulator and disables the low power voltage regulator after determining that the main voltage regulator is ready. The switching circuitry can be asynchronous.



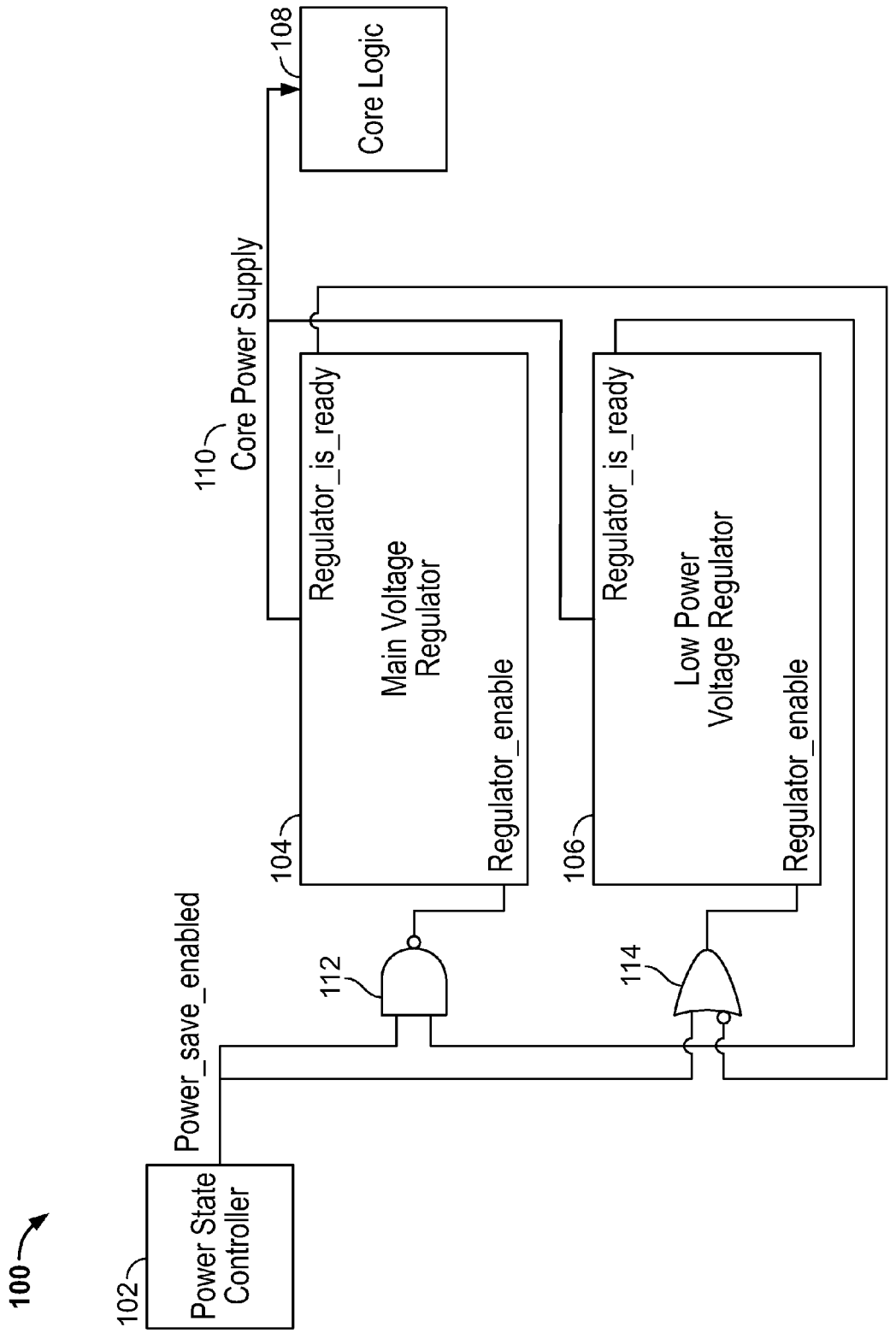

100
102
Power State Controller
Power_save_enabled
104
Main Voltage Regulator
Regulator_is_ready
Regulator_enable
106
Low Power Voltage Regulator
Regulator_is_ready
Regulator_enable
110
Core Power Supply
108
Core Logic
112
114

FIG. 1

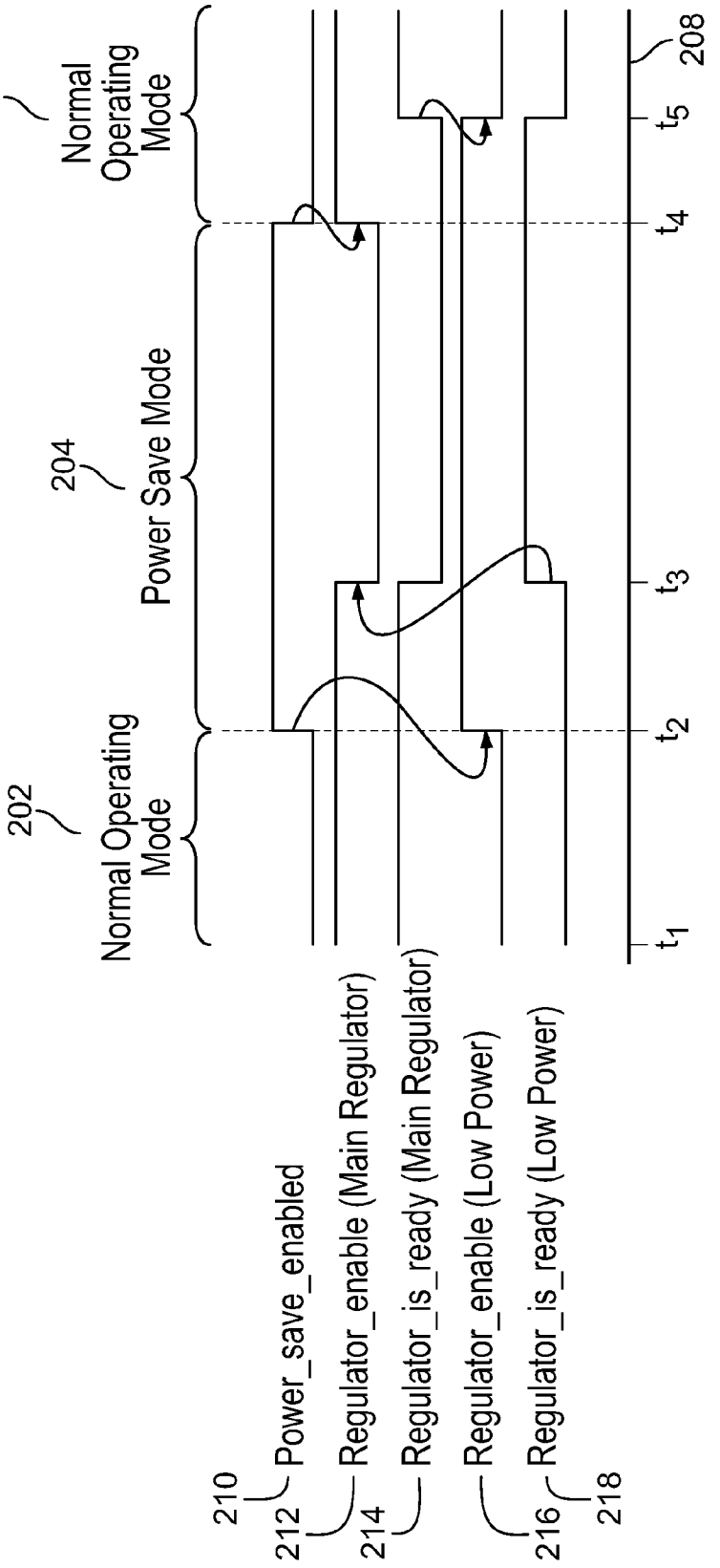

202
Normal Operating Mode
204
Power Save Mode
206
Normal Operating Mode
208
t1
t2
t3
t4
t5
210
Power_save_enabled
212
Regulator_enable (Main Regulator)
214
Regulator_is_ready (Main Regulator)
216
Regulator_enable (Low Power)
218
Regulator_is_ready (Low Power)

FIG. 2

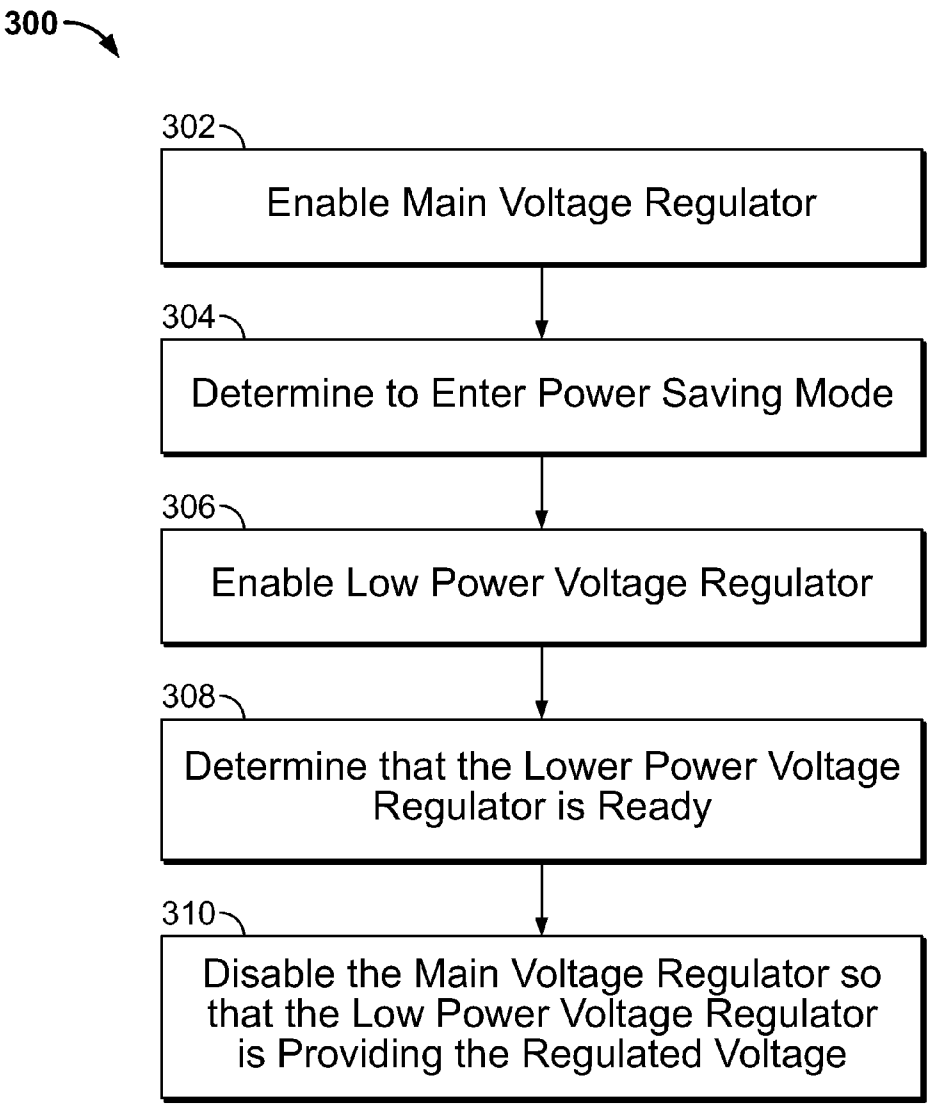

300
302
Enable Main Voltage Regulator
304
Determine to Enter Power Saving Mode
306
Enable Low Power Voltage Regulator
308
Determine that the Lower Power Voltage Regulator is Ready
310
Disable the Main Voltage Regulator so that the Low Power Voltage Regulator is Providing the Regulated Voltage

FIG. 3

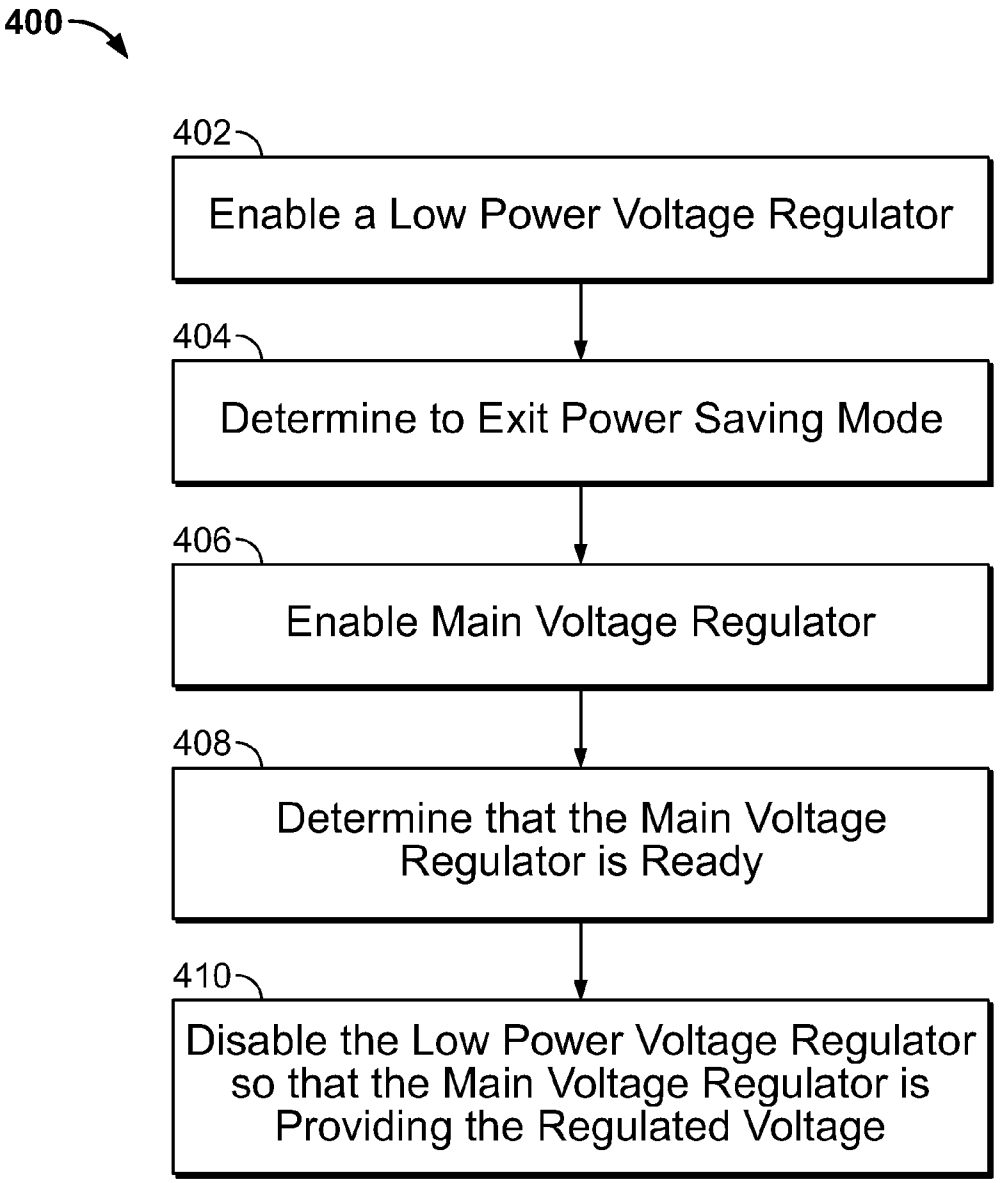

400
402
Enable a Low Power Voltage Regulator
404
Determine to Exit Power Saving Mode
406
Enable Main Voltage Regulator
408
Determine that the Main Voltage Regulator is Ready
410
Disable the Low Power Voltage Regulator so that the Main Voltage Regulator is Providing the Regulated Voltage

FIG. 4

DUAL REGULATOR SYSTEMS

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This application is the utility application of and claims the benefit and priority of U.S. Provisional Application Ser. No. 61/676,710 filed on Jul. 27, 2012, the entire contents of which are hereby incorporated by reference.

TECHNICAL FIELD

[0002] This disclosure relates generally to electronics and more particularly to voltage regulators.

BACKGROUND

[0003] A voltage regulator provides a regulated output voltage. For example, a voltage regulator can receive a voltage from a potentially unstable power supply and output a substantially constant lower voltage, which is useful for, e.g., digital circuits requiring a substantially constant voltage. In systems on a chip, the current drawn by the voltage regulator can become a significant contributor to the total power drawn by the chip in a power saving mode. Even though the core logic may not be operating in a power saving mode, the voltage regulator continues to draw current, and may be needed by certain components that continue operating in a power saving mode.

SUMMARY

[0004] A microcontroller system includes a main voltage regulator and a low power voltage regulator having a static current consumption less than the static current consumption of the main voltage regulator. A power state controller enables the low power voltage regulator during a power saving mode. On exiting the power saving mode, the power state controller enables the main voltage regulator and disables the low power voltage regulator after determining that the main voltage regulator is ready. The switching circuitry can be asynchronous.

[0005] Particular implementations of the testing circuit can provide one or more of the following advantages: 1) the system can use less power in power saving mode by switching to a low power voltage regulator; 2) the system need not use or activate a clock in order to switch from a main voltage regulator to a low power voltage regulator, which can reduce power usage both during the power saving mode and while entering and exiting the power saving mode.

[0006] The details of one or more disclosed implementations are set forth in the accompanying drawings and the description below. Other features, aspects, and advantages will become apparent from the description, the drawings and the claims.

BRIEF DESCRIPTION OF THE DRAWINGS

[0007] FIG. **1** is a schematic diagram of an example microcontroller system.

[0008] FIG. **2** is an example timing diagram illustrating the operation of the system of FIG. **1**.

[0009] FIG. **3** is a flow diagram of an example process performed by a power state controller for entering a microcontroller system into a power saving mode.

[0010] FIG. **4** is a flow diagram of an example process performed by a power state controller for exiting a power saving mode for a microcontroller system.

DETAILED DESCRIPTION

Example Microcontroller System

[0011] FIG. **1** is a schematic diagram of an example microcontroller system **100**. The system includes a power state controller **102**, a main voltage regulator **104**, a low power voltage regulator, a core logic module **108**, and a core power supply **110**.

[0012] The main voltage regulator is coupled to the core power supply and the core logic. The main voltage regulator is configured to provide a regulated voltage from the core power supply to the core logic. The low power supply is also coupled to the core power supply and the core logic, and the low power supply is configured to provide the regulated voltage from the core power supply to the core logic.

[0013] The low power voltage regulator has a low static current consumption less than a main static current consumption of the main voltage regulator. Typically, the low power voltage regulator will have a low current capability less than a main current capability of the main voltage regulator. For example, the lower power voltage regulator can have the lower static current consumption by virtue of having a smaller output buffer than the main voltage regulator, which generally also results in a lower current capability. As another example, the lower power voltage regulator can have the lower static current consumption by virtue of biasing circuitry within the lower power voltage regulator.

[0014] The power state controller is coupled to the main voltage regulator and the low power voltage regulator. The power state controller is configured to enable the low power voltage regulator during a power saving mode of the microcontroller. On exiting the power saving mode, the power state controller enables the main voltage regulator and, after determining that the main voltage regulator is ready, disables the main voltage regulator.

[0015] When the system is not in the power saving mode, the system can consume a large current in fulfilling the system's specifications. When the system is in the power saving mode, the system will generally not draw as much current. For example, some systems can draw a few micro amperes in a superficial power saving mode, or several hundreds of nano amperes in a deep power saving mode. In these power saving modes, a voltage regulator with a high current capability and a high static current consumption can become a significant contributor to the overall static current consumption of the system.

[0016] Hence, the system can save additional power during the power saving mode by switching to the low power voltage regulator while in the power saving mode and disabling the main voltage regulator so that it does not draw any substantial static current. The system can save even more power by using asynchronous switching circuitry. For example, the system as illustrated in FIG. **1** does not require the activation of a clock in order to perform the switch from the main voltage regulator to the low power voltage regulator, or to perform the switch from the low power regulator to the main voltage regulator when exiting the power saving mode.

[0017] The system includes, as an example of asynchronous circuitry, a NAND gate **112** and an OR gate **114** with an inverted input. The power state controller outputs a Power_

save_enabled signal to one of the inputs of the NAND gate and the non-inverted input of the OR gate. The power state controller drives the Power_save_enable signal high when the system is entering the power saving mode and low when the system is exiting the power saving mode.

[0018] The other input of the NAND gate is coupled to a ready output of the low power voltage regulator, and the output of the NAND gate is coupled to an enable input on the main voltage regulator. The low power voltage regulator drives the Regulator is ready signal high when the low power voltage regulator is ready. The main voltage regulator begins to start up when the Regulator_enable signal on the enable input of the main voltage regulator goes high.

[0019] The inverted input of the OR gate is coupled to a ready output of the main power voltage regulator, and the output of the OR gate is coupled to an enable input on the low power voltage regulator. The main voltage regulator drives the Regulator_is_ready signal high when the main voltage regulator is ready. The low power voltage regulator begins to start up when the Regulator enable signal on the enable input of the low power voltage regulator goes high.

[0020] The system optionally includes an energy storage device. The energy storage device can be, for example, a decoupling capacitor coupled between the core supply and ground, or a battery. The system can include a decoupling capacitor to filter the main voltage regulator's output, and that same decoupling capacitor can also be used for energy storage. The energy storage device can be used to provide power to the core logic in addition to power from the low voltage regulator while the system is exiting a power saving mode.

Example Timing Diagram

[0021] FIG. **2** is an example timing diagram illustrating the operation of the system **100** of FIG. **1**. A timeline **208** illustrates various points in time during the operation of the system.

[0022] At time t1, the system is in a normal operating mode **202**. The main voltage regulator is providing a regulated voltage to the core logic and the low power voltage regulator is disabled. The Power_save_enabled signal **210** is low, the Regulator_enable signal **212** of the main voltage regulator is high, the Regulator_is_ready **214** signal of the main voltage regulator is high, the Regulator_enable signal **216** of the low power voltage regulator signal is low, and the Regulator_is_ready **218** signal of the low power voltage regulator is low.

[0023] At time t2, the system enters the power saving mode **204**, and the power state controller drives the Power save enabled signal high. The Regulator_enable signal of the low power voltage regulator is also driven high, so the low power voltage regulator begins to start up. There is typically a time between when the low power voltage regulator begins to start up and when it is ready, e.g., due to charging of an inductor or other circuit element. During that time, the low power voltage regulator and the main voltage regulator can concurrently provide the regulated voltage to the core logic.

[0024] At time t3, the low power voltage regulator drives the Regulator is ready signal high. This results in the Regulator enable signal for the main voltage regulator going low, disabling the main voltage regulator and causing the Regulator_is_ready signal for the main voltage regulator go low.

[0025] At time t4, the system exits the power saving mode and reenters the normal operating mode **206**. The power state controller drives the Power_save_enabled signal low, resulting in the Regulator_enable signal for the main voltage regulator going high. The main voltage regulator begins to start up. There is typically a time between when the main voltage regulator begins to start up and when it is ready, e.g., due to charging of a capacitor or other circuit element. During that time, the low power voltage regulator and the main voltage regulator can concurrently provide the regulated voltage to the core logic. An optional energy storage device can provide additional power to the core logic to assist the low power voltage regulator.

[0026] At time t5, the main voltage regulator drives the Regulator_is_ready signal high. This results in the Regulator_enable signal for the low power voltage regulator going low, disabling the low power voltage regulator and causing the Regulator_is_ready signal for the low power voltage regulator to go low.

Example Operation Flowchart-Entering Power Saving Mode

[0027] FIG. **3** is a flow diagram of an example process **300** performed by a power state controller for entering a microcontroller system into a power saving mode. The system can be the example system **100** of FIG. **1**.

[0028] The power state controller enables a main voltage regulator (**302**). The main voltage regulator is coupled to a core power supply of the system and a core logic of the system. The main voltage regulator is providing a regulated voltage to the core logic.

[0029] The power state controller determines to enter a power saving mode (**304**). For example, the power state controller can receive a request to enter the power saving mode from user circuitry.

[0030] The power state controller enables a low power voltage regulator (**306**). For example, the power state controller can provide an enable signal to the low power voltage regulator. The power state controller can provide the enable signal without waiting for a clock signal to rise or fall. The low power voltage regulator has a low static current consumption less than a main static current consumption of the main voltage regulator. The low power voltage regulator can have a low current capability less than a main current capability of the main voltage regulator.

[0031] The low power voltage regulator is coupled to the core power supply and the core logic. In some implementations, both the low power voltage regulator and the main voltage regulator are providing the regulated voltage to the core logic during a time between enabling the low power voltage regulator and determining that the low power voltage regulator is ready.

[0032] The power state controller determines that the low power voltage regulator is ready (**308**). For example, the power state controller can receive a ready signal from the low power voltage regulator. In the example system of FIG. **1**, the power state controller includes a NAND gate **112** and an OR gate **114** with an inverted input to implement this feature.

[0033] As a consequence of determining that the low power voltage regulator is ready, the power state controller disables the main voltage regulator so that the low power voltage regulator is providing the regulated voltage to the core logic (**310**).

Example Operation Flowchart-Exiting Power Saving Mode

[0034] FIG. **4** is a flow diagram of an example process **400** performed by a power state controller for exiting a power

saving mode for a microcontroller system. The system can be the example system **100** of FIG. **1**.

[0035] The power state controller enables a low power voltage regulator (**402**). The low power voltage regulator is coupled to a core power supply of the system and a core logic of the system. The low power voltage regulator is providing a regulated voltage to the core logic.

[0036] The power state controller determines to exit a power saving mode (**404**). For example, the power state controller can receive a request to exit the power saving mode from user circuitry.

[0037] The power state controller enables a main voltage regulator (**406**). For example, the power state controller can provide an enable signal to the main voltage regulator. The power state controller can provide the enable signal without waiting for a clock signal to rise or fall. The low power voltage regulator has a low static current consumption less than a main static current consumption of the main voltage regulator. The low power voltage regulator can have a low current capability less than a main current capability of the main voltage regulator.

[0038] The main voltage regulator is coupled to the core power supply and the core logic. In some implementations, both the low power voltage regulator and the main voltage regulator are providing the regulated voltage to the core logic during a time between enabling the main voltage regulator and determining that the main voltage regulator is ready. In some implementations, the power state controller provides an additional voltage to the core logic from an energy storage unit during a time between enabling the main voltage regulator and determining that the main voltage regulator is ready.

[0039] The power state controller determines that the main voltage regulator is ready (**408**). For example, the power state controller can receive a ready signal from the main voltage regulator. In the example system of FIG. **1**, the power state controller includes a NAND gate **112** and an OR gate **114** with an inverted input to implement this feature.

[0040] As a consequence of determining that the main voltage regulator is ready, the power state controller disables the low power voltage regulator so that the main voltage regulator is providing the regulated voltage to the core logic (**410**).

[0041] While this document contains many specific implementation details, these should not be construed as limitations on the scope what may be claimed, but rather as descriptions of features that may be specific to particular embodiments. Certain features that are described in this specification in the context of separate embodiments can also be implemented in combination in a single embodiment. Conversely, various features that are described in the context of a single embodiment can also be implemented in multiple embodiments separately or in any suitable sub combination. Moreover, although features may be described above as acting in certain combinations and even initially claimed as such, one or more features from a claimed combination can, in some cases, be excised from the combination, and the claimed combination may be directed to a sub combination or variation of a sub combination.

What is claimed is:

1. A method performed by a power state controller of a microcontroller system, the method comprising:

enabling a main voltage regulator, the main voltage regulator being coupled to a core power supply of the microcontroller system and a core logic of the microcontroller system, the main voltage regulator providing a regulated voltage to the core logic;

determining to enter a power saving mode;

enabling a low power voltage regulator having a low static current consumption less than a main static current consumption of the main voltage regulator, the low power voltage regulator being coupled to the core power supply and the core logic;

determining that the low power voltage regulator is ready; and

disabling the main voltage regulator so that the low power voltage regulator is providing the regulated voltage to the core logic.

2. The method of claim **1**, wherein enabling the low power voltage regulator comprises providing an enable signal to the low power voltage regulator.

3. The method of claim **1**, wherein determining that the low power voltage regulator comprises receiving a ready signal from the low power voltage regulator.

4. The method of claim **1**, wherein both the low power voltage regulator and the main voltage regulator are providing the regulated voltage to the core logic during a time between enabling the low power voltage regulator and determining that the low power voltage regulator is ready.

5. The method of claim **1**, wherein the low power voltage regulator has a low current capability less than a main current capability of the main voltage regulator.

6. A method performed by a power state controller of a microcontroller system, the method comprising:

determining to exit a power saving mode, wherein, during the power saving mode, a low power voltage regulator is providing a regulated voltage to a core logic of the microcontroller system, the low power voltage regulator being coupled to a core power supply of the microcontroller system and the core logic;

enabling a main voltage regulator, the main voltage regulator being coupled to the core power supply and the core logic, the main voltage regulator having a main static current consumption higher than a low static current consumption of the low power voltage regulator;

determining that the main voltage regulator is ready; and

disabling the low power voltage regulator so that the main voltage regulator is providing the regulated voltage to the core logic.

7. The method of claim **6**, wherein enabling the main voltage regulator comprises providing an enable signal to the main voltage regulator.

8. The method of claim **6**, wherein determining that the main voltage regulator is ready comprises receiving a ready signal from the main voltage regulator.

9. The method of claim **6**, further comprising providing an additional voltage to the core logic from an energy storage unit during a time between enabling the main voltage regulator and determining that the main voltage regulator is ready.

10. The method of claim **6**, wherein the low power voltage regulator has a low current capability less than a main current capability of the main voltage regulator.

11. A system comprising:

a core power supply and a core logic;

a main voltage regulator coupled to the core power supply and the core logic;

a low power voltage regulator coupled to the core power supply and the core logic, the low power voltage regu-

lator configured for having a low static current consumption less than a main static current consumption of the main voltage regulator; and

a power state controller coupled to the main voltage regulator and the low power voltage regulator, the power state controller configured to:

enable the low power voltage regulator during a power saving mode;

on exiting the power saving mode, enable the main voltage regulator and disable the low power voltage regulator after determining that the main voltage regulator is ready.

12. The system of claim **11**, wherein the low power voltage regulator has a low current capability less than a main current capability of the main voltage regulator.

13. The system of claim **13**, wherein the main voltage regulator comprises a first output buffer having a first size, and wherein the low power voltage regulator comprises a second output buffer having a second size smaller than the first size.

14. The system of claim **11**, further comprising an energy storage unit, and wherein the power state controller is configured to provide an additional voltage to the core logic from the energy storage unit during a time between enabling the main voltage regulator and determining that the main voltage regulator is ready.

15. The system of claim **14**, wherein the energy storage unit is a decoupling capacitor.

16. The system of claim **11**, wherein the main voltage regulator comprises a ready output and an enable input, and wherein the main voltage regulator is configured to start up after receiving an enable signal on the enable input from the power state controller, and wherein the main voltage regulator is configured to provide a ready signal on the ready output when the main voltage regulator has completed starting up.

17. The system of claim **11**, wherein the low power voltage regulator comprises a ready output and an enable input, and wherein the low power voltage regulator is configured to start up after receiving an enable signal on the enable input from the power state controller, and wherein the low power voltage regulator is configured to provide a ready signal on the ready output when the low power voltage regulator has completed starting up.

18. The system of claim **11**, wherein the power state controller comprises first and second logic gates, a first output of the first logic gate being coupled to the main voltage regulator, and a second output of the second logic gate being coupled to the low power voltage regulator.

19. The system of claim **11**, wherein the main voltage regulator and the low voltage regulator are configured to concurrently supply a regulated voltage to the core logic during a time between enabling the main voltage regulator and determining that the main voltage regulator is ready.

20. The system of claim **11**, further comprising a system clock, wherein the power state controller is configured to disable the system clock during the power saving mode and enable the system clock on exiting the power saving mode.

* * * * *