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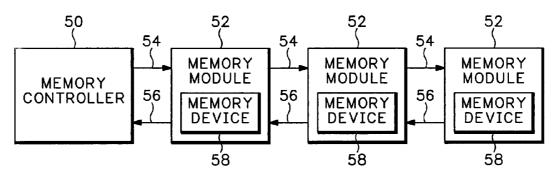
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(54) Title: MEMORY CHANNEL WITH BIT LANE FAIL-OVER



(57) Abstract: Memory apparatus and methods utilizing multiple bit lanes may redirect one or more signals on the bit lanes. A memory agent may include a redrive circuit having a plurality of bit lanes, a memory device or interface, and a fail-over circuit coupled between the plurality of bit lanes and the memory device or interface.





## INTERNATIONAL SEARCH REPORT

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IPC 7	FICATION OF SUBJECT MATTER G06F13/16		
According to	International Patent Classification (IPC) or to both national classification	ation and IPC	
B. FIELDS	SEARCHED		
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° Special ca	tegories of cited documents :	*T* later document published after the inter	mational filing date
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