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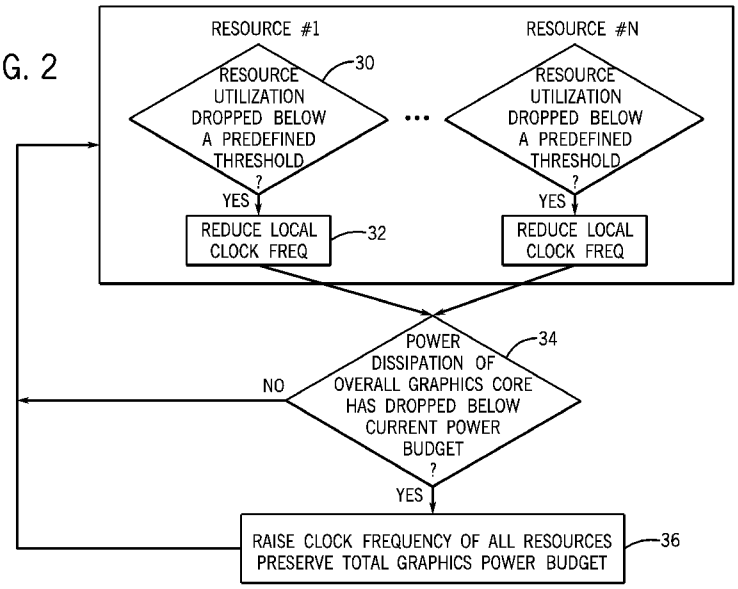
— *as to the identity of the inventor (Rule 4.17(i))*

— *as to applicant's entitlement to apply for and be granted a patent (Rule 4.17(ii))*

[Continued on next page]

(54) **Title**: DYNAMICALLY REBALANCING GRAPHICS PROCESSOR RESOURCES

FIG. 2



(57) **Abstract**: According to some embodiments, performance bottlenecks that arise in particular resources within a graphic processor unit may be alleviated by dynamically rebalancing workloads among the resources, with the goal of removing the current performance bottleneck, while at the same time maintaining power dissipation within a currently allocated power budget. In some embodiments this may be achieved by defining a separate clock domain for each of the plurality of graphics processor resources whose performance may then be rebalanced.

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DYNAMICALLY REBALANCING GRAPHICS PROCESSOR RESOURCES

Background

[0001] This relates generally to graphics processors.

[0002] Graphics processors are generally responsible for generating the displays that appear in computer systems. Each graphics processor core may include a number of different resources that perform different types of operations. For example a graphics core may include fixed function logic that implements the stages of a DirectX (DX) or other rendering pipeline, texture samplers that process textures, execution units that perform arithmetic and math operations, pixel back-ends that perform pixel fill and blend operations, etc.

[0003] Workloads that execute on a graphics core vary in their characteristics and may stress different resources available in the graphics core to different degrees, creating performance bottlenecks arising because of overloading of one resource relative to other resources. For example some workloads may be texture intensive and they create a performance bottleneck in the texture samplers. Other workloads may require intensive math operations creating a performance bottleneck in the execution units.

[0004] Furthermore the characteristics of a particular workload may change over time leading to performance bottlenecks that move dynamically from one resource to another.

Brief Description Of The Drawings

[0005] Some embodiments are described with respect to the following figures:

Figure 1 is a schematic depiction of a graphics processing unit core according to one embodiment;

Figure 2 is a flow chart for one embodiment to the present invention;

Figure 3 is a system depiction for one embodiment to the present invention; and

Figure 4 is a front elevational view for one embodiment of the present invention.

Detailed Description

[0006] According to some embodiments, performance bottlenecks that arise in particular resources within a graphic processor unit may be alleviated by dynamically rebalancing workloads among the resources, with the goal of removing the current performance bottleneck, while at the same time maintaining power dissipation within a currently allocated power budget. In some embodiments this may be achieved by defining a separate clock domain for each of the plurality of graphics processor resources whose performance may then be rebalanced.

[0007] By defining utilization metrics that quantify the current degree of utilization of each of a plurality of graphics processor resources, rebalancing may be implemented on a real time basis, given that work that is often scheduled on a particular graphics processor resource by submitting work requests into a queue that is specific to that resource. One example of a resource utilization metric is to the state of the work queue for a particular resource. That is, the more full or empty is the queue, the more or less overutilized is that resource and the greater the need for a rebalancing. However other utilization metrics may be utilized as well.

[0008] Referring to Figure 1, a graphics processing unit core 10 resources that can be rebalanced in some embodiments, include three-dimensional fixed functions 12, pixel back-end 18, and compute slices 22a and 22b. Each compute slice 22 includes a sampler 24 and a number of execution units 26. When a workload executes on a graphics core, a performance bottleneck may be created in any of the resources available on a graphics core, depending on the characteristics of that workload.

[0009] The graphics processor core may also include a cache 20, a media fixed function unit 14 and the memory interface 16.

[0010] In accordance with some embodiments, processing power can be dynamically transferred from underused to overused resources in the graphics core.

This may alleviate performance bottlenecks and improve overall performance within available power budgets in some embodiments.

[0011] Some graphics processor cores are targeted for very power limited market segments. These are often designs which operate in their frequency scaled region most of the time, where the graphics processor core operates at its minimum operating voltage, and clock frequency can decrease or increase within certain limits without having to change operating voltage as well.

[0012] Thus, in some embodiments, higher clock frequencies and greater power budget are allocated to graphics processor resources that are heavily utilized and lower clock frequencies and power budget are allocated to resources that are relatively more lightly utilized. The allocated clock frequency of each graphics processor resource may be increased or decreased over time, depending on how busy the resource is at any given point in time.

[0013] In practice this allocation may be achieved by a local decision taken by lightly utilized resources to lower their own clock frequency in one embodiment. As a result, the power dissipation of these more lightly utilized resources is reduced, thereby reducing the power dissipation of the overall graphics core below its currently allocated budget. Also, more heavily utilized resources in the graphics processor core may raise their clock frequency and fill the graphics processor core power budget back to allocated levels. At the end of a short transition period, the busier graphics resources end up using a higher clock frequency than before, relative to less busy graphics processor resources.

[0014] Different clock domains in the graphics processor core can be defined and managed by using a separate clock frequency for each graphics processor resource. Each clock frequency may come from a phase locked loop dedicated to a particular resource or from a single phase lock loop or a few phase lock loops that can divide a baseline clock frequency by various ratios. If all resources in the graphics processor core are powered from the same voltage regulator, then the fastest clock frequency required by the busiest graphics processor resource determines the voltage setting of the voltage regulator.

[0015] Alternatively, multiple voltage regulators, external to the core or integrated in the same chip with the core, may be used for different graphics processor resources, enabling some of the resources to raise their voltage and frequency independently, as needed, without forcing other graphics processor resources to operate at higher voltages as well. As a result, the busier graphics processor resources operate at a higher voltage and frequency than less busy graphics processor resources.

[0016] Another way of producing different clock domains is utilizing a single voltage domain and a single baseline clock frequency for all resources in the core, while allowing each resource to generate a lower effective local clock frequency by clock edge skipping. In clock edge skipping, a desired number of clock edges are masked. For example, masking two out three clock edges essentially divides the clock frequency by three.

[0017] For graphics processor cores that operate entirely inside their frequency scaled region most of the time, the baseline graphics clock frequency can rise and fall within certain limits while the operational voltage remains unchanged at its minimum value. Such graphics processor cores have significant room to rebalance the local clock frequencies of their resources without having to raise the voltage of operation above the minimum voltage, for most common sustained workloads and usage models.

[0018] Each resource in a graphics processor core may track its own utilization and make a decision to reduce its local clock frequency when utilization is low in one embodiment. Alternatively, there may be a centralized resource that tracks utilization of different resources and makes decisions on the local clock frequency of each resource.

[0019] If the power dissipation of the overall graphics processor core is dropped as a result of some resources reducing their clock frequency, then some power budget headroom is been created for the overall graphics core. This allows for an increase of the clock frequency of all resources, including those that are currently performance bottlenecks. Allowing an increase in clock frequency for performance

bottlenecks raises the performance level delivered by the graphics processor core as a whole. Raising the resource clock frequencies may, in some cases, also requiring the voltage of the overall graphics processor core or, in the case of multiple voltage regulators are used, of the busiest resources in the graphics processor core to change. However, many power limited designs which operate mostly inside their frequency scaled region do not need to raise the voltage most of the time.

[0020] In accordance with one embodiment shown in Figure 2, a rebalancing scheme may be implemented in software, firmware and/or hardware. In software and firmware embodiments it may be implemented by computer executed instructions stored in one or more non-transitory computer readable media such as a magnetic, optical or semiconductor storages.

[0021] In Figure 2, a number of different graphics processor resources are depicted. Each resource may check at diamond 30 whether the resource utilization has dropped below a predefined threshold. If not, the resource simply continues to periodically check whether the resource utilization has dropped below some predefined threshold.

[0022] Conversely if the resource utilization has dropped below a threshold then the local clock frequency may be reduced as indicated in block 32.

[0023] Then periodically a check (diamond 34) for all the resources may determine whether power dissipation of the overall graphics core has dropped below current budgeted levels. If not, the flow iterates.

[0024] Otherwise, the clock frequency of all the resources may be raised (block 36) preserving total graphics power budget. Then when the flow iterates back again to blocks 30 for each resource, those resources may progressively decrease their local clock frequencies as appropriate.

[0025] In other embodiments a check may determine whether utilization has increased above a predefined threshold and if such case, increase the local clock frequency. Other schemes may also be implemented according to some embodiments of the present invention.

[0026] Figure 3 illustrates an embodiment of a system 700. In embodiments, system 700 may be a media system although system 700 is not limited to this context. For example, system 700 may be incorporated into a personal computer (PC), laptop computer, ultra-laptop computer, tablet, touch pad, portable computer, handheld computer, palmtop computer, personal digital assistant (PDA), cellular telephone, combination cellular telephone/PDA, television, smart device (e.g., smart phone, smart tablet or smart television), mobile internet device (MID), messaging device, data communication device, and so forth.

[0027] In embodiments, system 700 comprises a platform 702 coupled to a display 720. Platform 702 may receive content from a content device such as content services device(s) 730 or content delivery device(s) 740 or other similar content sources. A navigation controller 750 comprising one or more navigation features may be used to interact with, for example, platform 702 and/or display 720. Each of these components is described in more detail below.

[0028] In embodiments, platform 702 may comprise any combination of a chipset 705, processor 710, memory 712, storage 714, graphics subsystem 715, applications 716, global positioning system (GPS) 721, camera 723 and/or radio 718. Chipset 705 may provide intercommunication among processor 710, memory 712, storage 714, graphics subsystem 715, applications 716 and/or radio 718. For example, chipset 705 may include a storage adapter (not depicted) capable of providing intercommunication with storage 714.

[0029] In addition, the platform 702 may include an operating system 770. An interface to the processor 772 may interface the operating system and the processor 710.

[0030] Firmware 790 may be provided to implement functions such as the boot sequence. An update module to enable the firmware to be updated from outside the platform 702 may be provided. For example the update module may include code to determine whether the attempt to update is authentic and to identify the latest update of the firmware 790 to facilitate the determination of when updates are needed.

[0031] In some embodiments, the platform 702 may be powered by an external power supply. In some cases, the platform 702 may also include an internal battery 780 which acts as a power source in embodiments that do not adapt to external power supply or in embodiments that allow either battery sourced power or external sourced power.

[0032] The sequence shown in Figure 2 may be implemented in software and firmware embodiments by incorporating them within the storage 714 or within memory within the processor 710 or the graphics subsystem 715 to mention a few examples. The graphics subsystem 715 may include the graphics processing unit and the processor 710 may be a central processing unit in one embodiment.

[0033] Processor 710 may be implemented as Complex Instruction Set Computer (CISC) or Reduced Instruction Set Computer (RISC) processors, x86 instruction set compatible processors, multi-core, or any other microprocessor or central processing unit (CPU). In embodiments, processor 710 may comprise dual-core processor(s), dual-core mobile processor(s), and so forth.

[0034] Memory 712 may be implemented as a volatile memory device such as, but not limited to, a Random Access Memory (RAM), Dynamic Random Access Memory (DRAM), or Static RAM (SRAM).

[0035] Storage 714 may be implemented as a non-volatile storage device such as, but not limited to, a magnetic disk drive, optical disk drive, tape drive, an internal storage device, an attached storage device, flash memory, battery backed-up SDRAM (synchronous DRAM), and/or a network accessible storage device. In embodiments, storage 714 may comprise technology to increase the storage performance enhanced protection for valuable digital media when multiple hard drives are included, for example.

[0036] Graphics subsystem 715 may perform processing of images such as still or video for display. Graphics subsystem 715 may be a graphics processing unit (GPU) or a visual processing unit (VPU), for example. An analog or digital interface may be used to communicatively couple graphics subsystem 715 and display 720.

For example, the interface may be any of a High-Definition Multimedia Interface, DisplayPort, wireless HDMI, and/or wireless HD compliant techniques. Graphics subsystem 715 could be integrated into processor 710 or chipset 705. Graphics subsystem 715 could be a stand-alone card communicatively coupled to chipset 705.

[0037] The graphics and/or video processing techniques described herein may be implemented in various hardware architectures. For example, graphics and/or video functionality may be integrated within a chipset. Alternatively, a discrete graphics and/or video processor may be used. As still another embodiment, the graphics and/or video functions may be implemented by a general purpose processor, including a multi-core processor. In a further embodiment, the functions may be implemented in a consumer electronics device.

[0038] Radio 718 may include one or more radios capable of transmitting and receiving signals using various suitable wireless communications techniques. Such techniques may involve communications across one or more wireless networks. Exemplary wireless networks include (but are not limited to) wireless local area networks (WLANs), wireless personal area networks (WPANs), wireless metropolitan area network (WMANs), cellular networks, and satellite networks. In communicating across such networks, radio 718 may operate in accordance with one or more applicable standards in any version.

[0039] In embodiments, display 720 may comprise any television type monitor or display. Display 720 may comprise, for example, a computer display screen, touch screen display, video monitor, television-like device, and/or a television. Display 720 may be digital and/or analog. In embodiments, display 720 may be a holographic display. Also, display 720 may be a transparent surface that may receive a visual projection. Such projections may convey various forms of information, images, and/or objects. For example, such projections may be a visual overlay for a mobile augmented reality (MAR) application. Under the control of one or more software applications 716, platform 702 may display user interface 722 on display 720.

[0040] In embodiments, content services device(s) 730 may be hosted by any national, international and/or independent service and thus accessible to platform

702 via the Internet, for example. Content services device(s) 730 may be coupled to platform 702 and/or to display 720. Platform 702 and/or content services device(s) 730 may be coupled to a network 760 to communicate (e.g., send and/or receive) media information to and from network 760. Content delivery device(s) 740 also may be coupled to platform 702 and/or to display 720.

[0041] In embodiments, content services device(s) 730 may comprise a cable television box, personal computer, network, telephone, Internet enabled devices or appliance capable of delivering digital information and/or content, and any other similar device capable of unidirectionally or bidirectionally communicating content between content providers and platform 702 and/display 720, via network 760 or directly. It will be appreciated that the content may be communicated unidirectionally and/or bidirectionally to and from any one of the components in system 700 and a content provider via network 760. Examples of content may include any media information including, for example, video, music, medical and gaming information, and so forth.

[0042] Content services device(s) 730 receives content such as cable television programming including media information, digital information, and/or other content. Examples of content providers may include any cable or satellite television or radio or Internet content providers. The provided examples are not meant to limit embodiments of the invention.

[0043] In embodiments, platform 702 may receive control signals from navigation controller 750 having one or more navigation features. The navigation features of controller 750 may be used to interact with user interface 722, for example. In embodiments, navigation controller 750 may be a pointing device that may be a computer hardware component (specifically human interface device) that allows a user to input spatial (e.g., continuous and multi-dimensional) data into a computer. Many systems such as graphical user interfaces (GUI), and televisions and monitors allow the user to control and provide data to the computer or television using physical gestures.

[0044] Movements of the navigation features of controller 750 may be echoed on a display (e.g., display 720) by movements of a pointer, cursor, focus ring, or other visual indicators displayed on the display. For example, under the control of software applications 716, the navigation features located on navigation controller 750 may be mapped to virtual navigation features displayed on user interface 722, for example. In embodiments, controller 750 may not be a separate component but integrated into platform 702 and/or display 720. Embodiments, however, are not limited to the elements or in the context shown or described herein.

[0045] In embodiments, drivers (not shown) may comprise technology to enable users to instantly turn on and off platform 702 like a television with the touch of a button after initial boot-up, when enabled, for example. Program logic may allow platform 702 to stream content to media adaptors or other content services device(s) 730 or content delivery device(s) 740 when the platform is turned "off." In addition, chip set 705 may comprise hardware and/or software support for 5.1 surround sound audio and/or high definition 7.1 surround sound audio, for example. Drivers may include a graphics driver for integrated graphics platforms. In embodiments, the graphics driver may comprise a peripheral component interconnect (PCI) Express graphics card.

[0046] In various embodiments, any one or more of the components shown in system 700 may be integrated. For example, platform 702 and content services device(s) 730 may be integrated, or platform 702 and content delivery device(s) 740 may be integrated, or platform 702, content services device(s) 730, and content delivery device(s) 740 may be integrated, for example. In various embodiments, platform 702 and display 720 may be an integrated unit. Display 720 and content service device(s) 730 may be integrated, or display 720 and content delivery device(s) 740 may be integrated, for example. These examples are not meant to limit the invention.

[0047] In various embodiments, system 700 may be implemented as a wireless system, a wired system, or a combination of both. When implemented as a wireless system, system 700 may include components and interfaces suitable for

communicating over a wireless shared media, such as one or more antennas, transmitters, receivers, transceivers, amplifiers, filters, control logic, and so forth. An example of wireless shared media may include portions of a wireless spectrum, such as the RF spectrum and so forth. When implemented as a wired system, system 700 may include components and interfaces suitable for communicating over wired communications media, such as input/output (I/O) adapters, physical connectors to connect the I/O adapter with a corresponding wired communications medium, a network interface card (NIC), disc controller, video controller, audio controller, and so forth. Examples of wired communications media may include a wire, cable, metal leads, printed circuit board (PCB), backplane, switch fabric, semiconductor material, twisted-pair wire, co-axial cable, fiber optics, and so forth.

[0048] Platform 702 may establish one or more logical or physical channels to communicate information. The information may include media information and control information. Media information may refer to any data representing content meant for a user. Examples of content may include, for example, data from a voice conversation, videoconference, streaming video, electronic mail ("email") message, voice mail message, alphanumeric symbols, graphics, image, video, text and so forth. Data from a voice conversation may be, for example, speech information, silence periods, background noise, comfort noise, tones and so forth. Control information may refer to any data representing commands, instructions or control words meant for an automated system. For example, control information may be used to route media information through a system, or instruct a node to process the media information in a predetermined manner. The embodiments, however, are not limited to the elements or in the context shown or described in Figure 3.

[0049] As described above, system 700 may be embodied in varying physical styles or form factors. Figure 4 illustrates embodiments of a small form factor device 800 in which system 700 may be embodied. In embodiments, for example, device 800 may be implemented as a mobile computing device having wireless capabilities. A mobile computing device may refer to any device having a processing system and a mobile power source or supply, such as one or more batteries, for example.

[0050] As described above, examples of a mobile computing device may include a personal computer (PC), laptop computer, ultra-laptop computer, tablet, touch pad, portable computer, handheld computer, palmtop computer, personal digital assistant (PDA), cellular telephone, combination cellular telephone/PDA, television, smart device (e.g., smart phone, smart tablet or smart television), mobile internet device (MID), messaging device, data communication device, and so forth.

[0051] Examples of a mobile computing device also may include computers that are arranged to be worn by a person, such as a wrist computer, finger computer, ring computer, eyeglass computer, belt-clip computer, arm-band computer, shoe computers, clothing computers, and other wearable computers. In embodiments, for example, a mobile computing device may be implemented as a smart phone capable of executing computer applications, as well as voice communications and/or data communications. Although some embodiments may be described with a mobile computing device implemented as a smart phone by way of example, it may be appreciated that other embodiments may be implemented using other wireless mobile computing devices as well. The embodiments are not limited in this context.

[0052] As shown in Figure 4, device 800 may comprise a housing 802, a display 804, an input/output (I/O) device 806, and an antenna 808. Device 800 also may comprise navigation features 812. Display 804 may comprise any suitable display unit for displaying information appropriate for a mobile computing device. I/O device 806 may comprise any suitable I/O device for entering information into a mobile computing device. Examples for I/O device 806 may include an alphanumeric keyboard, a numeric keypad, a touch pad, input keys, buttons, switches, rocker switches, microphones, speakers, voice recognition device and software, and so forth. Information also may be entered into device 800 by way of microphone. Such information may be digitized by a voice recognition device. The embodiments are not limited in this context.

[0053] Various embodiments may be implemented using hardware elements, software elements, or a combination of both. Examples of hardware elements may include processors, microprocessors, circuits, circuit elements (e.g., transistors,

resistors, capacitors, inductors, and so forth), integrated circuits, application specific integrated circuits (ASIC), programmable logic devices (PLD), digital signal processors (DSP), field programmable gate array (FPGA), logic gates, registers, semiconductor device, chips, microchips, chip sets, and so forth. Examples of software may include software components, programs, applications, computer programs, application programs, system programs, machine programs, operating system software, middleware, firmware, software modules, routines, subroutines, functions, methods, procedures, software interfaces, application program interfaces (API), instruction sets, computing code, computer code, code segments, computer code segments, words, values, symbols, or any combination thereof. Determining whether an embodiment is implemented using hardware elements and/or software elements may vary in accordance with any number of factors, such as desired computational rate, power levels, heat tolerances, processing cycle budget, input data rates, output data rates, memory resources, data bus speeds and other design or performance constraints.

[0054] One or more aspects of at least one embodiment may be implemented by representative instructions stored on a machine-readable medium which represents various logic within the processor, which when read by a machine causes the machine to fabricate logic to perform the techniques described herein. Such representations, known as “IP cores” may be stored on a tangible, machine readable medium and supplied to various customers or manufacturing facilities to load into the fabrication machines that actually make the logic or processor.

[0055] Various embodiments may be implemented using hardware elements, software elements, or a combination of both. Examples of hardware elements may include processors, microprocessors, circuits, circuit elements (e.g., transistors, resistors, capacitors, inductors, and so forth), integrated circuits, application specific integrated circuits (ASIC), programmable logic devices (PLD), digital signal processors (DSP), field programmable gate array (FPGA), logic gates, registers, semiconductor device, chips, microchips, chip sets, and so forth. Examples of software may include software components, programs, applications, computer programs, application programs, system programs, machine programs, operating

system software, middleware, firmware, software modules, routines, subroutines, functions, methods, procedures, software interfaces, application program interfaces (API), instruction sets, computing code, computer code, code segments, computer code segments, words, values, symbols, or any combination thereof. Determining whether an embodiment is implemented using hardware elements and/or software elements may vary in accordance with any number of factors, such as desired computational rate, power levels, heat tolerances, processing cycle budget, input data rates, output data rates, memory resources, data bus speeds and other design or performance constraints.

[0056] One or more aspects of at least one embodiment may be implemented by representative instructions stored on a machine-readable medium which represents various logic within the processor, which when read by a machine causes the machine to fabricate logic to perform the techniques described herein. Such representations, known as “IP cores” may be stored on a tangible, machine readable medium and supplied to various customers or manufacturing facilities to load into the fabrication machines that actually make the logic or processor.

[0057] The graphics processing techniques described herein may be implemented in various hardware architectures. For example, graphics functionality may be integrated within a chipset. Alternatively, a discrete graphics processor may be used. As still another embodiment, the graphics functions may be implemented by a general purpose processor, including a multicore processor.

[0058] References throughout this specification to “one embodiment” or “an embodiment” mean that a particular feature, structure, or characteristic described in connection with the embodiment is included in at least one implementation encompassed within the present invention. Thus, appearances of the phrase “one embodiment” or “in an embodiment” are not necessarily referring to the same embodiment. Furthermore, the particular features, structures, or characteristics may be instituted in other suitable forms other than the particular embodiment illustrated and all such forms may be encompassed within the claims of the present application.

[0059] While the present invention has been described with respect to a limited number of embodiments, those skilled in the art will appreciate numerous modifications and variations therefrom. It is intended that the appended claims cover all such modifications and variations as fall within the true spirit and scope of this present invention.

What is claimed is:

1. A method comprising:
analyzing workloads of resources within a graphics processing unit; and
rebalancing workloads among those resources.

2. The method of claim 1 including enabling different clock domains for different resources.

3. The method of claim 2 including checking whether resource utilization drops below a threshold.

4. The method of claim 3 including, if so reducing a resource's local frequency.

5. The method of claim 4 including checking whether overall power dissipation dropped due to reducing the resource's local frequency.

6. The method of claim 5 including if so raising clock frequencies of a plurality of resources.

7. The method of claim 1 including analyzing workloads of one or more of three-dimensional fixed functions, pixel back-end, or compute slices.

8. The method of claim 2 including using clock edge skipping.

9. One or more non-transitory computer readable media storing instructions to cause a processor to perform a sequence comprising:
analyzing workloads of components within a graphics processing unit; and
rebalancing workloads among those components.

10. The media of claim 9, the sequence further including enabling different clock domains for different resources.

11. The media of claim 10, the sequence further including checking whether component utilization drops below a threshold.

12. The media of claim 11, the sequence further including, if so, reducing a component's local frequency.

13. The media of claim 12, the sequence further including checking whether overall power dissipation dropped due to reducing the component's local frequency.

14. The media of claim 13, the sequence further including, if so, raising clock frequencies of a plurality of components.

15. The media of claim 9, the sequence further including analyzing workloads of one or more of three-dimensional fixed function, pixel back-end, or compute slice components.

16. The media of claim 10 the sequence further including using clock edge skipping.

17. A graphics processor comprising:
a first resource;
a second resource; and
a unit to analyze utilization of said resources and to rebalance workloads between said resources.

18. The processor of claim 17, including different clock domains for said resources.

19. The processor of claim 18, said processor to check whether resource utilization drops below a threshold.

20. The processor of claim 19, if so, said processor to reduce a resource's local frequency.

21. The processor of claim 20, said processor to check whether overall power dissipation dropped due to reducing the resource's local frequency.

22. The processor of claim 21, if so, said processor to raise clock frequencies of said resources.

23. The processor of claim 17, said processor to analyze workloads of one or more of a three-dimensional fixed function, a pixel back-end, or a computer slice.

24. The processor of claim 18, said processor to use clock edge skipping.

25. A system comprising:
a central processing unit; and
a graphics processor coupled to said unit, said graphics processor including a first resource, a second resource and a device to analyze utilization of said resources and to rebalance workloads between said resources.

26. The system of claim 25 including an operating system.

27. The system of claim 25 including a battery.

28. The system of claim 25 including firmware and a module to update said firmware.

29. The system of claim 25, said graphics processor having different clock domains for said resources.

30. The system of claim 29, said processor to use clock edge skipping.

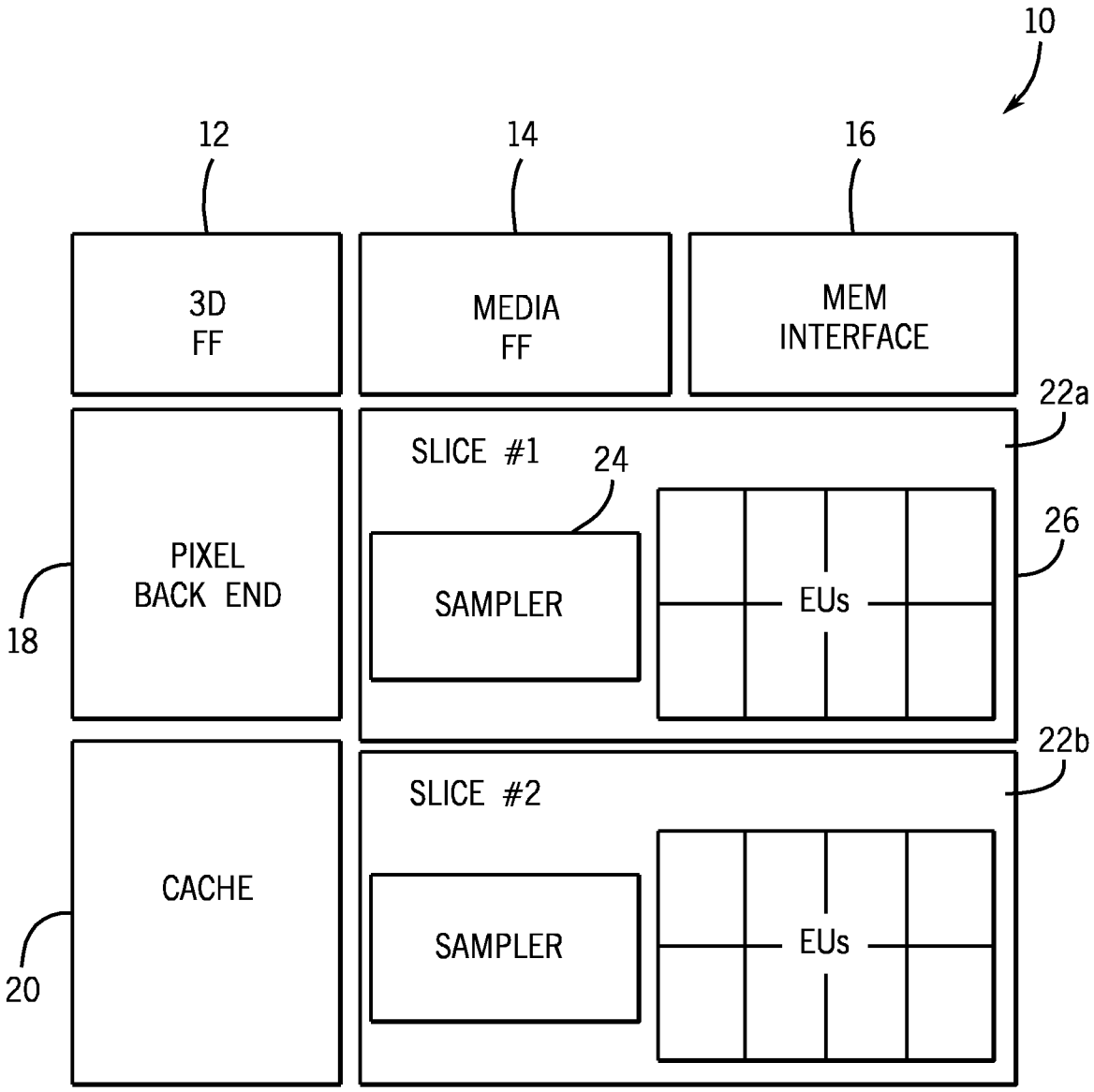
10
12
14
16
3D
FF
MEDIA
FF
MEM
INTERFACE
22a
SLICE #1
24
PIXEL
BACK END
SAMPLER
EUs
26
18
22b
SLICE #2
CACHE
SAMPLER
EUs
20

FIG. 1

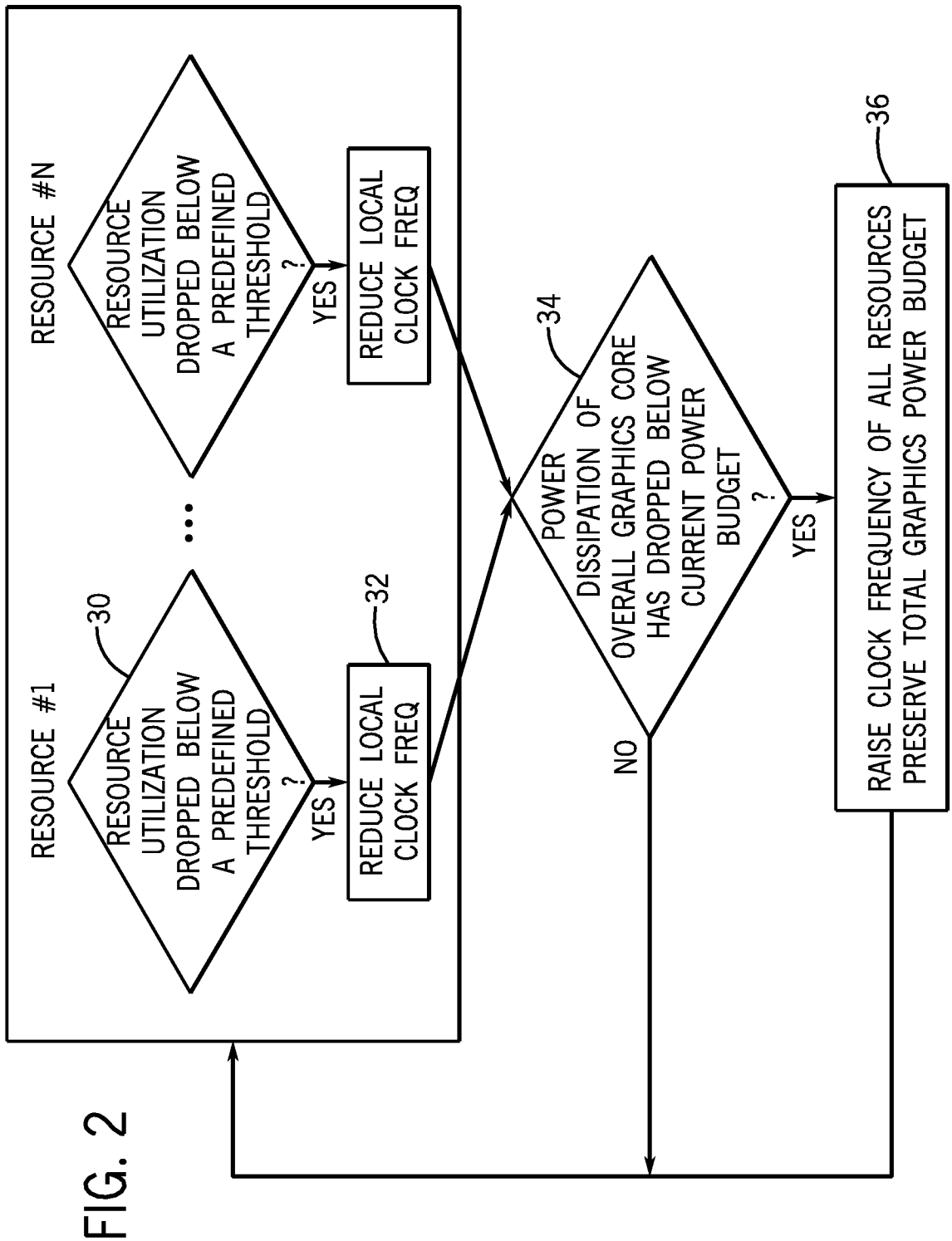
RESOURCE #1
RESOURCE #N
RESOURCE UTILIZATION DROPPED BELOW A PREDEFINED THRESHOLD ?
30
YES
REDUCE LOCAL CLOCK FREQ
32
34
POWER DISSIPATION OF OVERALL GRAPHICS CORE HAS DROPPED BELOW CURRENT POWER BUDGET ?
NO
YES
36
RAISE CLOCK FREQUENCY OF ALL RESOURCES PRESERVE TOTAL GRAPHICS POWER BUDGET

FIG. 2

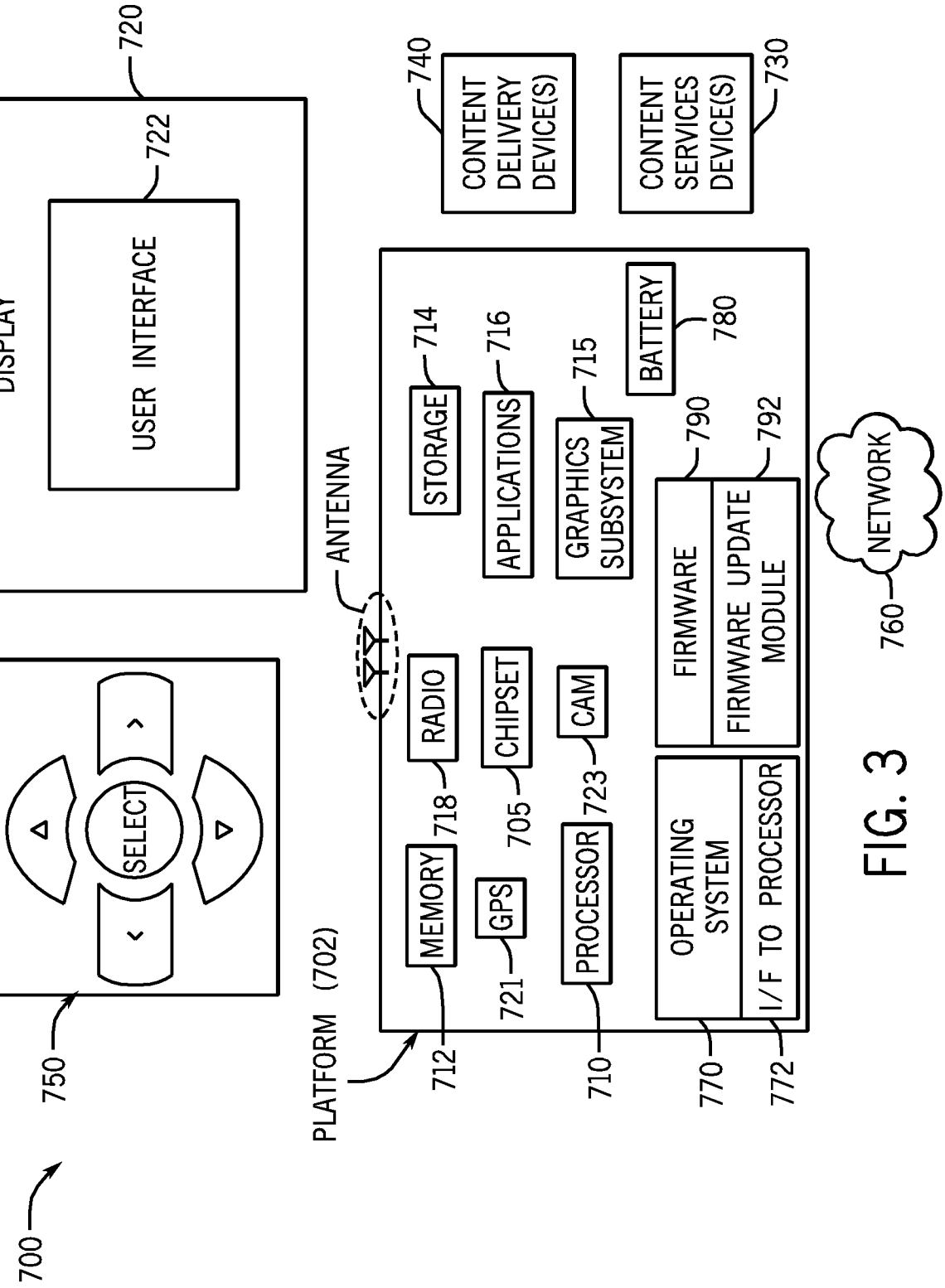
700
750
SELECT
720
DISPLAY
722
USER INTERFACE
ANTENNA
PLATFORM (702)
712
MEMORY
718
GPS
721
RADIO
CHIPSET
705
PROCESSOR
723
CAM
STORAGE
714
APPLICATIONS
716
GRAPHICS SUBSYSTEM
715
BATTERY
780
FIRMWARE
790
FIRMWARE UPDATE MODULE
792
OPERATING SYSTEM
770
I/F TO PROCESSOR
772
NETWORK
760
CONTENT DELIVERY DEVICE(S)
740
CONTENT SERVICES DEVICE(S)
730

FIG. 3

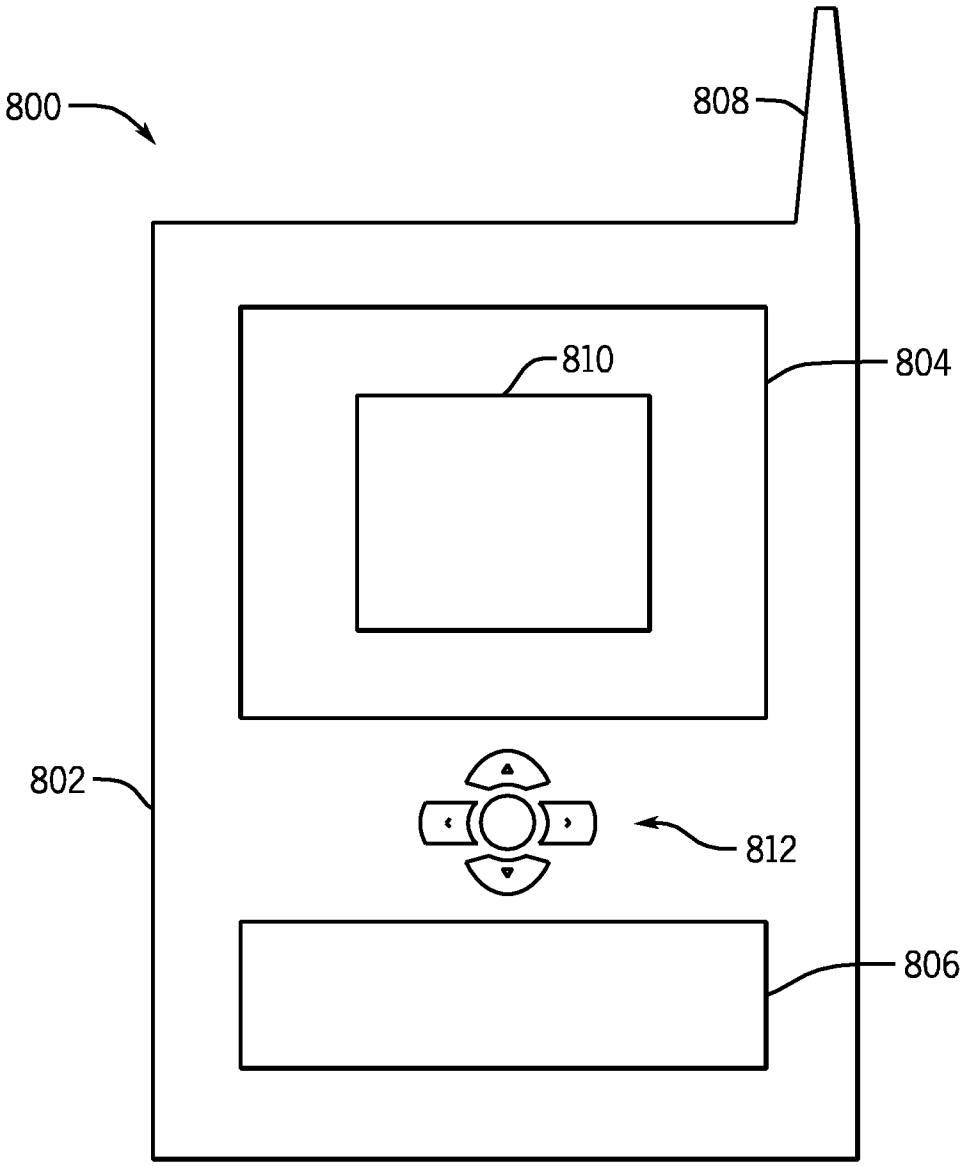

FIG. 4

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2013/048037

A. CLASSIFICATION OF SUBJECT MATTER

G06F 9/50(2006.01)i, G06F 9/06(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
G06F 9/50; G06F 1/06; G06F 15/80; G06T 15/00; G06T 1/00; G09G 5/00; G06F 9/06

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
Korean utility models and applications for utility models
Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
eKOMPASS(KIPO internal) & Keywords: graphics processor, rebalancing, workload

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X A	US 2005-0195181 A1 (OLEKSANDR KHODORKOVSKY) 08 September 2005 See abstract, paragraphs [0013-0014], claim 1, and figures 1-5.	1-4,9-12,17-20,25 ,26-28,29 5-8,13-16,21-24,30
A	US 2007-0206018 A1 (ATI Technologies Inc.) 06 September 2007 See abstract, paragraphs [0008]-[0012], and figures 1-7.	1-30
A	US 2005-0041031 A1 (FRANCK, R. DIARD) 24 February 2005 See abstract, paragraphs [0009]-[0015], and figures 1-5, 8.	1-30
A	WO 2005-086095 A1 (QUALCOMM INCORPORATED et al.) 15 September 2005 See abstract, paragraphs [0004]-[0007], and figures 2-5.	1-30

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"E" earlier application or patent but published on or after the international filing date
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"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents,such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
31 October 2013 (31.10.2013)	**01 November 2013 (01.11.2013)**

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INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.
PCT/US2013/048037

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		CN 1942900 C0	04/04/2007
		US 2005-0195183 A1	08/09/2005