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(54) Semiconductor device with surface integrated focusing element

(57) The semiconductor device comprises a semiconductor substrate (1), a sensor or sensor array (2) arranged at a main surface (10) of the substrate, an integrated circuit (3) arranged at or above the main surface, and a focusing element (4) formed within a further main surface (11) of the substrate opposite the main surface. The focusing element is preferably arranged opposite the sensor or sensor array (2), which may be a photosensor or photodetector or an array of photosensors or photodetectors, for instance.

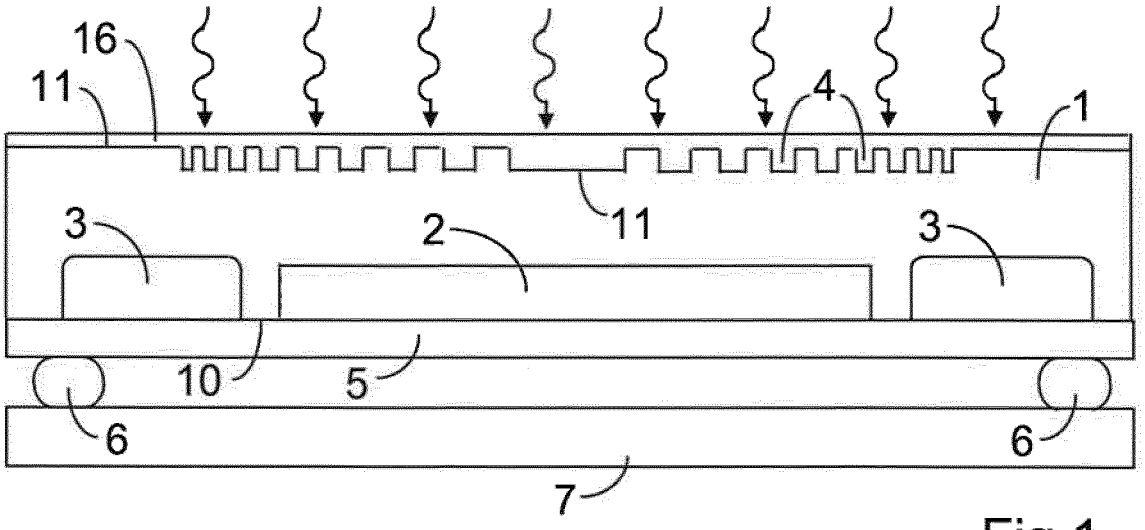

Fig 1

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Description

[0001] The invention relates to wafer-level integration of focusing elements in semiconductor devices like optical sensors. Conventional focusing elements, usually lenses, are discrete elements arranged in the package of the device. They require a lot of space and increase the packaging costs.

[0002] US 2008/0237761 A1 discloses a system and a method for enhancing light sensitivity of a back-side illumination image sensor. An integrated circuit includes a substrate and an image sensor device comprising at least one transistor formed over a first surface of the substrate and a photosensitive region. A color filter is disposed over an opposite second surface of the substrate. A micro-lens structure is disposed between the second substrate surface and the color filter.

[0003] US 2005/0212132 A1 discloses a chip package including a rigid cover disposed above the active surface of the chip to protect the chip and to enhance the structural strength of the chip package. The rigid cover exposes a plurality of bond pads, which are arranged on the active surface of the chip and carry conductive bumps. The height of the bumps above the surface is larger than the height of the rigid cover.

[0004] It is an object of the present invention to disclose a semiconductor device with a focusing element that does not essentially increase the height of the device and is suitable for wafer-level production. It is a further object of the invention to disclose a method of producing such a device. This object is achieved with the semiconductor device according to claim 1 and with the method of producing a semiconductor device according to claim 11. Embodiments and variants derive from the dependent claims.

[0005] The focusing element is formed within the rear surface of a semiconductor substrate or wafer with integrated components, which can be manufactured at the front side by a standard CMOS process, for instance. The focusing element does not occupy an additional volume of the device. Manufacturing requires only few additional process steps. The invention can be applied to sensor devices conventionally comprising a lens (infrared sensors, for instance) as a compact and cheap way of implementing integrated optics. The performance of many sensor devices (especially photodiodes, for instance) can be enhanced by the focusing element. The proposed invention is especially favourable in conjunction with photosensors that detect radiation in a wavelength range where silicon is transparent (typically infrared radiation).

[0006] The semiconductor device comprises a semiconductor substrate, a sensor or sensor array arranged at a main surface of the substrate, an integrated circuit arranged at or above the main surface, and a focusing element formed within a further main surface of the substrate opposite the main surface. The focusing element is preferably arranged opposite the sensor or sensor array, which may be a photosensor or photodetector or an array of photosensors or photodetectors, for instance.

[0007] The integrated circuit may be arranged in the semiconductor substrate.

[0008] Bump contacts may be arranged at or above the main surface of the semiconductor substrate. The bump contacts can be provided for external electrical connections.

[0009] In an embodiment of the semiconductor device, the focusing element is a diffracting element.

[0010] In a further embodiment, the focusing element is a zone plate comprising a set of radially symmetric Fresnel zones.

[0011] In a further embodiment, a covering layer is present on the focusing element to generate a phase shift zone plate.

[0012] In a further embodiment, the focusing element is a Fresnel lens.

[0013] In a further embodiment, a cover is arranged at or above the main surface to cover the sensor or sensor array or a cavity wherein the sensor or sensor array is arranged, and openings are provided in the cover for the accomodation of bump contacts. The integrated circuit may be arranged in the cover.

[0014] The method of producing a semiconductor device with focusing element comprises arranging a sensor or sensor array at a main surface of a semiconductor substrate, providing an integrated circuit at or above the main surface, and etching a focusing element in a further main surface of the substrate opposite the main surface.

[0015] In a variant of the method, the focusing element is etched in the shape of a zone plate or Fresnel lens.

[0016] In a further variant of the method, a cover is applied to the main surface, before the focusing element is etched. The cover is preferably rigid and can be a further semiconductor substrate or wafer, for instance, which may comprise the integrated circuit. The cover can be provided to cover the sensor or sensor array or a cavity wherein the sensor or sensor array is arranged.

[0017] In a further variant of the method, the cover is provided with openings for bump contacts. The bump contacts can be provided for external electrical connections.

[0018] The following is a detailed description of examples of the semiconductor device and of examples of the method for producing the semiconductor device.

Figure 1 is a cross section of an embodiment of the semiconductor device comprising a sensor or sensor array.

Figure 2 is a cross section of a further embodiment of the semiconductor device comprising a cover above the sensor or sensor array.

Figure 3 is a cross section of a further embodiment of the semiconductor device comprising an integrated circuit arranged in a cover above

the sensor or sensor array.

Figure 4 is a top view of the embodiment shown in Figure 1.

Figure 5 is a top view of a further embodiment.

Figure 6 is a cross section of an intermediate product of a method of producing the semiconductor device.

Figure 7 is a cross section according to Figure 6 in a state during etching of the focusing element.

Figure 8 is a cross section according to Figure 7 after the etching process.

Figure 9 is a cross section of an intermediate product according to Figure 6 for a further embodiment.

Figure 10 is a cross section according to Figure 9 after the application of a cover above the sensor or sensor array.

Figure 11 is a cross section according to Figure 10 in a state during etching of the focusing element.

Figure 12 is a cross section according to Figure 11 after the etching process.

Figure 13 is a cross section of an intermediate product according to Figure 9 for a further embodiment.

Figure 14 is a cross section according to Figure 13 after the application of a cover with an integrated circuit.

Figure 15 is a cross section according to Figure 14 in a state during etching of the focusing element.

Figure 16 is a cross section according to Figure 15 after the etching process.

Figure 1 is a cross section of an embodiment of the semiconductor device comprising a semiconductor substrate 1 with a main surface 10 and a further main surface 11 opposite the main surface 10. A sensor or sensor array 2, which may be a photodetector or an array of photodetectors, for instance, and an integrated circuit 3 are arranged at or near the main surface 10. The integrated circuit 3 can be provided for the operation of the sensor or sensor array 2. Details of the sensor or sensor array 2 and of the integrated circuit 3 are not essential and are not represented in the figures.

[0019] A focusing element 4 is arranged within the further main surface 11, preferably in a position opposite the sensor or sensor array 2. A wiring layer 5, which may comprise several structured metal layers embedded in intermetal dielectric, can be provided on the main surface 10 as a wiring of the integrated circuit 3. Optional bump contacts 6, which may be solder balls, for instance, can be arranged on contact areas or pads of the wiring layer 5 to provide external electrical connections. The semiconductor device can be mounted on a board 7, which may be a printed circuit board (PCB), for instance, by connecting the bump contacts 6 to contact areas or pads of the board 7.

[0020] As the focusing element 4 is formed within the further main surface 11, it does not require any additional volume, and the dimensions of the semiconductor device are therefore extremely small. The focusing element 4 can be provided with a covering layer 16, which may be an antireflective coating (AR), for instance. The focusing element 4 can be formed as a diffracting element, in particular as a zone plate comprising a set of radially symmetric Fresnel zones, which are spaced to generate constructive interference at the desired focus. Zone plates and their application to semiconductor devices are known per se. The Fresnel zones of the focusing element 4 are formed by concentric circular trenches of suitably varying diameters, widths and distances. A covering layer 16 of a suitable refractive material can be applied to fill the trenches, as shown in Figure 1, in order to produce a phase shift zone plate, wherein half wavelength phase delays are created between adjacent ring zones. The elevated regions located between the trenches can be provided with suitably sloping surfaces to form a Fresnel lens, which is also known per se from conventional optical devices and need not be described in detail.

[0021] A plurality of semiconductor devices as shown in Figure 1 can be produced on a wafer. A front side of the wafer is processed to form the sensors and the appertaining electronic circuits, which may especially be CMOS circuits, and the backside of the wafer is etched to produce focusing elements for each of the sensors or sensor arrays. An arrangement of a plurality of sensors in an array can especially be applied for image detection, for example. In this case a plurality of focusing elements may be arranged in a corresponding array opposite the sensors forming the array.

[0022] Figure 2 is a cross section of a further embodiment of the semiconductor device. Elements of the embodiment according to Figure 2 that correspond to elements of the embodiment according to Figure 1 are designated with the same reference numerals. The embodiment according to Figure 2 comprises a cover 8 on or above the main surface 10 of the semiconductor substrate 1. The cover 8 is preferably rigid and may be a further semiconductor substrate or wafer, for instance. If the sensor or sensor array 2 is arranged in a cavity 12 of the substrate 1, the cover 8 can be provided to cover

or close the cavity 12. If external electrical connections are to be formed by bump contacts, openings 9 are provided in the cover 8 for the accomodation of the bump contacts 6. The height of the bump contacts 6 has to exceed the height of the cover 8 at least slightly to allow the bump contacts 6 to be connected to contact areas or pads of the board 7. The depth of the openings 9 is typically not larger than about 100 μm.

[0023] Figure 3 is a cross section of a further embodiment of the semiconductor device. Elements of the embodiment according to Figure 3 that correspond to elements of the embodiment according to Figure 2 are designated with the same reference numerals. The embodiment according to Figure 3 comprises a cover 8 on or above the main surface 10 of the semiconductor substrate 1. The cover 8 is a further semiconductor substrate of wafer, which is provided with an integrated circuit 13. The substrate 1 may also comprise an integrated circuit 3, as in the embodiment according to Figure 2. Instead, the integrated circuit 13 of the cover 8 may be the only integrated circuit, as shown in the example of Figure 3. If no integrated circuit 3 is required in the substrate 1, the lateral dimensions of the semiconductor device are extremely small. This is especially advantageous if the lateral dimensions of the sensor or sensor array 2 are to be larger than in the examples shown in Figures 1 and 2.

[0024] Figure 4 is a top view of the embodiment according to Figure 1 or 2. A single semiconductor device is mounted on the board 7. The hidden contours of the integrated circuit 3 arranged in the semiconductor substrate 1 and of the bump contacts 6 are indicated with broken lines. In the embodiment according to Figure 1 or 2 and Figure 4, the integrated circuit 3 surrounds the sensor or sensor array 2, which is located opposite the focusing element 4. In Figure 4 the focusing element 4 is represented as a zone plate, but other structures are not meant to be excluded. The dash-dotted diagonal line indicates the position of the cross sections of Figures 1 and 2.

[0025] Figure 5 is a top view of a further embodiment, which differs from the embodiment according to Figure 4 in the arrangement of the integrated circuit 3. In the embodiment according to Figure 5, the integrated circuit 3 is confined to one side of the sensor or sensor array 2. The arrangement of the integrated circuit 3 may be varied according to individual requirements. The number and positions of the bump contacts 6 may also vary.

[0026] Methods of producing a semiconductor device with focusing element are described in the following in conjunction with Figures 6 to 16, which are cross sections of typical intermediate products of the described methods.

[0027] Figure 6 is a cross section of a semiconductor substrate 1 provided with the sensor or sensor array 2 and the integrated circuit 3 at the main surface 10. The semiconductor substrate 1 may be part of a wafer, wherein a plurality of sensors or sensor arrays 2 and a plurality of integrated circuits 3 are produced for a plurality of semiconductor devices. The integrated circuit 3 may be produced in a CMOS process, for example. A wiring layer 5 can be applied as usual by an arrangement of structured metal layers with dielectric material in between and with vertical electrical connections formed by plugs, for example. The details of the wiring layer 5 are not relevant to the invention and are therefore omitted.

[0028] Figure 7 is a cross section according to Figure 6 for a later stage of the method and shows the etching of the focusing element. To this end, a mask 14, which may be a resist mask, for instance, is applied to the further main surface 11 opposite the main surface 10. The mask 14 has openings in the regions where the trenches forming the focusing element are to be etched. In Figure 7 the attack of the etching agent is indicated with arrows pointing downwards.

[0029] Figure 8 is a cross section according to Figure 7 after the etching step. When the trenches of the focusing element 4 have reached their final depths, the etching process is stopped and the mask 14 is removed. Then the optional covering layer 16 and/or the optional bump contacts 6 can be applied. The wafer can subsequently be divided into single semiconductor devices, which can be mounted on a board 7 according to Figure 1.

[0030] Figure 9 is a cross section according to Figure 6 for an embodiment according to Figure 2. A cavity 12 is etched into the main surface 10 of the semiconductor substrate 1, and the sensor or sensor array 2 is arranged in the cavity 12.

[0031] Figure 10 is a cross section according to Figure 9 after the application of a cover 8, which can be a rigid cover like a further substrate or wafer, for example. The cover 8 is arranged on or above the main surface 10 and can especially be bonded to the wiring layer 5 by a conventional bonding process, for example. A dedicated bonding layer, which may be an oxide of the semiconductor material, for instance, may be applied between the wiring layer 5 and the cover 8 for this purpose. Figure 10 shows how the cover 8 covers or closes the cavity 12. The cover 8 can be provided with recesses 15 for the accomodation of optional bump contacts.

[0032] Figure 11 is a cross section according to Figure 10 for a later stage of the method and shows the etching of the focusing element. The elements of the cross section of Figure 11 that correspond to elements of the cross section of Figure 10 are designated with the same reference numerals. Figure 11 shows the mask 14 with openings in the regions where the trenches forming the focusing element are to be etched. The attack of the etching agent is indicated with arrows pointing downwards.

[0033] Figure 12 is a cross section according to Figure 11 after the etching step. The mask 14 has been removed. The recesses 15 can be opened by thinning the cover 8 to the level indicated in Figure 12 by the dotted line. This may be performed by grinding the cover 8 back, for example, until the intended thickness is obtained. Bump contacts 6 can be arranged in the opened recesses 15. The wafer is then divided into single semiconductor

devices, which can be mounted on a board 7 according to Figure 2.

[0034] Figure 13 is a cross section according to Figure 9 for the embodiment according to Figure 3. A cavity 12 is etched into the main surface 10 of the semiconductor substrate 1, and the sensor or sensor array 2 is arranged in the cavity 12. In this embodiment it is not necessary to integrate an electronic circuit in the semiconductor substrate 1 for the operation of the sensor or sensor array 2. However, an integrated circuit 3 may be provided in the semiconductor substrate 1 as in the embodiment according to Figure 2 and Figures 9 to 12.

[0035] Figure 14 is a cross section according to Figure 13 after the application of a cover 8, which is provided with the integrated circuit 13 for the operation of the sensor or sensor array 2. The cover 8 is preferably a further substrate or wafer, for example, and the integrated circuit 13 may be arranged opposite the sensor or sensor array 2. The cover 8 can be bonded to the wiring layer 5 by any conventional bonding process, for example. A dedicated bonding layer, which may be an oxide of the semiconductor material, for instance, may be applied between the wiring layer 5 and the cover 8 for this purpose. Figure 14 shows how the cover 8 covers or closes the cavity 12. The cover 8 can be provided with recesses 15 for the accomodation of bump contacts as in the method according to Figures 9 to 12.

[0036] Figure 15 is a cross section according to Figure 14 showing the etching of the focusing element. The elements of the cross section of Figure 15 that correspond to elements of the cross section of Figure 14 are designated with the same reference numerals. Figure 15 shows the mask 14 with openings in the regions where the trenches forming the focusing element are to be etched. The attack of the etching agent is indicated with arrows pointing downwards.

[0037] Figure 16 is a cross section according to Figure 15 after the etching step. The mask 14 has been removed. The recesses 15 can be opened by thinning the cover 8 to the level indicated in Figure 16 by the dotted line as in the method according to Figures 9 to 12. Bump contacts 6 can be arranged in the opened recesses 15. The wafer is then divided into single semiconductor devices, which can be mounted on a board 7 according to Figure 3.

[0038] The described invention allows the fabrication of an integrated focusing element at low cost. It can be employed in many applications to increase the intensity of the radiation impinging on the photosensor and to enhance the performance of the photosensor accordingly.

List of reference numerals

[0039]

1 semiconductor substrate
2 sensor or sensor array
3 integrated circuit
4 focusing element
5 wiring layer
6 bump contact
7 board
8 cover
9 opening
10 main surface
11 further main surface
12 cavity
13 integrated circuit
14 mask
15 recess
16 covering layer

Claims

1. A semiconductor device, comprising:

- a semiconductor substrate (1) with a main surface (10) and a further main surface (11) opposite the main surface (10),
- a sensor or sensor array (2) arranged at the main surface (10),
- an integrated circuit (3, 13) arranged at or above the main surface (10), and
- a focusing element (4) arranged at the further main surface (11),

characterized in that

- the focusing element (4) is formed within the further main surface (11).

2. The semiconductor device of claim 1, wherein the sensor or sensor array (2) is a photosensor or photodetector or an array of photosensors or photodetectors.

3. The semiconductor device of claim 1 or 2, wherein the focusing element (4) is a diffracting element.

4. The semiconductor device of one of claims 1 to 3, wherein the focusing element (4) is a zone plate comprising a set of radially symmetric Fresnel zones.

5. The semiconductor device of claim 4, further comprising: a covering layer (16) on the focusing element (4), the covering layer (16) generating a phase shift zone plate.

6. The semiconductor device of claim 1 or 2, wherein the focusing element (4) is a Fresnel lens.

7. The semiconductor device of one of claims 1 to 6, further comprising:

bump contacts (6) arranged at or above the main

surface (10) of the semiconductor substrate (1).

8. The semiconductor device of one of claims 1 to 7, wherein the integrated circuit (3) is arranged in the semiconductor substrate (1).

9. The semiconductor device of one of claims 1 to 8, further comprising:

a cover (8) arranged at or above the main surface (10), and
openings (9) in the cover (8) being provided for bump contacts (6).

10. The semiconductor device of claim 9, wherein the integrated circuit (13) is arranged in the cover (8).

11. A method of producing a semiconductor device with focusing element, comprising:

- arranging a sensor or sensor array (2) at a main surface (10) of a semiconductor substrate (1), and
- providing an integrated circuit (3, 13) at or above the main surface (10),

characterized in that

- a focusing element (4) is etched in a further main surface (11) of the substrate (1) opposite the main surface (10).

12. The method of claim 11, wherein the focusing element (4) is etched in the shape of a zone plate or Fresnel lens.

13. The method of claim 11 or 12, further comprising:

applying a cover (8) to the main surface (10), before the focusing element (4) is etched.

14. The method of claim 13, wherein the cover (8) is provided with the integrated circuit (13).

15. The method of claim 13 or 14, wherein the cover (8) is provided with openings (9) for bump contacts (6).

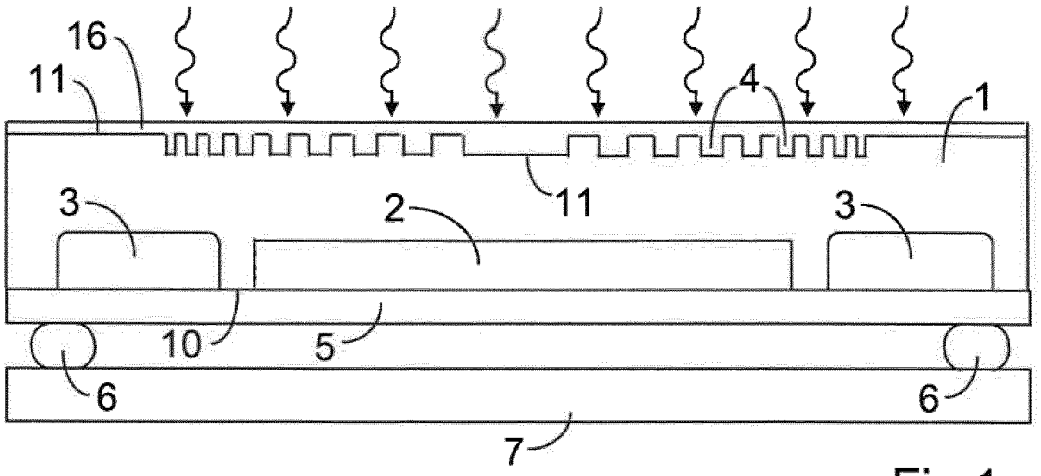

Fig 1

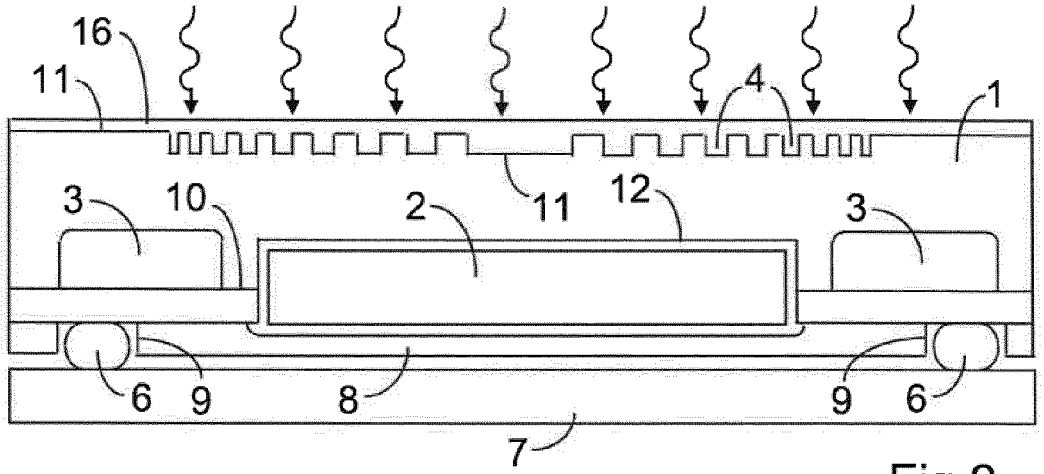

Fig 2

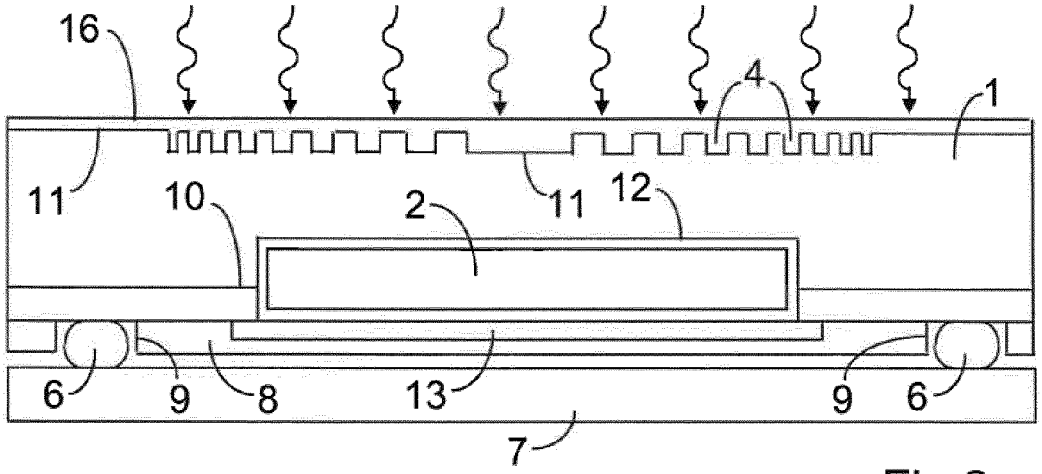

Fig 3

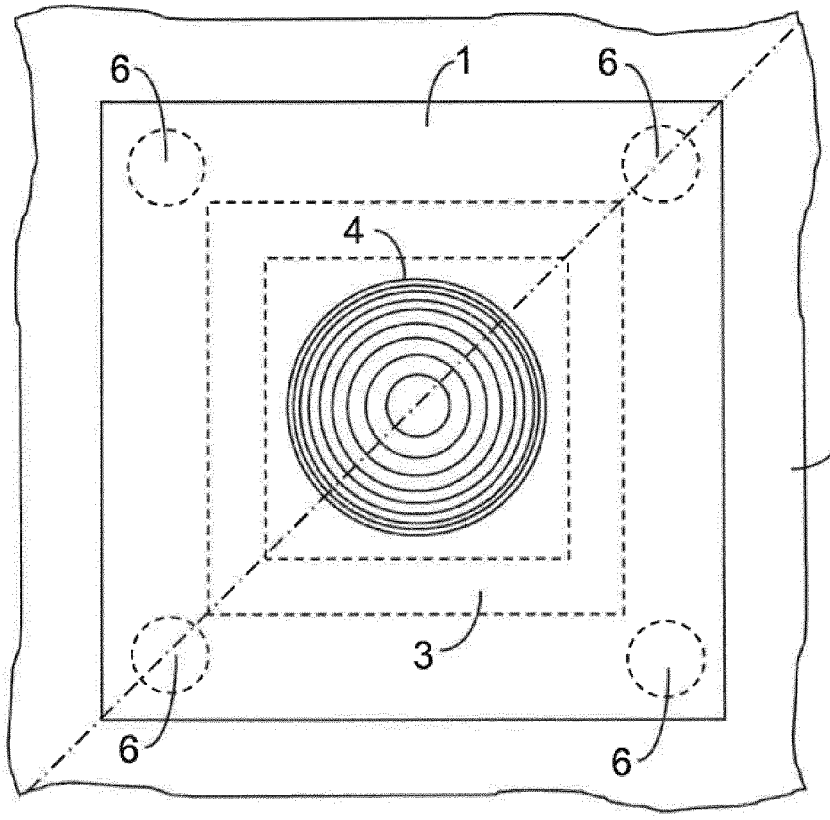

Fig 4

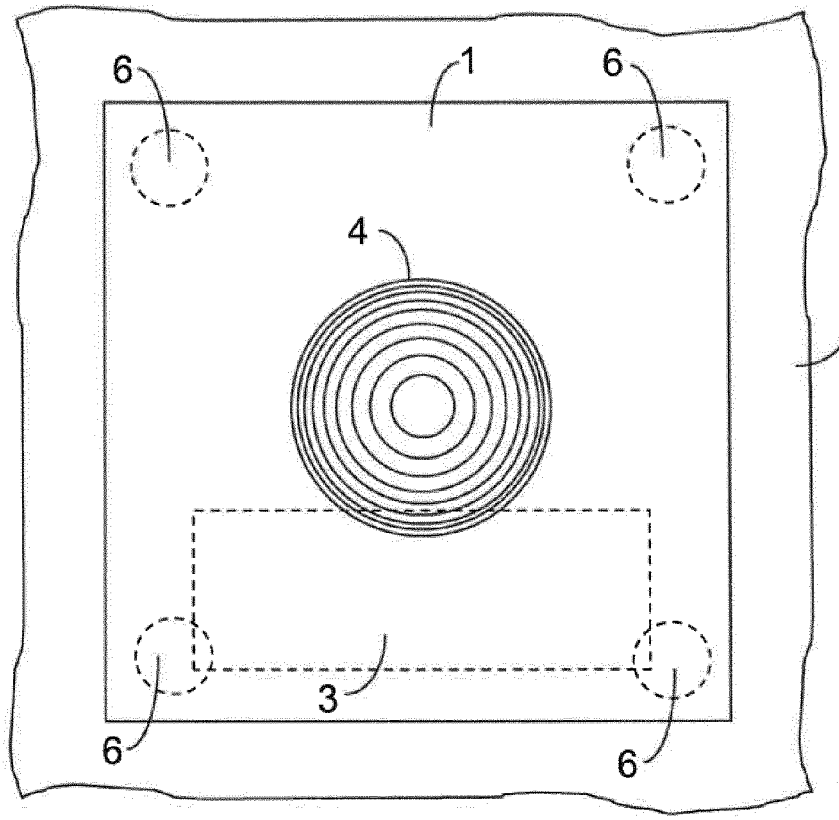

Fig 5

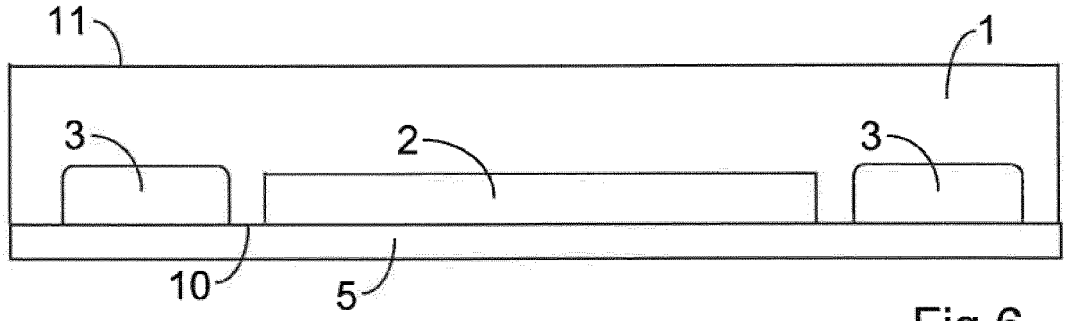

Fig 6

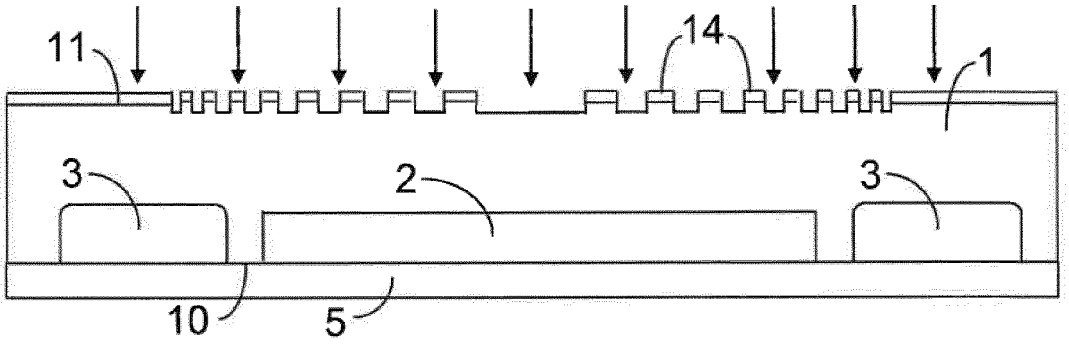

Fig 7

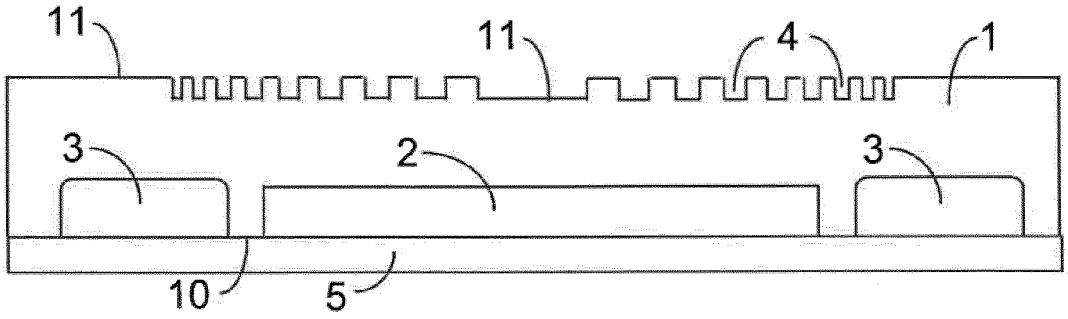

Fig 8

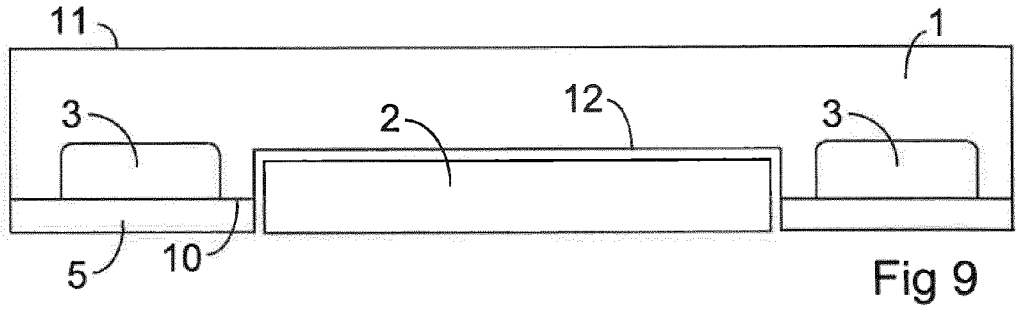

Fig 9

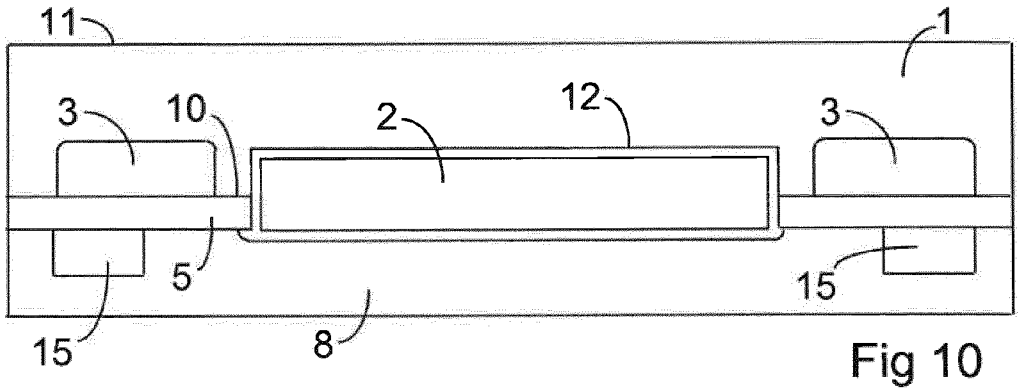

Fig 10

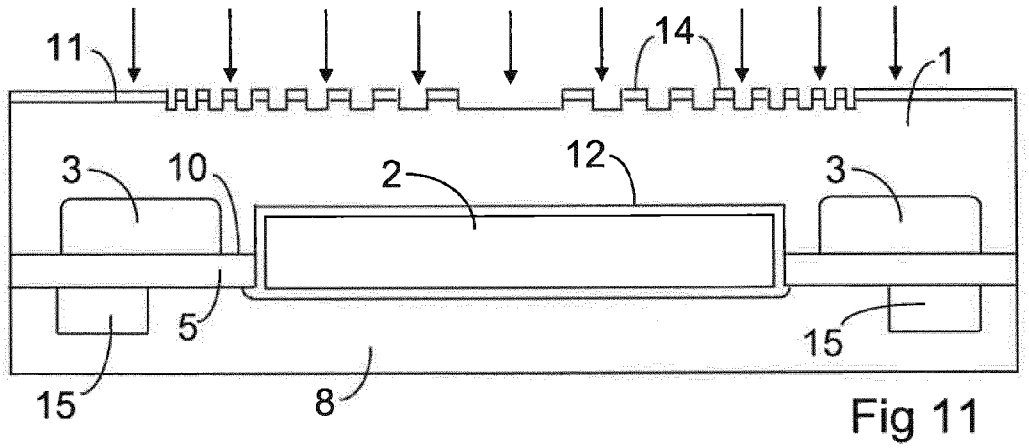

Fig 11

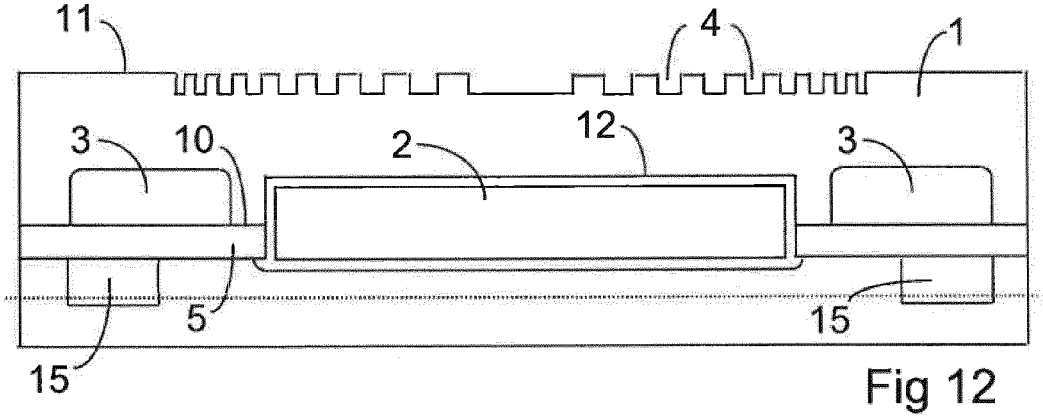

Fig 12

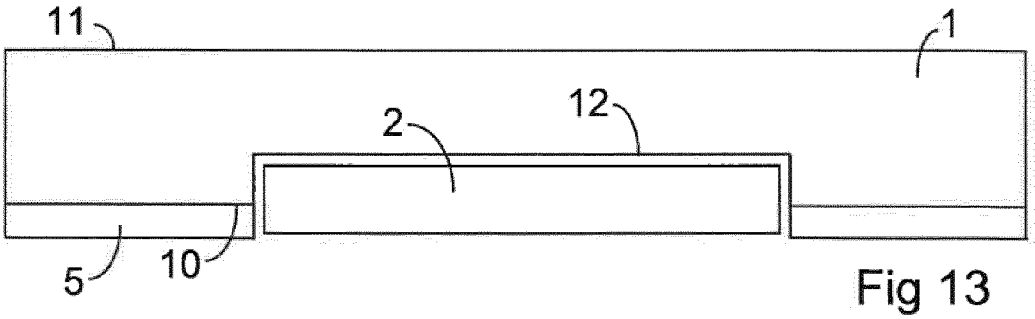

Fig 13

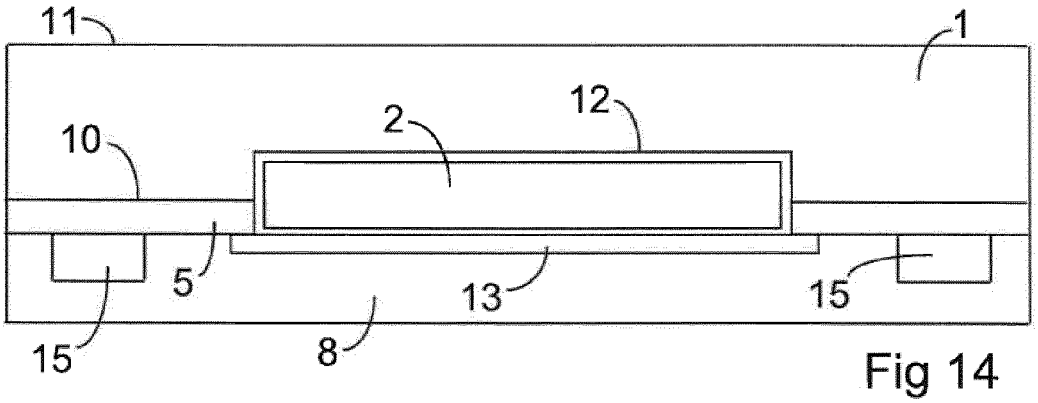

Fig 14

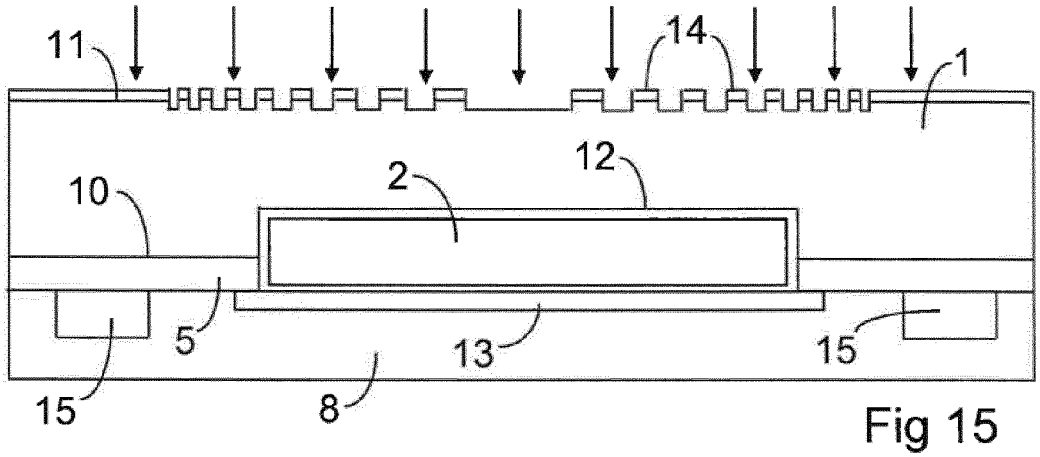

Fig 15

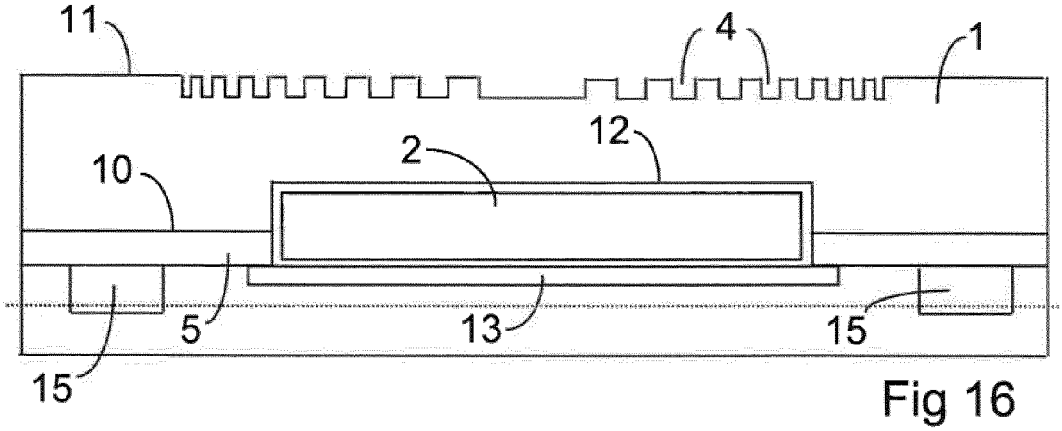

Fig 16

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European Patent Office
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EUROPEAN SEARCH REPORT

Application Number
EP 14 15 5574

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (IPC)
X	US 2013/168791 A1 (OGANESIAN VAGE [US]) 4 July 2013 (2013-07-04) * paragraphs [0014], [0017], [0020]; figures 1A-1G,3D *	1-15	INV. H01L27/146
X	US 2013/134535 A1 (LENCHENKOV VICTOR [US]) 30 May 2013 (2013-05-30) * paragraphs [0022] - [0025], [0035]; figure 3 *	1,2,6-8, 11,12	
A	US 2008/011937 A1 (TOSHIKIYO KIMIAKI [JP]) 17 January 2008 (2008-01-17) * the whole document *	1-15	
A	US 2008/261346 A1 (YANG WEN-KUN [TW] ET AL) 23 October 2008 (2008-10-23) * figures 1,2,6 *	1-15	

TECHNICAL FIELDS SEARCHED (IPC)
H01L

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
The Hague	3 April 2014	Cabrita, Ana

CATEGORY OF CITED DOCUMENTS

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EPO FORM 1503 03.82 (P04C01)

ANNEX TO THE EUROPEAN SEARCH REPORT ON EUROPEAN PATENT APPLICATION NO. EP 14 15 5574

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03-04-2014

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