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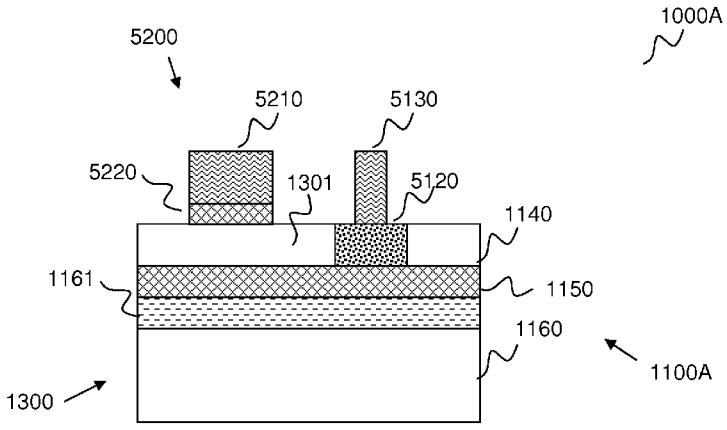
(54) Title: ANTIFUSE

Fig. 1A



(57) Abstract: The present invention relates to a semiconductor structure (1000A), comprising: a first semiconductor layer (1140); and a first program transistor (5200) and a first select transistor (1300) implementing a first antifuse cell (1000A), wherein the first semiconductor layers acts as the body (1301) of the first program transistor and as the body (1301) of the first select transistor; wherein a gate (5210) of the first program transistor and a gate (1160, 1161) of the first select transistor are on different sides of the first semiconductor layer.

Antifuse

The present invention relates to the field of electronics and in particular to the field of semiconductors. More specifically, it relates to the field of antifuses. Even more specifically, the present invention relates to a semiconductor structure, comprising a first semiconductor layer; and a first program transistor and a first select transistor implementing a first antifuse cell, wherein the first semiconductor layers acts as the body of the first program transistor and as the body of the first select transistor.

Antifuse cells are popular in the field of semiconductors, where they are often used as an implementation of a one-time programmable cell. For instance, they can be used for purposes such as recording of secret codes, production numbers, etc. In particular, an antifuse cell is a structure which can be used to record a digital value, such as 0 or 1, by creating, or not, an electrical connection between two electrodes. More specifically, by applying a high voltage between the two electrodes, a layer of insulator is broken and connection between the electrodes is achieved. Antifuse cells are therefore typically write-once memories.

Figure 5A illustrates an antifuse cell 5000A in accordance with the state of the art. Such cell is described, for instance, in non-patent literature “Comparison of embedded non-volatile memory technologies and their applications”, Linh Hong, Kilopass (retrieved from the internet at the address www.kilopass.com).

More specifically, the antifuse cell 5000A comprises a semiconductor substrate 5100 on which two transistors 5200, 5300 are realized: a program transistor 5200 comprising gate 5210 and gate oxide 5220, and a select transistor 5300 comprising gate 5310 and gate oxide 5320. The two transistors 5200 and 5300 are connected in series via a first connection region 5110. The other end of select transistor 5300 is connected to a second connection region 5120 which is then connected to a connection 5130.

The programming of the antifuse cell 5000A is carried out in the following manner Contact 5130 is at a positive voltage and transistor 5300 is in on state. When a high voltage is applied on the program transistor 5200, the oxide 5220 below the gate 5210 will break and a permanent electrical connection will be realized between the gate 5210 and the first connection region 5110. In this manner, if the high voltage is applied, a digital value of, for instance, 1, is recorded. Conversely, if the high voltage is not applied, a digital value of, for instance, 0, is recorded.

The reading of the antifuse cell 5000A is carried out by opening the select transistor 5300 with the application of the required voltage on its gate 5310. In this manner, the first connection region 5110 is connected to the second connection region 5120 and to the connection 5130. Therefore, by applying a voltage between the gate 5210 and the connection 5130, it is possible to detect the value stored in the antifuse cell 5000. In particular, with reference to the example above, if a current is flowing between the gate 5210 and the connection 5130 then a digital value of 1 is read. If no current is flowing then a digital value of 0 is read.

This implementation requires the usage of two transistors next to each other, as well as the presence of several connection regions, which take up a considerable area on the semiconductor substrate 5100.

Figure 5B illustrates an alternative antifuse cell 5000B in accordance with the state of the art.

Antifuse cell 5000B is advantageous over antifuse cell 5000A in that it doesn't require a first connection region 5110. More specifically, semiconductor substrate 5100B comprises only one connection region, namely second connection region 5120. This is achieved by realizing transistors 5200 and 5300 next to each other, such that they do not need a connection region in between.

However, such arrangement means that the high voltage used during the programming phase will be applied both to the gate 5210 and 5310. This would result in the oxide below the select transistor 5300 to be damaged too. In order to solve this problem, the select transistor 5300 is replaced by select transistor 5300B which is provided with a gate oxide 5320B thicker than the gate oxide 5220 of the program transistor 5200.

While this solution reduces the area by eliminating the need for first connection region 5110, it requires the usage of two different gate oxide thicknesses. This usually results in the problem that the select transistor 5300B, having the thicker gate oxide, cannot be realized with the minimum feature pitch, thereby resulting bigger than select transistor 5300, which increases again the area used by antifuse cell 5000. Additionally, the presence of two different gate oxides requires one additional mask as well as some manufacturing step, increasing costs.

The present invention has been realized with the aim of solving the above-mentioned problems.

In particular the present invention can relate to a semiconductor structure, comprising: a first semiconductor layer; and a first program transistor and a first select transistor implementing a first antifuse cell, wherein the first semiconductor layers acts as the body of the first program

transistor and as the body the first select transistor; wherein a gate of the first program transistor and a gate of the first select transistor are on different sides of the first semiconductor layer.

Thanks to such approach, it is possible to place the program transistor in series with the select transistor without a first connection region 5110, such as in Figure 5A, and without the usage of two oxide thicknesses such as in Figure 5B.

In some embodiments, the semiconductor structure can be a multi-gate semiconductor structure, and the gate of the first program transistor and the gate of the first select transistor are respectively one a back-gate and one a top-gate, or viceversa, of the multi-gate semiconductor structure.

Thanks to such approach, the realization of the semiconductor structure can be carried out with standard technology such as SOI, Finfets, etc.

In some embodiments, the semiconductor structure can further comprise at least one second program transistor implementing a second antifuse cell in combination with the first select transistor, wherein the first program transistor is connected in parallel with the at least one second program transistor.

Thanks to such approach, two antifuse cells can share a single select transistor and a single connection to both program transistors, thereby reducing the number of contacts necessary to operate the structure.

In some embodiments, the semiconductor structure can further comprise at least one third program transistor implementing a third antifuse cell in combination with the first select transistor, wherein the first program transistor is connected in series with the at least one third program transistor.

Thanks to such approach, it is possible to place the third and first program transistors next to each other, instead of separating them via a shared common output connection. This is advantageous since manufacturing design rules may allow a narrower pitch of the structure comprising two program transistors next to a connection, rather than a program transistor followed by a connection and a subsequent program transistor.

In some embodiments, the gate and gate oxide of any of the program transistors can be shaped such that the electric field of the gate is concentrated on a point or a line of the gate oxide.

Thanks to such approach, a lower programming voltage can be used in order to break the gate oxide.

In some embodiments, the first semiconductor layer comprises an etched region, the gate oxide can be placed on the first semiconductor layer and at least on a portion of the wall of the etched region, and the gate can be placed on the gate oxide, so as to realize an angle in correspondence of the etched region.

Thanks to such approach, it is possible to realize the shape of the gate and gate oxide such that the electric field of the gate is concentrated on a point of the gate oxide in a simple and effective manner.

The invention will be described in more detail by way of example hereinafter using advantageous embodiments and with reference to the drawings. The described embodiments are only possible configurations in which the individual features may however, as described above, be implemented independently of each other or may be omitted. Equal elements illustrated in the drawings are provided with equal reference signs. Parts of the description relating to equal elements illustrated in the different drawings may be left out. In the drawings

- Figure 1A schematically illustrates an antifuse cell 1000A in accordance with an embodiment of the present invention;
- Figure 1B schematically illustrates an antifuse cell 1000B in accordance with an embodiment of the present invention;
- Figures 2A and 2B schematically illustrate a NOR antifuse cells arrangement 2000 in accordance with an embodiment of the present invention;
- Figures 3A and 3B schematically illustrate a NAND antifuse cells arrangement 3000 in accordance with an embodiment of the present invention;
- Figures 4A and 4B schematically illustrate a further NAND antifuse cells arrangement 4000 in accordance with an embodiment of the present invention; and
- Figures 5A and 5B schematically illustrate antifuse cells in accordance with the state of the art.

A first embodiment of the invention will now be described with reference to he vertical cut view of Figure 1A.

The antifuse cell 1000A mainly differs from the antifuse cell 5000A due to the fact that the select transistor 5300 is not realized on the same surface of the semiconductor substrate as the program transistor 5200. On the other hand, a select transistor 1300 of antifuse cell 1000A is realized on the opposite side of the semiconductor substrate 1100A.

In particular, semiconductor substrate 1100A comprises a first semiconductor layer 1140, for instance Silicon, a bulk semiconductor layer 1160, for instance Silicon, and an insulating layer 1150, for instance Silicon oxide, in between. In some embodiment, the bulk semiconductor layer 1160 can be made conductive, while in some embodiments only a part 1161 of bulk semiconductor layer 1160 can be doped so as to be conductive. The semiconductor substrate 1100A may e.g. be obtained by a SmartCut® process. More specifically, this implies providing the semiconductor structure by forming a first intermediate insulating layer above the bulk semiconductor layer 1160; forming a second intermediate insulation layer above a second semiconductor substrate; bonding the first and the second intermediate insulation layers, thereby obtaining the insulating layer 1150, within a wafer transfer process and removing part of the second semiconductor substrate, thereby obtaining the first semiconductor layer 1140.

Thanks to such arrangement, it is possible to realize select transistor 1300 by using the bulk semiconductor 1160 as gate, the insulating layer 1150 as gate oxide and the first semiconductor layer 1140 as body 1301. In particular, the body 1301 can be easily realized by leaving a space between the body of the program transistor 5200 and the connection region 5120. In this manner, the lateral dimensions of the antifuse cell 1000A can be reduced when compared to the state of the art antifuse cells 5000A and 5000B.

Although this embodiment the gates/transistors are placed on “opposite side”, the invention is not limited thereto and can more generally be implemented as long as the gates/transistors are “not on the same side” of the common body they share. For instance, as illustrated in Figure 1A, gate 5210 can be on an upper surface of the first semiconductor layer 1140 while gate 1160, or 1161, can be on a lower surface of the first semiconductor layer 1140. A similar approach though could be realized in a technology employing vertical gates, one being placed on the right side of a semiconductor layer acting as a body and one being placed on the left side of the same semiconductor layer. Even more generally, although not illustrated in the Figures, the two transistors could be realized on different sides of the first semiconductor layer 1140, not necessarily opposite to each other. For instance gate 5210 can be on an upper surface of the first semiconductor layer 1140, as illustrated in Figure 1A, while gate 1160, or 1161, can be on a surface of the first semiconductor layer 1140 parallel to the cutting plane along which Figure 1A

is taken, or perpendicular to this plane and perpendicular as well to the plane of gate 5210. In other words, a gate could be on a horizontal surface of the first semiconductor layer 1140 while the other gate could be on a vertical surface of the first semiconductor layer 1140. All these approaches are advantageous, since they combine the two transistors on different sides of the first semiconductor layer 1140, such that the area they occupy on the wafer is reduced, compared to the case in which the two transistors are on the same side of the first semiconductor layer 1140.

Figure 1B schematically illustrates cut view of a further embodiment of the present invention. In particular, Figure 1B illustrates an antifuse cell 1000B based on the antifuse cell 1000A of Figure 1A in which the first semiconductor layer 1140B is etched in a region R1 such that the gate oxide 1220B and the gate 1210B of program transistor 1200B have an angle in correspondence with region R1. This locally increases, in correspondence with the angle, the electric field generated by applying a voltage on the gate 1210B, which makes it easier to break the gate oxide 1220B, thereby resulting in the application of a lower voltage requirements during the programming of antifuse cell 1000B compared to the programming of antifuse cell 1000A.

Although the illustrated embodiment provides a 90° angle, the present invention is not limited thereto and any arrangement that increases the electric field in a certain region of the gate oxide 1120B can be used instead. Additionally, although the embodiment illustrates both the gate oxide and the gate reaching the insulating layer 1150, the present invention is not limited thereto. Alternatively, or in addition, the gate can be shaped so as to only reach an intermediate depth of the first semiconductor layer 1140B.

Figure 2A schematically illustrates a vertical cut view of a physical implementation of a NOR antifuse cells arrangement in accordance with an embodiment of the present invention. Figure 2B illustrates the corresponding electrical scheme.

More specifically, the NOR antifuse cells arrangement 2000 comprises two program transistors 5201 and 5202 and one select transistor 1300. The two program transistors are connected each to one side of connection region 5120. Accordingly, when a voltage is applied on the gate of select transistor 1300, corresponding to the bulk semiconductor layer 1160, so as to make the transistor conducting, current can flow to the connection 5130 via the first program transistor 5201 and/or via the second program transistor 5202, depending on how each of the two program transistors has been programmed. Therefore, the resulting functionality of the structure is a NOR function of the programming of the two program transistors 5201 and 5202. This provides the advantage that only one select transistor can be used for two program transistors.

Figure 3A schematically illustrates a cut view of a physical implementation of a NAND antifuse cells arrangement in accordance with an embodiment of the present invention. Figure 3B illustrates the corresponding electrical scheme.

More specifically, the NAND antifuse cell arrangement 3000 comprises two program transistors 5203 and 5204 and one select transistor 1300. The two program transistors are placed next to each other and connected in series while the other end of program transistor 5204 is connected to second connection region 5120. Accordingly, when a voltage is applied on the gate of select transistor 1300, corresponding to the bulk semiconductor layer 1160, so as to make the transistor conducting, current can flow to the connection 5130 via the first program transistor 5201 and/or via the second program transistor 5202, depending on how each of the two program transistors has been programmed. Therefore, the resulting functionality of the structure is a NAND function of the programming of the two program transistors 5201 and 5202. In particular, any number program transistor is possible. These transistors are in series to the contact 5130.

In an exemplary programming method, select transistor 1300 is conducting, so an inversion layer is created in the layer 1301. Gate 5204 is floating and gate 5203 is at a high voltage. Due to the inversion layer, a high electric field is present between regions 5203 and 1301. In the area below gate 5203 the break of oxide 5220 will occur. During a first reading operation, select transistor 1300 is selected on, gate 5204 is floating and gate 5203 is at an on voltage. So a current flows from 5203 to 5130 via the inversion layer. During a second reading operation, select transistor 1300 is selected on, gate 5203 is floating. On gate 5204 an on voltage is applied. Since the gate oxide 5220 was not broken, no current flows from 5204 to 5130.

Although this embodiment has been illustrated with only two program transistors 5203 and 5204, the present invention is not limited thereto. Alternatively, or in addition, several other program transistors could be realized, all connected in series to program transistors 5203 and 5204. Still alternatively, or in addition, in all embodiments, several other program transistors could be realized in planes crossing the plane of the cut view of Figure 3A. For instance, in a perpendicular plane to the one of Figure 3A, one or two additional program transistors could be connected in a manner similar to what illustrated in Figure 3A. In all of those cases, a single select transistor may be used for some or all of the program transistors.

This is advantageous compared to the state of the art antifuse, where a series array could not be used, as each storage element needed an own select transistor. Additionally, since any number

of transistors can be placed in series, the NAND arrangement for a larger number of transistor consumes less area than the NOR arrangement.

Figures 4A and 4B illustrate a further antifuse cells arrangement 4000 in accordance with an embodiment of the present invention. In particular, while in the previous embodiments the cut view were taken along direction A-A' of Figure 4A, Figure 4B is a cut view of Figure 4A taken along direction B-B'.

More specifically, in Figures 4A and 4B, antifuse cells arrangement 4000 comprises six program transistor 1201B-1206B and two select transistors 1310-1320, separated by trench insulation lines 4500. Program transistors 1201B-1203B are associated, i.e. overlapping with, select transistor 1310. Program transistors 1204B-1206B are associated, i.e. overlapping with, select transistor 1320. As can be seen in the figure, the antifuse cell can be organized in such a manner that vertical adjacent program transistors, i.e. 1201B and 1204B are separated by a trench insulation 4400. This provides the beneficial advantage that a single select transistor 1310 can be used for a plurality of program transistors.

In this specific embodiment, the programming could be done by applying a high voltage on a given gate, i.e. 1210B, and a lower voltage on connection 5130. If the silicon 1301 has an inversion layer which also is connected to connection 5130 to a fixed voltage, the high voltage difference will break the gate oxide 1220B of program transistor 1201B. Similarly, by applying a high voltage on gate 1211B, and a lower voltage on connection 5131 while program transistor 1302 is conducting, the voltage difference will break the gate oxide 1220B of program transistor 1205B.

While only two rows are here illustrated, it will be clear to those skilled in the art that several rows can be implemented.

Moreover, the embodiment of Figures 4A and 4B could be realized also with some of the program transistors being the program transistors 1200B described by the embodiment of Figure 1B and some of the program transistors being the program transistors 5200 described by the embodiment of Figure 1A. Still further, the parallel placement of rows of program transistors 1201B-1203B and 1204B-1206B could be similar also if some or all of the rows are arranged in a NAND arrangement 3000 according to the embodiment of Figure 3A and 3B or arranged in a NOR arrangement 2000 according to the embodiment of Figure 2A and 2B.

More generally, although the embodiments of Figures 2A and 3A have been illustrated as being realized with a programming transistor 5200, the present invention is not limited thereto. Alternatively or in addition, they can also be implemented with one or more programming transistor 1200B.

Further, although the embodiments described above have been illustrated with the gate of the select transistor being realized by the entire bulk semiconductor layer 1160, the present invention is not limited thereto. In particular, the bulk semiconductor layer could be structures in such a manner so as to realize a plurality of independent gates, for a plurality of select transistors, each overlapping with one or more program transistors.

Additionally, although the embodiments have been illustrated with reference to a silicon on insulator structure, the present invention can be realized with any technology that allows the realization of a first transistor gate on one side of a semiconductor layer, acting as body, and of a second transistor gate on a second side of the semiconductor layer, in particular on the side opposite to the one on which the first gate is realized.

Additionally, although the embodiment have been illustrated with the select transistor being realized as a “back-gate transistor” with the insulting layer 1150 and the bulk semiconductor layer 1160, while the program transistor is realized as a “top-gate transistor” with a gate 5210 and a gate oxide 5220, the present invention is not limited thereto. Alternatively, or in addition, the two transistors could be switched. That is, the program transistor could be realized as a “back-gate transistor” with the insulting layer 1150 and the bulk semiconductor layer 1160, while the select transistor could be realized as a “top-gate transistor” with a gate 5210 and a gate oxide 5220.

Claims

1. A semiconductor structure (1000-4000), comprising:

   a first semiconductor layer (1140, 1140B); and

   a first program transistor (5200, 1200B) and a first select transistor (1300) implementing a first antifuse cell (1000A, 1000B), wherein the first semiconductor layer acts as the body (1301) of the first program transistor and as the body (1301) of the first select transistor;

   characterized in that

   a gate (5210, 1210B) of the first program transistor and a gate (1160, 1161) of the first select transistor are on different sides of the first semiconductor layer.

2. The semiconductor structure according to claim 1 wherein

   the semiconductor structure is a multi-gate semiconductor structure, and

   the gate of the first program transistor and the gate of the first select transistor are respectively one a back-gate and one a top-gate, or viceversa, of the multi-gate semiconductor structure.

3. The semiconductor structure according to any previous claim further comprising

   at least one second program transistor (5202) implementing a second antifuse cell in combination with the first select transistor, wherein

   the first program transistor (5201) is connected in parallel with the at least one second program transistor.

4. The semiconductor structure according to any previous claim further comprising

   at least one third program transistor (5204) implementing a third antifuse cell in combination with the first select transistor, wherein

   the first program transistor (5201) is connected in series with the at least one third program transistor.

5. The semiconductor structure according to any previous claim wherein

the gate and gate oxide of any of the program transistors are shaped such that the electric field of the gate is concentrated on a point (R1) or a line of the gate oxide.

6. The semiconductor structure according to claim 5 wherein

the first semiconductor layer comprises an etched region,

the gate oxide is placed on the first semiconductor layer and at least on a portion (R1) of the wall of the etched region, and

the gate is placed on the gate oxide, so as to realize an angle in correspondence of the etched region.

Fig. 1A

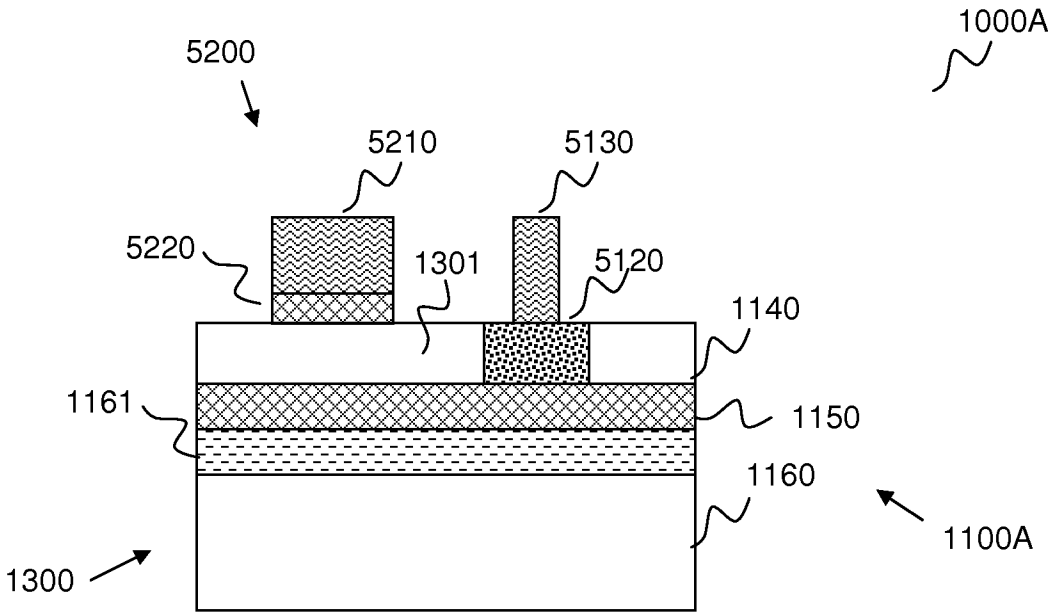

1000A
5200
5210
5130
5220
1301
5120
1140
1161
1150
1160
1100A
1300

Fig. 1B

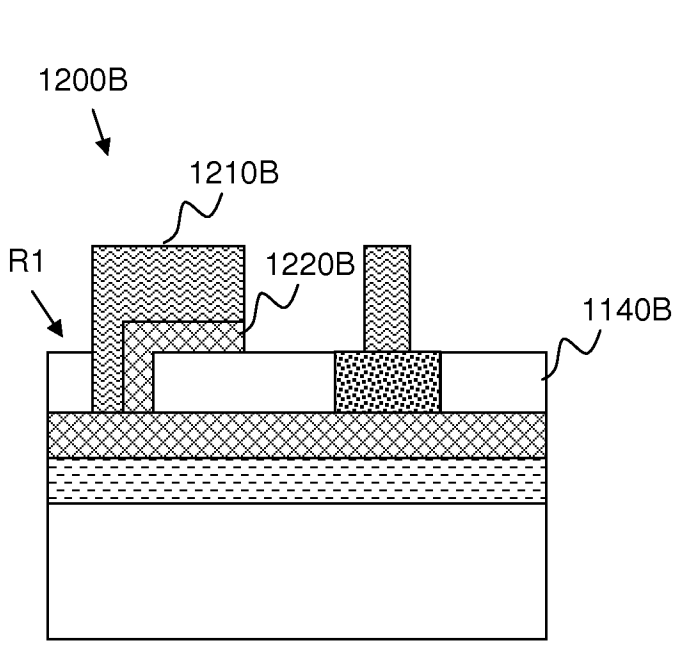

1000B
1200B
1210B
R1
1220B
1140B

Fig. 2A

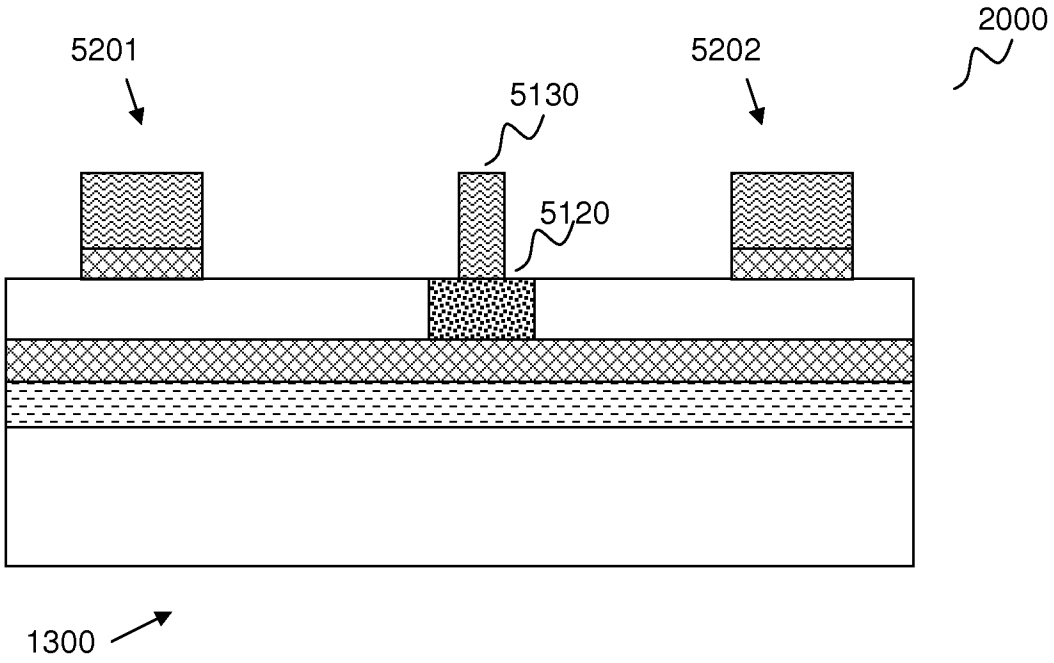


Fig. 2B

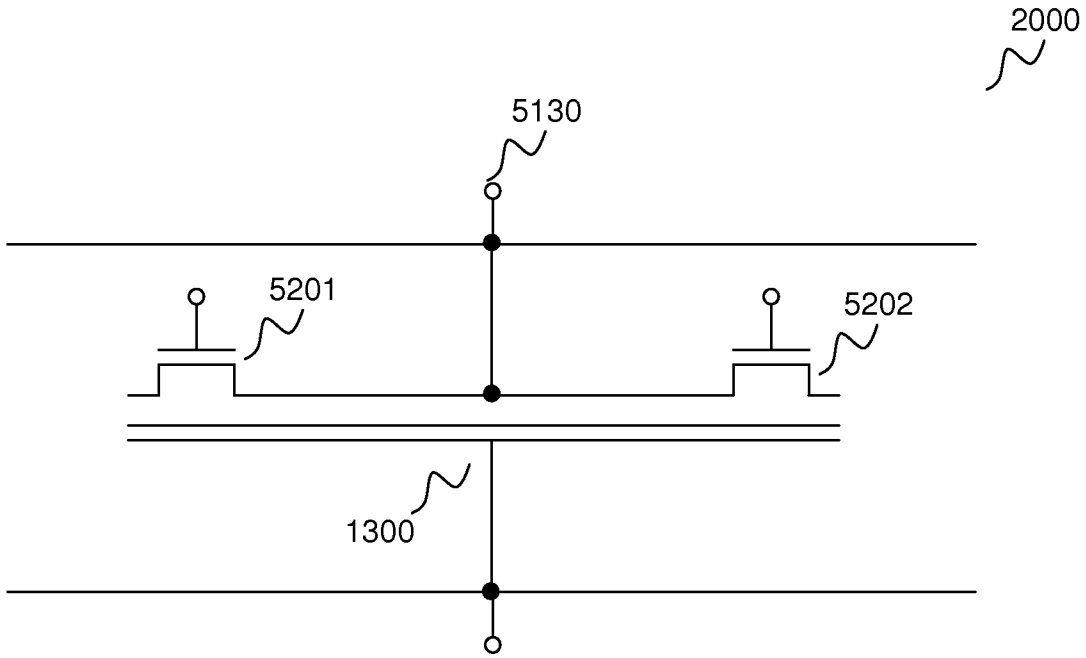


Fig. 3A

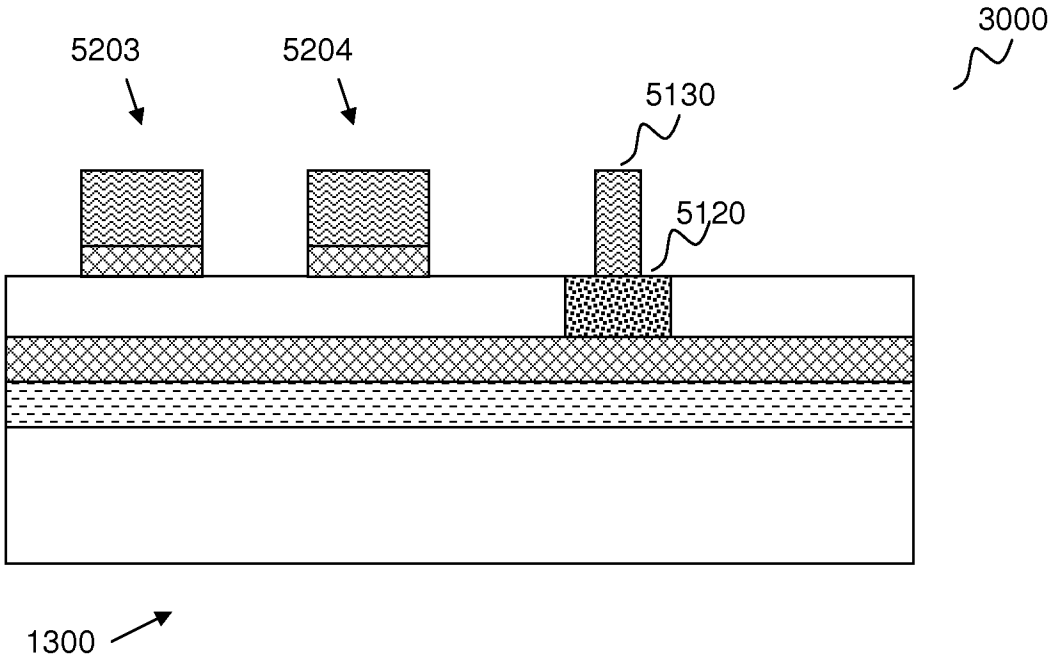


Fig. 3B

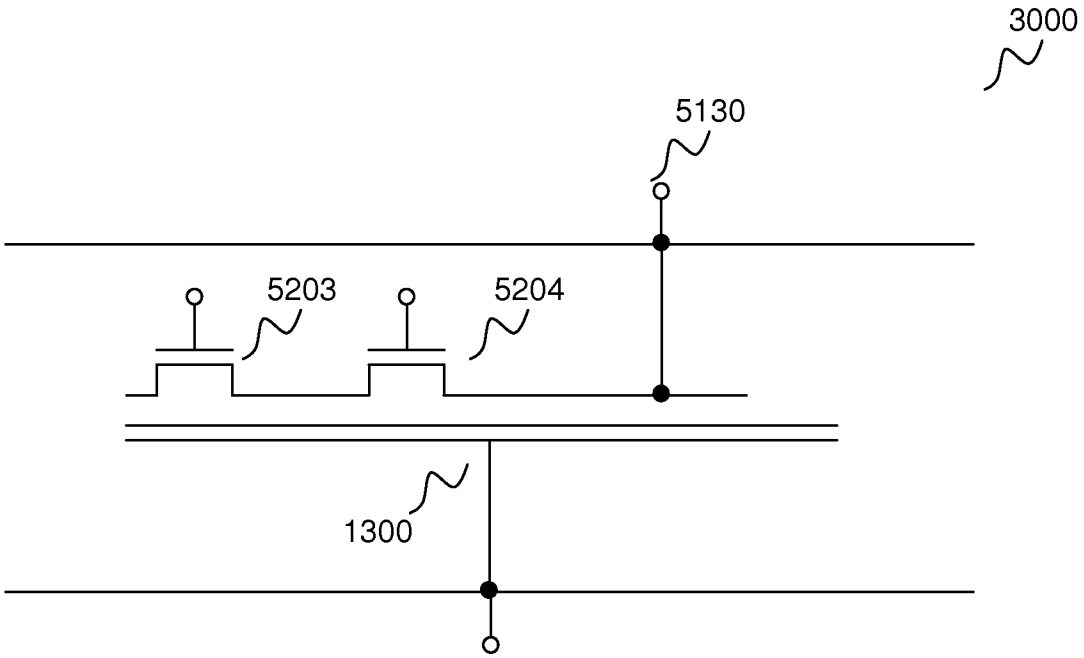


Fig. 4A

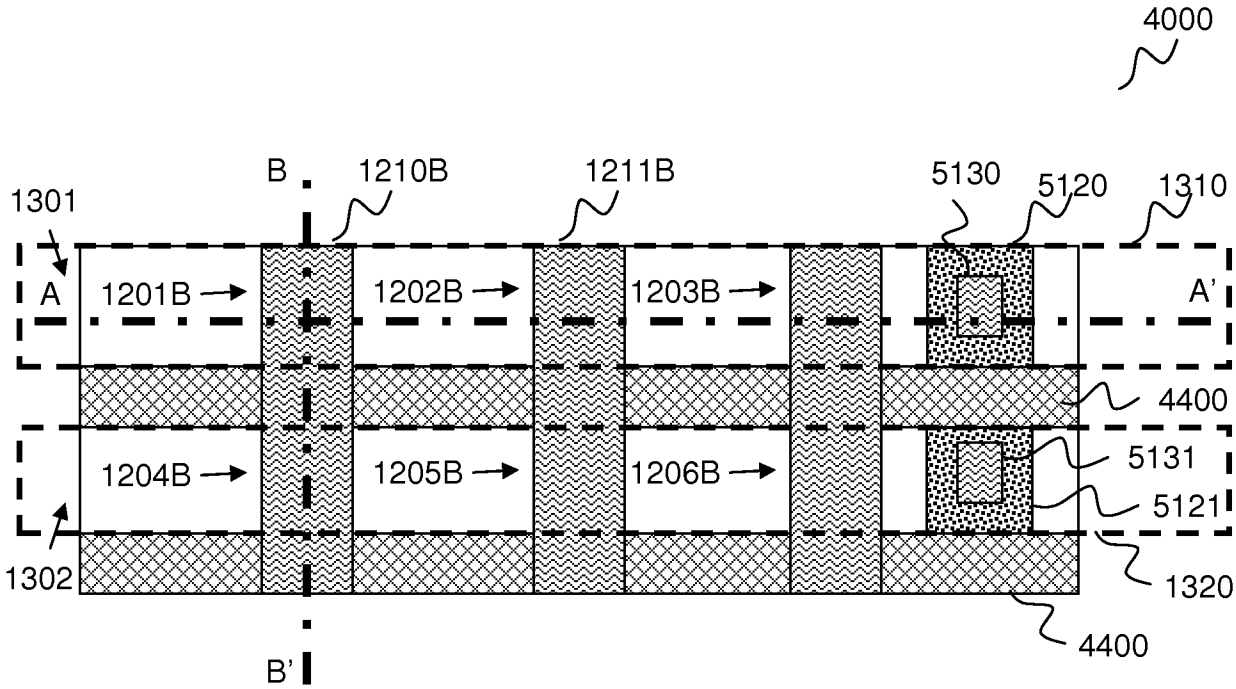

4000
B
1210B
1211B
5130
5120
1310
1301
A
1201B
1202B
1203B
A'
4400
1204B
1205B
1206B
5131
5121
1302
1320
4400
B'

Fig. 4B

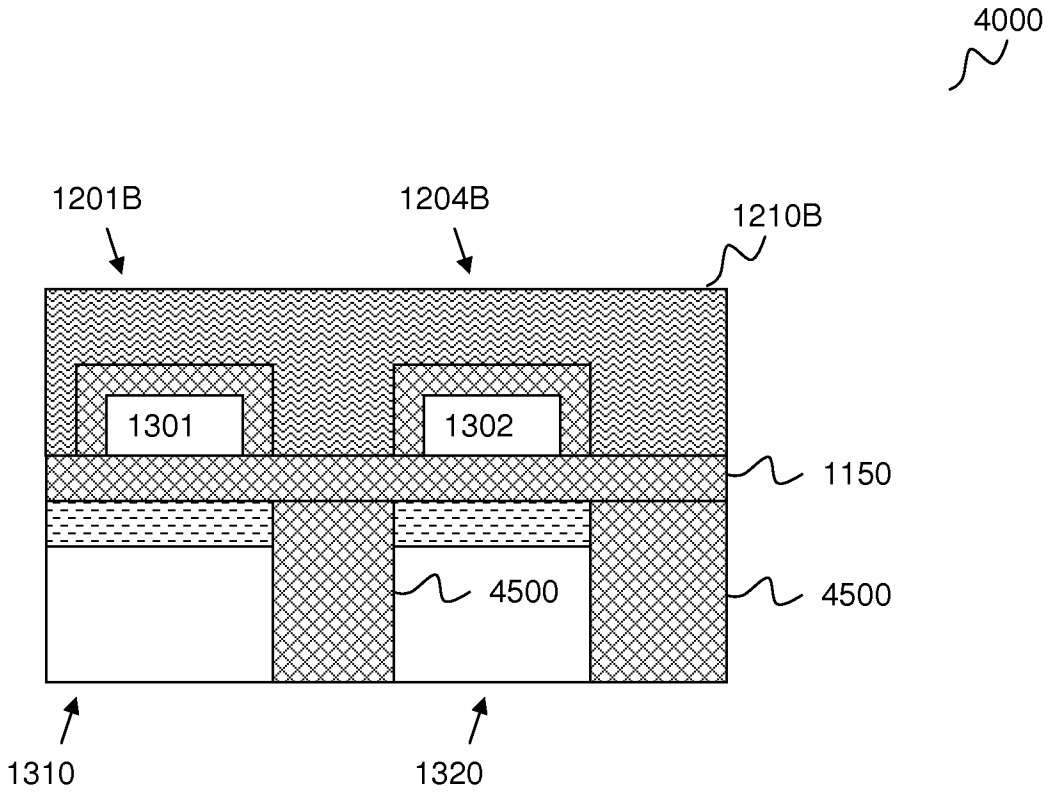

4000
1201B
1204B
1210B
1301
1302
1150
4500
4500
1310
1320

Fig. 5A

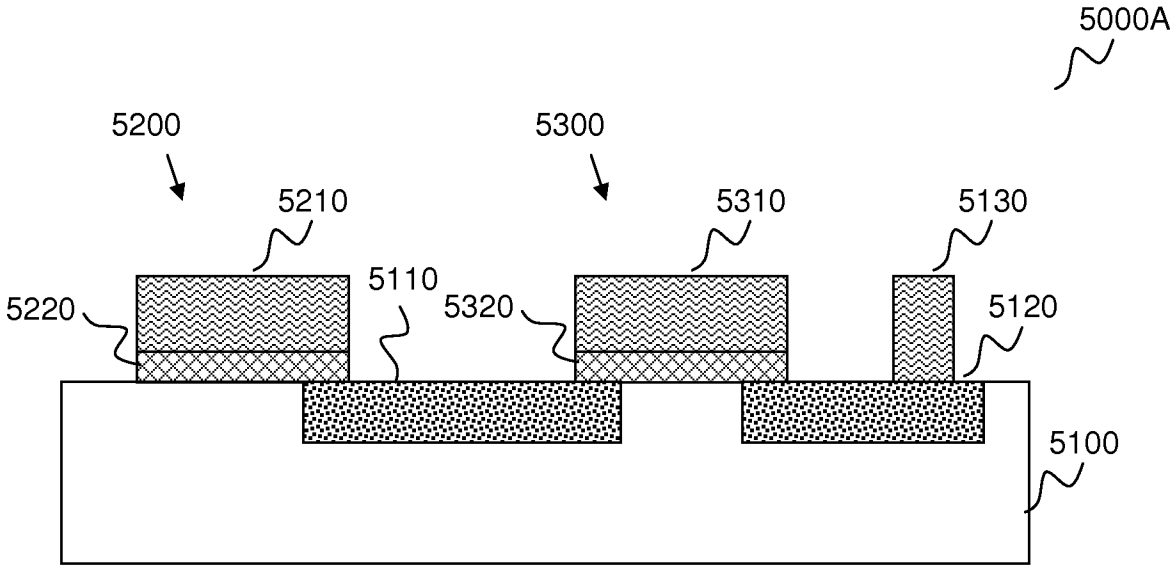
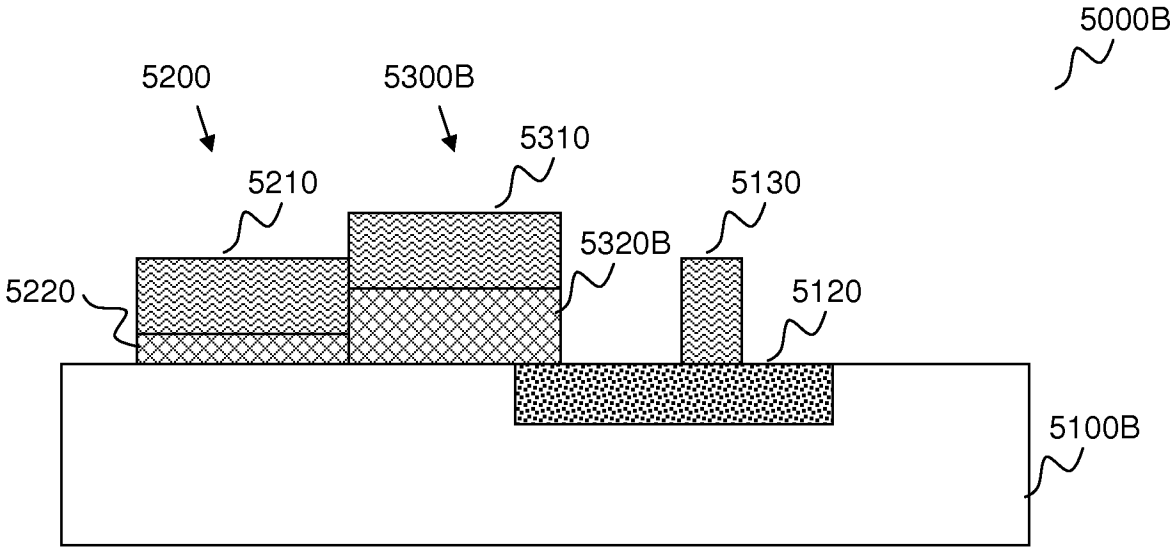

5000A
5200
5300
5210
5310
5130
5110
5220
5320
5120
5100

Fig. 5B


5000B
5200
5300B
5310
5210
5130
5320B
5220
5120
5100B

INTERNATIONAL SEARCH REPORT

International application No
PCT/EP2013/064138

A. CLASSIFICATION OF SUBJECT MATTER
INV. H01L27/10 H01L23/525 H01L27/12 G11C17/16 H01L27/112
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L G11C

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
EPO-Internal, INSPEC, IBM-TDB, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2006/234428 A1 (FURUKAWA TOSHIHARU [US] ET AL) 19 October 2006 (2006-10-19)	1,2,4,5
Y	abstract; claims; figure 15	3,6
Y	EP 1 389 782 A1 (ST MICROELECTRONICS SA [FR]) 18 February 2004 (2004-02-18) abstract; claims; figures 1,6	3
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[X] Further documents are listed in the continuation of Box C.

[X] See patent family annex.

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Date of the actual completion of the international search	Date of mailing of the international search report
15 July 2013	23/07/2013

Name and mailing address of the ISA/	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Fax: (+31-70) 340-3016	Wirner, Christoph

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INTERNATIONAL SEARCH REPORT

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