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(51) Int.Cl.⁶ H03L 7/08, H03M 1/66, H03L 7/18, H03L 7/089, H03L 7/085

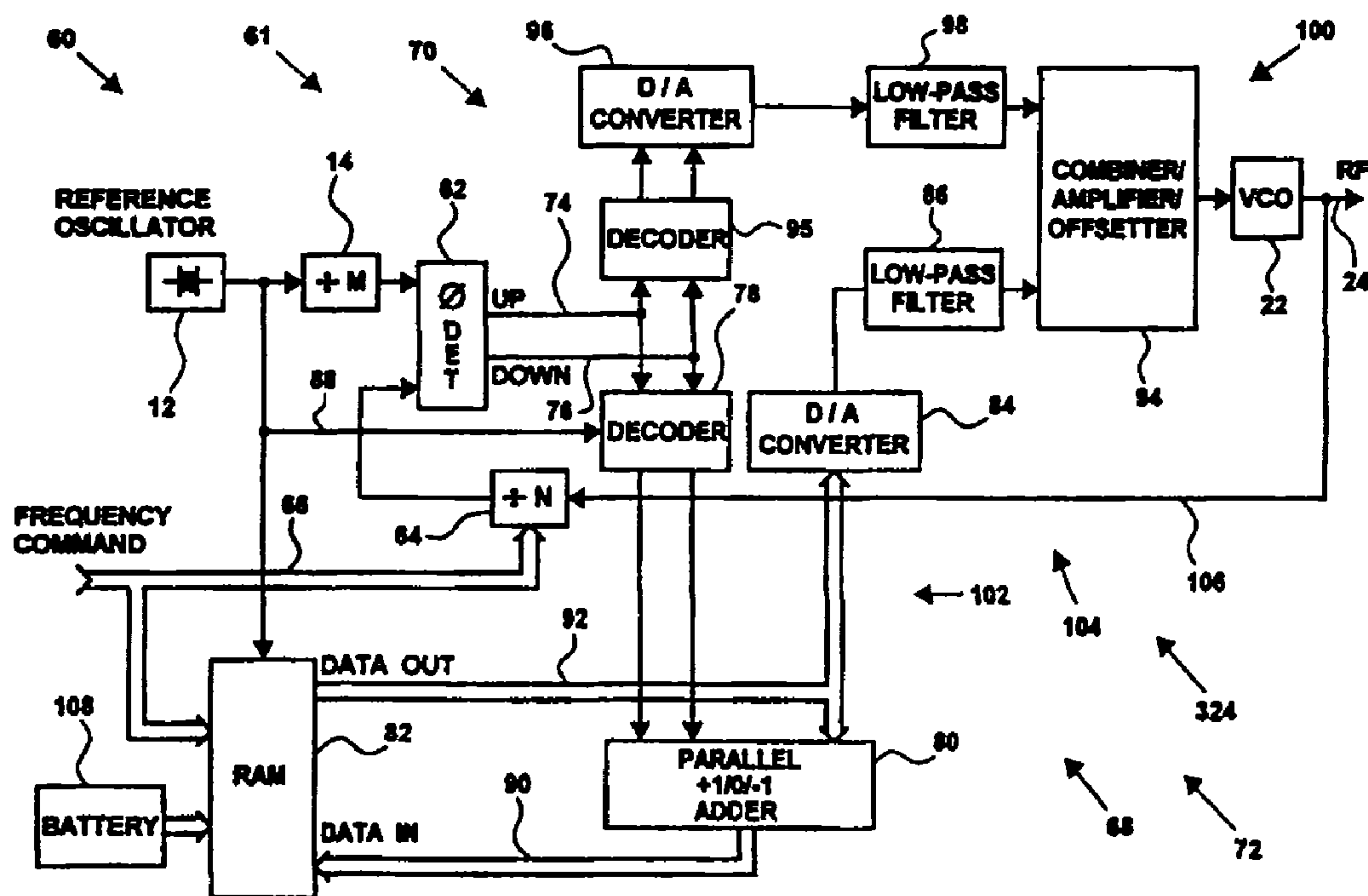
(30) 1997/10/21 (60/062,982) US

(30) 1997/12/09 (60/069,077) US

(30) 1998/10/14 (09/174,397) US

(54) **OSCILLATEURS ADAPTATIFS A SAUTS DE FREQUENCE**

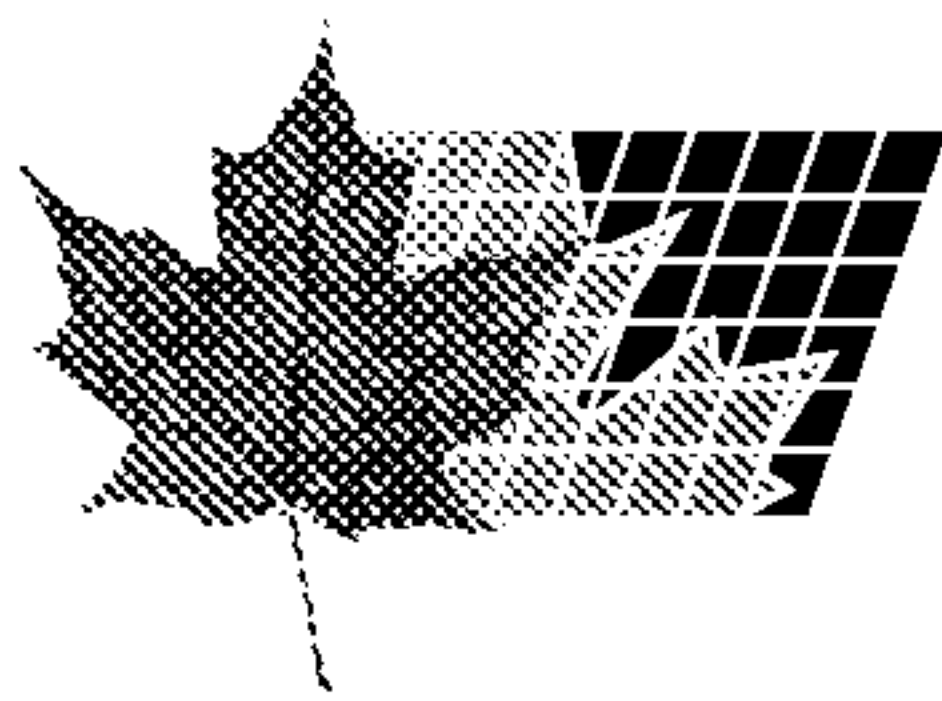
(54) **ADAPTIVE FREQUENCY-HOPPING OSCILLATORS**



(57) La voie d'aller (102) est canalisée par alimentation d'une tension à un oscillateur commandé en tension (22) et cette tension comprend deux composantes. Une composante est une tension de canalisation commandant l'oscillateur commandé en tension (22) à une fréquence s'approchant de la fréquence voulue. L'autre composante est une tension de correction de fréquence que l'oscillateur (60) à sauts de fréquence a apprise pour chaque fréquence canalisée à mesure qu'un détecteur de phase (62) et un intégrateur (68) ont verrouillé en phase de fréquence de sortie d'un oscillateur commandé en tension (22) sur chacune des fréquences canalisées, une

(57) Forward path (102) is channelized by supplying a voltage to a voltage-controlled oscillator (22), and this voltage includes two components. One component is a channelizing voltage that will drive the voltage-controlled oscillator (22) to a frequency that approximates the desired frequency. The other is a frequency-correction voltage that the frequency-hopping oscillator (60) has learned for each channelized frequency as a phase detector (62) and an integrator (68) have phase locked the output frequency of a VCO (22) to each of the channelized frequencies a plurality of times previously. Thus, the present invention includes a





(21) (A1) **2,308,209**
(86) 1998/10/16
(87) 1999/04/29

pluralité de fois préalablement. Ainsi, la présente invention comprend un procédé d'apprentissage dans lequel des variations de proportionnalités et de linéarités de l'oscillateur commandé en tension (22) et de composants tels que des résistances, un convertisseur A/N et un convertisseur N/A (84) sont corrigées par les tensions de correction de fréquence que l'oscillateur (60) à sauts de fréquence apprend, stocke et auxquelles il accède. De plus, le processus d'apprentissage compense la dérive due à la température.

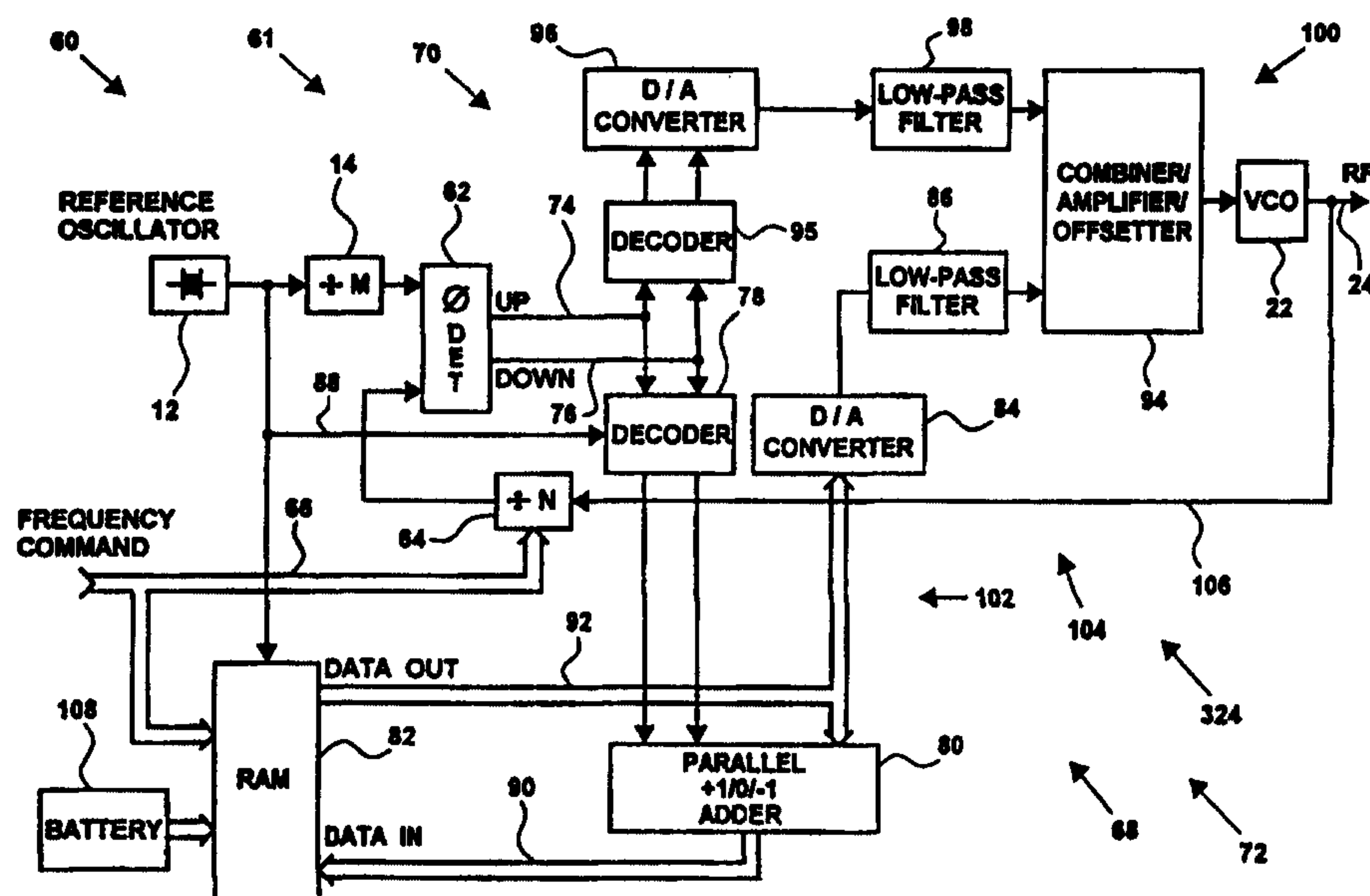
learning process in which variations in proportionalities and linearities of the VCO (22) and such components as resistors, an A/D converter and a D/A converter (84) are corrected by the frequency-correction voltages that the frequency-hopping oscillator (60) learns, stores, and accesses. Further the learning process compensates for temperature drifting.

PCT

WORLD INTELLECTUAL PROPERTY ORGANIZATION
International Bureau

INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(51) International Patent Classification ⁶ : H03L 7/08, 7/085, 7/089, 7/18, H03M 1/66	A1	(11) International Publication Number: WO 99/21281 (43) International Publication Date: 29 April 1999 (29.04.99)
(21) International Application Number: PCT/US98/21942 (22) International Filing Date: 16 October 1998 (16.10.98) (30) Priority Data: 60/062,982 21 October 1997 (21.10.97) US 60/069,077 9 December 1997 (09.12.97) US 09/174,397 14 October 1998 (14.10.98) US (71)(72) Applicant and Inventor: LAUTZENHISER, Lloyd, L. [US/CA]; Emhiser Research Limited, 110 Bowes Street, Parry Sound, Ontario P2A 2L7 (CA). (74) Agents: SHIMOLA, Howard, G.; Pearne, Gordon, McCoy & Granger, 1200 Leader Building, Cleveland, OH 44114 (US) et al.		(81) Designated States: AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, CA, CH, CN, CU, CZ, DE, DK, EE, ES, FI, GB, GE, GH, GM, HU, ID, IL, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MD, MG, MK, MN, MW, MX, NO, NZ, PL, PT, RO, RU, SD, SE, SG, SI, SK, SL, TJ, TM, TR, TT, UA, UG, US, UZ, VN, YU, ZW, ARIPO patent (GH, GM, KE, LS, MW, SD, SZ, UG, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GW, ML, MR, NE, SN, TD, TG). Published <i>With international search report.</i> <i>Before the expiration of the time limit for amending the claims and to be republished in the event of the receipt of amendments.</i>

(54) Title: ADAPTIVE FREQUENCY-HOPPING OSCILLATORS**(57) Abstract**

Forward path (102) is channelized by supplying a voltage to a voltage-controlled oscillator (22), and this voltage includes two components. One component is a channelizing voltage that will drive the voltage-controlled oscillator (22) to a frequency that approximates the desired frequency. The other is a frequency-correction voltage that the frequency-hopping oscillator (60) has learned for each channelized frequency as a phase detector (62) and an integrator (68) have phase locked the output frequency of a VCO (22) to each of the channelized frequencies a plurality of times previously. Thus, the present invention includes a learning process in which variations in proportionalities and linearities of the VCO (22) and such components as resistors, an A/D converter and a D/A converter (84) are corrected by the frequency-correction voltages that the frequency-hopping oscillator (60) learns, stores, and accesses. Further the learning process compensates for temperature drifting.

WO 99/21281

PCT/US98/21942

TITLE OF THE INVENTION
ADAPTIVE FREQUENCY-HOPPING OSCILLATORS

BACKGROUND OF THE INVENTION

5 Field of the Invention

The present invention relates generally to phase-locked oscillators and radio-frequency transmitters and receivers. More particularly, the present invention pertains to phase-locked oscillators in which adaptive circuitry is used to provide extremely fast phase locking, and adaptive frequency-hopping
10 oscillators that utilize adaptive phase-locked oscillators.

Since the transmitted information remains on a given frequency for a matter of seconds, or microseconds, and since the order of selection of frequencies can be changed rapidly and precisely, information can be successfully encoded by the use of frequency-hopping transmitters.

15 As an example, when used to transmit video signals, a frequency-hopping transmitter transmits each successive scan line at a different frequency.

A frequency-hopping transmitter is a transmitter that utilizes a frequency-hopping oscillator. In like manner, a frequency-hopping receiver is a receiver that utilizes a frequency-hopping oscillator. A frequency-hopping
20 oscillator is a phase-locked oscillator that is channelized and whose channelized frequencies can be accessed rapidly in response to a predetermined program.

Phase-locked oscillators are used in transmitters for producing an output frequency that is crystal referenced, for demodulating frequency
25 modulated signals in radio receivers, to achieve frequency deviation compression in frequency-modulated and phase-modulated receivers, and in various devices in which both rapid change to selected frequencies and precise frequency control are critical.

The use of phase-locked oscillators to achieve frequency deviation
30 compression in radio receivers is taught by Lautzenhiser in U.S. Patent 5,091,706, issued February 25, 1992; in U.S. Patent 5,497,509, issued March 5, 1996; and in U.S. Patent 5,802,462, issued September 1, 1998.

Phase-locked oscillators can be A.C. modulated, D.C. modulated, or both, as taught by Lautzenhiser in U.S. Patent 5,091,706; in U.S. Patent

5,097,230, issued March 17, 1992; and in U.S. Patent 5,311,152, issued May 10, 1994. In addition, phase-locked oscillators can be channelized as also taught by the aforesaid Lautzenhiser patents.

Channelized phase-locked oscillators can be used with programming
5 circuitry to provide frequency-hopping oscillators. However, for many applications, the frequency-hopping oscillator must be able to access newly-selected frequencies with great rapidity, preferably in the order of one microsecond.

A phase-locked oscillator includes both a forward path and a feedback
10 path. By definition, the forward path extends from a comparing device, through a VCO, to an output frequency conductor. And the feedback path extends from the output frequency conductor, through one or more frequency dividers which serve as channelizing devices, to the comparing device. In accordance with these definitions, the comparing device is not a part of either path.

15 In phase-locking oscillators, both the forward path and the feedback path are connected to a crystal-controlled reference oscillator by a comparing device, and phase lock is achieved when a feedback frequency from a voltage controlled oscillator equals the frequency of the reference oscillator.

Channelization of phase-locking oscillators is achieved by channelizing
20 the feedback path. And the feedback path is channelized by dividing frequencies in the feedback path by N, as shown herein, by any of the ways taught by Lautzenhiser in the aforesaid patents, by partial N manipulation, or by nearly any other method that is conceivable.

Since channelization of the feedback path is dependent only upon the
25 time required to divide the frequency in the feedback path by a different number, channelization of the feedback path is extremely rapid.

However, for frequency-hopping oscillators a frequency that approximates phase lock must be achieved rapidly, and the time to achieve phase lock depends upon loop frequency.

30 A.C. modulation of the forward path, at frequencies above the loop frequency, is achieved by applying an analog voltage, or modulating voltage, to the VCO via a modulation resistor, as taught in the aforesaid Lautzenhiser patents, or by any other suitable means.

D.C. modulation of the feedback path is achieved by digital manipulation of pulses in the feedback path, as taught by Lautzenhiser in the aforesaid patents, or by any other suitable means.

5 In phase-locked oscillators, an error signal is produced by a difference in a feedback frequency to a reference frequency. This error signal may be integrated by analog or digital circuitry.

In phase-locked oscillators that use an analog integrator, the error signal is time-integrated. This time-integrated error signal, which is a voltage, is applied to the VCO during the integration process. The error signal disappears
10 and integration stops when phase lock is achieved.

In phase-locked oscillators that use a digital integrator, the error signal is integrated by summing clock-timed UP, DOWN, and/or ZERO error signals. D/A conversion changes the digitally integrated error signal into voltage which is applied to the VCO during the integration process. The error signal
15 disappears and integration stops when phase lock is achieved.

Whether the integrator be an analog or a digital device, the final output of the integrator provides the voltage that is required to drive the VCO to an output frequency that phase locks. Voltages that will drive the VCO to output frequencies that approximate phase lock for various channels are called
20 channelizing voltages.

BRIEF SUMMARY OF THE INVENTION

The frequency-hopping oscillators of the present invention include adaptive circuitry with learning and recalling functions, thereby providing frequency-hopping oscillators in which an output frequency of a VCO can
25 channelized without waiting for phase locking.

Channelizing information, and/or frequency-correction information, is developed and stored that, when recalled will drive the output frequency to the desired channel almost instantly, and with very little deviation from frequencies that would phase lock for the respective channels.

30 Either the channelizing information, or the channelizing information plus frequency-correction information, not only channelizes, but also compensates for errors in proportionality and linearity of such components as

an A/D converter, a D/A converter, an analog combiner/offsetter, resistor values, and/or a VCO. Subsequent return to the same channelized frequency results in automatic correction for temperature drift of various components that may have
5 occurred since the channel was last accessed.

That is, adaptive circuitry stores channelizing information that can be recalled and converted into a plurality of channelization voltages, one for each channel. Thereafter, the output frequency of the VCO can be driven to channelized frequencies that approach phase lock without waiting for the
10 phase-locked oscillator to phase lock.

In a first embodiment, phase lock is achieved as channelizing information, as developed by digital integration, flows through a D/A converter and an analog combiner/offsetter to a VCO. Therefore, when phase lock occurs, the channelizing information compensates for all analog errors in
15 proportionality and linearity, including those in the VCO.

Therefore, when recalled and converted to channelizing voltages, the channelizing information compensates for all analog errors, such as errors in proportionality and linearity.

If a battery back-up is provided for volatile memory, at initialization, as
20 each channel is accessed and the frequency-hopping oscillator phase locks to each channelized frequency, the frequency-hopping oscillator learns its channelizing voltage, and the channelizing information that represents each channelizing voltage, is stored in digital form. Or, if battery retention of

volatile memory is not included, upon start-up, as each channel is accessed, the frequency-hopping oscillator phase locks to the respective frequencies. And the RAM stores the channelizing information.

5 Thereafter, when this channelizing information is recalled from memory and converted to a channelizing voltage, the output frequency of the VCO will be driven to a frequency that will phase lock except for temperature drift of components since last accessing the same channel.

10 The first and second embodiments include special circuitry that mimics analog circuitry. That is, these two embodiments each include a digital integrator, and the digital integrators include digital lead compensation, thereby providing loop stability for the digital integrators, even as analog integrators use a lead resistor in series with an integrating capacitor to achieve lead compensation and loop stability.

15 In a subcombination, the present invention includes an improved D/A converter. Whereas the primary design objective of prior-art D/A converters has been to produce output voltages that increase linearly in response to digital inputs, the present invention provides a nonlinear D/A converter that excels over prior-art D/A converters in both performance and cost when used in
20 applications such as are taught herein.

 More particularly, the nonlinear D/A converter of the present invention prevents "holes" in output voltages, allows lower cost resistors to be used, and allows a larger number of bits to be processed, even when low cost resistors are used. The D/A converter is nonlinear by virtue of including dual addresses
25 that are sufficiently large to prevent occlusion thereof by resistor tolerances.

 A D/A converter has dual addresses if identical voltages can be outputted with two different digital inputs. Conversely, a D/A converter is said to have "holes" if one digital input results in a voltage output that is too low,

and the next higher input results in a voltage output that is too high. Both dual addresses and holes in D/A converters are caused primarily by random accumulation of resistor tolerances.

5 In summary, in the present invention channelizing information and/or frequency-correction information is stored in digital form that, when converted to D.C. voltages and applied to the VCO, not only channelizes frequencies in the forward path almost instantaneously, but also corrects for variations in proportionalities and linearities of the analog components in addition to
10 correcting for temperature drift. And in all embodiments, optionally, a nonlinear D/A converter prevents holes in output voltages.

In a first aspect of the present invention, a method for successively producing selected ones of channelized output frequencies comprises: comparing a feedback frequency with a reference frequency for one of the
15 channelized output frequencies; developing increment/decrement signals in response to the comparing step; algebraic-sum storing increment/decrement pulses as a function of the increment/decrement signals; and driving the output frequency progressively closer to phase lock with the reference frequency in response to the algebraic-sum stored pulses substantially simultaneous with the
20 algebraic-sum storing step.

In a second aspect of the invention, a method for successively producing channelized output frequencies without interposing a storing step between selected ones of the channelized output frequencies comprises: comparing a feedback frequency with a reference frequency for one of the
25 channelized output frequencies; algebraic-sum storing increment/decrement pulses as a function of the comparing step; driving the output frequency progressively closer to phase lock with the reference frequency in response to the algebraic-sum stored pulses substantially simultaneous with the algebraic-sum storing step; and driving the output frequency toward the phase lock for

a second one of the channelized output frequencies in response to previously-stored channelizing information without interposing a storing step between the driving steps.

- 5 In a third aspect of the present invention, a method for rapidly and accurately producing selected ones of channelized output frequencies comprises: recalling previously-stored channelizing information for one of the channelized output frequencies; driving the output frequency toward phase lock with a reference frequency in response to the recalled channelizing information;
- 10 comparing a feedback frequency with the reference frequency; algebraic-sum storing increment/decrement pulses as a function of the comparing step; and driving the output frequency progressively closer to the phase lock with the reference frequency in response to the algebraic-sum stored pulses substantially simultaneous with the algebraic-sum storing step.
- 15 In a fourth aspect of the present invention, apparatus is provided for rapidly producing channelized output frequencies which comprises means for channelizing a feedback frequency into a plurality of output frequencies, the improvement in which producing one of the output frequencies comprises:
- 20 means for comparing the feedback frequency with a reference frequency; means, being operatively connected to said means for comparing, for developing increment/decrement signals as a function of said feedback frequency; means for algebraic-sum storing increment/decrement pulses as a function of the increment/ decrement signals; and means for driving the output frequency progressively closer to phase lock with the reference frequency in
- 25 response to the algebraic-sum stored pulses.

- In a fifth aspect of the present invention, apparatus is provided for rapidly producing channelized output frequencies which comprises means for channelizing a feedback frequency into a plurality of output frequencies, the improvement which comprises: means for comparing the feedback frequency
- 30 with a reference frequency for one of the channelized output frequencies;

means being operatively connected to said means for comparing, for algebraic-sum storing increment/decrement pulses as a function of the feedback frequency; means for driving the output frequency for the one channelized
5 output frequency progressively closer to phase lock with the reference frequency in response to the algebraic-sum-stored pulses; and means, comprising the means for algebraic-sum storing, for holding in digital storage, immediately prior to a change in channelizing the feedback frequency, channelizing information developed from producing the one output frequency.

10 In a sixth aspect of the present invention, apparatus is provided for rapidly producing channelized output frequencies in response to stored and subsequently-recalled channelizing information, the improvement which comprises: means for driving the output frequency toward phase lock with a reference frequency for one of the channelized output frequencies in response
15 to said recalled channelizing information; means for comparing a feedback frequency with the reference frequency for the one channelized output frequency; means being operatively connected to said means for comparing, for algebraic-sum storing pulses as a function of the feedback frequency; and means for driving the output frequency for the one channelized output
20 frequency progressively closer to phase lock with the reference frequency in response to the algebraic-sum stored pulses.

In a seventh aspect of the present invention, a method for phase locking an output frequency to a reference frequency comprises: comparing a feedback frequency with a reference frequency; developing
25 increment/decrement signals in response to the comparing step; driving the output frequency progressively closer to phase lock with the reference frequency as a function of the increment/decrement signals; digitally-developing a lead-compensation signal; and lead compensating the progressive driving step in response to the lead-compensation signal.

30 In an eighth aspect of the present invention, a phase-locked oscillator comprises a reference oscillator that produces a reference frequency, a phase

comparator that is operatively connected to the reference oscillator, a forward path that includes a radio-frequency oscillator and that extends from the phase comparator to an output of the radio-frequency oscillator, and a feedback path
5 that extends from the output of the radio-frequency oscillator to the comparator, the improvement which comprises: a digital integrator being interposed into the forward path intermediate of the phase comparator and the radio-frequency oscillator; and lead-compensator means, being operatively interposed into the forward path intermediate of the phase comparator and the radio-frequency
10 oscillator, for lead compensating the digital integrator.

In a ninth aspect of the present invention, a method for phase locking an output frequency to a reference frequency comprises: D/A converting; and making output voltages of a plurality of higher bits of the D/A converting step less than twice an output voltage of the next lower bit.

15 In a tenth aspect of the present invention, a phase-locked oscillator includes both a forward path and a feedback path, and the improvement comprises: a D/A converter being interposed into one of the paths; and means for making voltage steps for respective ones of a plurality of higher bits of the D/A converter smaller than a maximum total voltage for all lower bits.

20 In an eleventh aspect of the present invention, a learning method comprises: D/A converting; and making voltage-output steps of a respective ones of a plurality of higher bits of the D/A converting step less than twice an output of the next lower bit.

In a twelfth aspect of the present invention, an adaptive system
25 includes a learning path, and the improvement comprises: a D/A converter being interposed into the learning path; and means for making voltage steps for respective ones of a plurality of higher bits of the D/A converter smaller than a maximum total voltage for all lower bits.

In a thirteenth aspect of the present invention, a method comprises:
D/A converting digital bits into an analog output voltage; and making output-
voltage steps for each of respective ones of a plurality of higher bits lower than
5 a maximum total voltage output of all lower bits.

In a fourteenth aspect of the present invention, A D/A converter
comprises: means, comprising a plurality of higher bits and a plurality of lower
bits, for producing output voltages as a function of digital inputs; and means for
making output-voltage steps for each of respective ones of the higher bits
10 smaller than a maximum total voltage output of all lower bits.

In a fifteenth aspect of the present invention, a D/A converter
comprises: means, comprising a resistance ratio of interconnected resistors, for
producing voltage steps that double for each increasing bit; and means for
decreasing the voltage steps for each of a plurality of higher bits with respect to
15 the next lower bit; whereby the D/A converter produces an output voltage that
is a nonlinear and decreasing ratio of digital inputs.

BRIEF DESCRIPTION OF THE SEVERAL VIEWS OF THE DRAWINGS

FIGURE 1 is a schematic drawing of a prior-art phase-locked loop with
an analog integrator;

20 FIGURE 2 is a schematic drawing of a prior-art analog integrator for the
phase-locked loop of FIGURE 1 that includes lead compensation;

FIGURE 3 is a schematic drawing of a preferred embodiment of the
present invention in which an adaptive frequency-hopping oscillator utilizes
digital integration with lead compensation;

25 FIGURE 4 is a schematic drawing of a conventional D/A converter that
uses a ladder of R and 2R resistors;

FIGURE 5 is a diagram showing examples of variations in output voltages as caused by variations in resistances of in the D/A converter of FIGURE 4;

5 FIGURE 6A is a diagram showing, in stepped form, showing that holes in output voltages of the D/A converter of FIGURE 48 may be caused by variations in resistances of standard resistors;

FIGURE 6B is a diagram, similar to FIGURE 6A, but showing in stepped form that variations in resistances of standard resistors may result in duplicate
10 digital addresses;

FIGURE 7A is a diagram, showing in smoothed curve form, that variations in output voltages of the D/A converter of FIGURE 4 may cause holes;

FIGURE 7B is a diagram, showing in smoothed curve form, that
15 variations in resistances of standard resistors may result in duplicate digital addresses;

FIGURE 8 is a schematic drawing of a preferred embodiment of a nonlinear D/A converter for use with channelized phase locking oscillators and frequency hopping oscillators of the present invention;

20 FIGURE 9 is a diagram showing that voltage output vs. digital input for the conventional D/A converter of FIGURE 4 is linear;

FIGURE 10 is a diagram showing that voltage output vs. digital input for the nonlinear D/A converter of FIGURE 8;

FIGURE 11 is a block diagram of a second embodiment of the
25 nonlinear D/A converter of the present invention; and

FIGURE 12 is a schematic drawing of a preferred embodiment of the present invention, similar to that of FIGURE 3, except that a PROM is used to provide initial channelizing voltages.

DETAILED DESCRIPTION OF THE INVENTION

30 Referring now to FIGURES 1 and 2, before considering the preferred embodiment of the present invention, a brief review of phase-locked oscillators and integrators may be helpful. Also, it is appropriate to review integrators

with lead compensation, since lead compensation is necessary to achieve stability in phase-locked loops.

A prior-art phase-locked oscillator 10 of FIGURE 1 includes a reference oscillator 12, a divider 14 for dividing the reference frequency of the reference oscillator 12 by a constant value of M , a phase comparator, or phase detector, 16, an analog integrator 18, a coupling resistor 20, a voltage-controlled oscillator (VCO), or radio-frequency oscillator, 22, an output conductor 24, and a feedback conductor 26. A divider 28 may be included to achieve channelization of frequencies produced by the VCO 22 by dividing by selected values of N .

The phase-locked oscillator 10 also includes both a forward path 30 and a feedback path 32. The forward path 30 extends from the phase comparator 16 to the output conductor 24, and the feedback path 32 extends from the output conductor 24 to the phase comparator 16. Thus, by definition, the phase comparator 16 is in neither path 30 or 32.

The integrator 18, as shown in FIGURE 1, includes an operational amplifier 34, a coupling resistor 36, an integrating capacitor 38, and a lead-compensation resistor 42. However, in actual practice, an analog integrator 40 of FIGURE 2 is used.

The integrator 40 of FIGURE 2 includes an operational amplifier 43, the coupling resistor 36, the integrating capacitor 38, the lead-compensation resistor 42, and a reference-frequency spurious-suppressing capacitor 44.

The operational amplifier 43 of FIGURE 2 includes a positive input terminal 46 that is connected to ground, as shown, and a negative input terminal, or inverting input terminal, 48. As shown, the coupling resistor 36 is connected to the negative input terminal 48.

Since the positive input terminal 46 is grounded, the operational amplifier 43 will hold the negative input terminal 48 at virtual ground. Therefore, if a constant positive voltage is applied to an input node 50, a constant current will flow through the coupling resistor 36 that is a function of the constant voltage and the resistance of the resistor 36.

Because of the high input impedance of the operational amplifier 43, there will be negligible current into the negative input terminal, or inverting

input terminal, 48. This means that all of the current from the voltage applied to the input node 50 will flow into the capacitor 38 and through the resistor 42. Therefore, the current flow into the capacitor 38 and through the resistor 42 will be equal to the current flow through the resistor 36 until integration is
5 complete.

With a positive voltage at the input node 50, current flow is in a direction from the input node 50, to the negative input terminal 48, through the capacitor 38, and through the resistor 42 to an output node 52. Thus, positive and negative sides of the capacitor 38 are as shown for a positive input voltage
10 at the node 50, and the integrator 40 ramps a voltage negatively between the capacitor 38 and the resistor 42.

In addition, because of the aforementioned current flow through the resistor 42, and the voltage drop across the resistor 42, a voltage is produced at the node 52 that is more negative than the negatively ramped voltage that is
15 produced by the capacitor 38. This additional negative voltage provides lead compensation, and lead compensation is required for stability of phase-locked oscillators, such as the phase-locked oscillator 10 of FIGURE 1.

Referring now to FIGURE 3, before reciting the structure and operation in detail, a brief preview will be presented. This overview should not only be
20 clearly understandable, but also should make the detailed description easier to understand.

An adaptive frequency-hopping oscillator, or adaptive system, or learning system, 60 includes a phase locked oscillator 61. The phase locked oscillator 61 includes the reference oscillator 12, the divider 14, a phase
25 comparator, or phase detector 62, the VCO 22, the output conductor 24, and a divider 64 in which N is controllable digitally by a command signal in a command bus, or bundle of frequency-command conductors, 66.

Assuming that one channelized frequency has been selected for the first time by the frequency-command conductors 66, channelizing information for
30 this one channelized frequency is digitally integrated from frequency-correction information produced by the phase detector 62. That is, frequency-correction information is produced by phase detecting, decoding, and parallel adding.

This frequency-correction information continues to increase, and be digitally stored, until it becomes channelizing information, that, when D/A converted into a channelizing voltage, will drive the VCO 22 to an output frequency that approximately phase locks the reference oscillator 12.

5 Although the channelizing information for this one channelized frequency is developed and stored in digital form, it proceeds to the VCO 22 through D/A and analog components that produce errors. Therefore, when phase lock occurs, the channelizing information has been compensated for analog errors in proportionality and linearity.

10 Thereafter, when this one channelized frequency is selected and the respective channelizing information is recalled from digital memory and D/A converted into a channelizing voltage, the VCO 22 will be driven to an output frequency that almost equals the output frequency at phase lock.

 Further, each time that this same channelized frequency is selected, the
15 channelizing information is updated for any error in output frequency such as temperature drift of analog or D/A components. Error signals proceed from the phase comparator 62 at the speed of the reference oscillator 12, so that this updating occurs regularly, even if the output frequency remains at this one channelized frequency for very short periods of time.

20 Continuing to refer to FIGURE 3, the frequency-hopping oscillator 60 utilizes a digital integrator 68 and a lead compensator, or lead signal means, 70. The digital integrator 68 and the lead compensator 70 provide a digital integrator 72 with lead compensation. However, before discussing the digital
25 integrator 68 and the lead compensator 70 it is important to consider the phase comparator, or phase detector, 62 in more detail.

 The phase comparator 62, which preferably is Motorola part number 45152, has three output states. That is, outputs in an UP conductor 74 and a DOWN conductor 76 may separately be either a 1 or a 0.

 When a (0-1) output state occurs, the UP conductor 74 produces a 0,
30 and the DOWN conductor 76 produces a 1, because the frequency produced by the VCO 22 is too low. When a (1-0) output state occurs, the UP conductor 74 produces a 1, and the DOWN conductor 76 produces a 0, because the

frequency of the VCO 22 is too high. And when both of the conductors, 74 and 76, produce a 1, the frequency-hopping oscillator 60 is phase locked.

The digital integrator 68 includes a pulse decoder 78, a parallel adder 80, and a RAM 82. A D/A converter 84 and a low-pass filter 86 convert the
5 digital signal to an analog voltage that is suitable for driving the VCO 22.

In operation, the decoder 78 receives one or more of the three output states of the phase comparator 62 and reproduces the same states as two-bit digital outputs. The parallel adder 80, which is a sixteen bit device, utilizes the two-bit digital outputs of the decoder 78 as sixteen zeros, fifteen zeros followed
10 by a one, or sixteen ones. Any one of the two-bit outputs will remain constant until the output condition of the phase comparator 62 changes to another one of the three output states.

Digital integration is achieved as follows: the RAM 82, which is connected to the reference oscillator 12 by a sampling-rate conductor 88,
15 accepts a first sample of the digital output provided by the decoder 78 via the parallel adder 80 and a 16-bit data-in bus 90. This first sample is stored in the RAM 82.

At the frequency of the reference oscillator 12, this first sample is delivered back to the parallel adder 80 via a 16-bit data-out bus 92 to be
20 algebraically summed with a second sample, the algebraic sum of the first and second samples are delivered to the RAM 82 via the data-in bus 90, this algebraic sum is delivered back to the parallel adder 80 via the data-out bus 92, and this cycle repeats until the frequency-hopping oscillator 60 is in phase lock until the frequency command in the command bus 66 is changed.

25 Simultaneously with the process of digital integration as described above, the progressively and algebraically summed values are delivered to the D/A converter 84 which is capable of processing sixteen bits of information, an analog voltage outputted by the D/A converter 84 is delivered to the low-pass filter 86, and the filtered analog voltage is applied to the VCO 22 through a
30 combiner/amplifier/offsetter 94 until the frequency-hopping oscillator 60 phase locks.

This process of digital integration is repeated the first time a frequency command in the command bus 66 selects a channelized frequency by changing

the value of N, thereby changing the output frequency at which the frequency-hopping oscillator 60 will phase lock. And, each time the frequency-hopping oscillator 60 phase locks to a selected frequency, the digitally-integrated outputs are stored in the RAM 82.

5 The next time the frequency-hopping oscillator 60 hops to a channelized frequency, the frequency command changes the value of N, and the RAM 82 cooperates with the D/A converter 84, the low-pass filter 86, and the combiner/amplifier/offsetter 94 to supply a channelizing voltage to the VCO 22, and thereby drive the VCO 22 to an output frequency that approximates
10 phase lock for the selected channelized frequency. And this channelizing occurs in less than one microsecond.

 It can be seen that the digital values stored in the RAM 82 are the values that, for a given time and temperature, correct for production variations in proportionality, nonlinearities, and temperature drifts of the D/A converter
15 84, the combiner/amplifier/offsetter 94, and the VCO 22.

 That is, as the RAM 82 digitally integrates a channelizing voltage that will phase lock the system, the RAM-stored digital values are inherently compensated for analog inaccuracies of the D/A converter 84, the combiner/amplifier/offsetter 94, and the VCO 22. That is, phase lock was
20 accomplished by applying RAM-accumulated values that kept correcting until phase lock was achieved. And the same RAM-accumulated voltages are used subsequently to channelize the VCO 22.

 It is important to notice that the stored values will be updated each time a given channelized frequency is produced, unless that channelized
25 frequency is already in phase lock, if the frequency-hopping oscillator 60 remains at that channelized frequency for a period of time that allows the phase comparator 62 to provide even one signal in one of the conductors, 74 or 76.

 For example, if the reference oscillator 12 is producing a reference frequency of 8.0 megahertz, and the divider 14 is dividing by 128, the phase
30 detector 62 will be operating with a reference frequency of 62,500 hertz.

 In this example, in 125 nanoseconds after receiving either an UP or a DOWN signal from the phase detector 62, the RAM 82 will obtain a sample for

algebraic addition to the value previously stored in the RAM 82 for that given channelized frequency.

Continuing to refer to FIGURE 3, as previously mentioned, the digital integrator 72 includes the lead compensator 70. And, as also previously
5 mentioned, the lead compensator 70 performs the function of the resistor 42 of FIGURES 1 and 2.

That is, referring to FIGURES 1 and 2, if the phase comparator 16 of FIGURE 1 places a negative potential on the node 50 of FIGURE 2, the resistor 42 of FIGURE 2 makes the output at the node 52 more negative than the
10 negative side of the capacitor 38.

Referring again to FIGURE 3, the lead compensator 70 functions in a similar manner. Whether the outputs from the UP conductor 74 and the DOWN conductor 76 result in a +1 or a -1 output from the decoder 78, since the output of a decoder 95 is always of the same sign as the output of the
15 decoder 78, the output of the decoder 95 is a lead-compensating signal. All that remains is to apply this lead-compensating signal to the VCO 22 as a voltage.

In the preferred embodiment of FIGURE 3, application of the lead-compensating signal to the VCO 22 is via a two-bit D/A converter 96, a low-pass filter 98, and the combiner/amplifier/offsetter 94.
20

The combiner/amplifier/offsetter 94 algebraically adds the lead-compensating signal, as converted to an analog voltage by the D/A converter 96 and filtered by the low-pass filter 98, to the output of the digital integrator 68, as stored in the RAM 82, and as converted to an analog voltage by the D/A
25 converter 84 and filtered by the low-pass filter 86.

The combiner/amplifier/offsetter 94 serves three functions, as named. It functions as an algebraic summer of analog voltages, it amplifies the summed signal, and it offsets the summed and amplified signal to a voltage that is in the linear tuning range of the VCO 22.

30 The frequency-hopping oscillator 60 includes a phase-locked loop 100. The phase-locked loop 100 includes both a forward path 102 and a feedback path 104. The forward path 102 extends from the phase comparator 62 to the output conductor 24 via the digital integrator 68, the combiner/amplifier/

offsetter 94, and the VCO 22. The feedback path 104 extends from the output conductor 24 to the phase detector 62 via a feedback conductor 106 and the divider 64 and includes both the divider 64 and the feedback conductor 106.

5 If a backup battery 108 is included at the factory, the frequency-hopping oscillator 60 will learn to compensate for variations in component proportionalities and nonlinearities during burn-in. If the battery 108 is not included, the frequency-hopping oscillator 60 will learn to compensate for variations in component proportionalities and nonlinearities each time the
10 frequency-hopping oscillator 60 is turned on.

 In operation, a frequency is selected by a source separate from, and not a part of, the present invention. The command for this frequency is delivered to the RAM 82 via the command bus 66 through which a digitalized address representing this selected frequency is transmitted.

The command bus 162 handles sixteen bits, and the digital components listed above are 16-bit devices, except that the A/D converter 120 is a 14-bit device that delivers thirteen bits plus an algebraic sign.

5 The phase-locked oscillator 112 includes a reference oscillator 136, a divider 138, a phase detector, or phase comparator, 140, a coupling resistor 142, an analog integrator 144, a coupling resistor 146, a voltage-controlled oscillator (VCO), or radio-frequency oscillator, 148, an output conductor 150, and a divider 152. The integrator 144 also includes a lead-compensation resistor 153.

10 The phase-locked oscillator 112 includes a phase-locked loop 154, and the phase-locked loop 154 includes both a forward path 156 and a feedback path 158.

The forward path 156 extends from the phase detector 140 to the output conductor 150, and includes the resistor 142, the integrator 144, the resistor 146, and the VCO 148, but does not include either the phase detector 140 or the output conductor 150.

The feedback path 158 extends from the output conductor 150 to the phase detector 140, and includes the divider 152, but does not include the phase detector 140.

20 The phase-locked oscillator 112 is a conventional design except for the inclusion of an integrator reset, or switch, 160 which is depicted herein as a switch, but preferably is a semiconductor, such as a field effect transistor. Optionally, other phase-locked oscillators, such as those disclosed in the aforesaid Lautzenhiser patents, may be used by adding the integrator reset 160.

25 Each time the frequency-hopping oscillator 110 is hopped to a new channel, a new frequency-correcting voltage is stored in analog form in the follow and hold 118, converted to digital form in the A/D converter 120 as frequency-correction information, added to the channelizing information that was previously digitally stored in the RAM 132.

30 Considering the frequency-hopping oscillator 110 of FIGURE 4 in detail, a frequency is selected by a source separate from, and not a part of, the present invention. The command for this frequency is delivered to the

frequency-command-change detector 116 by the command bus 162 through which a digitalized address representing this selected frequency is transmitted.

The frequency-command-change detector 116 and the sequencer 114 initiate and/or control the following steps in the order listed:

- 5 follow and hold 118 to HOLD
- integrator 144 to RESET
- latch RAM 132 data to D/A register 124
- latch new frequency command to N register 134
- release integrator reset 160
- 10 initiate A/D converter 120
- wait for conversion complete signal from A/D converter 120
- follow and hold 118 to FOLLOW
- address MUX 130 to previous register 128
- latch adder/subtractor 122 to RAM 132
- 15 address MUX 130 to normal position
- latch new frequency command to previous register 128

In response to a change in the digitalized address, the frequency-command-change detector 116, which is connected to the sequencer 114 as shown, switches the follow and hold 118 to HOLD, thereby storing, in analog
20 form, the voltage that had been produced by the integrator 144 up to the time that the frequency-command-change detector 116 sensed a change in the frequency command in the command bus 162.

The voltage produced by the integrator 144 and stored in the follow and hold 118 is a frequency-correction voltage, whether or not the frequency-
25 hopping oscillator 110 phase locks, or has phase locked at any time previously to the channel wherein the integrator 144 produces a voltage.

That is, any voltage stored in the follow and hold 118 is a frequency-correction voltage, and when A/D converted becomes frequency-correction information. Whereas channelizing information recalled from the RAM 132
30 and converted to analog form by the D/A converter 126 produces a channelizing voltage.

After the frequency-correction voltage previously produced by the integrator 144 has been stored by the follow and hold 118, the sequencer 114

closes the integrator reset 160, thereby discharging an integrating capacitor 164 that is a part of the integrator 144. Opening of the integrator reset 160 will be discussed subsequently.

5 The new frequency command, or address, as chosen externally, and as delivered though the command bus 162 in digital form, is sent to the address MUX 130. The normal mode for the address MUX 130 is to accept commands from the command bus 162, rather than accepting commands from the previous register 128, so it is not necessary for the sequencer 114 to provide an ADDRESS SELECT signal.

10 The address MUX 130 sends the new address, or new frequency command, in digital form, to the RAM 132 via address conductors 166. The sequencer 114 causes the RAM 132 to go to the new address, and prestored data, or channelizing information, corresponding to a channelizing voltage that will produce the new frequency, is latched into the D/A register 124 by the
15 sequencer 114, via data-out conductors 168, and then delivered to the D/A converter 126 via conductors 170.

The D/A converter 126 then supplies an analog voltage to the VCO 148 via a resistor 172 that corresponds to the channelizing information that was supplied to the D/A converter 126. This analog voltage that is supplied through
20 the resistor 172 to the VCO 148 provides a means for analog channelizing of the output frequency of the VCO 148 to frequencies that approach phase-locked precision.

If it were not for the fact that the channelizing voltage, which is digitally stored as channelizing information, that is supplied to the VCO 148
25 from the RAM 132, the D/A register 124, and the D/A converter 126, to the VCO 148 includes a frequency-correction voltage that has been added to a channelizing voltage, this analog voltage would move the output frequency of the VCO 148 to only an approximation of the desired channelized frequency.

Precise channelization would occur only after the phase-locked loop
30 154 phase locked to the reference oscillator 136, and the time to phase lock would depend upon time restraints placed on phase locking by the integrator 144 which functions as a low-pass filter.

However, the frequency-correction voltages compensate for variations in proportionality and linearity of the analog components. That is, since the frequency-correction voltages reflect the corrections in channelizing voltages that are required to actually phase lock, the frequency correction voltages
5 correct for errors in proportionality and linearity of the VCO 148, the follow and hold 118, the A/D converter 120, and the D/A converter 126.

Further, since the integrator 144 will continue to integrate frequency-correction voltages, or to integrate subsequent ones of frequency-correction voltages, until the frequency-hopping oscillator 110 is phase locked, the
10 frequency-correction voltages will compensate for the resistors 146 and 172.

Returning to detailed description of FIGURE 4, the sequencer 114 now latches the new frequency command into the N register 134, so that the N register 134 cooperates with the divider 152 to provide means for digitally channelizing the feedback path 158.

15 At this time, both the forward path 156 and the feedback path 158 have been channelized to the new output frequency, and the VCO 148 is producing an output frequency that is substantially the same as will be produced microseconds later when the phase-locked oscillator 112 actually phase locks.

20 Next, the sequencer 114 opens the integrator reset 160 thereby preparing the integrator 144 for the task of developing a frequency-correction voltage for the newly addressed frequency.

Changing the frequency-hopping oscillator 110 to a new output frequency can be accomplished in less than one microsecond. Therefore, the
25 output frequency of the frequency-hopping oscillator 110 will be very close to phase locking in a very short time.

The remaining steps do not factor into the time that is required to produce an output frequency that approximates phase locking. Nor, do they pertain exclusively to the process of actual phase locking. Instead, the steps
30 that follow prepare the way for the frequency-hopping oscillator 110 to hop, with great precision, to the same frequency the next time it is addressed. More particularly, the following steps pertain to apparatus and method for algebraically summing and storing channelizing information that, when

converted to analog form, produces analog channelizing voltages that are corrected for analog errors sensed by frequency-correction voltages.

The sequencer 114 now changes the mode of the A/D converter 120 to INITIATE, so that the frequency-correction voltage that has been held in the follow and hold 118 is digitalized. Upon completion of conversion, the A/D converter 120 sends a CONVERSION COMPLETE signal to the sequencer 114, and the sequencer 114 returns the follow and hold 118 to FOLLOW.

With the follow and hold 118 in the FOLLOW mode, it now accepts a new frequency-correction voltage from the output of the integrator 144 as the integrator 144 works to phase lock the frequency-hopping oscillator 110 at a new frequency.

Remembering that the digital signal that was produced by the A/D converter 120 is the frequency-correction voltage that was obtained during phase locking of the previously-commanded frequency, it is time to consider some of the steps that are necessary to sum this frequency-correction voltage with the channelizing voltage that pertains to the same channelized frequency. Thus, it is necessary to access both the frequency command for this previous frequency and its channelizing voltage before the frequency-correction voltage and the channelizing voltage can be summed.

The sequencer 114 now switches the address MUX 130 to PREVIOUS REGISTER, so that the MUX 130 accesses the previous frequency command from the previous register 128 via a previous-command conductor 174 and sends it to the RAM 132 via the address conductor 166. That is, the address that is now delivered to the RAM 132 by the address MUX 130 from the previous register 128 is the same frequency command that was in effect when the follow and hold 118 stored the frequency-correction voltage of the integrator 144, and that was digitalized by the A/D converter 120.

The previous channelizing voltage, that corresponds to the previous frequency command and that has been prestored in the RAM 132 as channelizing information, is now latched into the parallel adder/subtractor 122. The parallel adder/subtractor 122 then algebraically adds the previous channelizing voltage and the previous frequency-correction voltage. This

algebraic sum is delivered to the RAM 132 via a data-in conductor 176 and is latched therein by the sequencer 114.

That is, the parallel adder/subtractor 122 algebraically sums, in digital form, the channelizing voltage that will drive the VCO 148 to approximately
5 the previously-addressed frequency, with the frequency-correction voltage that the integrator 144 developed as it phase locked the phase-locked oscillator 112 for the previously-addressed frequency.

Thereafter, when a frequency command commands this previously-addressed frequency, channelizing information is recalled from the RAM 132
10 and converted to an analog channelizing voltage, and the initial frequency developed by the VCO 148 will be very close to phase locking the frequency-hopping oscillator 110. As can be seen from the discussion that follows, the frequency-hopping oscillator 110 also compensates for temperature drift of components as the frequency-hopping oscillator 110 continues to learn, store,
15 retrieve, and use error correction voltages that are crystal referenced.

With each successive addressing of any hopped frequency, a new error signal, or frequency-correction voltage, will be developed and digitally summed with the channelizing voltage for the addressed frequency, so that when the same frequency is accessed at a later time, the frequency-hopping
20 oscillator 110 will have learned to drive its VCO 148 to a frequency that is very near to phase locking.

Continuing to describe the present invention, subsequent to latching the digitalized summed voltages into the RAM 132, the sequencer 114 switches the address MUX 130 back to its normal position, and finally, the sequencer
25 114 latches the address of the new frequency command, that is presently in the command bus 162, to the previous register 128, so that this present frequency command will be available as the previous frequency command when next the address MUX 130 accesses the previous register 128.

As described above, the present invention channelizes both the forward
30 path 156 and the feedback path 158 of the phase-locked loop 154 that is a part of the phase-locked oscillator 112. Channelization of the forward path 156 is achieved by supplying a voltage to the VCO 148 that includes two components, and channelization of the feedback path 158 is achieved by

changing the number of pulses in the feedback path 158 by such devices as the divider 152.

One component for channelizing the forward path 156 is a channelizing voltage that will drive the VCO 148 to approximately the desired frequency. The other is a frequency-correcting voltage that the phase detector 140 and the integrator 144 have found, when last accessing this same frequency, to be necessary to phase lock the phase-locked loop 154.

Therefore, any VCO 148 of a given type, from any manufacturing batch, without regard to individual volt-to-frequency proportionalities, without regard to individual linearities or deviations from linearity, and without regard to the actual resistances of the resistors 146 and 172, when driven by a voltage that is the sum of a voltage that approximately channelizes the VCO 148 and the frequency-correction voltage for that channel, will produce an output frequency that is extremely close to phase locking.

As an example of the operation of the present invention: assume the VCO 148 produces an output frequency of 1.0 GHz in response to an input voltage of 1.0 volts D.C. Assuming that the resistors, 146 and 172 have equal resistances, and assuming that the integrator 144 is at zero volts D.C., the output of the D/A converter 126 that feeds the resistor 172 must be 2.0 volts D.C.

Now assume that a new output frequency is to be 2.0 GHz, and that it requires 2.0 volts D.C. to drive the VCO 148 to this new output frequency. The RAM 132 then outputs channelizing information that was stored for this same frequency previously, causing the D/A converter 126 to output 4.0 volts D.C. Assuming that zero volts is produced by the integrator 144, the 4.0 volts D.C. from the D/A converter 126 results in 2.0 volts D.C. being applied to the VCO 148 after division of the 4.0 volts by the resistors, 146 and 172.

Now assume that time/temperature drift of the VCO 148 and/or the resistors, 146 and 172, requires an input of 2.1 volts D.C. to output 2.0 GHz, so the output frequency of the VCO 148 in response to 2.0 volts D.C is too low. Over the next few cycles of the phase-locked loop 154, a frequency-correction voltage of 0.2 volts D.C. will be developed by the phase detector

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Summarizing, the adaptive frequency-hopping oscillator 60 achieves quick hopping by channelizing both the forward path 102 and the feedback path 104, and by developing, storing, and accessing channelizing information that is compensated for variations in proportionality, linearity, and temperature drift of analog and D/A components. This channelizing information, when D/A converted to a channelizing voltage, will drive the VCO 22 to an

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output frequency that is substantially phase locked in less than one microsecond.

Therefore, the phase-locked oscillator 61 is an adaptive system in
5 which the frequency-hopping oscillator 60 learns, stores, and retrieves
channelizing voltages that will drive the frequency output of the VCO 22 to
precise frequencies.

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hopping oscillator 110 of FIGURE 4 may be used in combination with any suitable method for D.C. modulating the feedback path 158.

Combining the frequency-hopping oscillator 110 of FIGURE 4 of the present patent application with FIGURE 6 of Lautzenhiser, U.S. Patent
5 5,091,706, which is reproduced herein as FIGURE 5, is via a correction-receiving conductor 184 and a frequency-producing conductor 186, both shown on FIGURES 4 and 5.

Referring again to FIGURE 5, in a D.C. modulated phase-locked oscillator 200 that generally corresponds to the D.C. modulated phase-locked
10 oscillator of FIGURE 6 of the referenced Lautzenhiser patent, a modulation signal, in the form of analog voltages, is applied to a modulation conductor 202.

The modulation voltages are conducted from the modulation conductor 202 to the VCO 148 via the modulation conductor 180 and the modulation
15 resistor 182 to achieve A.C. modulation of the output frequency. D.C. modulation is achieved by conducting the modulation voltages from the modulation conductor 202 to a modulation oscillator 204 via a modulation conductor 206. D.C. modulation of the phase-locked oscillator 200 is achieved as described in detail in Lautzenhiser, U.S. Patent 5,091,706, which is
20 incorporated herein by reference thereto.

Combining the adaptive frequency-hopping oscillator 110 of FIGURE 4 with the phase-locked oscillator 200 of FIGURE 5 includes connecting the integrator 144 of FIGURES 4 and 5 to the follow and hold 118 of FIGURE 4 via the conductor 184, and connecting the D/A converter 126 of FIGURE 4 to the
25 VCO 148 via the frequency-producing conductor 186 and the resistor 172 of FIGURES 4 and 5. In addition, the integrator reset 160 must be connected across the capacitor 164 of FIGURE 5, as shown in FIGURES 4 and 5.

As pertaining to frequency-hopping, when the frequency-hopping oscillator 110 of FIGURE 4 is combined with the phase-locked oscillator 200 of
30 FIGURE 5, the resultant device functions as described in conjunction with FIGURE 4, but in addition to being capable of being A.C. modulated at frequencies above that of the loop frequency, the resultant circuitry is now also capable of lower frequency A.C. modulation as well as D.C. modulation.

Referring now to FIGURE 6, a frequency-hopping oscillator 220 generally includes components as named and numbered in conjunction with the embodiment of FIGURE 4. However, the sequencer 114 of FIGURE 4 is renumbered as sequencer 222 to describe different sequences, the parallel
 5 adder/subtractor 122 has been omitted, a 2X multiplier 224 has been inserted between the VCO 148 and the follow and hold 118, and a backup battery 226 has been added to the RAM 132 to provide nonvolatile memory.

The frequency-command-change detector 116 and the sequencer 222 initiate and/or control the following steps:

- 10 follow and hold 118 to HOLD
- integrator 144 to RESET
- latch RAM 132 data to D/A register 124
- latch new frequency command to N register 134
- release integrator reset 160
- 15 initiate A/D converter 120
- wait for conversion complete signal from A/D converter 120
- follow and hold 118 to FOLLOW
- address MUX 130 to previous register 128
- latch A/D converter 120 output to RAM 132
- 20 address MUX 130 to normal position
- latch new frequency command to previous register 128

The operation of the frequency-hopping oscillator 220 of FIGURE 6 is easily understood after reading the detailed description of the FIGURE 4 embodiment, so that a brief description of the FIGURE 6 embodiment will
 25 suffice.

In operation, as the phase-locked loop 154 phase locks to the reference oscillator 136, the voltage developed at the VCO 148 is received by a conductor 228 and is multiplied by two by the 2X multiplier 224, the multiplied signal is received by the follow and hold 118, the multiplied signal
 30 is converted to digital by the A/D converter 120, and the multiplied signal is stored in the RAM 132.

Preferably, a battery, such as the backup battery 108 of FIGURE 3, is included in all embodiments to preserve data in the RAM 82 or 132. Thus, during burn-in of systems at the factory, the frequency-hopping oscillator 60
5 will develop and store channelizing information.

Referring now to FIGURE 4, a prior-art D/A converter 240 includes bits, or digital inputs, 242 for sixteen bits of binary-coded information, and an output voltage node 244. The D/A converter 240 includes a plurality of resistors R

and a plurality of resistors $2R$. Each of the resistors R have equal resistances. In like manner, all of the resistors $2R$ have equal resistances, but their resistances are twice the values of the resistances of the resistors R .

5 Any combination of the digital inputs 242 may be connected selectively to 10.0 volts, or any other suitable voltage to represent a digital input 242 of "1," or connected to ground to represent a digital input 242 of "0". The resultant voltage output at the node 244 will be a function of the digital inputs 242, as determined by connecting selective ones of the inputs 242 to
10 10.0 volts or ground.

For example, with 10.0 volts applied to sixteen digital inputs 242, that is with sixteen digital inputs 242 equal to a digital "1," the digital input will be 65,535 which is one less than 2.0 to the 16th power, and the theoretical voltage output will be $(10 \times 65,535)/65,536 = 9.999847$.

15 Referring now to FIGURE 5, a voltage curve 250 illustrates some of the variations in output voltage vs. digital input that commonly occur with the prior-art D/A converter 240 of FIGURE 4.

While, in the discussion that follows, problems caused by error in resistances of the resistors $2R$ will be discussed, it should be apparent the errors
20 in the resistors R will also be involved, since each pair of R and $2R$ resistors outputs a voltage to the next higher bit.

At a digital input of 16,383, the first fourteen bits, or digital inputs, 242 are at "1". But at a digital input of 16,384, a fifteenth digital input 242 of FIGURE 4 is at "1" and the fourteen digital inputs 242 that were at "1" are now
25 at "0". Therefore, errors in resistances in the fourteen resistors $2R$ of FIGURE 4 that had inputted a digital 16,383 and whose errors in resistances may be accumulative either negatively or positively, are now connected to ground rather than to 10.0 volts, and a resistor $2R$ at the fifteenth bit 242 that represents a digital 16,384 is connected to 10.0 volts.

30 The change from the accumulative error of the fourteen resistors $2R$ that were connected to 10.0 volts to an error in a single, or fifteenth, resistor $2R$ being connected to the 10.0 volts may result in the voltage curve 250 stepping vertically up to a curve 252, or stepping vertically down to a curve 254 in response to a change from 16,383 to 16,384 in a digital input 242.

As a second example, at a digital input of 32,767, fifteen digital inputs 242 of FIGURE 4 are at "1". But at a digital input of 32,768, a sixteenth digital input 242 is at "1" and the fifteen inputs 242 that were at "1" are now at "0".

- 5 Therefore, errors in resistances in fifteen of the resistors 2R of FIGURE 4, that may be accumulative either negatively or positively, are now replaced by a single resistor 2R at the sixteenth bit 242.

- 10 This change from the accumulative error of the fifteen resistors 2R to an error in the single, or sixteenth, resistor 2R may result in the voltage curve 250 stepping vertically up to a curve 256, or stepping vertically down to a curve 258 in response to a change from 32,767 to 32,768 in a digital input.

- Referring now to FIGURES 6A and 6B, rather than the voltage output of the prior-art D/A converter 240 being in the form of a smooth curve, as illustrated in FIGURE 5, in actuality, an output voltage curve 260 steps
15 upwardly in steps 262 with each increase in a digital input. FIGURES 6A and 6B are included to teach the same truths as FIGURE 5, but illustrate them differently.

- As illustrated by the output voltage curve 260 of FIGURE 6A, a sharp increase 264 in output voltage may occur when a digital input of 32,767 is
20 increased to 32,768 and errors in fifteen resistors 2R are replaced by an error in a different resistor 2R at the sixteenth bit 242. In like manner, in FIGURE 6B, a sharp decrease 266 in an output voltage curve 268 may occur when a digital input is changed from 32,767 to 32,768 and the errors in fifteen resistors 2R are replaced by an error in a different resistor 2R at the sixteenth bit 242.

- 25 Referring now to FIGURE 7A, an output voltage curve 270 of the prior-art D/A converter 240 of FIGURE 4 shows how one or more holes may occur because of accumulative errors of the resistors 2R, and replacement by a single resistor 2R. A hole refers to a phenomena in which a certain digital address will result in an output voltage 272 that is lower than needed, and a digital
30 address that is one bit larger will result in an output voltage 274 that is too high.

Referring now to FIGURE 7B, an output voltage curve 276 of the prior-art D/A converter 240 of FIGURE 4 shows that, rather than producing holes, accumulative errors in the resistors R and 2R may produce duplicate

digital addresses. A duplicate digital address refers to a phenomena in which a desired output voltage can be obtained by either of two different digital addresses.

5 As an example, in the output voltage curve 276, as shown in FIGURE 7B, an output of 5.0 volts can be obtained by inputting a digital input of 32,668, or it can be obtained by inputting a digital input of 32,868. In like manner, in the present example, various voltages can be outputted in response to either of two digital inputs that are disposed between 32,668 and 32,868, as
10 can be seen by inspection of FIGURE 7B.

Referring again to FIGURES 4 and 5, the objective of prior-art D/A converters has been to convert digital inputs, in binary form, to output voltages that increase linearly with an increase in the digital input. As shown and described above, it has been difficult to produce D/A converters that do not
15 have holes. And the greater the number of bits in a given design, the more difficult and expensive it has been to build D/A converters that do not contain holes.

In contrast to prior-art D/A converters in which output linearity has been the design criteria, the present invention provides a nonlinear D/A
20 converter. In the discussion that follows it will become apparent that the nonlinear D/A converters of the present invention not only solve the problem of holes, but also provide apparatus that can be manufactured at much lower cost, and in which the number of bits can be increased without incurring either functional or cost limitations.

25 Referring now to FIGURE 8, a nonlinear D/A converter 280 includes a plurality of the resistors R, three of which are labeled R16, R15, and R14 to identify them with their respective bits, and a plurality of the resistors 2R, three of which are labeled 2R16, 2R15, and 2R14 to identify them with their respective bits. The resistors R are arranged as shown, with resistances of
30 resistors 2R nominally being twice as large as resistances of resistors R, as described in conjunction with FIGURE 4, a plurality of the digital inputs 242, and the output voltage node 244. However, in addition to resistors R and 2R, the nonlinear D/A converter 280 includes a plurality of resistors ΔR , three of

which are labeled ΔR_{16} , ΔR_{15} , and ΔR_{14} to identify them with their respective bits.

For the sake of simplicity, for the discussion that follows, reference to resistors will be made without individual bit designation. That is, R, 2R, and ΔR will be used to refer to resistors for all bits.

This series arrangement of resistors 2R with ΔR illustrates the use, in an actual design, of resistors 2R with resistances, whether fixed or variable, that are greater than twice the resistance of the resistors R.

The effect of increasing the resistances of the resistors 2R, is to insert dual addresses, as shown in FIGURE 7B, at each bit 242 wherein the resistances of the respective resistors 2R have been increased, thereby eliminating any possibility of holes.

As can be appreciated, as the number of bits 242 increase in response to increasing digital inputs 242, and the number of resistors 2R that are used to convert the digital number increases, accumulative errors in the resistors 2R can cause holes that more seriously effect D/A conversion. Therefore, while it may not be necessary to use the resistors ΔR for all bits, a sufficient number must be included to prevent holes, or to avoid the expense of providing, or matching, the resistors precisely enough to prevent holes.

Ideally, each higher bit will produce a slightly smaller voltage than the sum of all smaller bits. Thus, it can be seen that resistances of each of the resistors ΔR will not necessarily be equal. And, since the resistances of the ΔR resistors merely symbolize increasing of resistances of the resistors 2R, it becomes apparent that the resistors 2R may not be equal.

Optionally, rather than increasing resistances of the resistors 2R, decreasing resistances of some, or all, of the resistors R will also produce a nonlinear D/A converter as taught herein. And, it becomes apparent that the resistances of all of the resistors R may not necessarily be equal. Instead, in accordance with individualized design criteria, resistances of all of the resistors, R and 2R, may be computer determined.

Referring now to FIGURES 4 and 9, the D/A converter 240 of FIGURE 4 produces an output voltage curve 284 of FIGURE 9 that is, at least theoretically, linearly proportional to digital inputs 242, but that may have a

plurality of holes as described in conjunction with FIGURES 6A and 7A, or duplicate addresses, as described in conjunction with FIGURES 6B and 7B, depending upon actual resistances of the resistors R and 2R and their
5 accumulative resistances.

Referring now to FIGURES 7B, 8, and 10, but more particularly to FIGURE 10, if the resistances of all of the resistors 2R are increased, an output voltage curve 288, rather than being linear, will slope downwardly, as shown.

In some applications, such as with the phase-locked oscillators 112 and
10 200, the presence of holes can cause the loop to "hunt," since at one address the voltage output will be too low, and the very next higher address will result in a voltage that is excessively high. The D/A converter 280 of the present invention eliminates any possibility of holes.

While the voltage output of the D/A converter 280 is intentionally
15 nonlinear, it should be recognized that, in adaptive systems, such as the frequency-hopping oscillators 60 and 310 described herein, nonlinearity of components, such as the D/A converter 84 has no effect on the precision of the system. In contrast, holes in the voltage output can degrade preciseness of any adaptive system seriously.

The D/A converter 280 of FIGURE 8 may be constructed with
20 resistances of resistors R increased by resistances of resistors ΔR for all sixteen bits 242. If so, resistors that are less precise than those commonly used in 12-bit D/A converters, and therefore more economical, can be used.

Or, since it is not particularly difficult to build 8-bit A/D converters that
25 do not contain holes, the present invention may be practiced by custom manufacturing of a 16-bit A/D converter in which only the higher bits include resistances that are equal to resistors R plus ΔR .

Referring now to FIGURE 11, a 16-bit D/A converter 292 includes a 12-bit D/A converter 294 with twelve lower bits, or twelve digital inputs, 296, a 4-bit D/A converter 298 with four higher bits, or four higher digital inputs, 300,
30 an analog scaler/summer 302, and an output node 304.

First, assume that the 16-bit converter 292 is a conventional D/A converter 240 as described in conjunction with FIGURE 7, and assume 65,536

volts as a digital "1" for the digital inputs, 296 and 300. Since there are 65,536 steps in a sixteen-bit D/A converter, each step would be 1.0 millivolt per step.

A maximum voltage output of the 12-bit D/A converter 294 occurs
5 when all twelve digital inputs 296 are a digital "1." At this time, the digital input is 4,095. Therefore, the output voltage is $4,095 \text{ bits} \times 1.0 \text{ millivolt per bit} = 4.095 \text{ volts}$.

When separate ones of the thirteenth, fourteenth, fifteenth, and
sixteenth bits 300 are at a digital "1", the digital inputs are 4,096, 8,192,
10 16,384, and 32,768, respectively. Thus, it can be seen that each of the four higher digital inputs 300 doubles the voltage output.

It follows that, if the 12-bit D/A converter 294 produces less than 4.095
volts, there will be a hole when the digital input is increased by one, and a
digital "1" at one of the thirteen bits 300 of the 4-bit D/A converter 298
15 replaces twelve bits 296 of the 12-bit D/A converter 294.

However, in the 16-bit D/A converter 292 of FIGURE 11, the analog
scaler/summer 302 is used to scale an output voltage in a conductor 306 of the
4-bit D/A converter 298 to any suitable value lower than 4.095 volts. For
instance, if the analog scaler/summer 302 decreases the steps produced by the
20 4-bit D/A converter 298 from 4.095 volts to 3.0 volts, as 3.0 volt increments are added to output voltages of the 12-bit D/A converter 294 that extend up to a maximum of approximately 4.095 volts, any possibility of holes in the four higher bits 300 is eliminated. Instead of the possibility of any holes, there are duplicate digital addresses that will produce the same output voltage, similarly
25 to those shown and described in conjunction with FIGURE 7B.

In the example above, to reach any output voltage between 3.0 and
4.095, the 4-bit D/A converter 298 can have an output of either 0.0 or 3.0
volts. If the output of the 4-bit D/A converter 298 is 0.0 volts, the output of
the 12-bit D/A converter 294 will range from 0.0 to 4.095 volts, but if the
30 output of the 4-bit D/A converter 298 is 3.0 volts, the output of the 12-bit D/A converter 294 will range from 0.0 to 1.095 volts.

Referring now to FIGURES 8, 10, and 11, and summarizing the D/A
converters 280 and 292, in stark contrast to prior-art D/A converters, the D/A
converters 280 and 292 are designed to produce nonlinear outputs in response

to digital inputs. In the D/A converters 280 and 292 holes are eliminated by intentionally providing dual digital addresses that are of sufficient size that resistor tolerances cannot eliminate them. These dual digital addresses are
5 provided by scaling steps 262 of FIGURE 6B in the output voltage 260 of one bit, 242 or 300, lower than a voltage output produces when all lower bits, 242 or 296, are at a digital "1".

In the D/A converter 280 this scaling is done by changing ratios of one or more of the resistors R and/or 2R. In the D/A converter 292 some of the
10 higher bits 300 are scaled before summing with output voltages of the lower bits 296. Alternately, rather than changing resistances of resistors R and/or 2R, input voltages to some of the higher bits 242 can be scaled. That is, the phase locked oscillator 61 of FIGURES 3 or 12 that utilizes D/A conversion could practice the present invention by scaling input voltages to some of the higher
15 bits 242.

It follows that, even if very-low quality resistors are used, if voltage outputs are scaled as the number of the bit increases, as taught herein, D/A converters can be constructed with any desired number of bits without any danger of holes existing in output voltages.

20 Finally, any adaptive or learning system, or any other electronic system that utilizes a D/A converter, can practice the present invention by scaling output voltages for some of the higher bits, or all of the bits, by any of the means taught herein.

Referring now to FIGURE 12, an adaptive frequency-hopping oscillator, or adaptive system, 310 includes components as identified in conjunction with
25 the adaptive frequency-hopping oscillator 60 of FIGURE 3, except as included in the following description.

A PROM 312 is preloaded with channelizing information such that when this channelizing information is converted to an analog channelizing
30 voltage via the D/A converter 84, the output frequency of the frequency-hopping oscillator 310 will be near phase lock.

The channelizing information that is preloaded into the PROM 312 may be values that will produce output frequencies having nominal, or handbook, performance characteristics, but that will produce output frequencies
35 that vary

in accordance with actual variations in proportionality and linearity of the D/A converter 84, the combiner/amplifier/offsetter 94, and the VCO 22. Even though the values of the channelizing information that are burned into the
5 PROM 312 are only average values, several seconds in achieving phase lock at start-up is saved by the PROM 312.

If the PROM 312 is of the electrically-erasable type, the PROM 312 may be manually programmed, starting from an average value, to produce a zero output from a RAM 314. Or, if the RAM 314 includes sixteen bits or
10 more, the frequency-hopping oscillator 310 may be run through all channelized frequencies, and then the phase-locking values of the channelizing information that developed in the RAM 314 may be duplicated in the PROM 312, thereby extending the adaptive characteristics of the frequency-hopping oscillator 310 to the PROM 312.

15 Starting with the PROM 312 loaded by any suitable method, such as any of the three described above, if, upon start-up, the VCO 22 is operating at too low an output frequency, for a given channel, to phase lock with the reference oscillator 12, the decoder 78 commands a parallel adder 316 to place digitalized frequency-correcting information into the RAM 314. Then the
20 contents of the RAM 314 are added to the digital output of the PROM 312 by a parallel adder 318. The result is an analog channelizing voltage, as produced by the D/A converter 84, driving the VCO 22 to phase lock.

Preferably, the PROM 312 is, at least, a 16-bit device. However, unless the RAM 314 is used to determine the channelizing information that is
25 to be burned into the PROM 312, the RAM 314 may be an 8-bit device. Or, it may include even fewer bits, since it will need to store only frequency-correction information that supplements that of the PROM 312.

In summary, the present invention provides not only improved phase-locked oscillators, improved frequency-hopping oscillators, and an improved D/A converter in which holes are eliminated, but also adaptive phase-locked
5 oscillators and adaptive frequency-hopping oscillators with D/A converters that are free from holes in output voltages.

It should be understood that channelizing information may be developed, as taught in FIGURE 3; or it may be information that has been obtained from some source, and is merely stored, as taught in FIGURE 12.

10 When channelizing information has been developed by frequency-correction information to the point that the channelizing information will drive the output frequency to almost phase lock, it is proper to call it corrected channelizing information.

Frequency-correcting information may be a single sample provided by a
15 phase comparison step. Or as in FIGURE 12, frequency-correction information may be made up of successively-summed and stored frequency-correction information, that when recovered from storage, such as from the RAM 314, and used in conjunction with approximate channelizing information, such as stored in the PROM 312, will drive an output frequency very near to phase lock.

20 Referring finally to FIGURES 3 and 12, the phase detector 62 produces UP and DOWN signals, the decoder 82 converts the UP/DOWN signals into +1, 0, and -1 signals. That is, the decoder 82 produces an output that tells the RAM, 82 of FIGURE 3 or 314 of FIGURE 4 whether to add pulses, subtract pulses, or do nothing. Saying it another way, the decoder produces increment,
25 do-nothing, and decrement signals.

The RAMS, 82 and 314, are pulsed by the sampling rate conductor 88 at the frequency of the reference oscillator, and pulses are algebraically summed into the RAM, 82 or 314 at the frequency of the reference oscillator.

If, for instance, the reference oscillator 12 is producing a frequency of
30 62,500 Hertz, and if the phase locking oscillator 61 is not at phase lock after hopping to a new channel in response to previously-stored channelizing information, a frequency-correction pulse is algebraically summed into the RAM, 82 or 314, in intervals of about 0.00002 seconds.

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The decoder 78 provides means for developing increment/decrement signals, which are +1 and -1, as a function of the feedback frequency. The parallel adder, 80 or 316, the RAM, 82 or 314, and the reference oscillator 12 provide means for algebraic-sum storing increment/decrement pulses as a function of the increment/decrement signals, and at the speed of the reference oscillator 12. The RAM, 82 or 314, and the D/A converter 84 provide means for driving the output frequency progressively closer to phase lock with the reference frequency in response to the algebraic-sum stored pulses.

Alternately, the decoder 78, the parallel adder, 80 or 316, the RAM, 82 or 314, and the reference oscillator 12 provide means for algebraic-sum storing increment/decrement pulses as a function of the feedback frequency, and at the speed of the reference oscillator 12.

The means, 78, for developing increment/decrement signals as a function of the feedback frequency includes means for developing "0" or "do-nothing" signals when the feedback frequency phase locks with the reference frequency, so that pulses are neither added to, nor subtracted from, the RAM, 82 or 314, when phase lock occurs.

In like manner, the means, 78, 80, and 82, or 78, 316, and 314, for storing increment/decrement pulses as a function of the feedback frequency includes means for developing "0" or "do-nothing" signals when the feedback frequency phase locks with the reference frequency, so that pulses are neither added to, nor subtracted from, the RAM, 82 or 314, when phase lock occurs.

Generation of frequency-correcting information is via a learning path 324 of FIGURE 3 and a learning path 328 of FIGURE 12. The learning path, 324 or 328, includes components of a system that function together to provide frequency-correction information, thereby providing an adaptive system that compensates for lack in precision in proportionality and/or linearity and temperature drift in components that include analog inputs or outputs.

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The learning path 324 of FIGURE 3 includes the phase detector 62, the decoder 78, the parallel adder 80, the RAM 82, the D/A converter 84, the low-pass filter 86, the combiner/amplifier/offsetter 94, the VCO 22, and the
5 feedback path 104.

The learning path 328 of FIGURE 12 includes the phase detector 62, the decoder 78, the parallel adder 316, the RAM 314, the parallel adder 318, the D/A converter 84, the low-pass filter 86, the combiner/amplifier/offsetter 94, the VCO 22, and the feedback path 104.

10 When the D/A converter, 280 or 292 is included in the learning path, 324 or 328, a learning system is provided in which: "holes" in output voltages, as shown in FIGURES 6A and 7A, are eliminated; dual digital addresses for the same output voltage are provided, as shown in FIGURES 6B and 7B; the output
15 voltage of a higher bit is less than the total output voltage of all remaining lower bits; the output voltage of a higher bit is less than twice the voltage output of the next lower bit; the voltage output is nonlinear and a decreasing ratio of digital inputs, as shown in FIGURE 10; and the D/A converters, 280 and 292, can be manufactured using low cost resistors with relatively-large variations in resistances.

20 While specific apparatus and method have been disclosed in the preceding description, and while part numbers have been inserted parenthetically into the claims to facilitate understanding of the claims, it should be understood that these specifics have been given for the purpose of disclosing the principles of the present invention and that many variations thereof will
25 become apparent to those who are versed in the art. Therefore, the scope of the present invention is to be determined by the appended claims, and without any limitation by the part numbers inserted parenthetically in the claims.

INDUSTRIAL APPLICABILITY

The present invention is applicable to oscillators, transmitters,
30 receivers, adaptive learning devices, and other devices in which rapid and accurate channelizing of output frequencies is a necessity.

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CLAIMS

WHAT IS CLAIMED IS:

1. A method for successively producing selected ones of channelized
5 output frequencies, which method comprises:
- a) comparing a feedback frequency with a reference frequency for one of said channelized output frequencies;
 - b) developing increment/decrement signals in response to said comparing step;
 - 10 c) algebraic-sum storing increment/decrement pulses as a function of said increment/decrement signals; and
 - d) driving said output frequency progressively closer to phase lock with said reference frequency in response to said algebraic-sum stored pulses substantially simultaneous with said algebraic-sum storing step.
- 15 2. A method for successively producing channelized output frequencies without interposing a storing step between selected ones of said channelized output frequencies, which method comprises:
- a) comparing a feedback frequency with a reference frequency for one of said channelized output frequencies;
 - 20 b) algebraic-sum storing increment/decrement pulses as a function of said comparing step;
 - c) driving said output frequency progressively closer to phase lock with said reference frequency in response to said algebraic-sum stored pulses substantially simultaneous with said algebraic-sum storing step; and
 - 25 d) driving said output frequency toward said phase lock for a second one of said channelized output frequencies in response to previously-stored channelizing information without interposing a storing step between said driving steps.
3. A method for rapidly and accurately producing selected ones of
30 channelized output frequencies, which method comprises:
- a) recalling previously-stored channelizing information for one of said channelized output frequencies;

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b) driving said output frequency toward phase lock with a reference frequency in response to said recalled channelizing information;

c) comparing a feedback frequency with said reference frequency;

5 d) algebraic-sum storing increment/decrement pulses as a function of said comparing step; and

e) driving said output frequency progressively closer to said phase lock with said reference frequency in response to said algebraic-sum stored pulses substantially simultaneous with said algebraic-sum storing step.

10 5. A method as claimed in Claims 1, 2, or 3 in which:

a) said method further comprises D/A converting said algebraic-sum stored pulses substantially simultaneous with said algebraic-sum storing step; and

15 b) said step of driving said output frequency progressively closer in response to said algebraic-sum stored pulses comprises driving said output frequency in response to said D/A converted pulses.

7. A method as claimed in Claims 1 or 2 in which said method further comprises battery-maintaining said algebraic-sum stored pulses.

20 8. A method as claimed in Claim 3 in which said method comprises nonvolatile storing of said channelizing information.

9. A method as claimed in Claims 1 or 2 in which:

a) said method further comprises storing channelizing information, recalling said stored channelizing information, and driving said output frequency toward said phase lock, all prior to said comparing step; and

25 b) said algebraic-summing step comprises algebraic-sum storing said pulses with said stored channelizing information.

10. A method as claimed in Claim 3 in which said algebraic-summing step comprises storing said pulses separately from said previously-stored channelizing information.

11. A method as claimed in Claims 1, 2, or 3 in which:

a) said method further comprises D/A converting said algebraic-sum stored pulses substantially simultaneous with said algebraic-sum storing step;

5 b) said D/A converting step comprises providing dual addresses for a plurality of output voltages; and

c) said step of driving said output frequency progressively closer in response to said algebraic-sum stored pulses comprises driving said output frequency in response to said D/A converted pulses.

10 12. A method as claimed in Claims 1, 2, or 3 in which:

a) said method further comprises D/A converting said algebraic-sum stored increment/decrement pulses substantially simultaneous with said algebraic-sum storing step;

15 b) said D/A converting step comprises making voltage-output steps of respective ones of higher bits lower than a maximum total voltage output of all lower bits; and

c) said step of driving said output frequency progressively closer in response to said algebraic-sum stored pulses comprises driving said output frequency in response to said D/A converted pulses.

20 13. A method as claimed in Claims 1, 2, or 3 in which said method further comprises:

a) developing digital lead-compensation information;

25 b) analog summing said digital lead-compensation information and said algebraic-sum stored pulses substantially simultaneous with said algebraic-sum storing step; and

c) said step of driving said output frequency progressively closer in response to said algebraic-sum stored pulses comprises driving said output frequency in response to said analog summing step.

14. A method as claimed in Claim 3 in which:

30 a) said method further comprises nonvolatile storing channelizing information prior to said recalling step;

b) said algebraic-sum storing of pulses comprises storing separately from said stored channelizing information;

5 c) said method further comprises D/A converting said algebraic-sum stored increment/decrement pulses substantially simultaneous with said algebraic-sum storing step;

d) said D/A converting step comprises making voltage-output steps of respective ones of higher bits lower than a maximum total voltage output of all lower bits; and

10 e) said step of driving said output frequency progressively closer in response to said algebraic-sum stored pulses comprises driving said output frequency in response to said D/A converted pulses.

15. A method as claimed in Claims 1, 2, or 3 in which:

15 a) said step of driving said output frequency progressively closer comprises D/A converting said algebraic-sum stored pulses substantially simultaneous with said algebraic-sum storing step; and

b) said D/A converting step comprises making a plurality of higher bits each produce an output voltage that is less than twice that of the next lower bit.

20 21. A method as claimed in Claims 1 or 3 in which said method further comprises lead compensating said step of driving said output frequency progressively closer.

22. A method as claimed in Claims 1, 2, or 3 in which said method further comprises:

25 a) decoding digital lead-compensation information as a function of said comparing step; and

b) lead compensating said output frequency in response to said decoding step.

23. A method as claimed in Claims 1, 2, or 3 in which said method further comprises:

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- a) D/A converting said digitally-stored pulses substantially simultaneous with said storing step thereof;
- b) decoding digital lead-compensation information;
- 5 c) D/A converting said lead-compensation information;
- d) analog summing said D/A converted lead-compensation information and said D/A converted pulses; and
- e) said step of driving said output frequency progressively closer comprises using said analog summed D/A lead-compensation information and
- 10 said converted pulses.

24. Apparatus (60 or 310) for rapidly producing channelized output frequencies which comprises means (64) for channelizing a feedback frequency into a plurality of output frequencies, the improvement in which producing one of said output frequencies comprises:

15 means (62), for comparing said feedback frequency with a reference frequency;

means (78), being operatively connected to said means for comparing, for developing increment/decrement signals as a function of said feedback frequency;

20 means (80 and 82, or 316 and 314) for algebraic-sum storing increment/decrement pulses as a function of said increment/decrement signals; and

means (82 and 84, or 314 and 84) for driving said output frequency progressively closer to phase lock with said reference frequency in response to

25 said algebraic-sum-stored pulses.

25. Apparatus (60 or 310) for rapidly producing channelized output frequencies which comprises means (64) for channelizing a feedback frequency into a plurality of output frequencies, the improvement which comprises:

means (62) for comparing said feedback frequency with a reference

30 frequency for one of said channelized output frequencies;

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means (78, 80, and 82, or 78, 316, and 314), being operatively connected to said means for comparing, for algebraic-sum storing increment/decrement pulses as a function of said feedback frequency;

5 means (82 and 84, or 314 and 84) for driving said output frequency for said one channelized output frequency progressively closer to phase lock with said reference frequency in response to said algebraic-sum-stored pulses; and

means, comprising said means for algebraic-sum storing, for holding in digital storage, immediately prior to a change in channelizing said feedback frequency, channelizing information developed from producing said one output frequency.

26. Apparatus (60 or 310) for rapidly producing channelized output frequencies in response to stored and subsequently-recalled channelizing information, the improvement which comprises:

15 means (82 and 84, or 314 and 84) for driving said output frequency toward phase lock with a reference frequency for one of said channelized output frequencies, in response to said recalled channelizing information;

means (62) for comparing a feedback frequency with said reference frequency for said one channelized output frequency;

20 means (78, 80, and 82, or 78, 316, and 314), being operatively connected to said means for comparing, for algebraic-sum storing increment/decrement pulses as a function of said feedback frequency; and

means (82 and 84, or 314 and 84) for driving said output frequency for said one channelized output frequency progressively closer to said phase lock with said reference frequency in response to said algebraic-sum stored pulses.

30. Apparatus (60) as claimed in Claims 24, 25, or 26 in which:

said means for driving said output frequency progressively closer comprises a D/A converter (280) that is operatively connected to said means for algebraic-sum storing; and

said D/A converter comprises means (R, 2R, ΔR_{16} , ΔR_{15} , or ΔR_{16}) for making a voltage output of a plurality of higher bits less than twice that of the next lower bit.

5 33. Apparatus (60 or 310) as claimed in Claims 24, 25, or 26 in which:
said means for algebraic-sum storing comprises a parallel adder (80 or 316) and a RAM (82 or 314); and

said apparatus further comprises means, comprising a lead compensator (70), for lead compensating said progressive driving of said output frequency.

10 34. Apparatus (60 or 310) as claimed in Claims 24, 25, or 26 in which
said means for producing said channelized output frequencies comprises means (95) for digitally developing a lead-compensating signal.

 35. Apparatus (60) as claimed in Claims 24, 25, or 26 in which:
said means for progressively driving said output frequency comprises a
15 D/A converter (280) that is operatively connected to said means (82 or 314) for algebraic-sum storing; and

said D/A converter comprises means (R, 2R, ΔR_{16} , ΔR_{15} , ΔR_{14}) for providing an output voltage that is a decreasing ratio of digital inputs.

 36. Apparatus (60 or 310) as claimed in Claim 24 in which:
20 said means for comparing comprises a phase detector (62) that is operatively connected to said reference frequency and to said feedback frequency;

said means for developing increment/decrement signals comprises a pulse decoder (78) that is operatively connected to said phase comparator;

25 said means for algebraic-sum storing comprises a parallel adder (80 or 316) that is operatively connected to said pulse decoder, and a RAM (82 or 314) that is operatively connected to said parallel adder; and

means (95), being operatively connected to said phase comparator, for digitally developing a lead-compensator signal.

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37. Apparatus (60) as claimed in Claims 24, 25, or 26 in which:
said means for progressively driving said output frequency comprises a
D/A converter (280) that is operatively connected to said means (82 or 314) for
5 algebraic-sum storing; and

said D/A converter comprises means (R, 2R, ΔR_{16} , ΔR_{15} , ΔR_{14}) for
providing voltage steps for respective ones of a plurality of higher bits that are
smaller than a maximum total voltage generated by all lower bits.

38. A method for phase locking an output frequency to a reference
10 frequency, which method comprises:

a) comparing a feedback frequency with said reference frequency;
b) developing increment/decrement signals in response to said
comparing step;

c) driving said output frequency progressively closer to phase lock with
15 said reference frequency as a function of said increment/decrement signals;

d) digitally-developing a lead-compensation signal; and

e) lead compensating said progressive driving step in response to said
lead-compensation signal.

39. A method as claimed in Claim 38 in which:

20 a) said progressive driving step comprises D/A converting subsequent to
said developing step and prior to said driving step; and

b) said D/A converting step comprises making output voltage steps of
respective ones of higher bits lower than a total voltage output of all lower bits.

40. A method as claimed in Claim 38 in which:

25 a) said progressive driving step comprises D/A converting subsequent to
said developing step and prior to said driving step; and

b) said D/A converting step comprises making output voltages of each
of a plurality of higher bits less than twice an output voltage of the next lower
bit.

41. A phase-locked oscillator (61) which comprises a reference oscillator (12) that produces a reference frequency, a phase comparator (62) that is operatively connected to said reference oscillator, a forward path (102) that includes a radio-frequency oscillator (22) and that extends from said phase comparator to an output of said radio-frequency oscillator, and a feedback path (104) that extends from said output of said radio-frequency oscillator to said comparator, the improvement which comprises:

a digital integrator (68) being interposed into said forward path intermediate of said phase comparator and said radio-frequency oscillator; and
lead-compensator means (70), being operatively interposed into said forward path intermediate of said phase comparator and said radio-frequency oscillator, for lead compensating said digital integrator.

42. A phase-locked oscillator (61) as claimed in Claim 41 in which said integrator (68) comprises:

a decoder (78) that is operatively connected to said phase comparator and to said reference frequency; and

a parallel adder (80 or 316) that is operatively connected to said decoder.

43. A phase-locked oscillator (61) as claimed in Claims 41 or 42 in which said phase-locked oscillator comprises a D/A converter (84) being interposed into said forward path (102); and

said D/A converter comprises means (R, 2R, ΔR_{16} , ΔR_{15} , ΔR_{14} , or 302) for providing voltage steps for respective ones of a plurality of higher bits that are each smaller than a maximum total voltage generated by all lower bits.

44. A method for phase locking an output frequency to a reference frequency comprises:

a) D/A converting; and

b) making output voltages of a plurality of higher bits of said D/A converting step less than twice an output voltage of the next lower bit

45. A phase-locked oscillator (61 or 112) having both a forward path (102 or 156) and a feedback path (104 or 158), the improvement which comprises:

5 a D/A converter (84 or 126) being interposed into one of said paths;
and

 means (R, 2R, ΔR_{16} , ΔR_{15} , ΔR_{14} , or 302) for making voltage steps for respective ones of a plurality of higher bits (242 or 300) of said D/A converter smaller than a maximum total voltage for all lower bits.

10 46. A learning method comprises:

 a) D/A converting; and

 b) making voltage-output steps of respective ones of a plurality of higher bits of said D/A converting step less than twice an output of the next lower bit.

15 47. An adaptive system (60, 110, or 310) having a learning path (324, 326, or 328), the improvement which comprises:

 a D/A converter (84 or 126) being interposed into said learning path;
and

 means (R, 2R, ΔR_{16} , ΔR_{15} , ΔR_{14} , or 302) for making voltage steps for
20 respective ones of a plurality of higher bits (242 or 300) of said D/A converter smaller than a maximum total voltage for all lower bits.

 48. A method which comprises:

 a) D/A converting digital bits into an analog output voltage; and

 b) making output-voltage steps for each of respective ones of a plurality
25 of higher bits lower than a maximum total voltage output of all lower bits.

 49. A method as claimed in Claim 48 in which said making step comprises applying a lower input voltage to said plurality of higher bits.

 50. A method as claimed in Claim 48 in which said making step comprises selectively proportioning resistances for said D/A converting step.

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51. A method as claimed in Claim 48 in which:

a) said D/A converting step comprises separately D/A converting said higher bits into a first output voltage;

5 b) said D/A converting step further comprises separately D/A converting said lower bits into a second output voltage;

c) said making step comprises applying different input voltages to said higher bits; and

10 d) said method further comprises summing voltage outputs of said separate D/A converting steps.

52. A method as claimed in Claim 48 in which:

a) said D/A converting step comprises separately D/A converting said higher bits into first output voltages;

15 b) said D/A converting step further comprises separately D/A converting said lower bits into second output voltages;

c) said making step comprises selectively proportioning resistances for one of said separate D/A converting steps; and

d) said method further comprises summing voltage outputs of said separate D/A converting steps.

20 53. A D/A converter (280 or 292) which comprises:

means, comprising a plurality of higher bits (242 or 300) and a plurality of lower bits (242 or 296), for producing output voltages as a function of digital inputs; and

25 means (R, 2R, ΔR_{16} , ΔR_{15} , ΔR_{14} , or 302) for making output-voltage steps for each of respective ones of said higher bits (242 or 300) smaller than a maximum total voltage output of all lower bits (242 or 296).

54. A D/A converter (280 or 292) as claimed in Claim 53 in which said means for making said output-voltage steps smaller for said higher bits (242 or 300) comprises means for applying lower voltages to said higher bits.

55. A D/A converter (280) as claimed in Claim 53 in which:
said D/A converter comprises a pair of resistors (R and 2R) for each of
said bits;

5 each pair of said resistors includes a predetermined resistance ratio; and
 said means for making said output-voltage steps smaller for said higher
bits (242) comprises means (R, 2R, ΔR_{16} , ΔR_{15} , ΔR_{14}) for changing said ratio
for some of said bits.

56. A D/A converter (292) as claimed in Claim 53 in which:
10 said D/A converter comprises a higher-bit D/A converter (298) for said
higher bits (300), a lower-bit D/A converter (294) for said lower bits (296), and
means (302) for summing voltage outputs of said higher-bit and lower-bit D/A
converters; and
 said means (302) for making said output-voltage steps smaller for said
15 higher bits comprises means for applying lower voltages to said higher-bit D/A
converter.

57. A D/A converter (292) as claimed in Claim 53 in which:
 said D/A converter comprises a higher-bit D/A converter (298) for said
higher bits (300), a lower-bit D/A converter (294) for said lower bits (296), and
20 means (302) for summing voltage outputs of said higher-bit and lower-bit D/A
converters; and
 said means (302) for making said output-voltage steps smaller for said
higher bits comprises means (302) for proportioning said output-voltage steps of
said higher-bit D/A converter.

25 58. A D/A converter (292) as claimed in Claim 53 in which:
 said D/A converter comprises a higher-bit D/A converter (298) for said
higher bits (300), a lower-bit D/A converter (294) for said lower bits (296), and
means (302) for summing voltage outputs of said higher-bit and lower-bit D/A
converters;
30 said higher-bit D/A converter comprises a pair of resistors (R and 2R)
for each of said bits, and each pair of said resistors includes a first
predetermined resistance ratio;

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said lower-bit D/A converter comprises a pair of resistors (R and 2R) for each of said bits, and each pair of said resistors includes a second predetermined resistance ratio; and

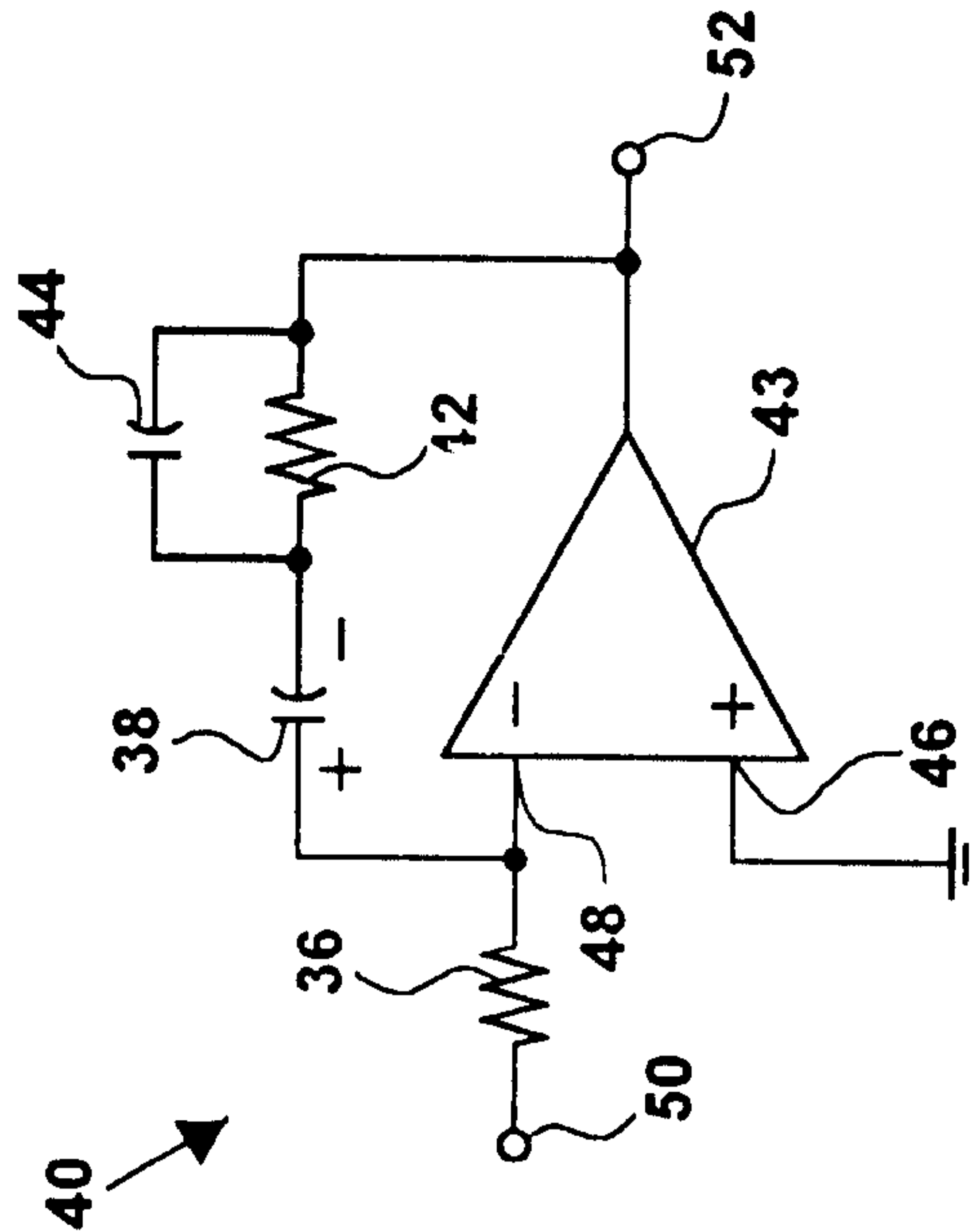
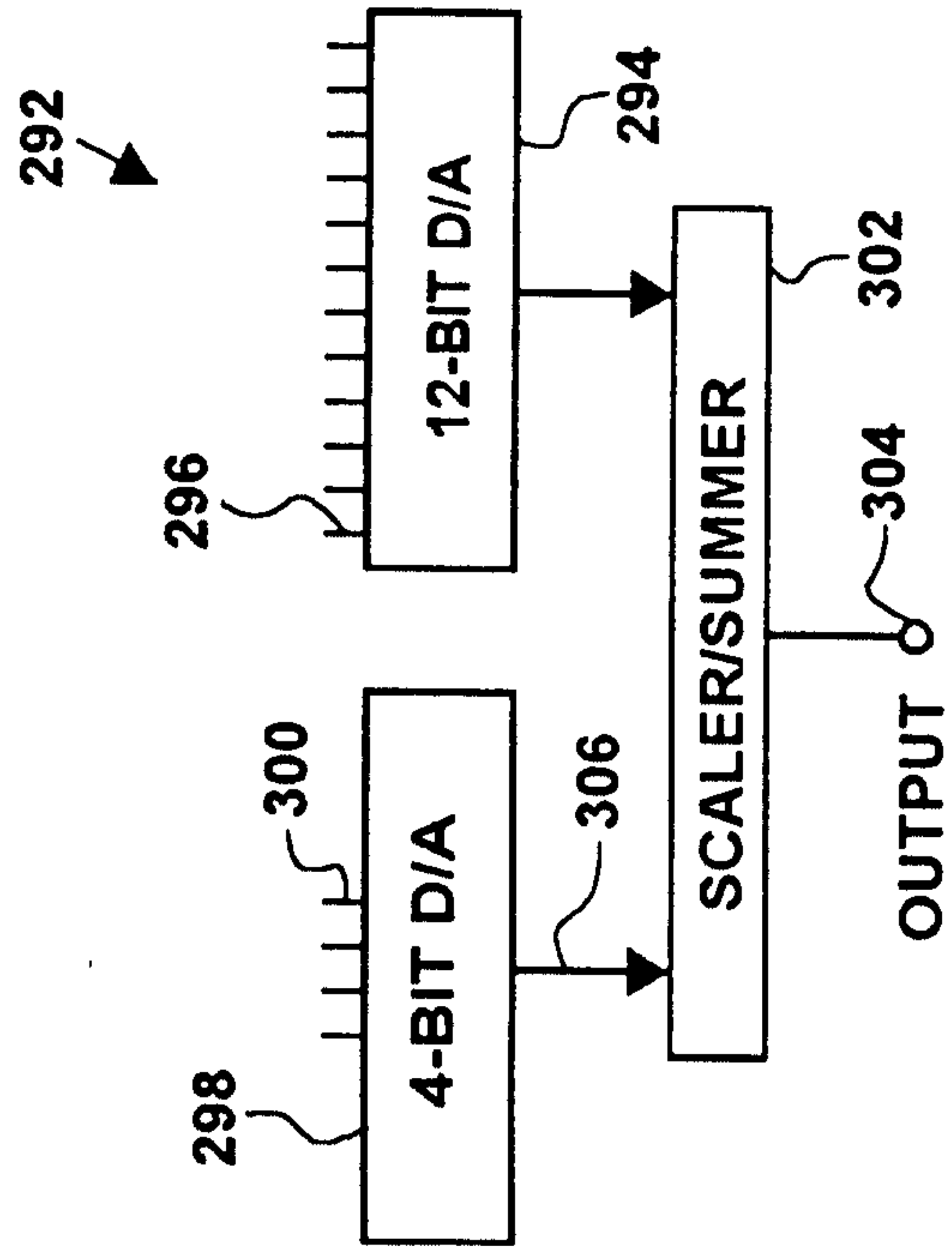
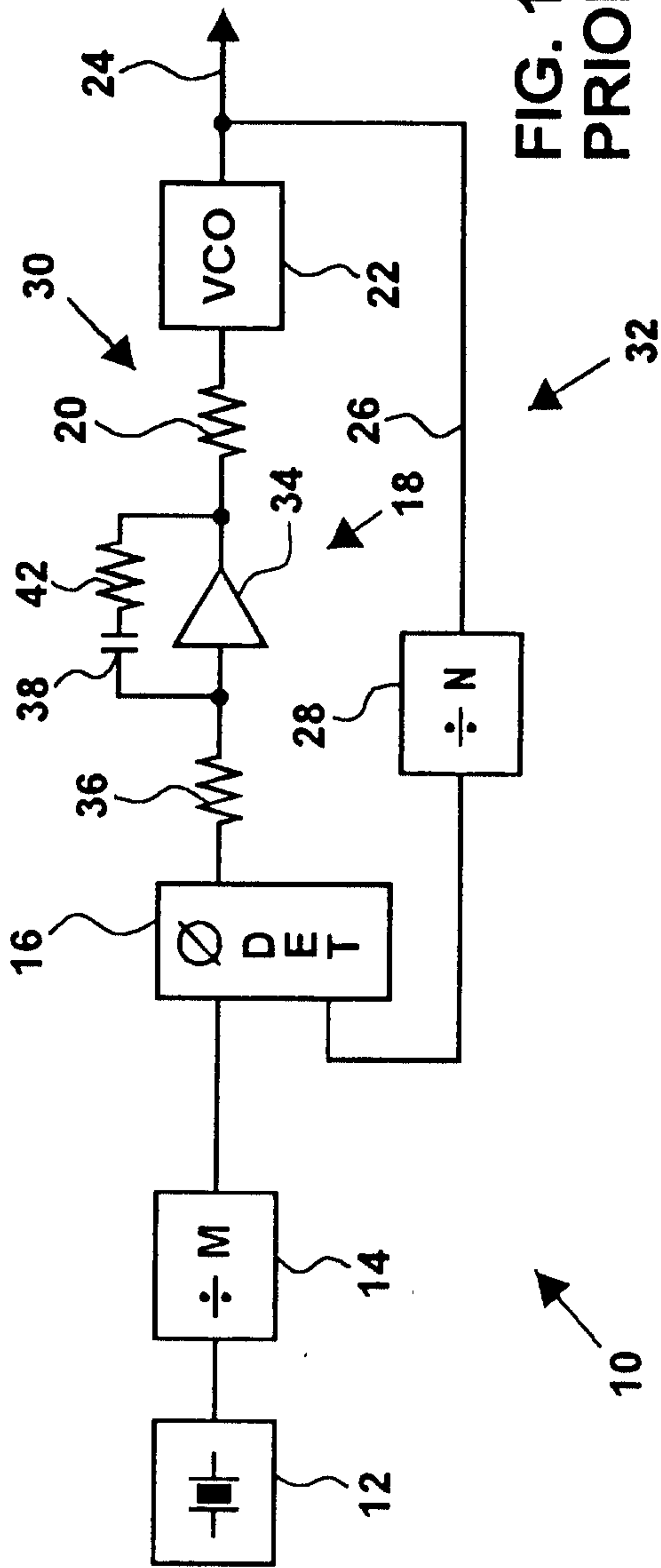
5 said means for making said output-voltage steps smaller for said higher bits comprises means (302) for making said first ratio different than said second ratio.

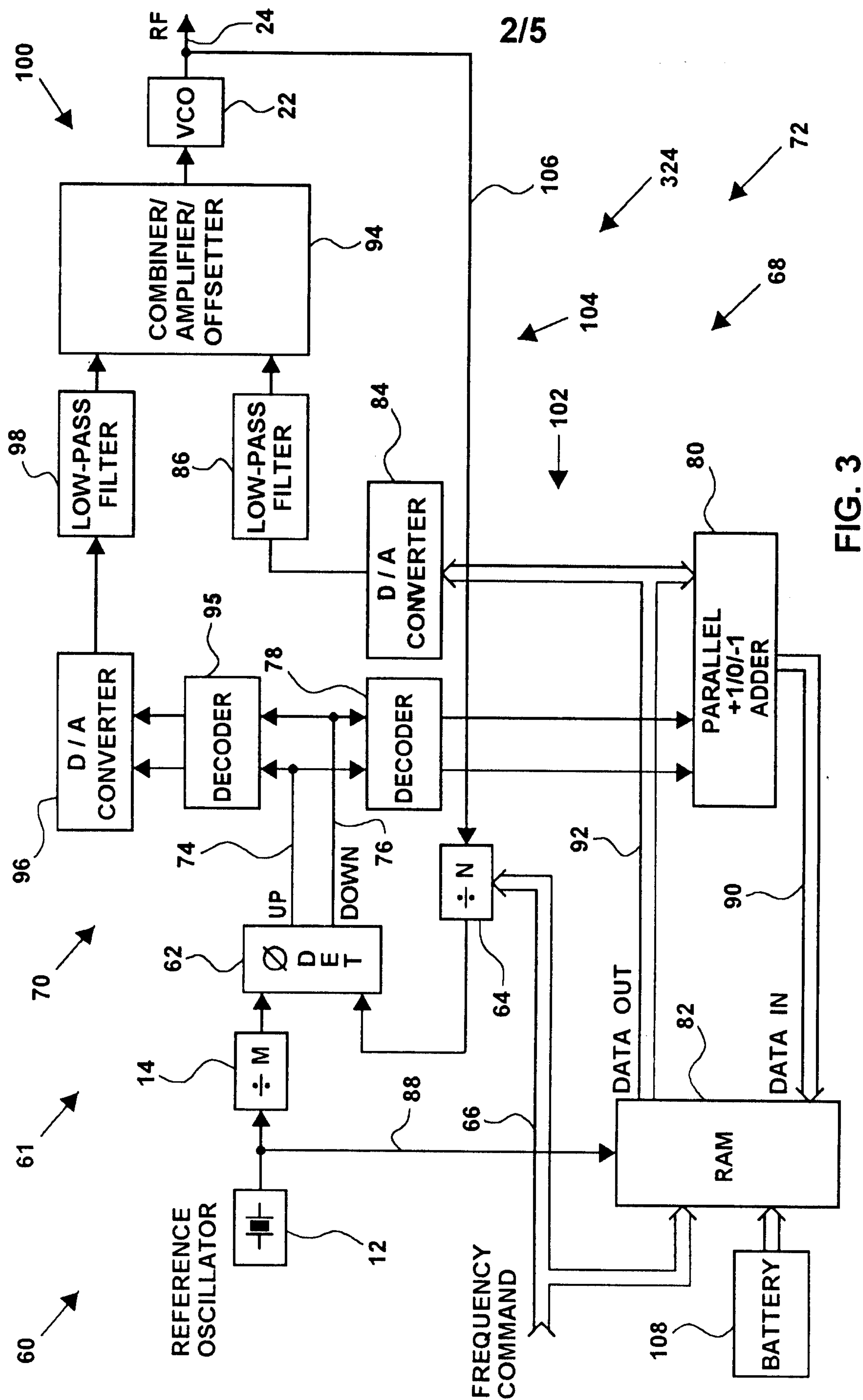
59. A D/A converter (280 or 292) which comprises:

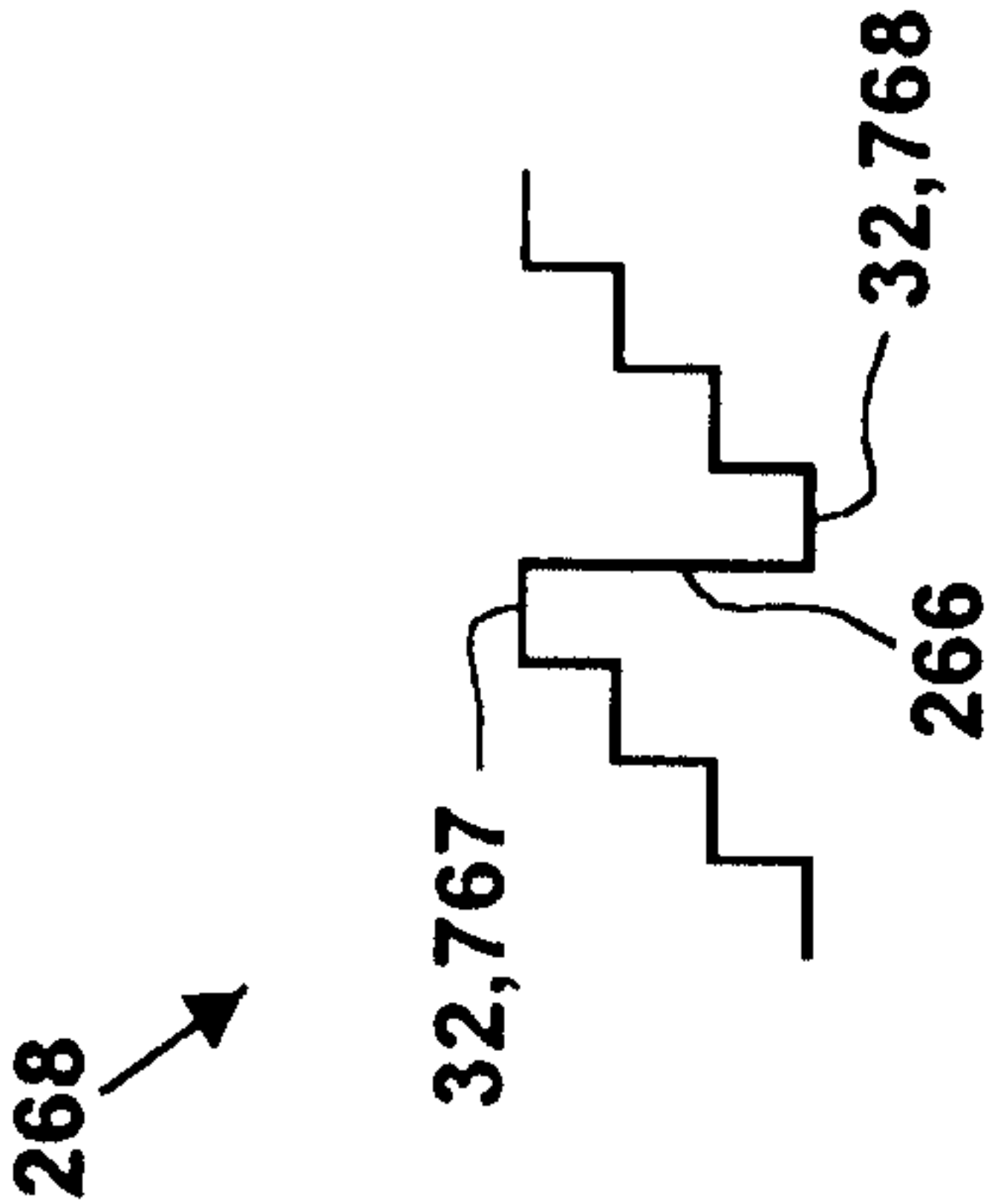
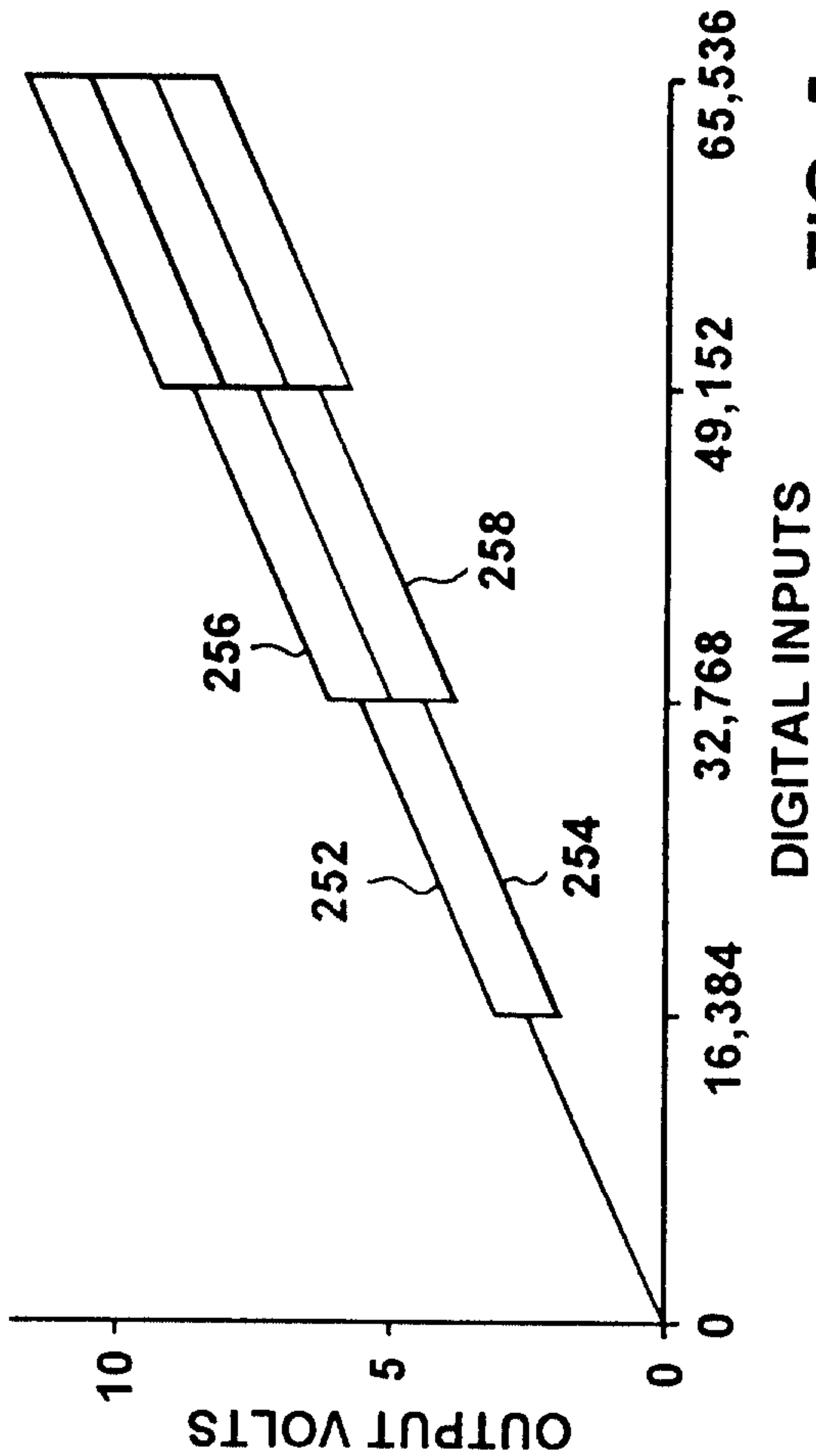
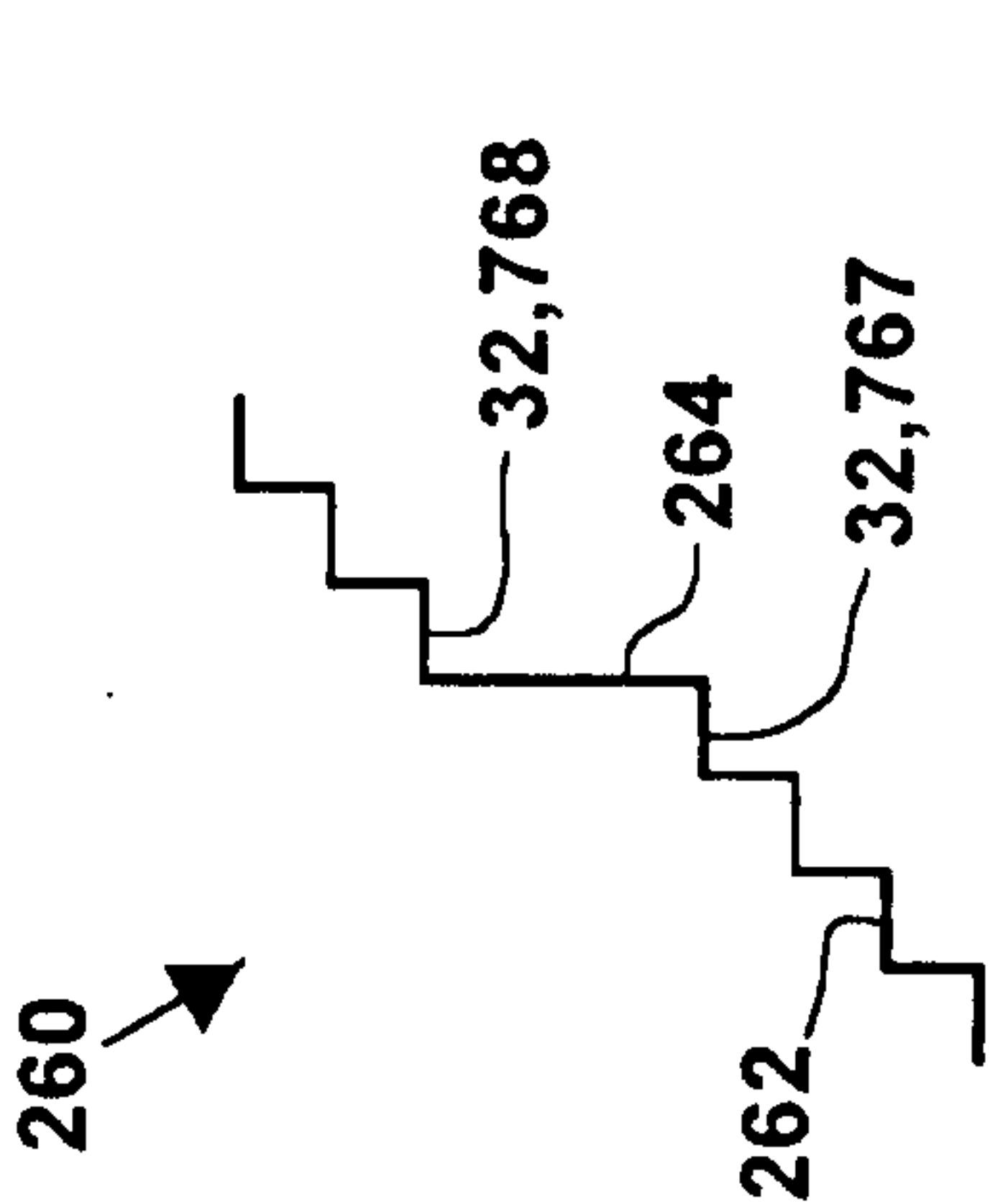
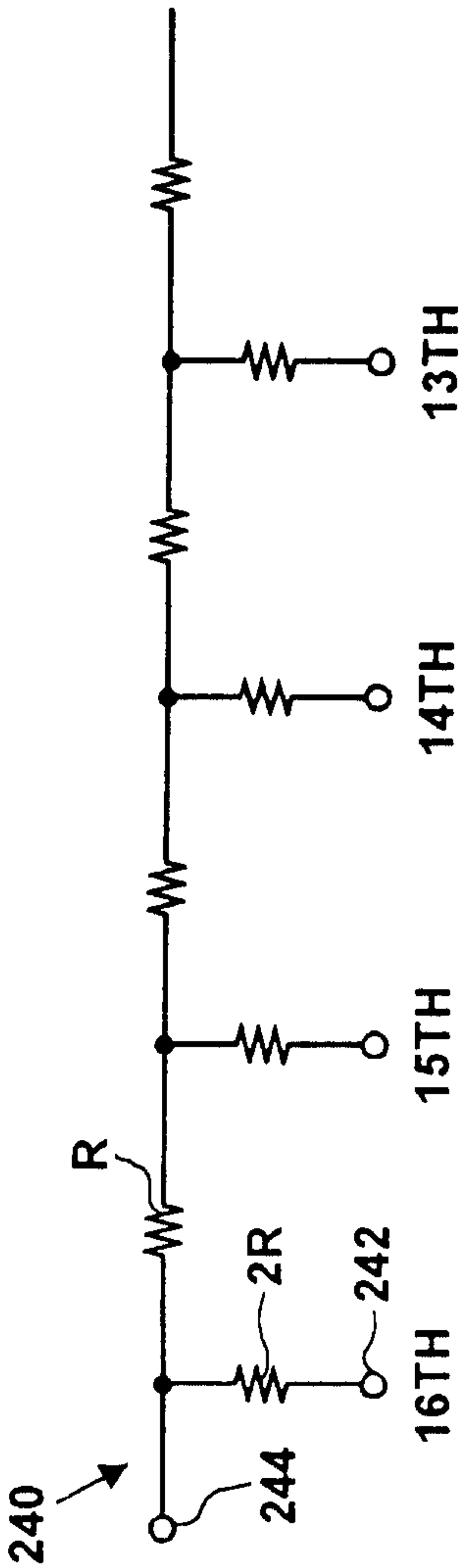
means, comprising a resistance ratio (R, 2R) of interconnected resistors,
10 for producing voltage steps that double for each increasing bit; and

means (ΔR_{16} , ΔR_{15} , ΔR_{14} , or 302) for decreasing said voltage steps for each of a plurality of higher bits (242) with respect to the next lower bit; whereby

said D/A converter produces an output voltage that is a nonlinear and
15 decreasing ratio of digital inputs.







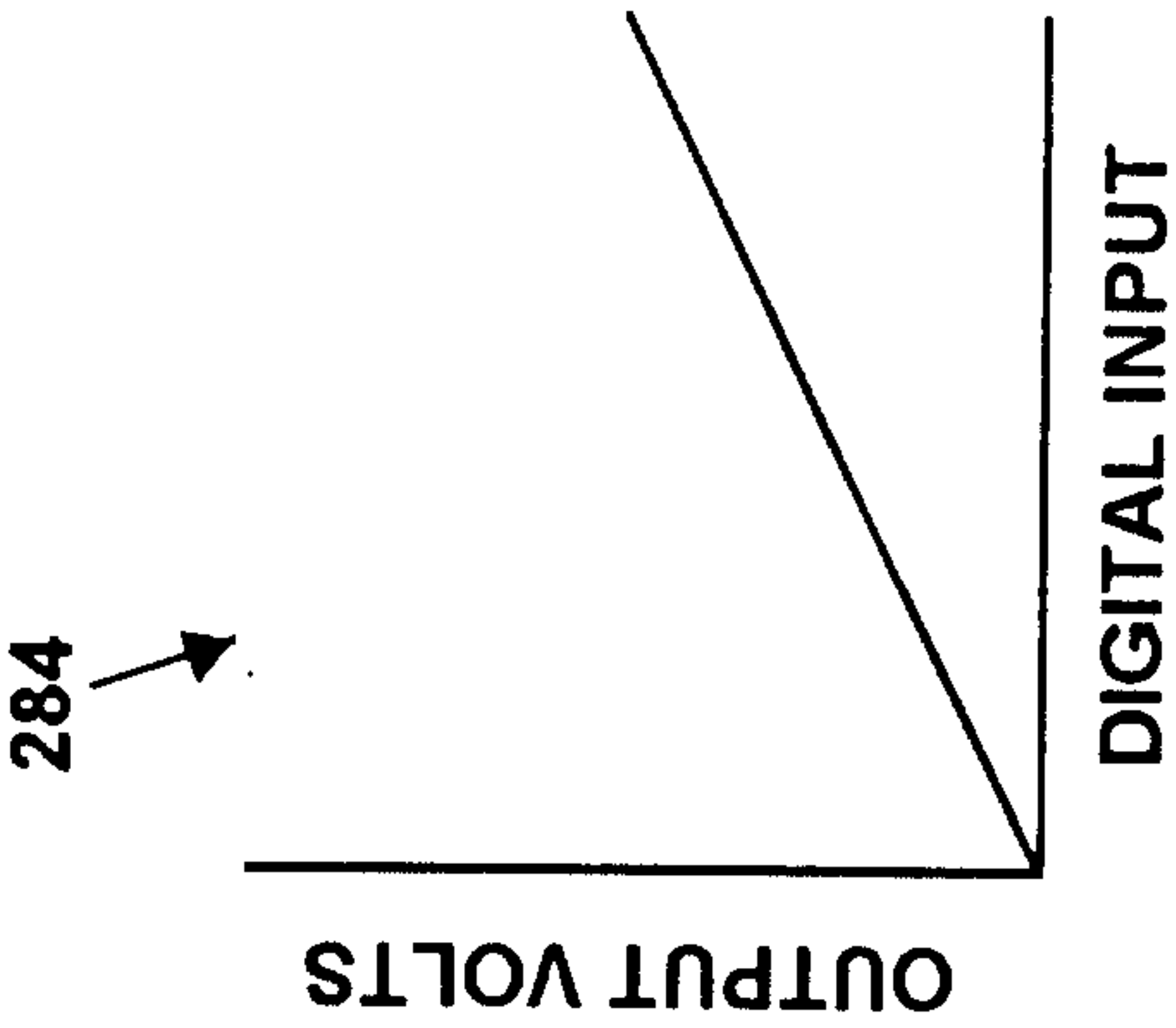


FIG. 9

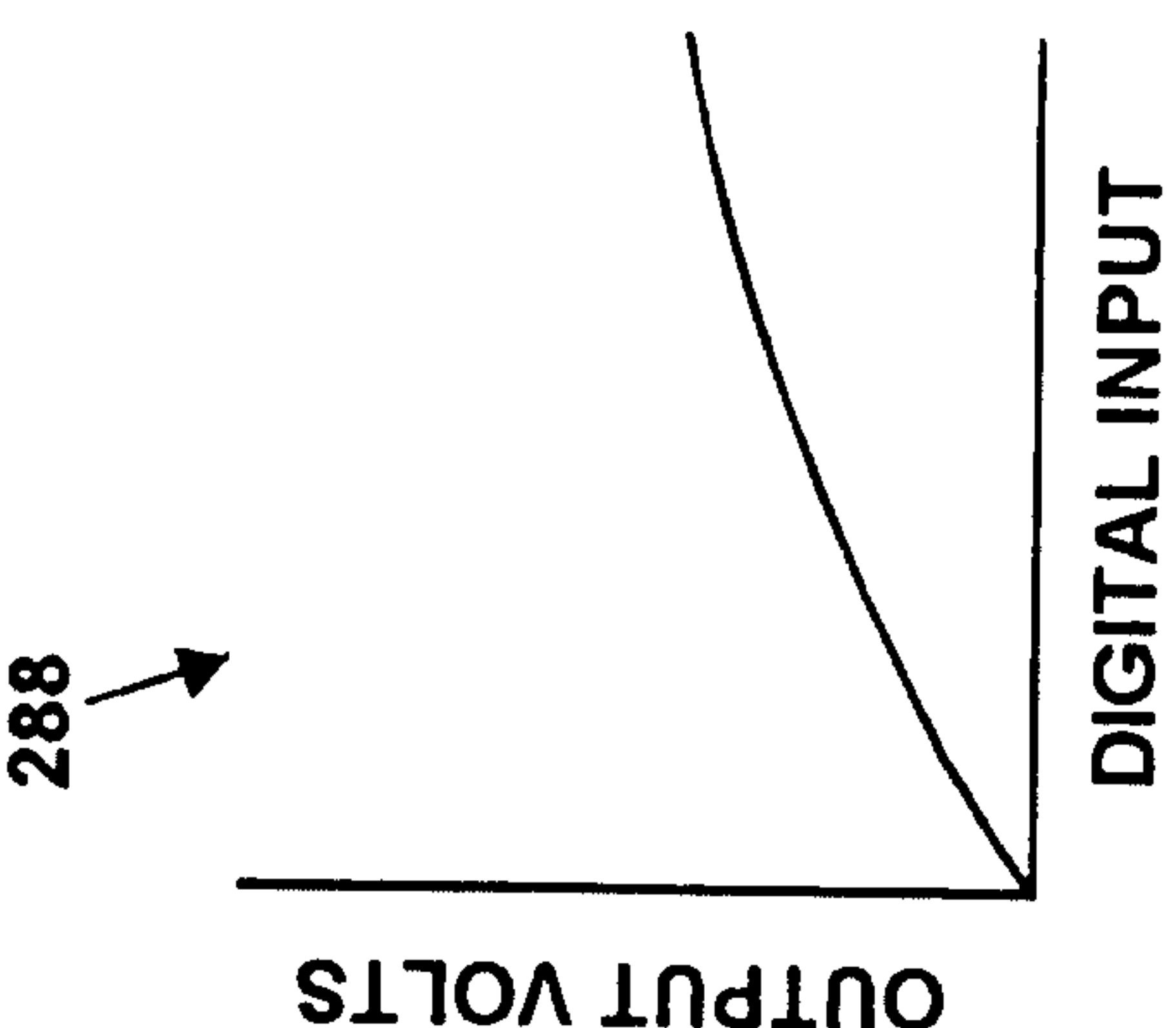


FIG. 10

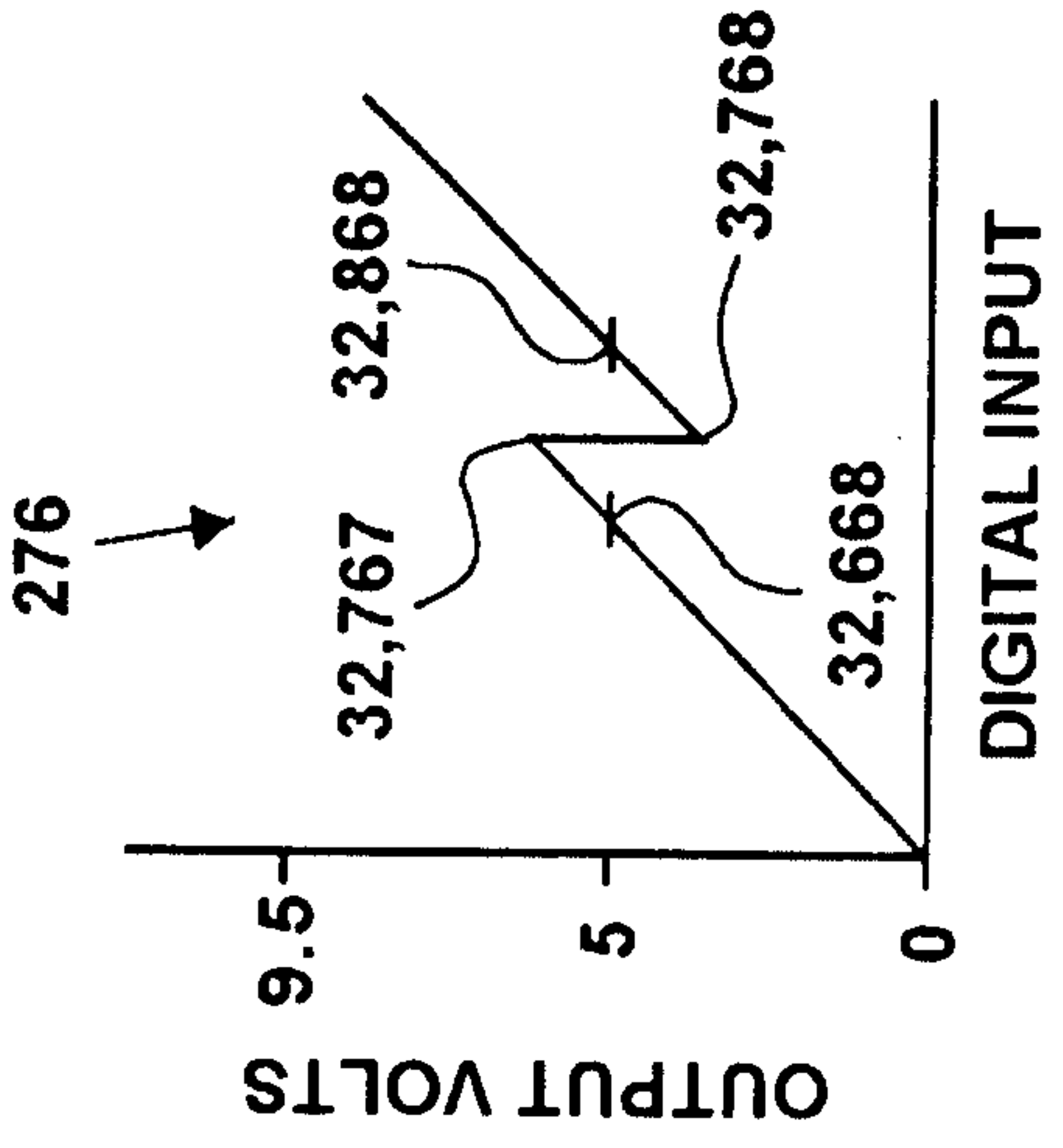


FIG. 7B

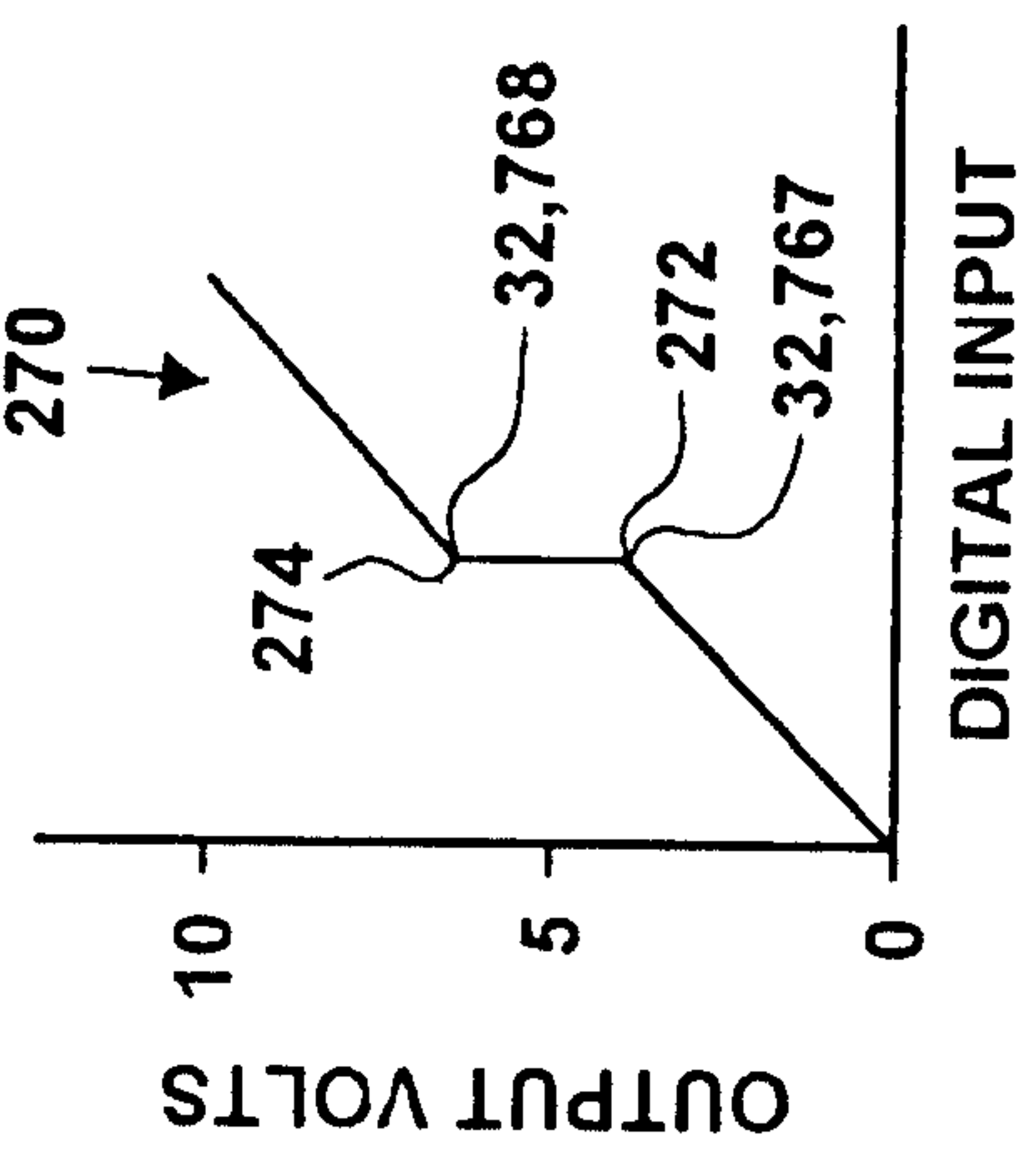


FIG. 7A

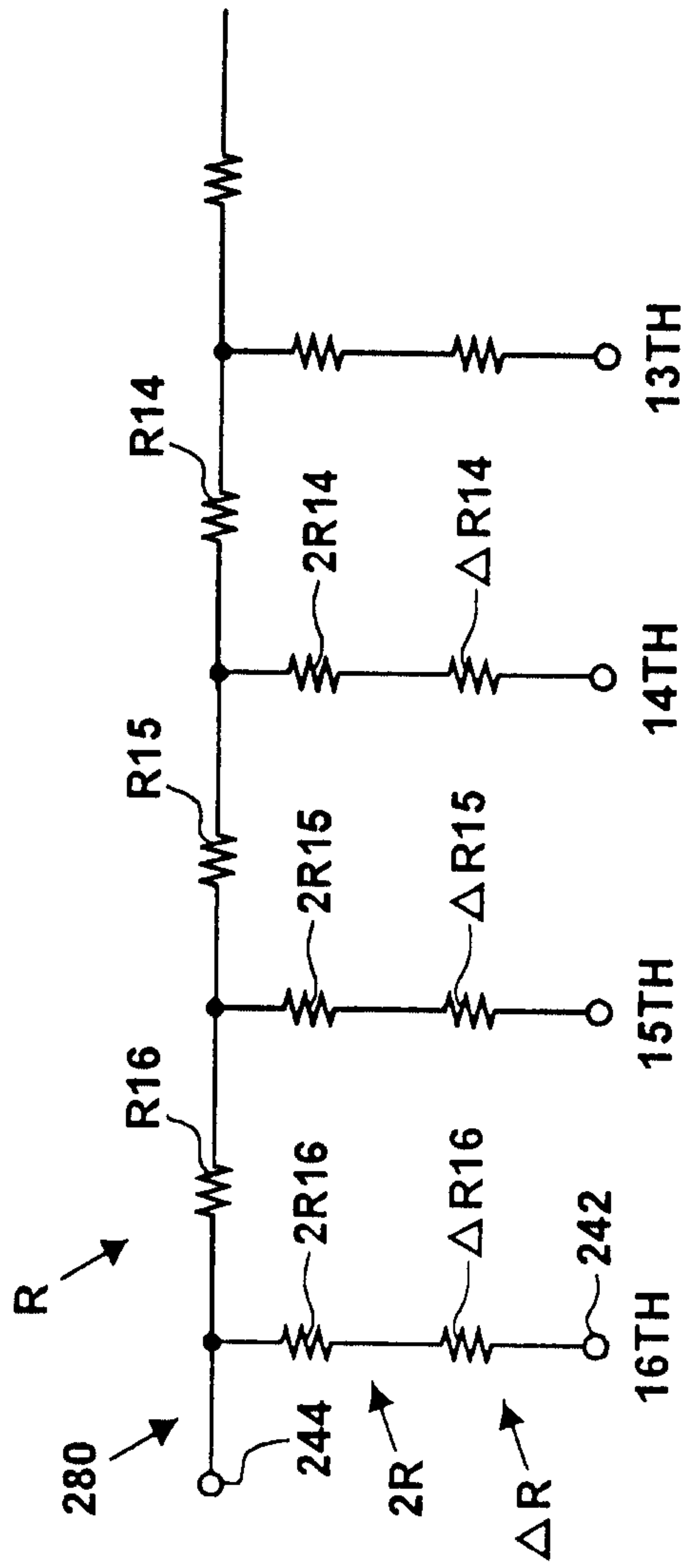


FIG. 8

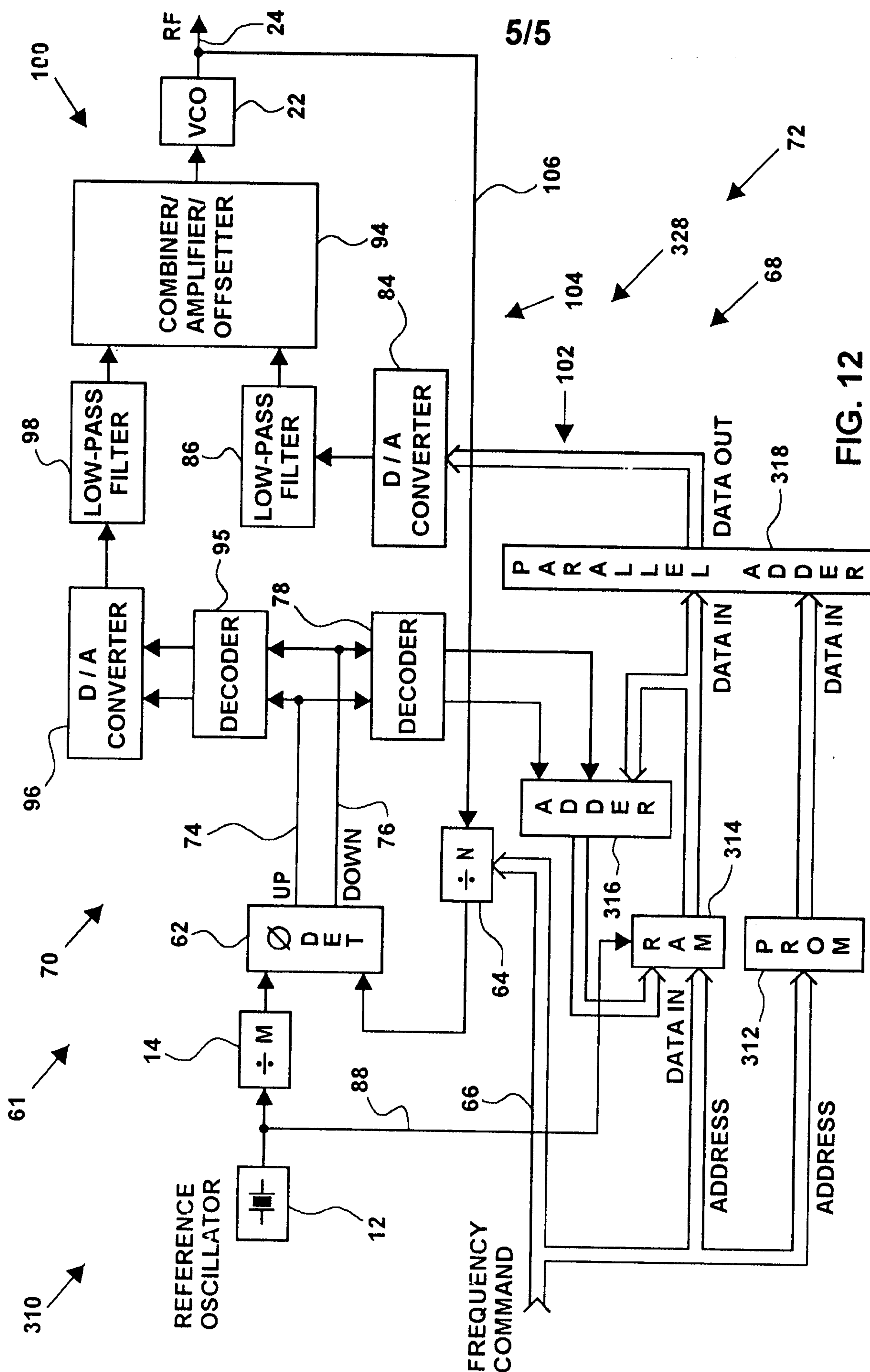


FIG. 12

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