United States Patent [19]

Winkler

[11] **3,774,729**

[45] **Nov. 27, 1973**

[54] **SPEED PATTERN GENERATOR FOR ELEVATOR SYSTEMS**

[75] Inventor: **Charles L. Winkler**, Pittsburgh, Pa.

[73] Assignee: **Westinghouse Electric Corporation**, Pittsburgh, Pa.

[22] Filed: **May 17, 1972**

[21] Appl. No.: **254,006**

[52] **U.S. Cl.** ..... **187/29 R**

[51] **Int. Cl.** **B66b 1/30**

[58] **Field of Search** 187/29

[56] **References Cited**

UNITED STATES PATENTS

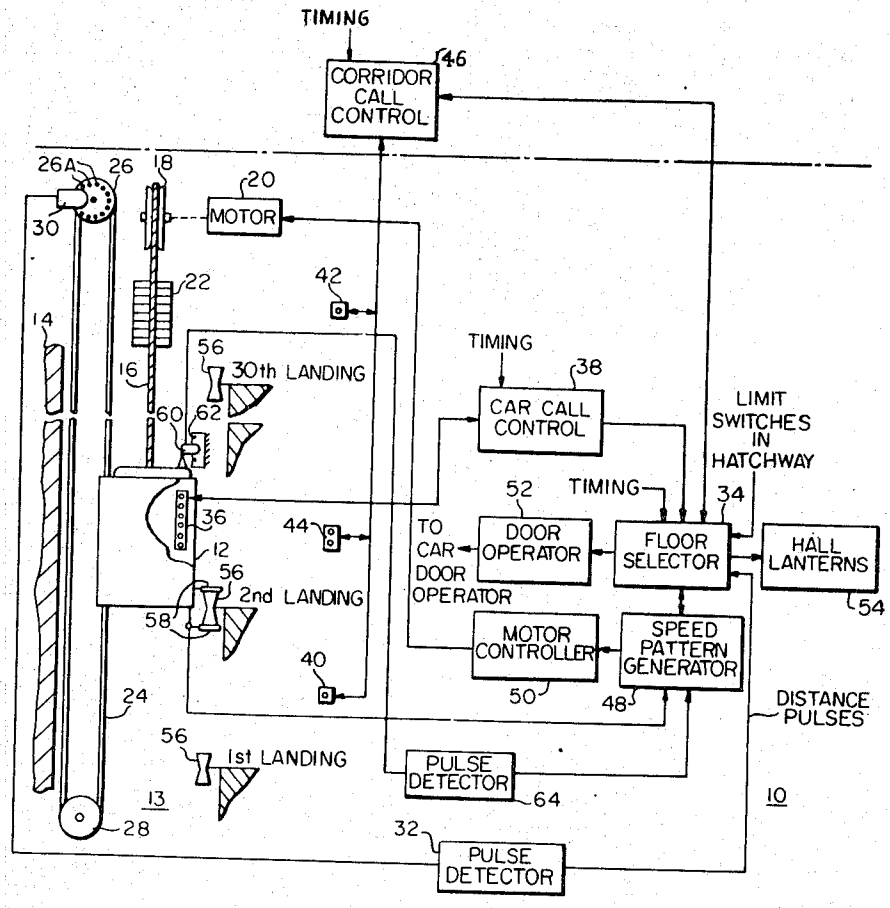
3,523,232	8/1970	Hall et al.	187/29
3,526,300	9/1970	Ferrot	187/29
3,627,080	12/1971	Yuminaka et al.	187/29

Primary Examiner—Bernard A. Gilheany
Assistant Examiner—W. E. Duncanson, Jr.
Attorney—A. T. Stratton et al.

[57] **ABSTRACT**

A speed pattern generator for elevator control which provides a time dependent speed reference pattern, with control over maximum jerk directly incorporated into the pattern itself. The speed pattern is developed by starting with a step signal whose two magnitudes determine maximum jerk. The specific magnitude of the step signal which is selected, and time spent at each magnitude of the step signal is determined by acceleration and speed feedback circuits. The step or jerk signal is integrated to provide an acceleration signal, and the acceleration signal is integrated to provide a speed pattern signal which, regardless of how fast the elevator system responds thereto, positively limits the maximum jerk.

17 Claims, 23 Drawing Figures



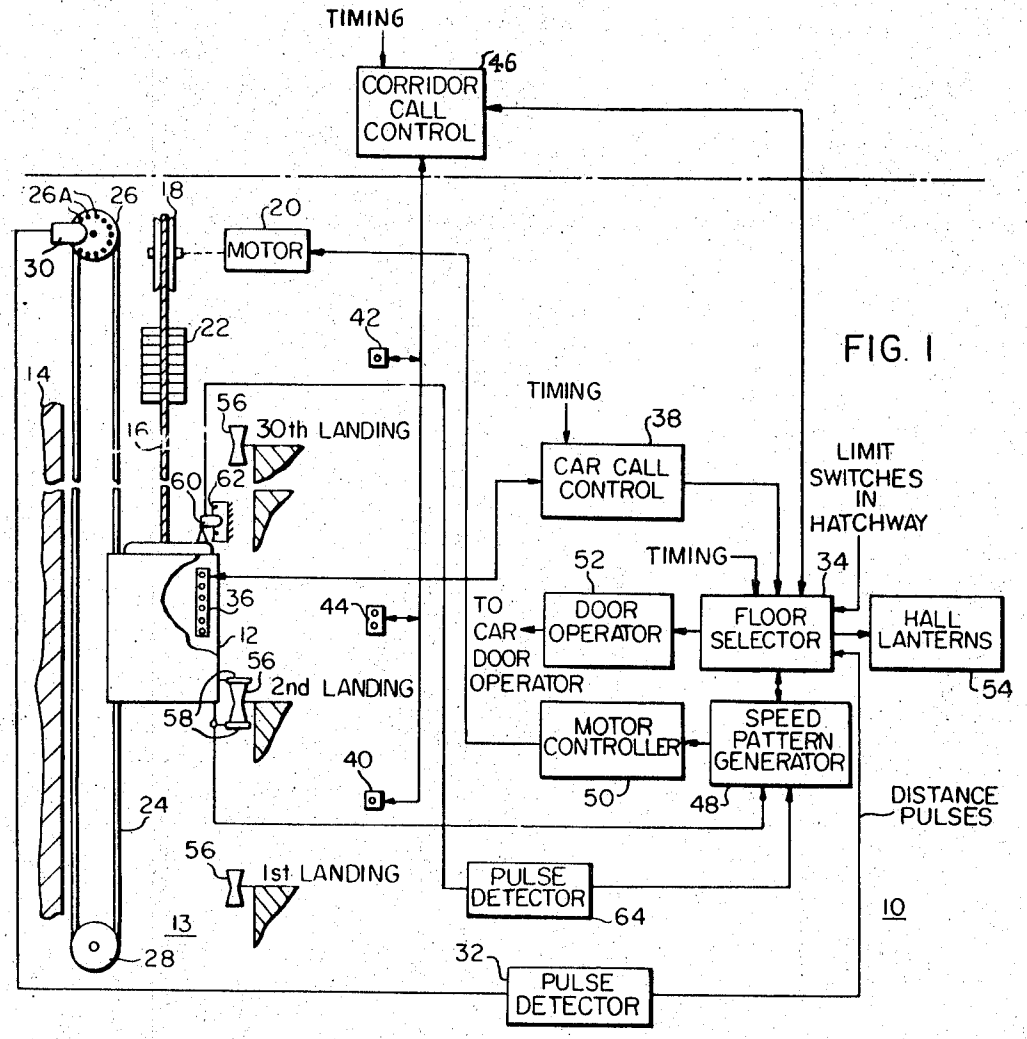

TIMING
CORRIDOR CALL CONTROL
46
26A
26
18
20
MOTOR
30
22
42
14
56
30th LANDING
16
60
62
TIMING
38
CAR CALL CONTROL
LIMIT SWITCHES IN HATCHWAY
52
TIMING
34
36
44
TO CAR DOOR OPERATOR
DOOR OPERATOR
FLOOR SELECTOR
HALL LANTERNS
54
12
56
2nd LANDING
58
MOTOR CONTROLLER
SPEED PATTERN GENERATOR
40
50
48
24
DISTANCE PULSES
56
1st LANDING
PULSE DETECTOR
64
10
13
28
32
PULSE DETECTOR

FIG. 1

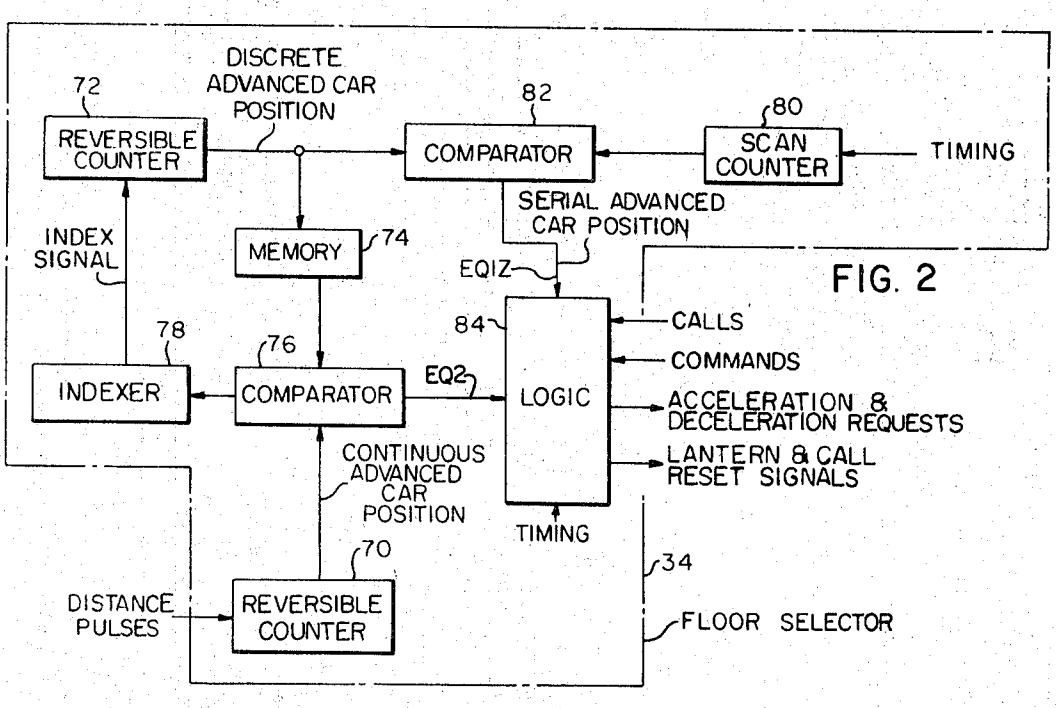
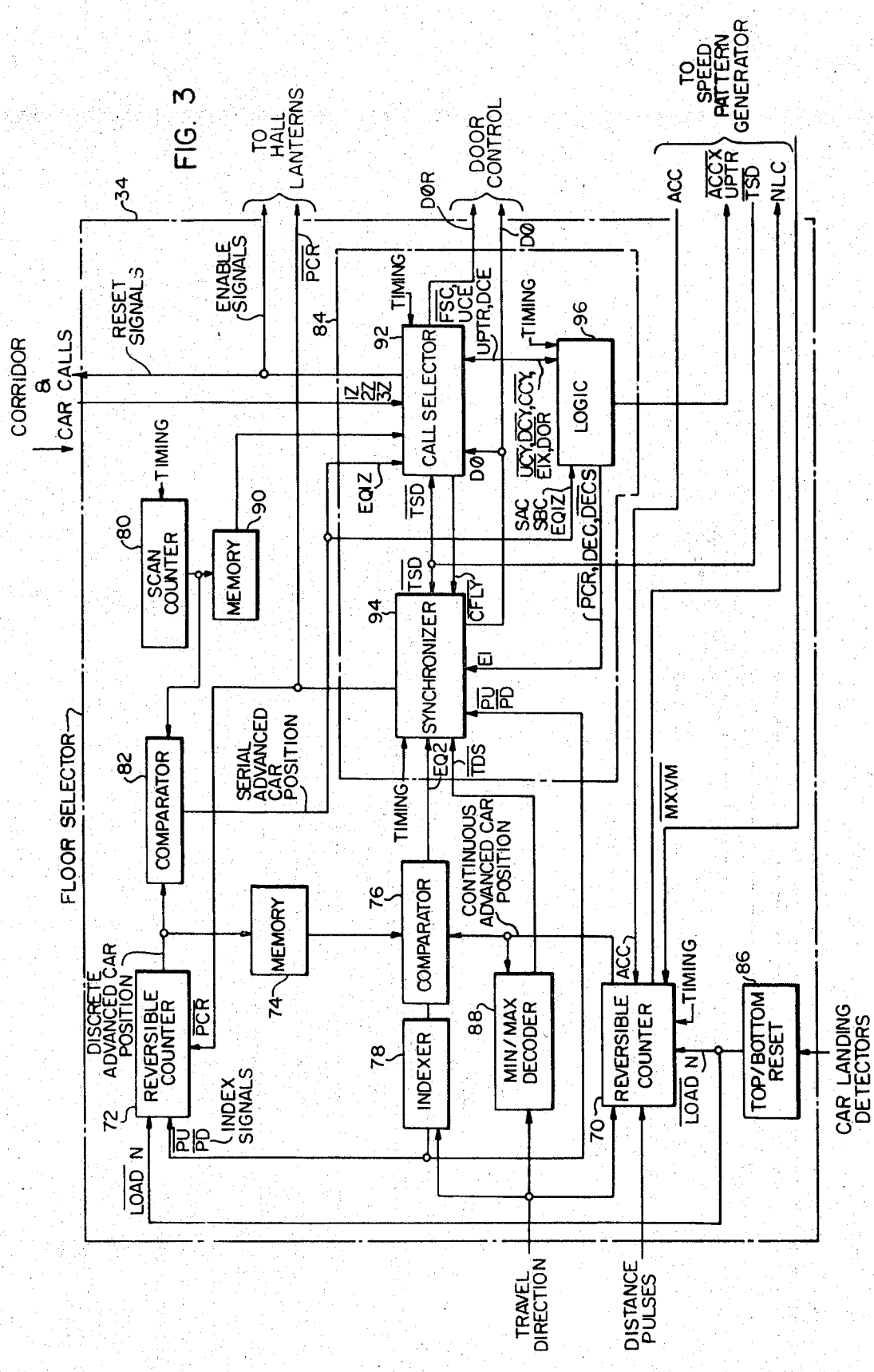

72
DISCRETE ADVANCED CAR POSITION
82
80
REVERSIBLE COUNTER
COMPARATOR
SCAN COUNTER
TIMING
SERIAL ADVANCED CAR POSITION
INDEX SIGNAL
MEMORY
74
EQIZ
84
CALLS
78
76
COMMANDS
INDEXER
COMPARATOR
EQ2
LOGIC
ACCELERATION & DECELERATION REQUESTS
CONTINUOUS ADVANCED CAR POSITION
LANTERN & CALL RESET SIGNALS
TIMING
70
34
DISTANCE PULSES
REVERSIBLE COUNTER
FLOOR SELECTOR

FIG. 2

FIG. 3


CORRIDOR & CAR CALLS
RESET SIGNALS
ENABLE SIGNALS
TO HALL LANTERNS
DOOR CONTROL
TO SPEED PATTERN GENERATOR
ACC
ACCX
UPTR
TSD
NLC
DØR
DØ
34
84
92
CALL SELECTOR
TIMING
FSC, UCE
UPTR, DCE
96
LOGIC
UCY, DCY, CCY
EIX, DOR
SAC
SBC
EQIZ
PCR, DEC, DECS
EQIZ
TSD
DØ
90
MEMORY
80
SCAN COUNTER
94
SYNCHRONIZER
CFLY
EI
PU
PD
TSD
EQ2
TDS
82
COMPARATOR
SERIAL ADVANCED CAR POSITION
FLOOR SELECTOR
TIMING
76
COMPARATOR
CONTINUOUS ADVANCED CAR POSITION
74
MEMORY
78
INDEXER
88
MIN/MAX DECODER
72
REVERSIBLE COUNTER
DISCRETE ADVANCED CAR POSITION
PCR
INDEX SIGNALS
PU
PD
LOAD N
ACC
MXVM
70
REVERSIBLE COUNTER
TIMING
LOAD N
86
TOP/BOTTOM RESET
CAR LANDING DETECTORS
TRAVEL DIRECTION
DISTANCE PULSES

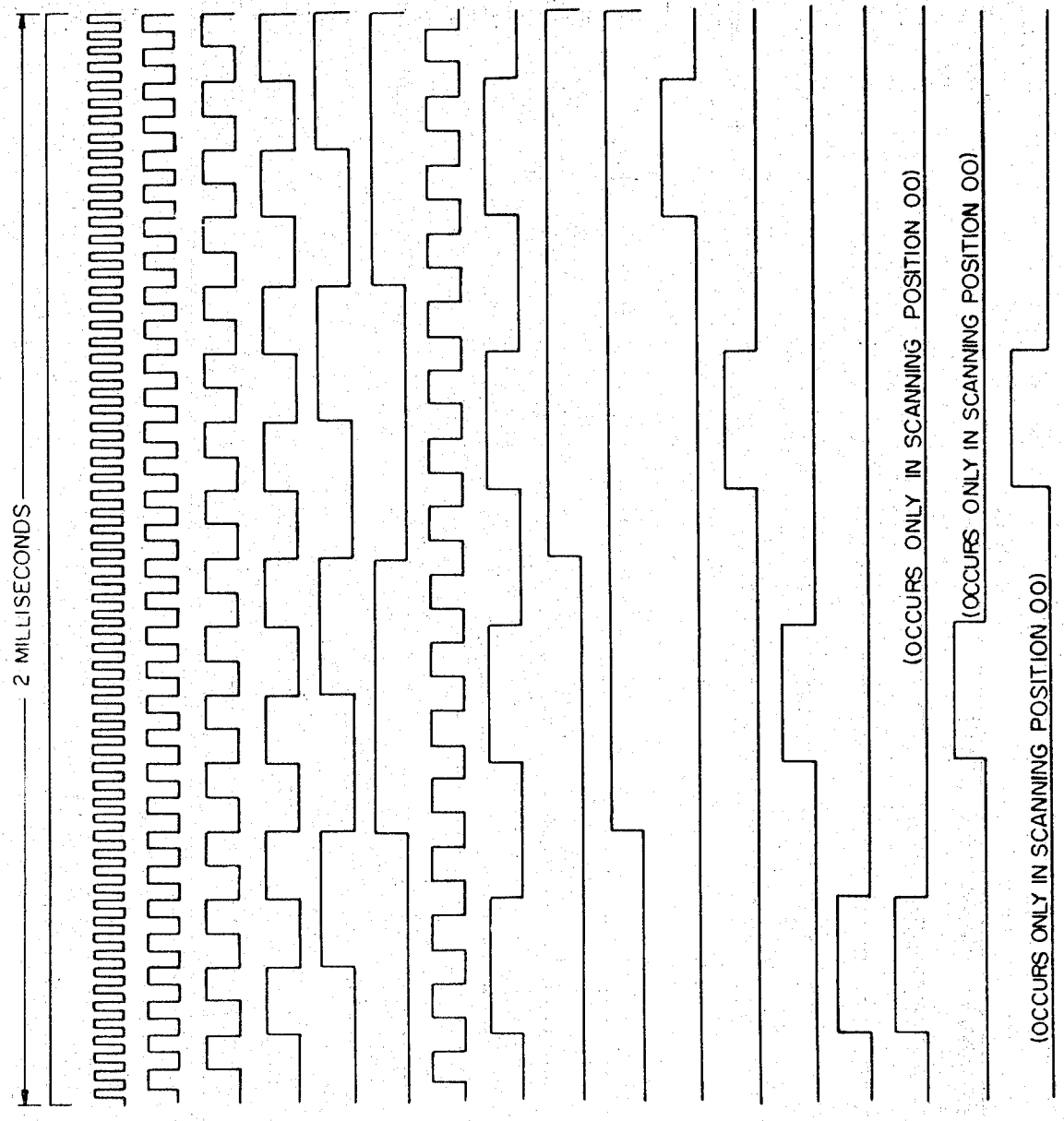

2 MILLISECONDS
00
K32
K16
K08
K04
K02
K01
K08S
K02S
KP5
$\overline{STC} = \overline{K01} \cdot \overline{KP5}$
$S4 = K01 \cdot KP5 \cdot K02S$
$S3 = \overline{K01} \cdot KP5 \cdot K02S$
$S2 = K01 \cdot \overline{KP5} \cdot K02S$
$S1 = \overline{K01} \cdot \overline{KP5} \cdot K02S$
S100
S200
S300
(OCCURS ONLY IN SCANNING POSITION 00)
(OCCURS ONLY IN SCANNING POSITION 00)
(OCCURS ONLY IN SCANNING POSITION 00)

FIG. 4

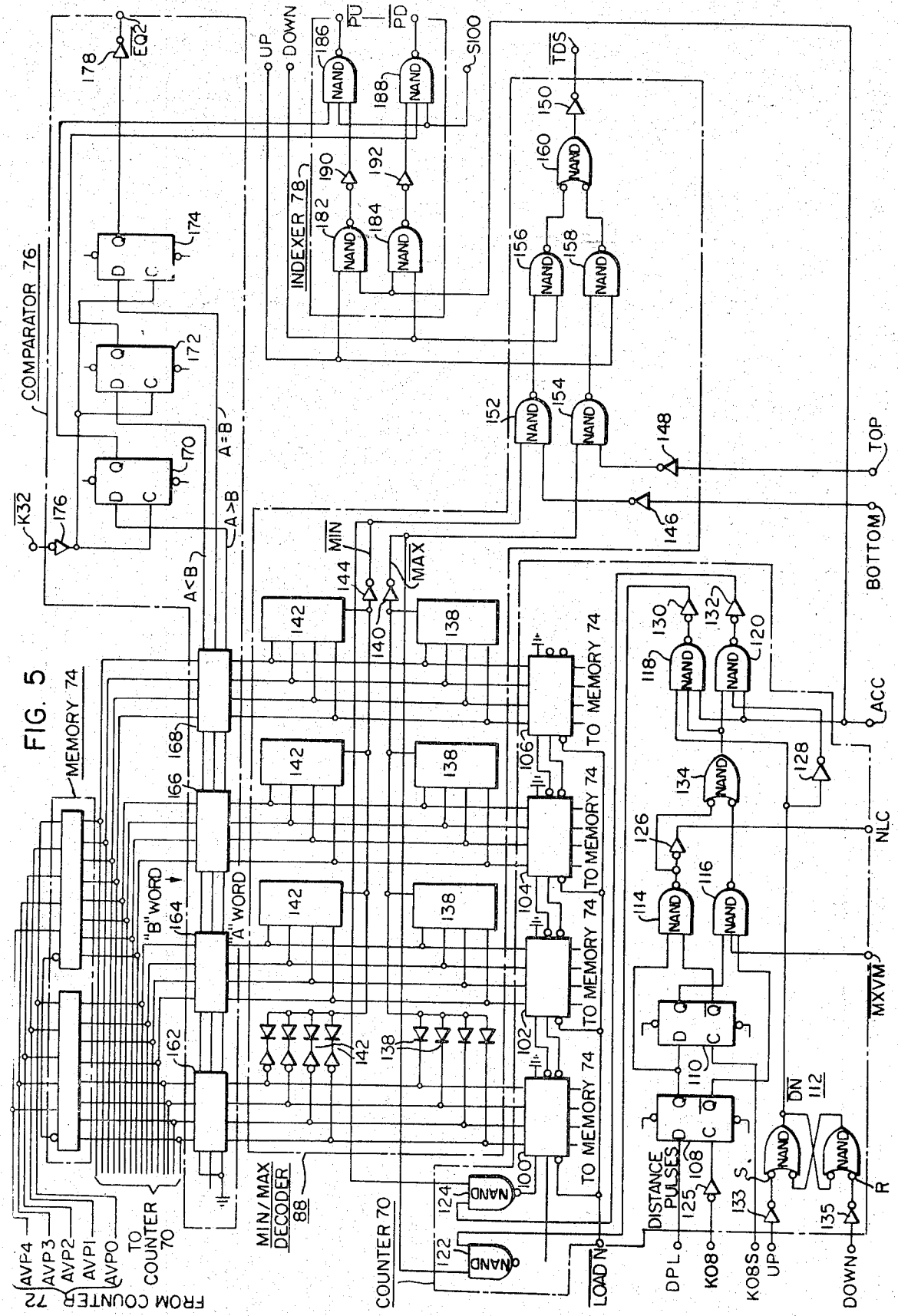

COMPARATOR 76
INDEXER 78
MEMORY 74
MIN/MAX DECODER 88
COUNTER 70
TO COUNTER 70
FROM COUNTER 72
AVP4
AVP3
AVP2
AVP1
AVP0
"A" WORD
"B" WORD
A<B
A=B
A>B
K32
EQ2
UP
DOWN
PU
PD
S100
TDS
MIN
MAX
TOP
BOTTOM
ACC
NLC
MXVM
LOAD N
DISTANCE PULSES
DPL
K08
K08S
UP
DOWN
DN
S
R
NAND
TO MEMORY 74

FIG. 5

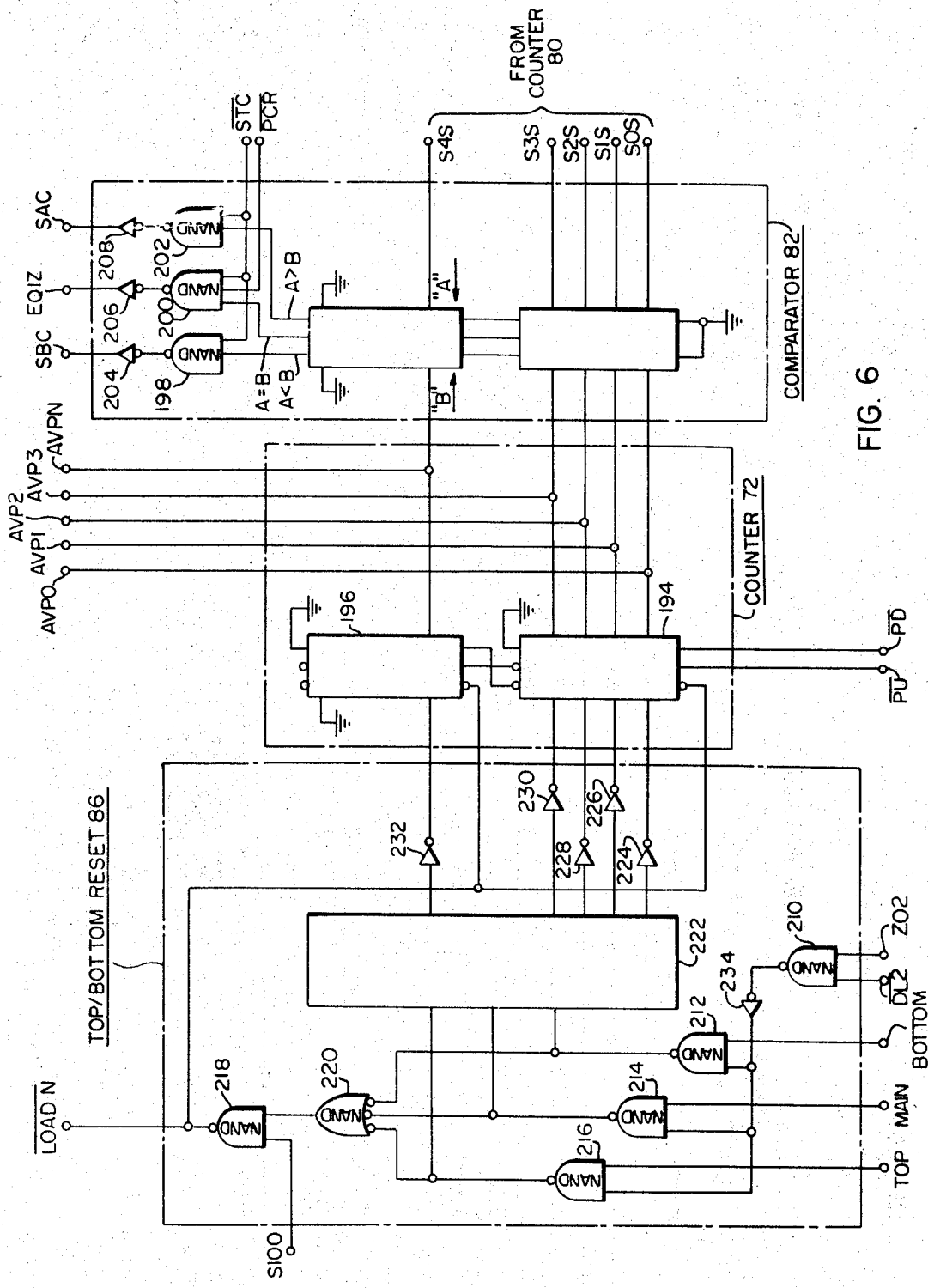

FROM COUNTER 80
STC
PCR
S4S
S3S
S2S
S1S
S0S
SAC
EQIZ
SBC
208
206
204
202
200
198
NAND
A>B
A=B
A<B
"A"
"B"
COMPARATOR 82
AVPN
AVP3
AVP2
AVP1
AVP0
COUNTER 72
196
194
PD
PU
230
226
228
224
232
TOP/BOTTOM RESET 86
222
210
202
234
212
214
216
218
220
LOAD N
S100
BOTTOM
MAIN
TOP

FIG. 6

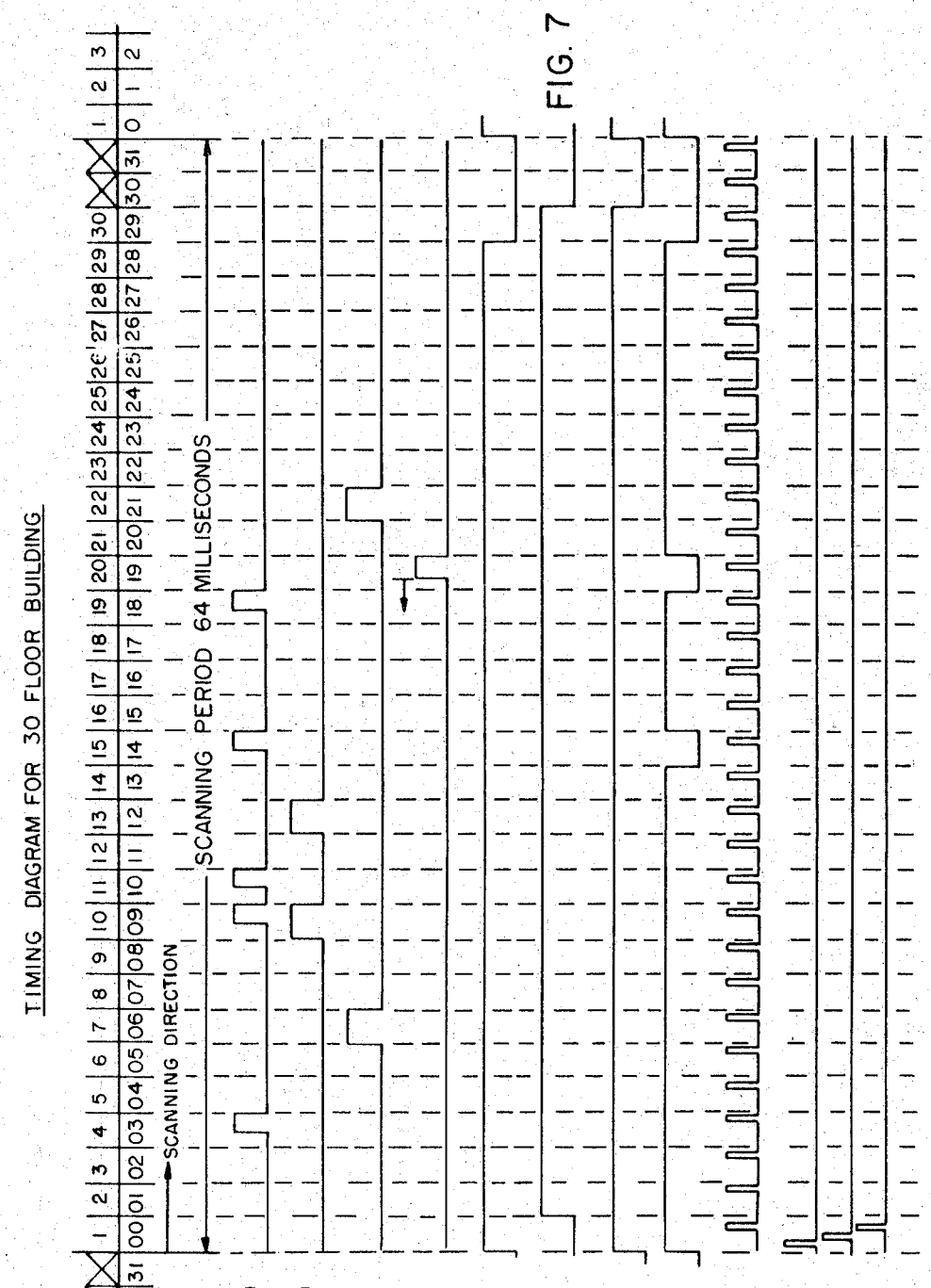

TIMING DIAGRAM FOR 30 FLOOR BUILDING
FLOOR POSITION
SCANNING POSITION
SCANNING DIRECTION
SCANNING PERIOD 64 MILLISECONDS
CAR CALLS (3Z)
UP CORRIDOR CALLS (1Z)
DOWN CORRIDOR CALLS(2Z)
ADVANCED CAR POSITION (EQ1Z)
MT00 (UP CALLS)
MT01 (DOWN CALLS)
CEN
ALTERNATE CEN
S4
S100
S200
S300

FIG. 7

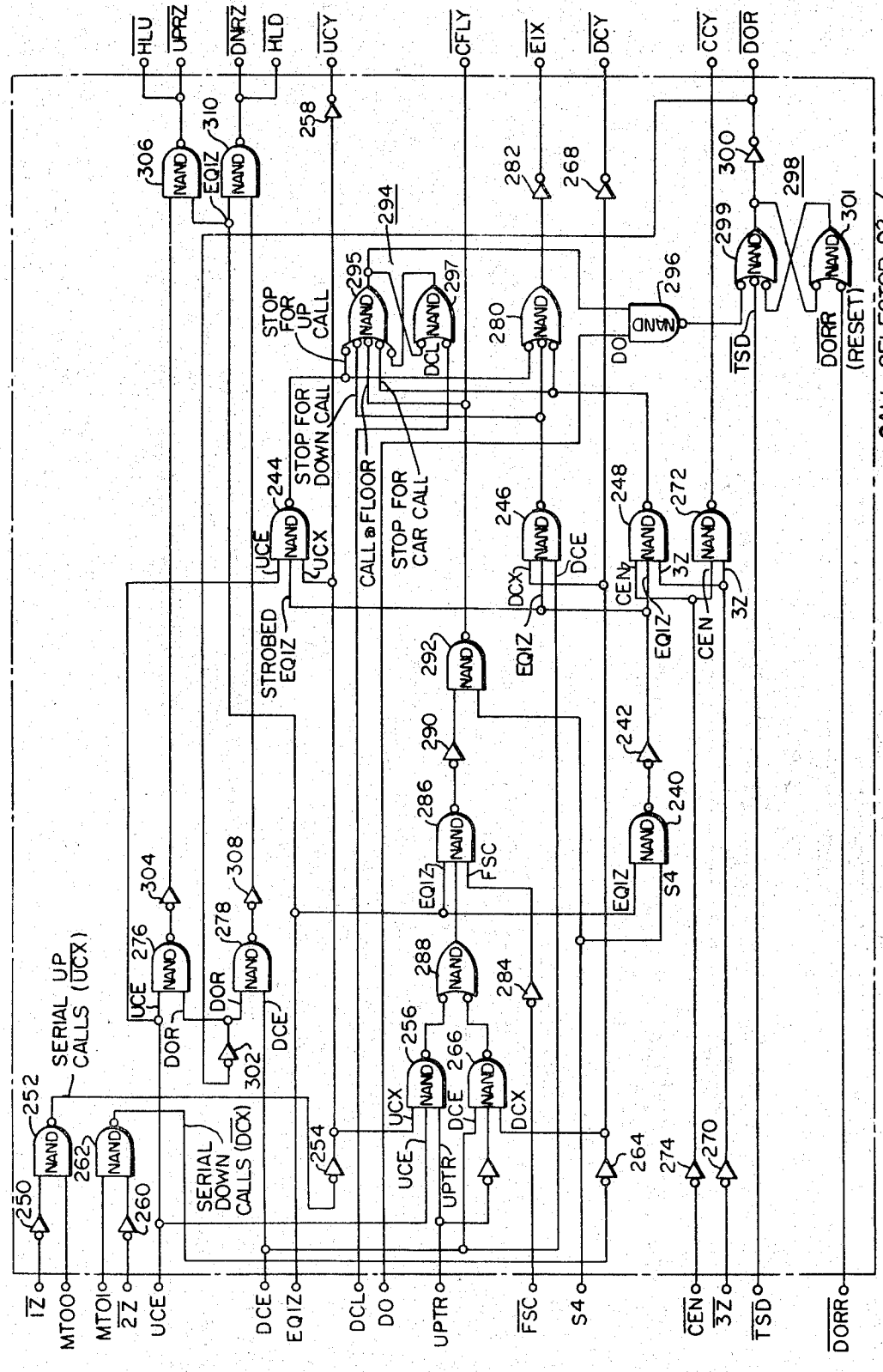

HLU
UPRZ
DNRZ
HLD
UCY
CFLY
EIX
DCY
CCY
DOR
CALL SELECTOR 92
SERIAL UP CALLS (UCX)
SERIAL DOWN CALLS (DCX)
STOP FOR UP CALL
STOP FOR DOWN CALL
CALL @ FLOOR
STOP FOR CAR CALL
STROBED EQIZ
EQIZ
UCE
DOR
DCE
UCX
DCX
UPTR
FSC
S4
CEN
3Z
TSD
DORR
(RESET)
DO
DCL
NAND
AND

FIG. 8

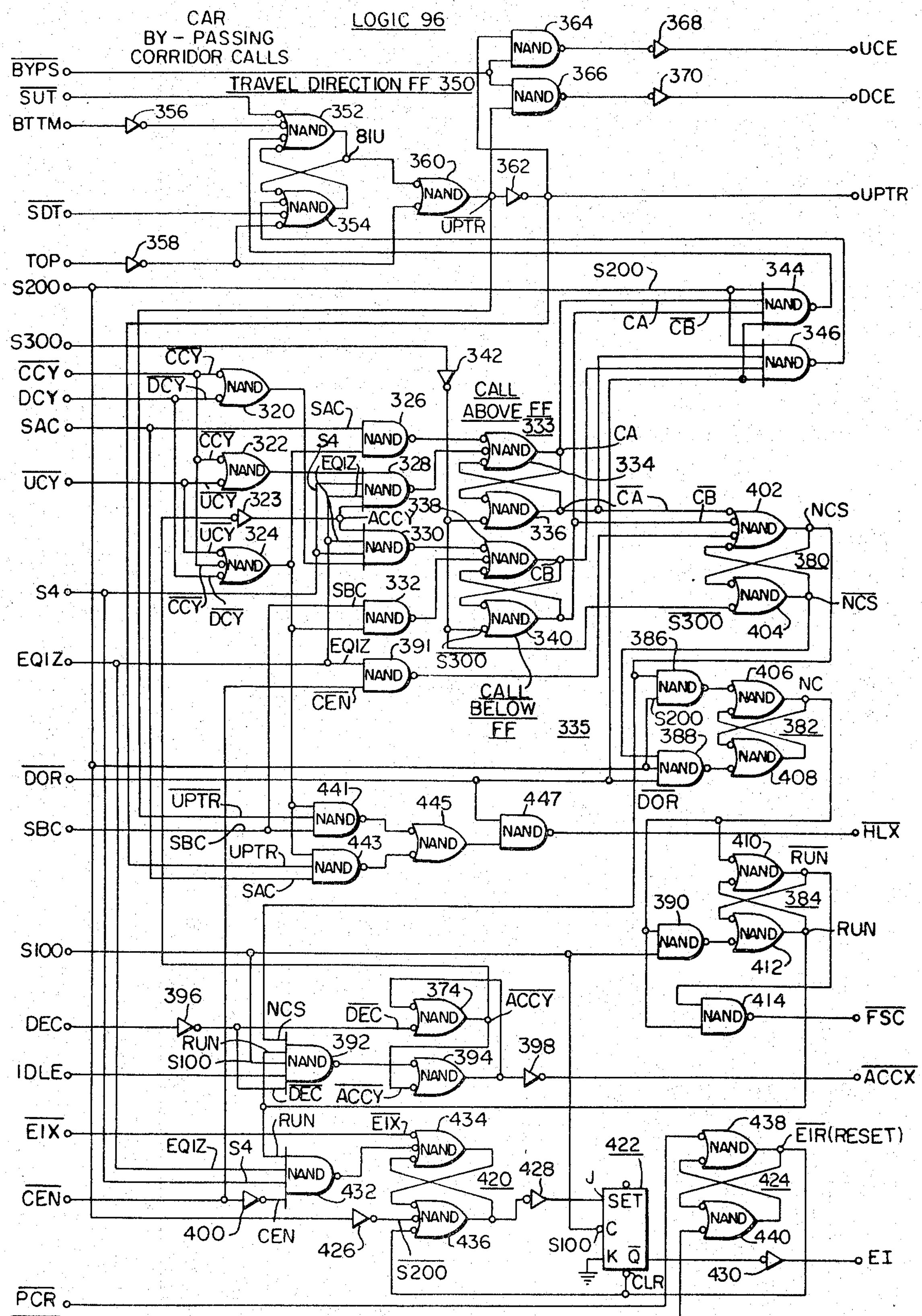

CAR
BY - PASSING
CORRIDOR CALLS
LOGIC 96
TRAVEL DIRECTION FF 350
CALL ABOVE FF 333
CALL BELOW FF 335
BYPS
SUT
BTTM
SDT
TOP
S200
S300
CCY
DCY
SAC
UCY
S4
EQIZ
DOR
SBC
S100
DEC
IDLE
EIX
CEN
PCR
DECS
UCE
DCE
UPTR
NCS
HLX
RUN
FSC
ACCX
EIR(RESET)
EI
NAND
CA
CB
ACCY
NC
SET
J
C
K
Q
CLR

FIG. 9

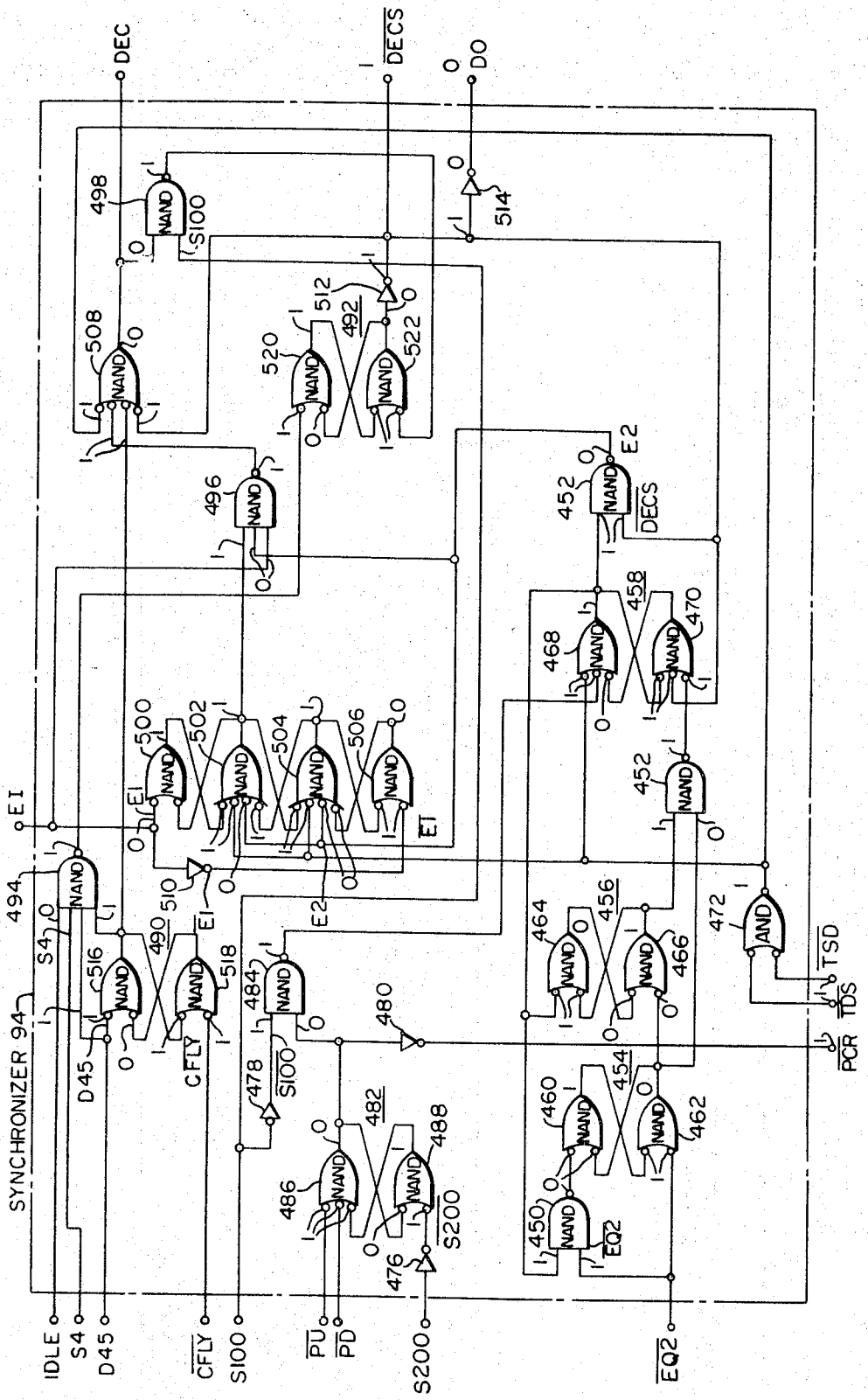
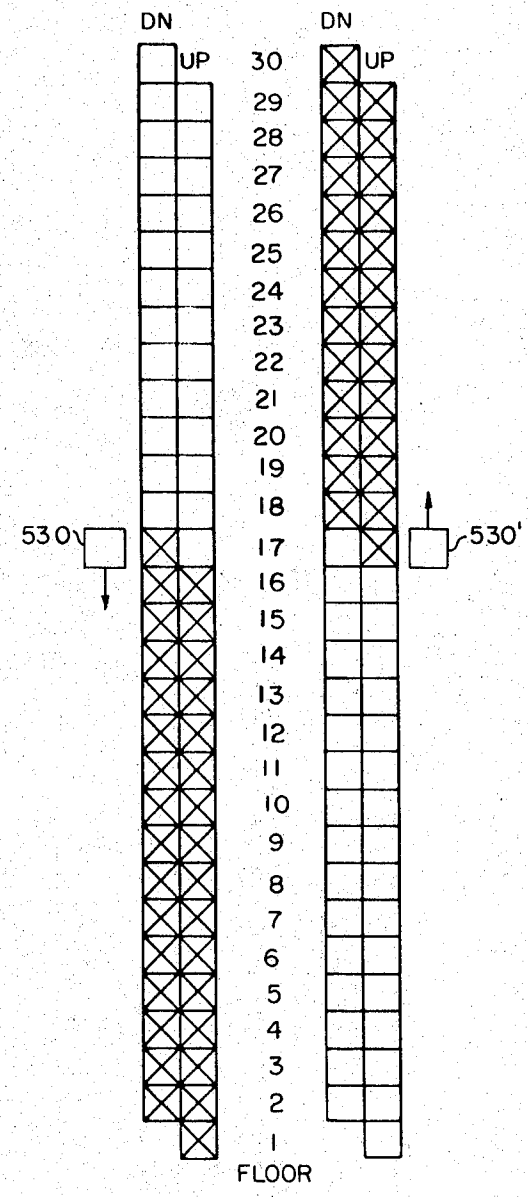

DEC
DECS
DO
498
S100
514
508
512
492
520
522
496
E2
452
DECS
458
468
470
452
500
502
504
506
EI
ET
494
S4
490
510
EI
E2
516
518
484
480
464
456
466
472
AND
TSD
TDS
PCR
SYNCHRONIZER 94
D45
CFLY
478
S100
482
454
460
462
486
488
S200
450
EQ2
476
IDLE
S4
D45
CFLY
S100
PU
PD
S200
EQ2

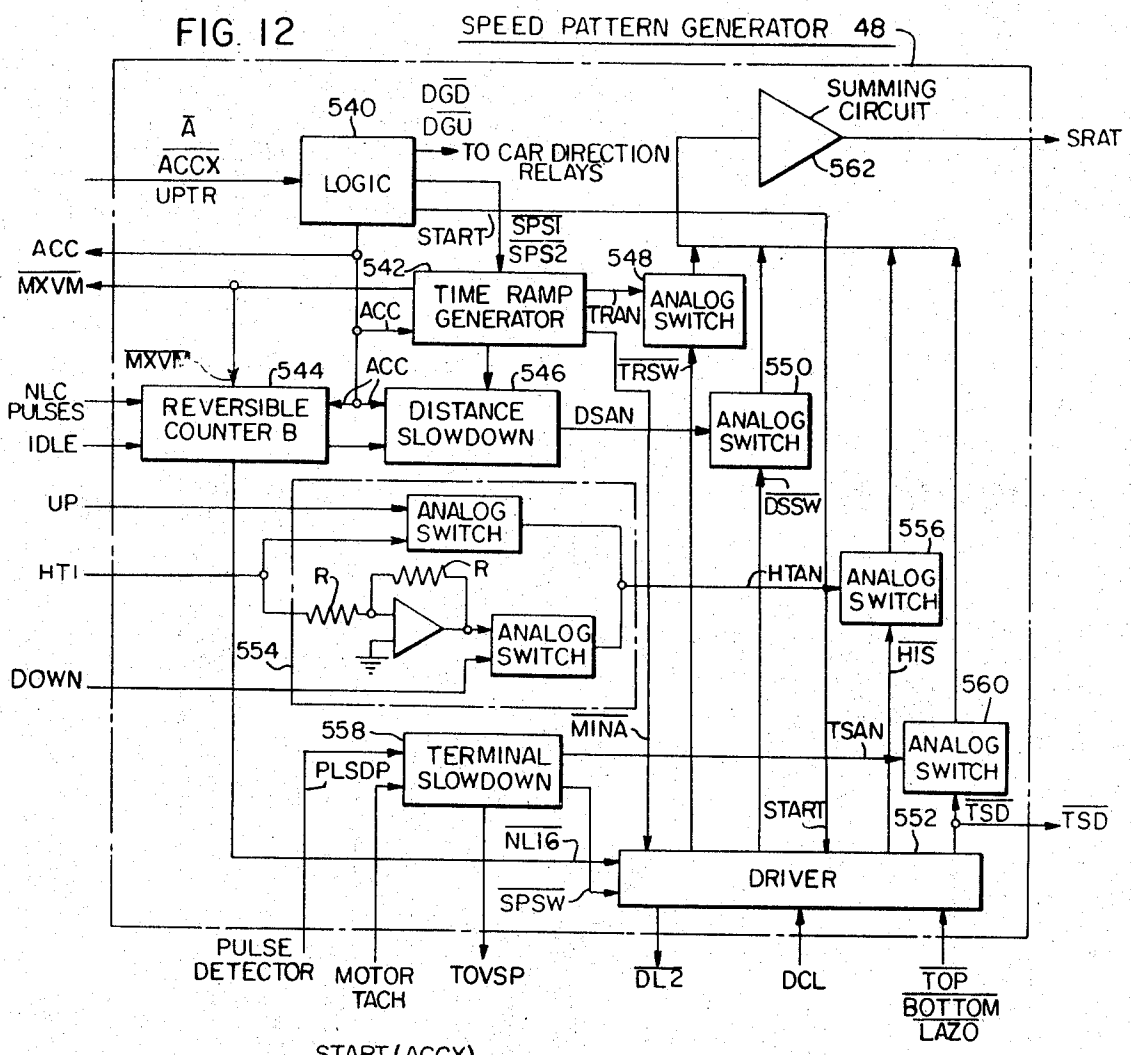
FIG. 10



CORRIDOR CALLS CAR CAN CONSIDER WHEN TRAVELLING IN A GIVEN DIRECTION

FIG. 11

FIG. 12


SPEED PATTERN GENERATOR 48
SUMMING CIRCUIT
562
SRAT
540
LOGIC
TO CAR DIRECTION RELAYS
UPTR
ACCX
ACC
MXVM
START
SPS1
SPS2
542
548
TIME RAMP GENERATOR
ANALOG SWITCH
TRAN
TRSW
550
544
546
REVERSIBLE COUNTER B
NLC PULSES
IDLE
DISTANCE SLOWDOWN
DSAN
DSSW
UP
HTI
DOWN
554
R
556
HTAN
HIS
560
MINA
TSAN
558
TERMINAL SLOWDOWN
PLSDP
552
TSD
NL16
SPSW
DRIVER
PULSE DETECTOR
MOTOR TACH
TOVSP
DL2
DCL
TOP
BOTTOM
LAZO

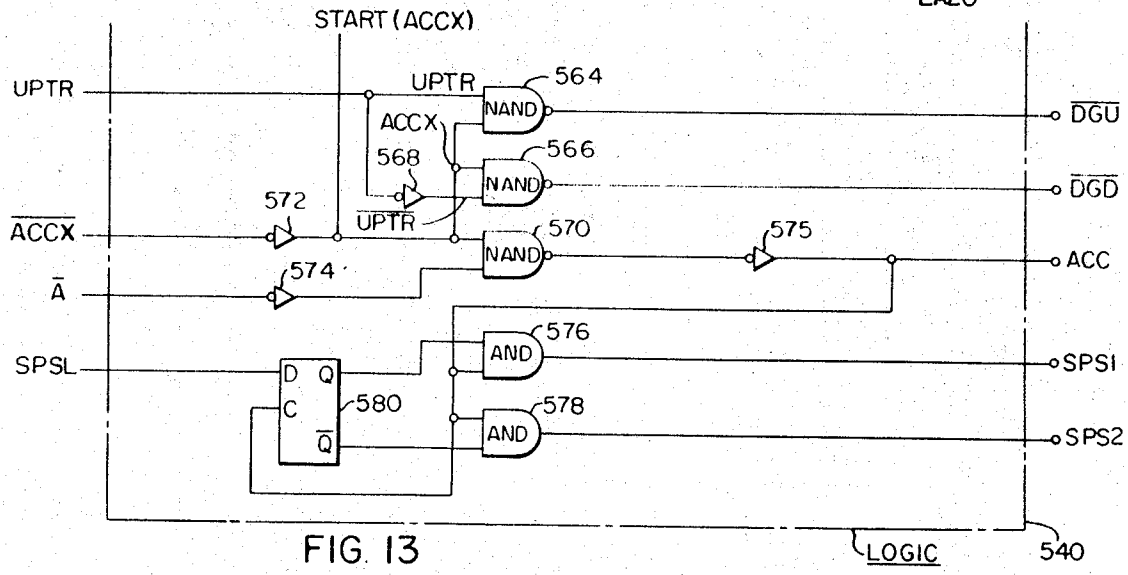

START (ACCX)
UPTR
ACCX
A
SPSL
564
566
568
572
570
575
574
576
578
580
NAND
AND
D
C
Q
DGU
DGD
ACC
SPS1
SPS2
LOGIC
540

FIG. 13

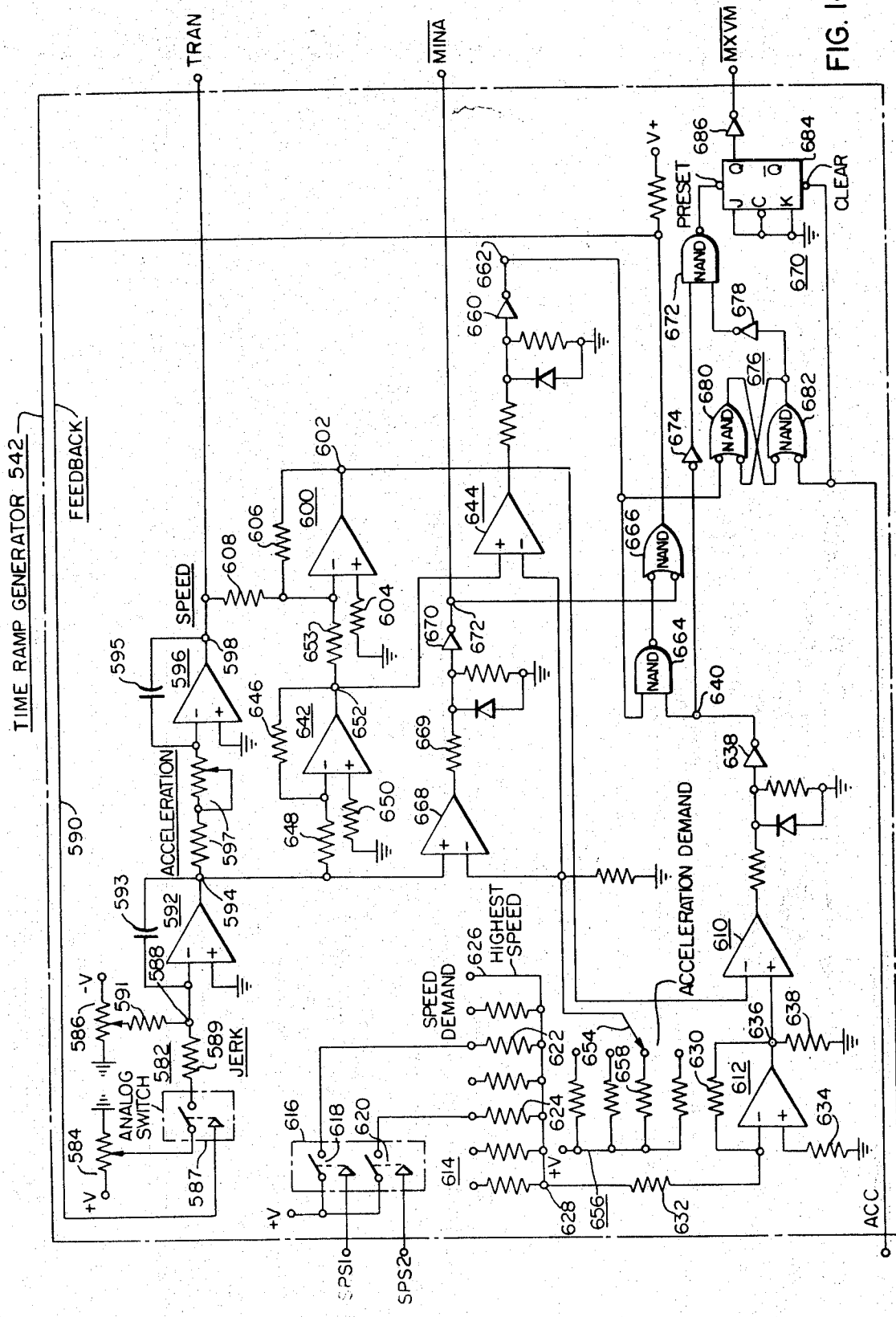

TIME RAMP GENERATOR 542
FEEDBACK
590
TRAN
MINA
MXVM
ACC
SPS1
SPS2
+V
-V
SPEED
ACCELERATION
JERK
ANALOG SWITCH
SPEED DEMAND
HIGHEST SPEED
ACCELERATION DEMAND
PRESET
CLEAR
NAND
584
586
587
588
589
591
592
593
594
595
596
597
598
600
602
604
606
608
610
612
614
616
618
620
622
624
626
628
630
632
634
636
638
640
642
644
646
648
650
652
653
654
656
658
660
662
664
666
668
669
670
672
674
676
678
680
682
684
686

FIG. 14

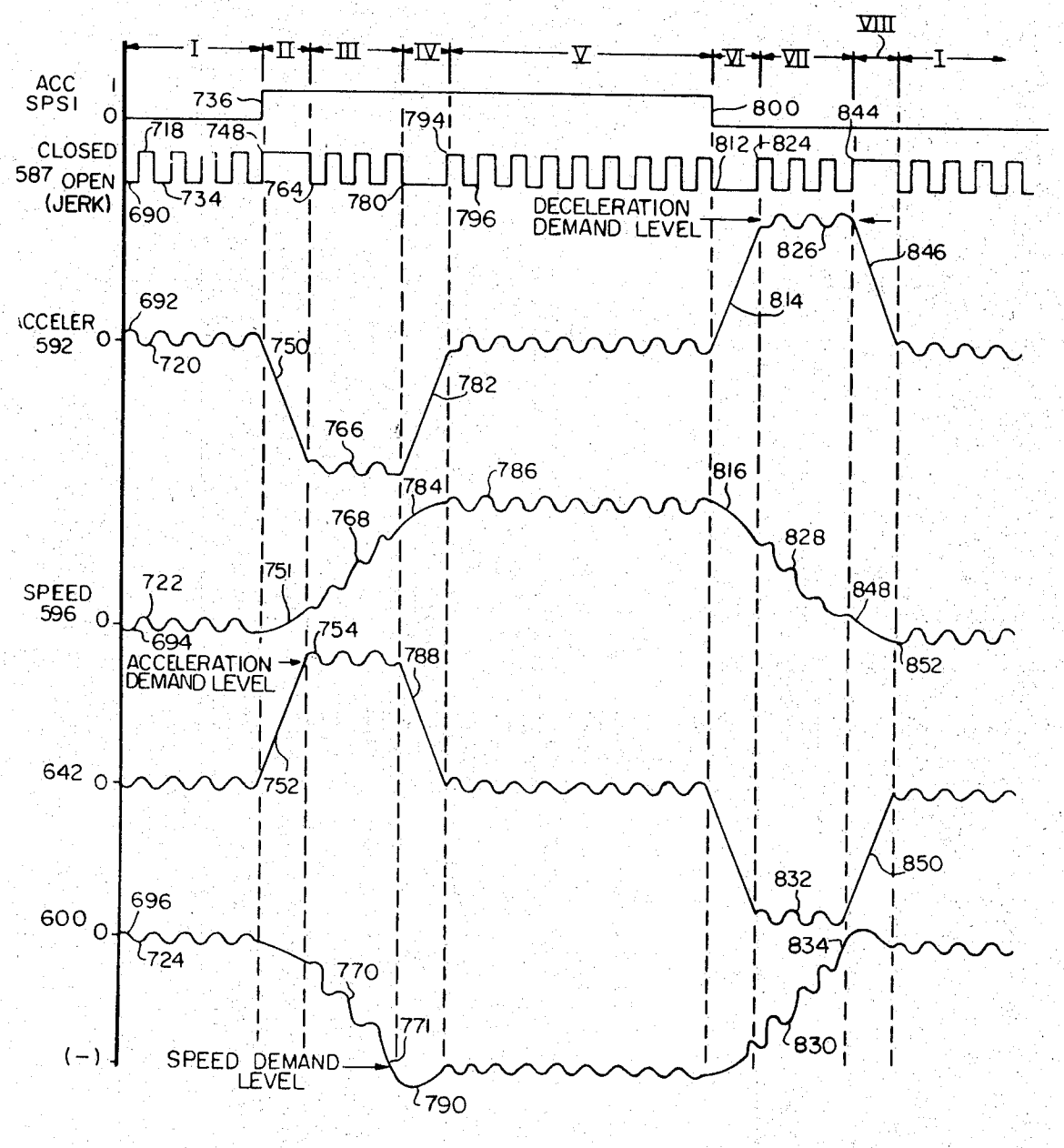

I
II
III
IV
V
VI
VII
VIII
I
ACC
SPSI
1
0
736
800
844
718
748
794
812
824
CLOSED
587 OPEN
(JERK)
690
734
764
780
796
DECELERATION
DEMAND LEVEL
826
846
692
814
ACCELER
592
0
720
750
782
766
784
786
816
768
828
722
751
848
SPEED
596
0
694
754
788
852
ACCELERATION
DEMAND LEVEL
642
0
752
850
832
696
600
0
724
770
834
771
830
(-)
SPEED DEMAND
LEVEL
790

FIG. 15A

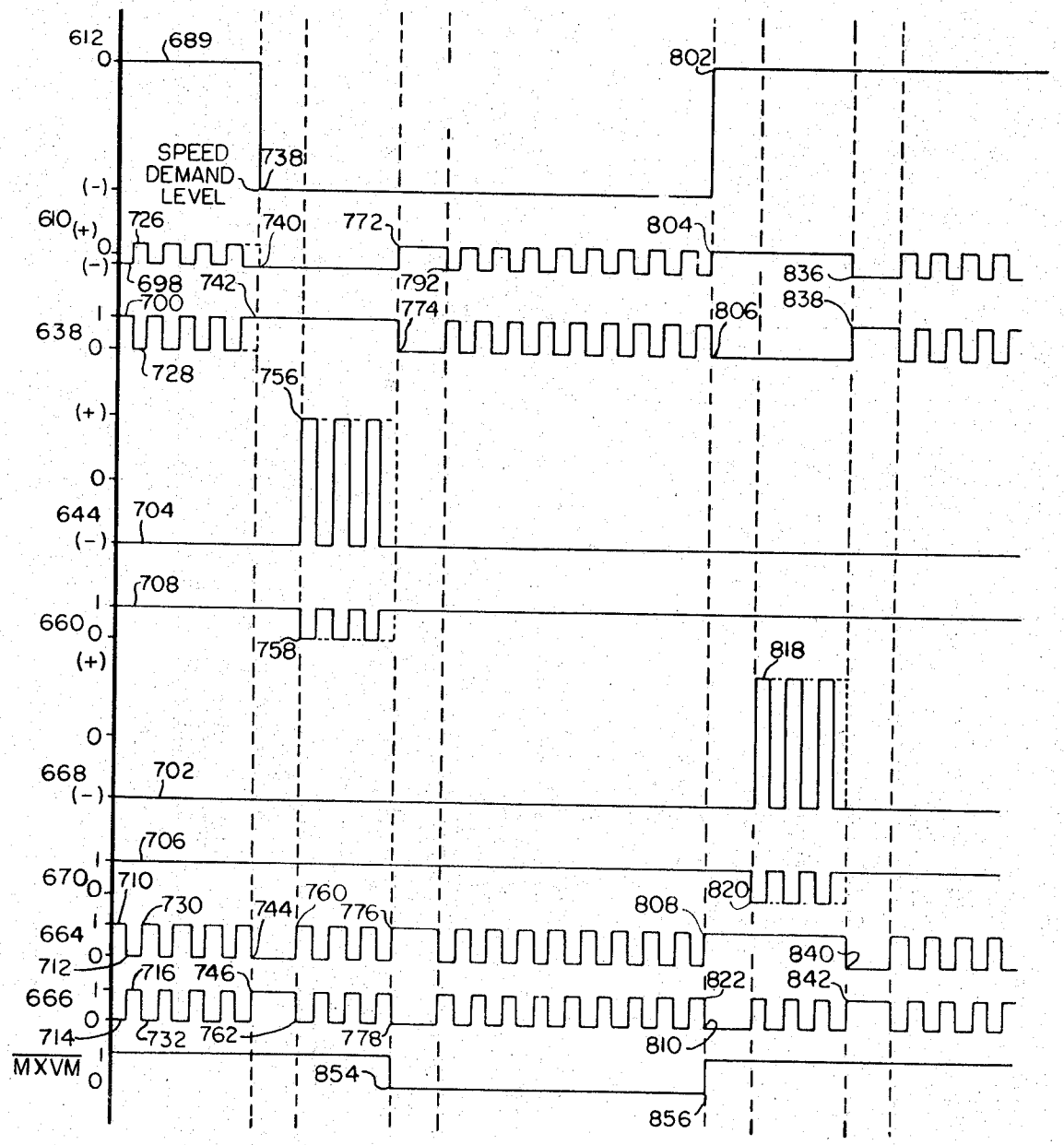

612
0
689
802
SPEED DEMAND LEVEL
738
(-)
610
(+)
0
(-)
726
740
772
804
836
698
742
792
700
774
806
838
638
1
0
728
756
(+)
0
644
704
(-)
708
660
1
0
758
818
(+)
0
668
702
(-)
706
670
1
0
710
730
744
760
776
808
820
664
1
0
712
716
746
822
840
842
666
1
0
714
732
762
778
810
MXVM
1
0
854
856

FIG. 15B

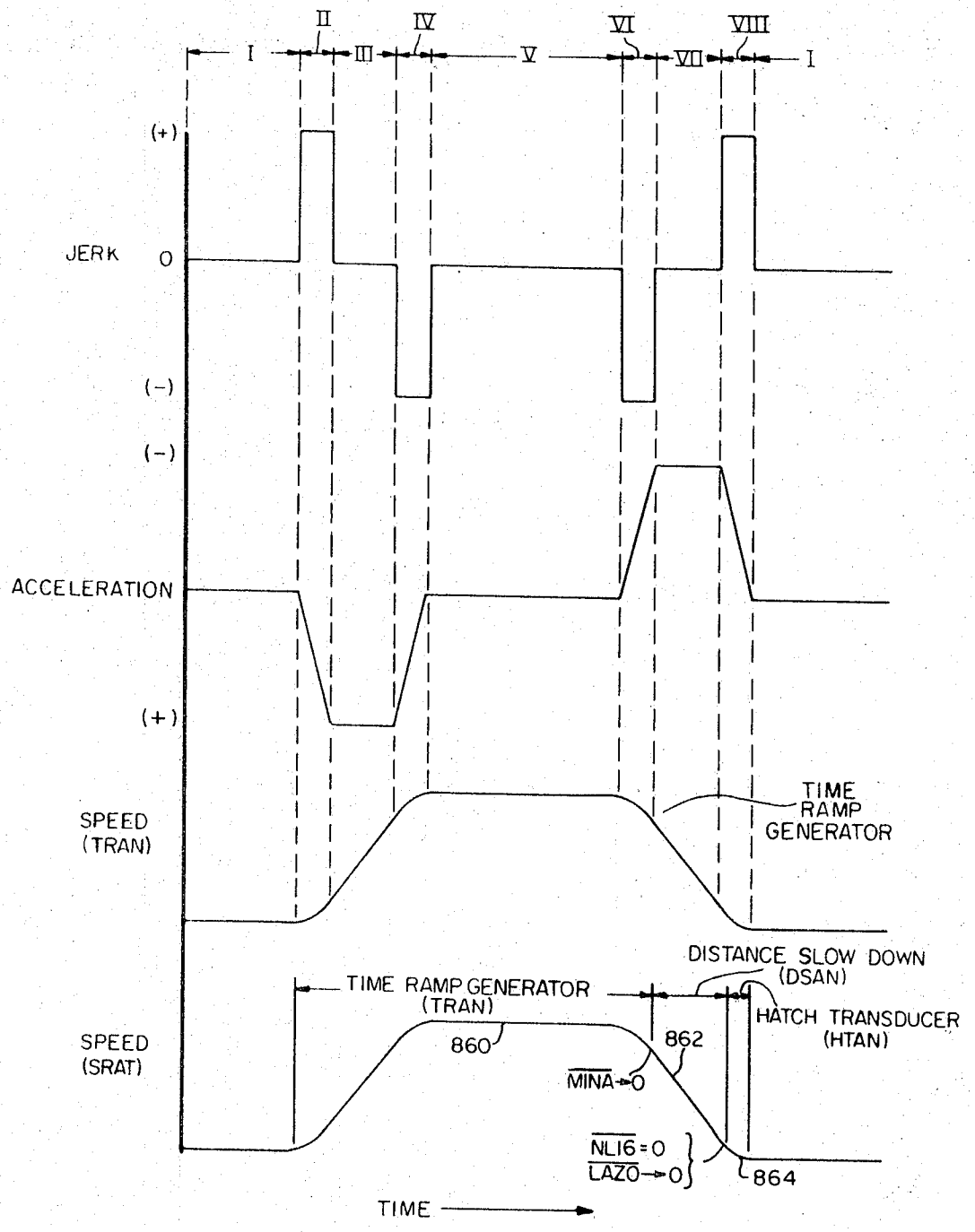

I
II
III
IV
V
VI
VII
VIII
I
(+)
JERK
0
(-)
(-)
ACCELERATION
(+)
SPEED
(TRAN)
TIME
RAMP
GENERATOR
DISTANCE SLOW DOWN
(DSAN)
TIME RAMP GENERATOR
(TRAN)
HATCH TRANSDUCER
(HTAN)
SPEED
(SRAT)
860
862
MINA→0
NLI6=0
LAZO→0
864
TIME

FIG. 16

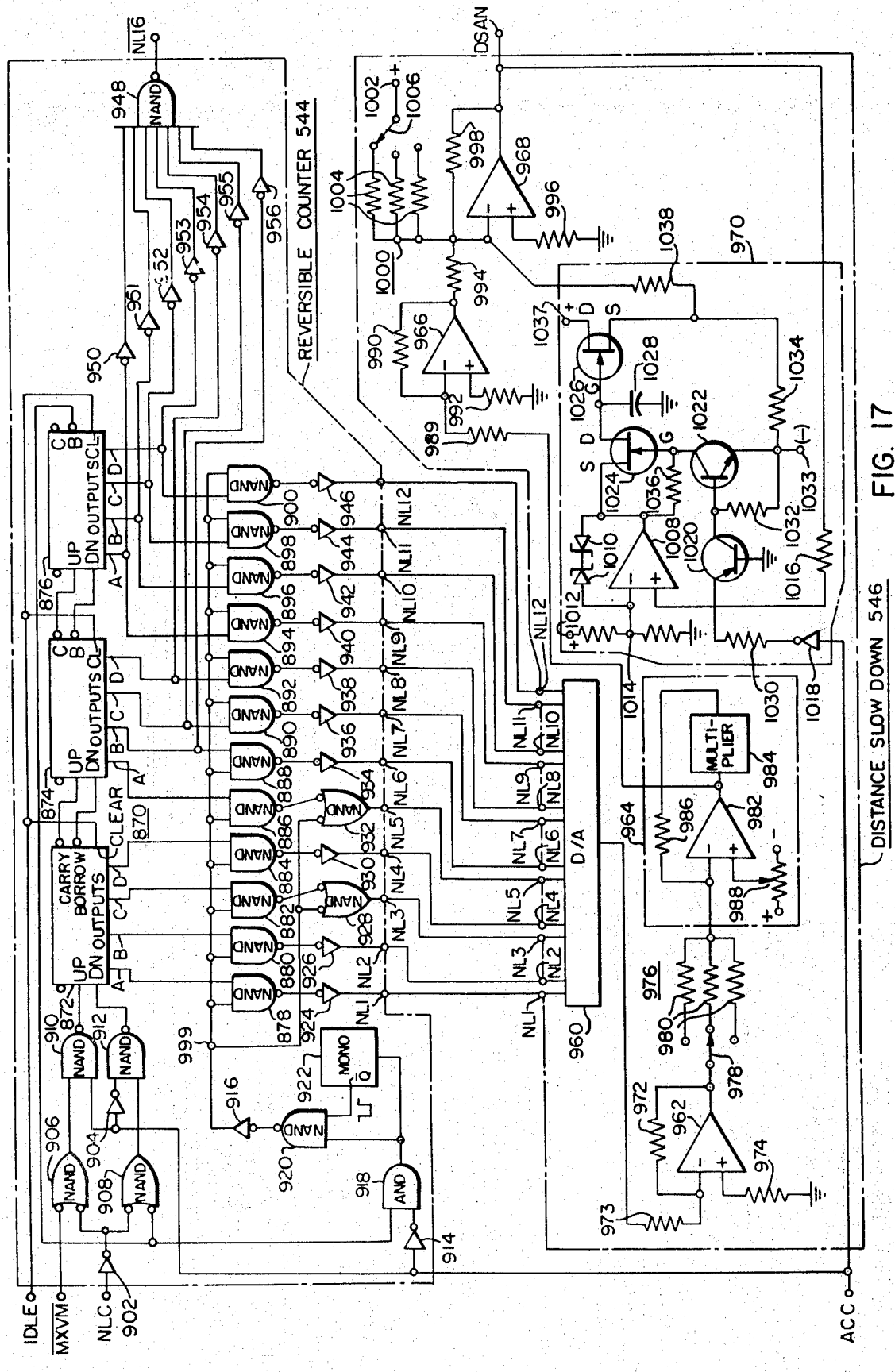

REVERSIBLE COUNTER 544
DISTANCE SLOW DOWN 546
D/A
MULTI-PLIER
MONO
NAND
AND
UP DN OUTPUTS CL
CARRY BORROW
CLEAR
IDLE
MXVM
NLC
ACC
DSAN
NL16
NL12
NL11
NL10
NL9
NL8
NL7
NL6
NL5
NL4
NL3
NL2
NL1

FIG. 17

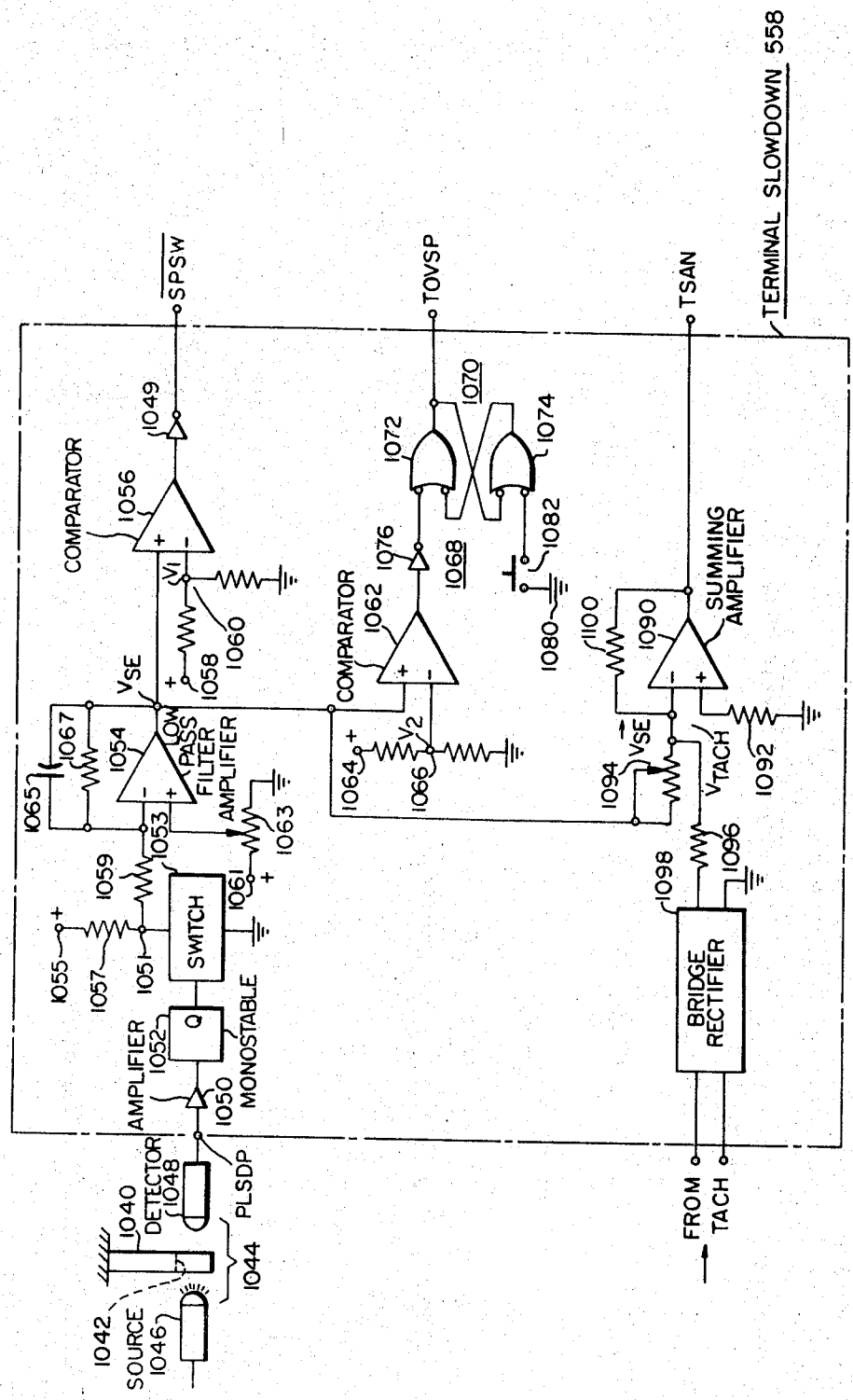

SPSW
TOVSP
TSAN
TERMINAL SLOWDOWN 558
1049
COMPARATOR
1056
V1
1060
1058
VSE
1067
1054
LOW PASS FILTER AMPLIFIER
1065
1053
1063
1059
1061
1055
1057
1051
SWITCH
MONOSTABLE
Q
1052
AMPLIFIER
1050
DETECTOR
1048
1040
PLSDP
1044
1042
SOURCE
1046
1070
1072
1074
1076
1068
1082
1080
COMPARATOR
1062
V2
1064
1066
1100
1090
SUMMING AMPLIFIER
1094
VSE
VTACH
1092
1096
1098
BRIDGE RECTIFIER
FROM TACH

FIG. 18

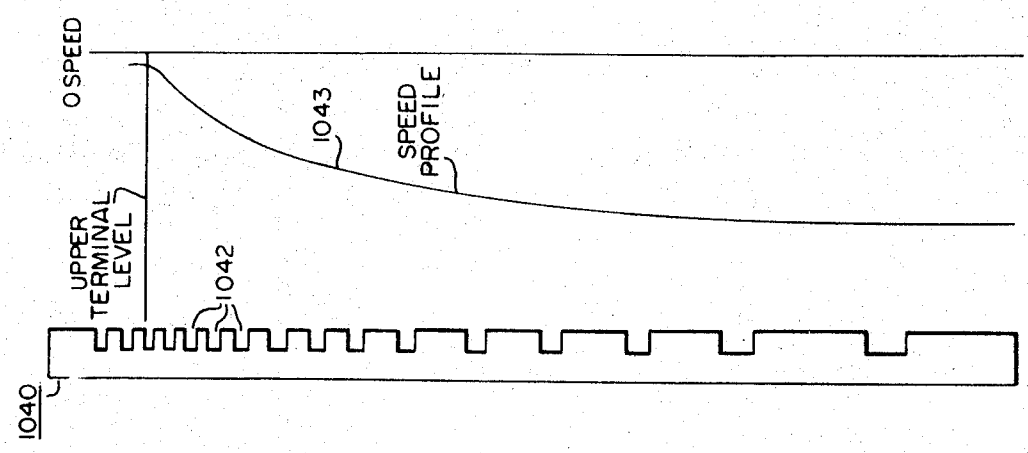

0 SPEED
1043
SPEED PROFILE
UPPER TERMINAL LEVEL
1042
1040

FIG. 19

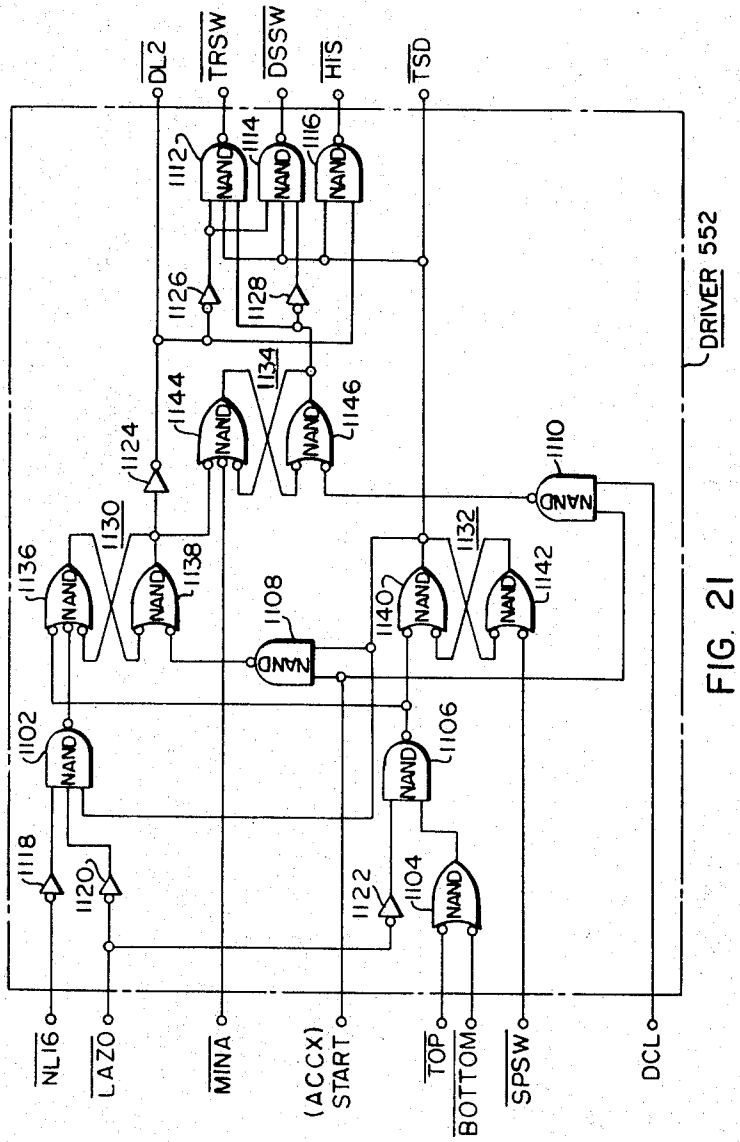
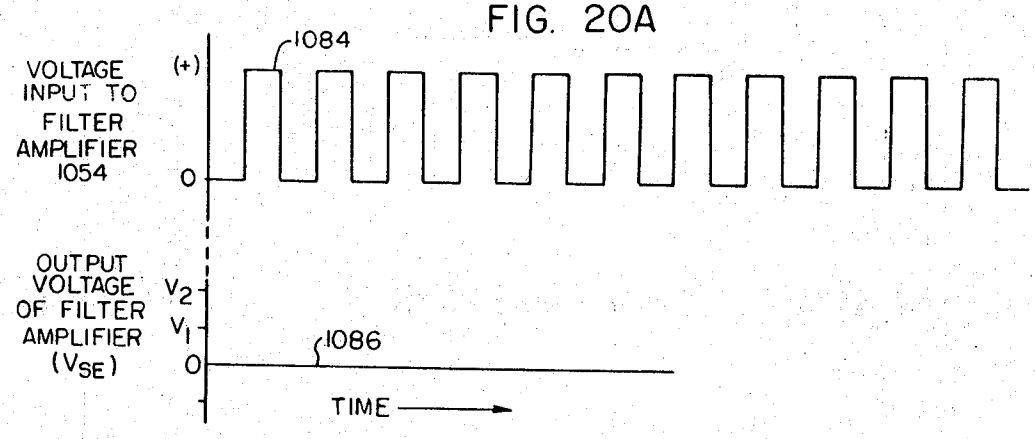

DL2
TRSW
DSSW
HIS
TSD
NAND
1112
1114
1116
1126
1128
1134
1144
1146
1124
1130
1136
1138
1108
1140
1132
1142
1110
1102
1106
1118
1120
1122
1104
DRIVER 552
NL16
LAZO
MINA
(ACCX) START
TOP
BOTTOM
SPSW
DCL

FIG. 21

FIG. 20A



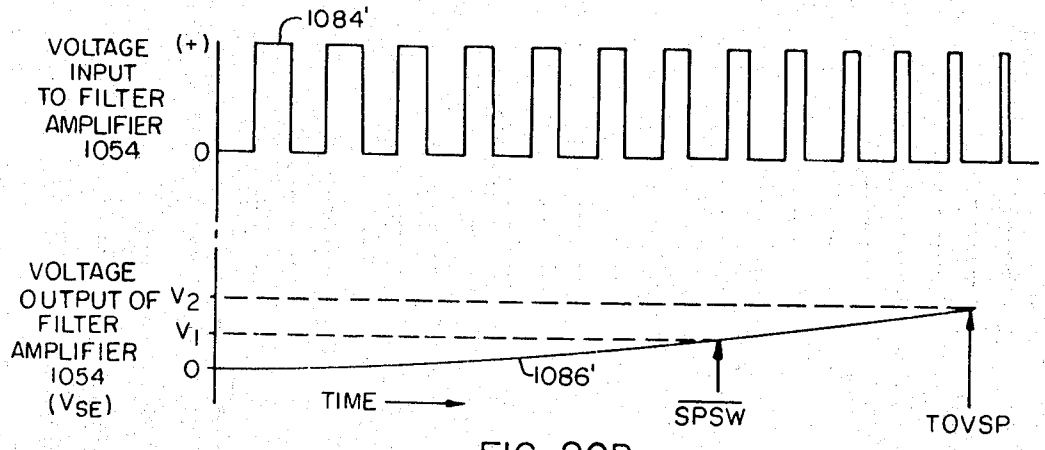


FIG. 20B

SPEED PATTERN GENERATOR FOR ELEVATOR SYSTEMS

CROSS-REFERENCES TO RELATED APPLICATIONS

Certain of the apparatus disclosed but not claimed in the present application, is claimed in the following concurrently filed, copending applications:

Application Ser. No. 254,007, filed May 17, 1972, entitled "FLOOR SELECTOR FOR AN ELEVATOR SYSTEM," which application is assigned to the same assignee as the present application.

Application Ser. No. 254,119, filed May 17, 1972, entitled "DISTANCE SLOWDOWN CONTROL FOR ELEVATOR SYSTEMS," which application is assigned to the same assignee as the present application.

Application Ser. No. 254,005, filed May 17, 1972, entitled "TERMINAL SLOWDOWN CONTROL FOR ELEVATOR SYSTEMS," which application is assigned to the same assignee as the present application.

BACKGROUND OF THE INVENTION

1. Field of the Invention

The invention relates in general to elevator systems, and more specifically to a speed pattern generator for elevator systems.

2. Description of the Prior Art

Elevator systems which utilize electromechanical controllers provide no direct control of jerk via the speed pattern, but depend upon other factors to limit jerk. The design of the car dynamic controller is a compromise between a plurality of criteria, such as system response time, landing characteristics, and value of deceleration during the slowdown phase. During installation of the elevator system, the system is carefully adjusted to provide the required jerk limitation, which again involves compromise between factors such as deceleration overshoot, landing overshoot, and oscillations in car speed during acceleration. Further, the system may require periodic readjustment of jerk, if the parameters of the dynamic system drift due to aging, temperature and wear.

Elevator systems with solid state controllers may provide control over maximum jerk in the speed pattern itself. For example, U.S. Pat. No. 3,523,232 discloses a position versus time pattern generator, which develops an acceleration signal and then superposes jerk constraint on the acceleration signal via an integrator. This jerk constraint acceleration signal is integrated twice to obtain the command position signal with respect to time. U.S. Pat. No. 3,350,612 uses a capacitor to smooth the transitions between the various portions of a pattern signal.

SUMMARY OF THE INVENTION

The present invention is a new and improved speed pattern generator of the solid state type, which provides a time optimum speed pattern signal with controlled jerk incorporated into the speed pattern. Further, the maximum jerk is directly controlled, and adjustable.

More specifically, an on-off type signal or step signal is provided which represents the value of jerk, or rate of change of acceleration. The step signal is switchable between first and second magnitudes, with the actual jerk to which the elevator car will be subjected being determined by the signal magnitudes.

The first and second magnitudes of the step or jerk signal provide currents of opposite polarity. The current responsive to the magnitude selected is integrated to provide a signal representing car acceleration, or deceleration, and the acceleration signal is integrated to generate the time dependent speed reference signal for the motor controller.

Acceleration and speed feedback loops select one of the two magnitudes of the jerk signal, to incorporate the jerk constraint during the transition periods between: (1) zero car speed and maximum acceleration, (2) maximum acceleration and maximum velocity, (3) maximum velocity and maximum deceleration, and (4) maximum deceleration and zero car speed. During the period when the car is at rest, and during the periods of constant acceleration and constant velocity or speed, the feedback circuits switch the jerk signal between its two magnitudes such that jerk is averaged to zero, with the switching rate being faster than the response time of the elevator car.

The time dependent speed pattern provides a pattern for a complete run, and may be used to control a complete run on relatively low speed elevator systems. On higher speed elevator systems, the time dependent speed pattern may be used for certain phases of the run, with the time dependent signal being replaced by distance dependent reference signals for other phases of the run. For example, the time dependent speed pattern may be used to accelerate the car and for the full speed phase, switching to a distance dependent slowdown signal when maximum deceleration is reached during the slowdown phase.

In the disclosed speed pattern generator, the value of jerk is not dependent upon system transfer functions, there is no need for field adjustment, and since there is no interaction between jerk control and other parameters, the other parameters may be optimized independently of the jerk control.

BRIEF DESCRIPTION OF THE DRAWINGS

The invention may be better understood, and further advantages and uses thereof more readily apparent, when considered in view of the following detailed description of exemplary embodiments, taken with the accompanying drawings, in which:

FIG. 1 is a partially schematic and partially block diagram illustrating an elevator system which may utilize the teachings of the invention;

FIG. 2 is a block diagram of a floor selector which embodies the basic concepts of the invention;

FIG. 3 is a block diagram of a floor selector which embodies the basic concepts of the invention, and additionally illustrates a preferred embodiment thereof;

FIG. 4 is a timing diagram for scanning position zero of the scan counter, which illustrates the development of certain of the timing signals used in the floor selector;

FIG. 5 is a schematic diagram of a counter, decoder, memory, comparator and indexer suitable for use in the floor selector shown in FIG. 3;

FIG. 6 is a schematic diagram of a counter, comparator, and top/bottom reset suitable for use in the floor selector shown in FIG. 3;

FIG. 7 is a timing diagram for a 30 floor building which illustrates certain signals explanatory of the operation of the floor selector shown in FIG. 3;

FIG. 8 is a schematic diagram of a call selector suitable for use in the floor selector shown in FIG. 3;

FIG. 9 is a schematic diagram of logic circuitry suitable for use in the floor selector shown in FIG. 3;

FIG. 10 is a schematic diagram of a synchronizer suitable for use in the floor selector shown in FIG. 3;

FIG. 11 is a diagram which illustrates which corridor calls a car can consider when it is set for up and down travel;

FIG. 12 is a block diagram of a speed pattern generator which may be used in the elevator system shown in FIG. 1;

FIG. 13 is a schematic diagram of logic circuitry suitable for use in the speed pattern generator shown in FIG. 12;

FIG. 14 is a schematic diagram of a time ramp generator suitable for use in the speed pattern generator shown in FIG. 12;

FIG. 15 is a graph illustrating the waveforms at various circuit points of the time ramp generator shown in FIG. 14;

FIG. 16 is a graph illustrating time dependent jerk, acceleration, and speed signals for the speed pattern generator shown in FIG. 12;

FIG. 17 is a schematic diagram of a distance slow-down circuit suitable for use in the speed pattern generator shown in FIG. 12;

FIG. 18 is a schematic diagram of a terminal slow-down circuit suitable for use in the speed pattern generator shown in FIG. 12;

FIG. 19 illustrates a terminal slow-down blade of the type which may be used in conjunction with a pulse generator to provide pulses for the terminal slow-down circuit shown in FIG. 18;

FIGS. 20A and 20B are graphs which illustrate the operation of the terminal slow-down circuit shown in FIG. 18; and

FIG. 21 is a schematic diagram of a driver circuit which may be used in the speed pattern generator shown in FIG. 12.

DESCRIPTION OF PREFERRED EMBODIMENTS

FIG. 1

Referring now to the drawings, and FIG. 1 in particular, there is shown an elevator system **10** wherein a car **12** is mounted in a hatchway **13** for movement relative to a structure **14** having a plurality of landings, such as **30,** with only the first, second and 30 landings being shown in order to simplify the drawing. The car **12** is supported by a rope **16** which is reeved over a traction sheave **18** mounted on the shaft of a drive motor **20,** such as a direct current motor as used in the Ward-Leonard drive system. A counterweight **22** is connected to the other end of the rope **16.** A governor rope **24,** which is connected to the top and bottom of the car **12,** is reeved over a governor sheave **26** located above the highest point of travel of the car in the hatchway **13,** and over a pulley **28** located at the bottom of the hatchway. A pickup **30** is disposed to detect movement of the car **12** through the effect of circumferentially spaced openings **26A** in the governor sheave **26.** The openings in the governor sheave are spaced to provide a pulse for each standard increment of travel of the car, such as a pulse for each 0.5 inch of car travel. Pickup **30,** which may be of any suitable type, such as optical or magnetic, provides pulses in response to the movement of the openings **26A** in the governor sheave. Pickup **30** is connected to a pulse detector **32** which provides distance pulses for a floor selector **34.** Distance pulses may be developed in any other suitable manner, such as by a pickup disposed on the car which cooperates with regularly spaced indicia in the hatchway.

Car calls, as registered by pushbutton array **36** mounted in the car **12,** are recorded and serialized in car call control **38,** and the resulting serialized car call information is directed to the floor selector **34.**

Corridor calls, as registered by pushbuttons mounted in the corridors, such as the up pushbutton **40** located at the first landing, the down pushbutton **42** located at the thirtieth landing, and the up and down pushbuttons **44** located at the second and other intermediate landings, are recorded and serialized in corridor call control **46.** The resulting serialized corridor call information is directed to the floor selector **34.**

The floor selector **34** processes the distance pulses from pulse detector **32** to develop information concerning the position of the car **12** in the hatchway **13,** and also directs these processed distance pulses to a speed pattern generator **48** which generates a speed reference signal for a motor controller **50,** which in turn provides the drive voltage for motor **20.**

The floor selector **34** keeps track of the car **12,** the calls for service for the car, provides the request to accelerate signal to the speed pattern generator **48,** and provides the deceleration signal for the speed pattern generator **48** at the precise time required for the car to decelerate according to a predetermined deceleration pattern and stop at a predetermined floor for which a call for service has been registered. The floor selector **34** also provides signals for controlling such auxiliary devices as the door operator **52,** the hall lanterns **54,** and controls the resetting of the car call and corridor call controls when a car or corridor call has been serviced.

Landing, and leveling of the car at the landing, is accomplished by a hatch transducer system which utilizes inductor plates **56** disposed at each landing, and transformer **58** disposed on the car **12.**

The motor controller **50** includes a speed regulator responsive to the reference pattern provided by the speed pattern generator **48.** The speed control may be derived from a comparison of the actual speed of the motor and that called for by the reference pattern by using a drag magnet regulator, such as disclosed in U.S. Pat. Nos. 2,874,806 and 3,207,265, which are assigned to the same assignee as the present application. The precision landing system using inductor plates **56** and transformer **58** is described in detail in U.S. Pat. No. 3,207,265.

An overspeed condition near either the upper or lower terminal is detected by the combination of a pickup **60** and slowdown blades, such as a slowdown blade **62.** The pickup **60** is preferably mounted on the car **12,** and a slowdown blade is mounted near each terminal. However, a single slowdown blade mounted on the car could cooperate with pickups disposed near each terminal. The slowdown blade has spaced openings, such as a toothed edge, with the teeth spaced to generate pulses in the pickup **60** when there is relative motion between them, which pulses are processed in pulse detector **64** and directed to the speed pattern generator **48** where the pulses are used to detect overspeed.

FIG. 2

FIG. 2 is a block diagram of floor selector **34**, which embodies the basic concepts thereof. The distance pulses from the pulse detector **32** are applied to a reversible counter **70**, which starts with ZERO count at the lowest or first landing, counts up when the car is travelling upwardly, and counts down when the car is travelling downwardly. Counter **70** is forcibly reset to ZERO at the bottom landing, in the event it is a few counts off, and it may also be reset to the count representing the uppermost landing when it arrives at that floor, to correct any error in the count. Counter **70** is preferably a binary counter having the number of bits necessary to count to the binary number determined by the standard increment used to generate a pulse, and the height between the lowest and uppermost floors.

Counter **70** is arranged to output a binary number which continuously changes as the car moves relative to the structure, to continuously indicate the advanced car position, as opposed to the actual position of the car in the hoistway. This continuous advanced car position is the point at which the car could be brought to a stop from its current velocity under a predetermined deceleration schedule. The continuous advanced car position is more important than the actual position of the car in high speed elevator systems, as several floors are needed to bring the car to a smooth stop without unnecessary stress on the passengers.

As disclosed in the hereinbefore mentioned U.S. Pat. No. 3,589,474, the continuous advanced car position may be generated directly in the reversible counter **70** by generating pulses at twice the rate of the distance pulses when the car is accelerating, and at the same rate as the distance pulses when the car is travelling at constant speed. When deceleration is initiated, the counting of the distance pulses is discontinued such that when the car comes to a stop, the count in the counter reflects the actual car position.

A second reversible counter **72** provides a signal which indicates the discrete advanced car position in terms of floor number. The second reversible counter **72** is also preferably a binary counter, having the number of bits necessary to provide a binary word for the uppermost floor. Counter **72** may be reset at one or both of the terminals, and it is indexed up or down, as required, as the count of the continuous advanced car position changes, as will be hereinafter described.

A read only memory **74** is provided, which, when addressed by the binary word of counter **72**, which represents the discrete advanced car position with a floor number, outputs a binary word having the number of bits necessary to describe the exact location of that floor relative to the structure, with a resolution of the same standard increment used to generate pulses, such as 0.5 inch. The read only memory is preferably a matrix of fused diodes, with the presence of a diode corresponding to a logical ONE, while a missing diode, i.e., one in which its fuse has been blown, represents a logical ZERO. A diode may be disconnected from the matrix by discharging a charged capacitor across it and blowing the fuse in series with it. Thus, the read only memory may be precisely set for each floor of the structure it is associated with, during field installation. For example, the elevator car is leveled at the bottom floor, the counter **70** is reset to all ZERO's, the floor selector for the read only memory **74** is set to the bottom floor and the bits of counter **70** are each connected to a bit of the read only memory through an inverter and a switch, which when actuated, discharges a capacitor through the associated diode of the read only memory if the inverted bit of counter **70** is a logical ONE. Thus, when counter **70** registers all ZERO's at the bottom landing, the inverted bits are all ONE's and all of the diodes of the read only memory **74** would be disconnected from the circuit for floor position one. The car is then moved by a hand operation to the next landing and leveled exactly with the floor without overshooting. The count of counter **70** thus describes the exact location of this floor relative to the structure, and the word or floor selector of the read only memory is set to the second word. Depressing the switch will set the second word of the memory to the count in the counter **70**. This sequence is repeated until the exact location of all of the floors have been preset into the read only memory. Thus, addressing memory **74** with a word from counter **72** containing the number of bits necessary to describe the number of a floor, causes the memory **74** to output a word having the number of bits necessary to accurately describe the location of the floor in the structure with the same resolution used in counter **70** to describe the continuous advanced car position. For example, a 5 bit input word describing a floor number may output a 16 bit word describing the location of that floor in the structure.

A bit-by-bit comparator **76** is provided which compares the binary output words of counter **70** and memory **74**. When the binary words of counter **70** and memory **74** are equal, comparator **76** outputs an equality signal EQ2. Thus, when the car is travelling upwardly, when the binary words of counter **70** and memory **74** are equal, the equality signal EQ2 is generated. The equality signal EQ2 indicates slowdown must be initiated at this time or the car cannot stop at the discrete advanced car position. If deceleration is not initiated at that point, counter **70** will continue to count up in response to the distance pulses, the binary word of counter **70** will exceed the binary word of memory **74**, and comparator **76** provides a signal for indexer **78**. Indexer **78** provides a signal for counter **72** which increments the counter **72** to output the binary word for the next higher floor.

When the car is travelling downwardly and the binary word of counter **70** becomes equal to the binary word of memory **74**, the equality signal EQ2 is generated. If deceleration is not initiated at this time, counter **70** will continue to count down in response to the distance pulses and as soon as the binary word of counter **70** is less than the binary word of memory **74**, comparator **76** provides a signal for indexer **78**, which in turn provides an index signal for counter **72**, decrementing counter **72** by one floor to indicate the floor number of the next lower floor. The output of memory **74** is thus changed to the address of that floor.

A third counter **80** is provided which is a continuous scan type counter, preferably of the binary type, which starts at ZERO, counts to a predetermined binary number in a predetermined period of time, and starts the next predetermined period of time at ZERO again, thus dividing each succeeding predetermined period of time into a plurality of intervals or time slots. The location of the same interval in any predetermined period of time is thus identified by the same binary number. The number of intervals in each scanning period is deter-

mined by the number of floors in the structure, with the number of intervals being at least as large as the number of floors. A five bit scan counter, for example, will provide 32 intervals before automatically resetting to ZERO and starting the next scanning period. If the number of floors is greater than 32, a six bit counter will provide 64 intervals, etc. The length of time for each interval is determined by the rate at which call information can be gathered from the car and corridor pushbuttons, which rate is limited due to noise pickup in the travelling cable. A time interval of 2 milliseconds has been found to be satisfactory. Thus, with a five bit scan counter, a predetermined scan period would be 32 times 2 or 64 milliseconds, with each of the 32 intervals occupying 2 milliseconds of the period. The scan counter 80 is controlled by a master system clock.

A second bit-by-bit comparator 82 is provided which compares the binary output word of counter 72, which describes the floor number of a discrete advanced car position, with the binary output of the scan counter 80. Comparator 82 provides a signal EQIZ during each predetermined period of time when the binary number of the scanning position of the scan counter 80 is equal to the binary word of counter 72. Signal EQIZ may thus be termed the serial advanced car position signal, as it locates the advanced car position at the specific interval or time slot of the scan which identifies the floor of the advanced car position.

A logic circuit 84 receives car and corridor calls, with the car calls, up corridor calls, and down corridor calls each being in serial form, synchronized with the scan counter. Thus, a car call for a predetermined floor would appear in the time slot or interval for that floor, as developed by the scan counter. In like manner, up and down corridor calls from specific floors would appear in their associated intervals of each scan period. The logic circuit 84 detects coincidence of a call for service, which the car is conditioned to serve, for the floor of the advanced car position. If the car travel direction is up, the car is conditioned to consider car and corridor calls registered for the floors ahead of its travel direction. The car will handle all requests for up service ahead of it, and when there are no more requests for up service, it is conditioned to go to the highest registered call for down service, and then serve all requests for down travel registered ahead of it. Once no calls ahead of it request down service, the car is conditioned to go to the lowest call requesting up service, and handle all calls for up service ahead of it.

The coincidence of a call for service for the floor of the serial advanced car position signal is memorized by the logic circuit 84, and when the equality signal EQ2 is generated by the comparator 76, deceleration is immediately initiated, which prevents counter 70 from registering any further distance pulses. The count of counter 72 thus is not indexed, and when the car stops at the floor at which service was requested, the discrete advanced car position and the continuous advanced car position will both be the actual car position. If coincidence of a request for service for the floor of the discrete advance car position is not detected before the equality signal EQ2 is generated by comparator 76, the next distance pulse will cause the comparator to provide a signal for indexer 78, which indexes counter 72 to provide a binary number representing the number of the next floor at which the car can stop.

FIG. 3

FIG. 3 is a block diagram of floor selector 34, which presents a detailed functional view of a preferred embodiment of the invention, with like reference numerals in FIGS. 2 and 3 indicating like components, which will not be described in detail since they have already been described relative to FIG. 2.

More specifically, FIG. 3 includes a top/bottom reset means 86 which is responsive to car landing detectors at the top and bottom floors to provide a load signal, termed $\overline{\text{LOAD N}}$ for the counters 70 and 72. Memories addressed by the specific terminal location output a binary word describing the location, i.e., a floor number with respect to counter 72 and the location of the floor in the structure with respect to counter 70, which words are loaded into the counters when the $\overline{\text{LOAD N}}$ counter signal is generated.

A min/max decoder 88 is provided which detects arrival of the continuous advanced car position at the top and bottom floors and initiates terminal slowdown with a signal $\overline{\text{TDS}}$ in the event coincidence of the serial advanced car position signal EQIZ with a call for service for the approaching terminal does not occur before the generation of the equality signal EQ2.

A read only memory 90 is provided which is preset to identify which intervals, if any, are not assigned to floors, and to identify the intervals which do not have up and down corridor calls, i.e., the upper and lower floors, respectively.

The logic circuit 84 of FIG. 2 is shown in greater detail in FIG. 3. Logic circuit 84 includes a call selector circuit 92, a synchronizer circuit 94, and a logic circuit 96. The call selector circuit 92 receives the serial advanced car position signal EQ1Z and detects any coincidence between signal EQ1Z and the serial up and down corridor calls, and car calls, 1Z, 2Z and 3Z, respectively. When coincidence is detected, a coincidence signal $\overline{\text{EIX}}$ is generated which is synchronized in the logic circuit 96 and applied to the synchronizer 94 as signal EI. The synchronizer determines if the request to stop at the floor of the advanced car position signal EI occurs prior to the generation of the equality signal EQ2 by comparator 76. If the EI signal is received by the synchronizer 94 prior to its receiving the equality EQ2, a deceleration request signal DEC is generated which is processed by the logic circuit 96 to provide a signal $\overline{\text{ACCX}}$ for the speed pattern generator 48. If an EI signal is not received by the time the equality signal EQ2 is generated, comparator 76 provides a signal for indexer 78, and indexer 78 provides a pulse-up or pulse-down signal $\overline{\text{PU}}$ or $\overline{\text{PD}}$, respectively, for indexing counter 72 to output the binary word representing the floor number where the car can stop according to the predetermined deceleration schedule. The remaining signals shown in FIG. 3 will be described when the circuits for performing the various functions are described.

FIG. 4

Before describing the circuits which may be used in the floor selector 34, it will helpful to illustrate the development of some of the timing signals used in the operation of the floor selector. FIG. 4 is a timing diagram which illustrates the signals generated during scanning position ZERO, termed 00, of the scan counter 30 shown in FIG. 2, which will be assumed to be a 2 milli-

second interval. The system or master clock is a 32 Khz. signal, termed K32, from which the other timing signals are derived. Signals K16, K08, K04, K02, K01 and KP5 are 16 Khz., 8 Khz., 4 Khz., 2 Khz., 1 Khz., and 500 hz. square wave timing or clock signals, respectively, developed by dividing the basic clock signal K32 in a binary counter.

Clock signals K08S and K02S are developed by shifting clock signals K08 and K02, respectively, forward by 90 degrees.

Clock signal $\overline{STC}$ is developed by inverting clock signals K01 and KP5 and using these inverted signals as inputs for a NAND gate ($\overline{STC} = \overline{KO1 \cdot KP5}$).

Clock signals S1, S2, S3 and S4 are developed in the first, second, third and fourth quadrants, respectively, of each scanning position, with signal S1 being equal to $\overline{KO1 \cdot KP5} \cdot KO2S$, signal S2 being equal to $KO1 \cdot \overline{KP5} \cdot K02S$, signal S3 being equal to $\overline{KO1} \cdot KP5 \cdot KO2S$, and signal S4 being equal to $KO1 \cdot KP5 \cdot KO2S$.

All of the preceeding signals are developed during each scanning position of scan counter 80.

Clock signals S100, S200 and S300 are developed only during scanning position 00 of scan counter 80, with signal S100 being equal to 00·S2, signal S200 being equal to 00·S2, and signal S300 being equal to 00·S3.

In order to better understand the following detailed description of circuits which may be used in the invention, the signals generated by the various circuits, and the functions thereof, are listed below. Timing signals are not listed, as they are shown in FIG. 4.

SIGNAL	FUNCTION
ACC	CAR TO ACCELERATE OR TRAVEL AT FULL SPEED
$\overline{ACCX}$	ACCELERATION REQUEST
AVP0–AVP4	ADVANCED CAR POSITION IN BINARY
BOTTOM	CAR IS WITHIN 18" OF BOTTOM TERMINAL
$\overline{BYPS}$	CAR BYPASSING CORRIDOR CALLS
CA	CALL ABOVE FLOOR OF ADVANCED CAR POSITION
CB	CALL BELOW FLOOR OF ADVANCED CAR POSITION
CCY	SERIAL CAR CALLS
CEN	CALL ENABLE
CFLY	CALL AT FLOOR DURING FIRST SCAN
DCE	DOWN CALL ENABLE
$\overline{DCL}$	DOORS CLOSED
$\overline{DCY}$	SERIAL DOWN CALLS
DEC	DECELERATION REQUEST
$\overline{DECS}$	SYNCHRONIZED DEELERATION REQUEST
$\overline{DGD}$	SIGNAL TO DRIVE "GO DOWN" INTERFACE RELAY
$\overline{DGU}$	SIGNAL TO DRIVE "GO UP" INTERFACE RELAY
$\overline{DL2}$	SIGNAL TO DRIVE LANDING INTERFACE
$\overline{DO}$	DOOR OPEN REQUEST ENABLE
$\overline{DOR}$	DOOR OPEN REQUEST
$\overline{DORR}$	RESET-DOOR OPEN REQUEST
DOWN	SIGNAL WHICH IS TRUE WHEN CAR IS SET TO TRAVEL DOWN
DPL	DISTANCE PULSES
DNRZ	SERIAL DOWN CORRIDOR CALL RESET
DSAN	SPEED PATTERN FROM DISTANCE SLOWDOWN CIRCUIT
DSSW	DRIVING SIGNAL FOR DSAN SWITCH
D45	DOOR MASTER RELAY DRIVER
E1 CALL AT ADVANCED CAR POSITION	
E1X	REQUEST FOR STOP
$\overline{EQ1Z}$	SERIAL CAR POSITION
$\overline{EQ2}$	ADVANCED CAR POSITION EQUAL TO FLOOR LEVEL
$\overline{FSC}$	FIRST SCAN
HLd	ENABLE FOR DOWN HALL LANTERNS
HLU	ENABLE FOR UP HALL LANTERNS
HLX	HALL LANTERN ENABLE
HT1	SIGNAL FROM HATCH TRANSDUCER
HTAN	SIGNAL FROM HATCH TRANSDUCER CIRCUIT
$\overline{HIS}$	DRIVER SIGNAL FOR HTAN SWITCH
$\overline{IDLE}$	CAR IDLE, READY TO MAKE RUN
$\overline{LAZO}$	CAR ±10 INCHES FROM FLOOR LEVEL
$\overline{LOAD\ N}$	LOAD CAR POSITION COUNTERS
MAIN	CAR WITHIN 18 INCHES OF MAIN FLOOR
$\overline{MINA}$	MAXIMUM DECELERATION
MTOO	MEMORY TRACK
MTO1	MEMORY TRACK
$\overline{MXVM}$	MAXIMUM VELOCITY
NC	LOGIC ZERO WHEN NO CALLS
NCS	LOGIC ZERO WHEN NO CALLS
NLC	INPUT PULSES TO COUNTER 544
NL1–NL12	OUTPUT OF DISTANCE TO GO TO LANDING COUNTER 544
$\overline{NL16}$	CAR IS WITHIN 16 INCHES OF LANDING ZONE
$\overline{PCR}$	INDICIATES ADVANCED CAR FLOOR POSITION HAS CHANGED
$\overline{PD}$	PULSE ADVANCED CAR POSITION COUNTER DOWN
PLSDP	PULSES FROM TERMINAL SLOWDOWN BLADE
$\overline{PU}$	PULSE ADVANCED CAR POSITION UP
SAC	SCANNING ABOVE ADVANCED CAR POSITION
SBC	SCANNING BELOW ADVANCED CAR POSITION
$\overline{SDT}$	SET SELECTOR FOR DOWN TRAVEL
$\overline{SPSL}$	SPEED SELECTION SWITCH
$\overline{SPSW}$	TERMINAL OVERSPEED DETECTED
SPS1	SPEED SELECTION NO. 1
SPS2	SPEED SELECTION NO. 2
SRAT	SPEED PATTERN SIGNAL FOR MOTOR CONTROLLER
START	SIGNAL TO START CAR IN RESPONSE TO ACCELERATION REQUEST
$\overline{SUT}$	SET SELECTOR FOR UP TRAVEL
SOS–S4S	SCANNING SIGNALS
$\overline{TDS}$	TERMINAL STOP SIGNAL
TOP	CAR WITHIN 18' OF TOP FLOOR
TOVSP	EXCESSIVE TERMINAL OVERSPEED
TSAN	AUXILIARY SPEED PATTERN USED DURING TERMINAL SLOWDOWN
$\overline{TSD}$	CAR ON TERMINAL SLOWDOWN WHEN LOGIC O
$\overline{TRAN}$	TIME DEPENDENT SPEED PATTERN
$\overline{TRSW}$	DRIVER SIGNAL FROM TRAN
$\overline{UCE}$	UP CALL ENABLE
$\overline{UCY}$	SERIAL UP CORRIDOR CALLS
UP	SIGNAL WHICH IS TRUE WHEN CAR IS SET TO TRAVEL UP
UPRZ	SERIAL UP CORRIDOR CALL RESET
$\overline{UPTR}$	UP TRAVEL
$\overline{ZO2}$	CAR WITHIN 2 INCHES OF FLOOR LEVEL
$\overline{1Z}$	SERIAL UP CORRIDOR CALLS
$\overline{2Z}$	SERIAL DOWN CORRIDOR CALLS
$\overline{3Z}$	SERIAL CAR CALLS

FIGURE 5

FIG. 5 is a schematic diagram of a reversible counter, a decoder, a read only memory, a comparator, and an indexer, which may be used for the counter 70, min/-max decoder 88, the memory 74, the comparator 76, and indexer 78 shown in FIG. 3, with like reference numerals in FIGS. 3 and 5 indicating like components.

Counter 70 includes a plurality of 4 bit synchronous binary counters, with four counters 100, 102, 104 and 106 being illustrated. The actual number of bits, and thus the actual number of cascaded counters required, depends upon the standard increment used to provide the distance pulses, and the distance between the lowest and uppermost floors.

Counter 70 requires that the distance pulses, termed DPL pulses, which are generated by the governor sheave 26 and converted to logic level by the pulse detector 32 shown in FIG. 1, be generated at double rate during acceleration of the car, to establish a continuous advanced car position, at normal rate after the car reaches maximum velocity, and to be discontinued when the car initiates deceleration, in order for the ad-

vanced car position and actual car position to coincide as the car comes to a stop at a landing. The DPL pulses must be directed to the count-up or count-down inputs of counter **70**, depending upon the direction of car travel. The speed pattern generator **48** requires that it receive the distance pulses at the rate they are generated at all times during car movement. All of these functions are provided by the circuit which includes first and second type D, positive edge triggered flip-flops **108** and **110**, a cross-coupled NAND gate flip-flop **112**, first, second, third, fourth fifth, sixth and seventh NAND gates **114, 116, 118, 120, 124** and **134**, respectively, first, second, third, fourth, fifth, sixth and seventh NOT gates or inverters **125, 126, 128, 130, 132, 133** and **135**, respectively.

The DPL distance pulses are applied to an input terminal which is identified with the same letters as the signal applied thereto, as are the input and output terminals in all of the various figures to be described herein. Input terminal DPL is connected to the D input of flip-flop **108**. Clock signals **K08** are connected to the C input of flip-flop **108** via inverter **125**. The Q output of flip-flop **108** is connected to the D input of flip-flop **110** and to an input of NAND gate **114**. The $\overline{Q}$ output of flip-flop **108** is connected to an input of NAND gate **116**. Clock signals **K08S** are connected to the C input of flip-flop **110**. The Q and $\overline{Q}$ inputs of flip-flop **110** are connected to inputs of NAND gates **116** and **114**, respectively. Input terminal $\overline{MXVM}$ is connected to an input of NAND gate **116**. Signal $\overline{MXVM}$, as will be hereinafter described, is generated by the speed pattern generator **48**, with signal $\overline{MXVM}$ going to logical ZERO when the elevator car reaches maximum velocity.

The output of NAND gate **114** is connected to an input of NAND gate **134**, and via inverter **126** to an output terminal NLC. Output terminal NLC provides distance pulses NLC when pulses are generated by the governor sheave, at the same rate that they are generated. The output of NAND gate **116** is connected to the other input of NAND gate **134**.

The output of NAND gate **134** is connected to inputs of both NAND gates **118** and **120**.

Flip-flop **112** is a travel direction flip-flop, with its set input S connected to an input terminal UP via inverter **133**, and its reset input connected to an input terminal DOWN via inverter **135**. Signals UP and DOWN are logic signals responsive to the direction of car travel, with signal UP being a logical ONE when the car is travelling up and signal DOWN being a logical ONE when the car is travelling down. The useful output of flip-flop **112** is termed $\overline{DN}$, and it is connected to an input of NAND gate **118**, and to an input of NAND gate **120** via inverter **128**.

An input terminal ACC is connected to the remaining inputs of both NAND gates **118** and **120**. Signal ACC, which is provided by the speed pattern generator **32**, becomes true or a logical ONE when the brake relay for the drive motor is picked up, and false or a logical ZERO when the car is requested to initiate deceleration.

The output of NAND gate **118** is connected to an input of NAND gate **122** via inverter **130**. The output of NAND gate **120** is connected to an input of NAND gate **124** via inverter **132**. The remaining inputs of NAND gates **122** and **124** are connected to the $\overline{MAX}$ and $\overline{MIN}$ outputs of min/max decoder **88**, and, as will hereinafter be explained, signal $\overline{MAX}$ becomes true, or logical ZERO when the output word of the continuous advanced car position (counter **70**), is equal to the binary word describing the upper terminal floor, and signal $\overline{MIN}$ becomes true or logical ZERO when the output word of the continuous advanced car position is all ZERO's, describing the lower terminal floor.

In the operation of counter **70**, it will be assumed that the car is set for up travel, with signal UP being true, and the car is starting to accelerate. Input terminal UP is at the logical ONE level and input terminal DOWN is at the logical ZERO level, which, when both are inverted, sets flip-flop **112**. The output signal $\overline{DN}$ will be at the logic ONE level, applying a logic ONE to an input of NAND gate **118**, and a logic ZERO to an input of NAND gate **120** via inverter **128**. Thus, NAND gate **120** is blocked. When the brake relay is picked up, signal ACC will go to the logic ONE level, since the car is not decelerating. Thus, a pulse appearing at the output of NAND gate **134** will drive the output of NAND gate **118** low, and inverter **130** will apply a logic ONE to the input of NAND gate **122**. As long as the continuous advanced car position is not at the upper terminal, $\overline{MAX}$ will be at the logic ONE level, and gate **122** will output a logic ZERO each time the output of NAND gate **134** goes low. The output of NAND gate **122** is connected to the "count up" input of counter **100**.

NAND gate **134** is operated by the combination of flip-flops **108** and **110**, and NAND gates **114** and **116**, to output twice as many pulses as distance pulses received, until the car reaches maximum velocity, as signaled by $\overline{MXVM}$ going low. Flip-flop **108** receives distance pulses DPL at its D input from terminal DPL and it is clocked by timing signals **K08** via inverter **125**. The Q output of flip-flop **108** applies pulses at the rate of the distance pulses to NAND gate **114**, and NAND gate **114** provides an input to NAND gate **134** and to the NLC output terminal. Thus, as long as distance pulses are received, they will be applied at the rate they are received to an input of NAND gate **134** and to output terminal NLC.

Flip-flop **110** has its D input connected to the Q output of flip-flop **108**, and it is clocked by timing signals **K08S**, which is the **K08** clock signal shifted forward by 90°. This arrangement causes flip-flop **110** to switch **90** degrees later than flip-flop **108** in the 8 Khz. clock signal, resulting in, for each distance pulse, output Q of flip-flop **108** and output $\overline{Q}$ of flip-flop **110** both being at the logic ONE level for 90 degrees, driving the output of NAND gate **114** low for 90 degrees. This overlapping occurs at the start of the positive Q output of flip-flop **108**, and the termination of the $\overline{Q}$ output of flip-flop **110**, which provides the pulse near the start of the DPL pulse.

This overlapping of logic ONE states also occurs between the $\overline{Q}$ and Q outputs of flip-flops **108** and **110**, respectively, at the termination of the Q output of flip-flop **110** and at the start of the $\overline{Q}$ output of flip-flop **108**, providing a pulse at the output of NAND **116** near the termination of a DPL pulse, which pulse is therefore spaced from the pulse provided at the output of NAND gate **114** in response to a DPL pulse.

Since the outputs of NAND gates **114** and **116** are high until driven low near the start and finish of a DPL pulse, respectively, the output of NAND gate **134** is driven high twice for each DPL pulse, thus providing pulses to the count-up input of counter **100** at twice the

DPL rate, while pulses are provided at the same rate as the DPL pulses at output terminal NLC.

When the car reaches maximum velocity, signal $\overline{MXVM}$ goes low, blocking gate **116**, and the count-up input of counter **100** then receives pulses at the same rate as the distance pulses are received. When deceleration of the car is initiated, signal ACC goes low, blocking gate **118** from sending any further pulses to counter **100**, enabling the count of counter **70** to coincide with the actual car position as the car comes to a stop at a landing.

When the car is travelling downwardly, the direction flip-flop **112** blocks NAND gate **118** and enables NAND gate **120**, directing the output of NAND gate **134** to the count-down input of counter **100** via NAND gate **124**, as long as $\overline{MIN}$ is high.

The min/max decoder **88** forces deceleration of the car when the continuous advanced car position, indicated by the count of counter **70**, reaches either terminal, and it also blocks counter **70** from registering any further distance pulses when this situation occurs. The $\overline{MAX}$ output of decoder **88** is responsive to a plurality of diodes **138** connected to the output of counter **70** which are at the logic ONE level when the continuous advanced car position is equal to the binary word describing the position of the upper terminal floor. When these diodes all have their cathode electrode connected to a logical ONE, the input side of an inverter **140**, which is connected to the anode electrodes of the diodes, goes high, and the output of inverter **140** is driven low to provide a true $\overline{MAX}$ signal.

The $\overline{MIN}$ output of decoder **88** is responsive to a plurality of serially connected inverter/diode combinations, referred to generally with reference numeral **142**, which are connected to the outputs of counter **70**. When the outputs of counter **70** are all at the logic ZERO level, indicating that the continuous advanced car position is the lowest floor, the input side of an inverter **144**, which is connected to the anode electrodes of the diodes, is high, due to the inverters, and the output of inverter **144** is at the logic ZERO level.

The $\overline{MIN}$ and $\overline{MAX}$ outputs are used to terminate the counting of counter **70**, as hereinbefore described, and they are also used to initiate terminal slowdown via the circuit which includes input terminals BOTTOM, TOP, UP and DOWN, inverters **146**, **148** and **150**, NAND gates **152**, **154**, **156**, **158** and **160** and output terminal $\overline{TDS}$.

Input terminals BOTTOM and TOP are connected to limit switches in the hatchway, which cause the BOTTOM and TOP input terminals to be at a logical ONE level when the car is within **18** inches of the bottom and top floors, respectively. Thus, NAND gates **152** and **154** are enabled as long as the car is not within **18** inches of either terminal. NAND gates **156** and **158** are responsive to car direction, with NAND gate **156** being enabled when the car is set to travel downwardly, and NAND gate **158** being enabled when the car is set to travel upwardly.

In the operation of the min/max decoder, assume that the car is travelling upwardly. Signals $\overline{MIN}$ and $\overline{MAX}$ are both at the logic ONE level, as are the inverted BOTTOM and TOP signals. Thus, the outputs of NAND gates **152** and **154** are at the logic ZERO level, the outputs of NAND gates **156** and **158** are both at the logic ONE level, the output of NAND gate **160** is at the logic ZERO level, and the output of inverter **150** is a logic ONE, providing a high or false $\overline{TDS}$ signal. When the output of counter **70** reaches the binary word which describes the upper floor, signal $\overline{MAX}$ goes low, the output of NAND gate **154** goes high, the output of NAND gate **158** goes low, the output of NAND gate **160** goes high, and the output of inverter **150** goes low, the true level for the terminal slowdown signal $\overline{TDS}$. Signal $\overline{TDS}$ is applied to the synchronizer **94**, as will be hereinafter explained.

In a similar manner, when the car is travelling downwardly and signal $\overline{MIN}$ goes low, indicating that the continuous advanced car position has arrived at the lower terminal, the output of NAND gate **152** goes high, the output of NAND gate **156** goes low, the output of NAND gate **160** goes high, and the output of inverter **150** goes low.

Memory **74**, which may be a read-only memory such as Intersil No. IM 5600, is arranged, at the time of the installation of the elevator, to output a binary number which is the exact binary address of the floor relative to the structure, using the standard increment, represented by the binary number which is responsive to the floor of the discrete advanced car position, as determined by counter **72**.

Comparator **76** includes a plurality of bit-by-bit comparators **162**, **164**, **166** and **168**, having an input for the "A" word connected to outputs of counters **100**, **102**, **104** and **106**, and an input for the "B" word connected to the output of memory **74**. Memory **74** is of the type which has three outputs. An $A < B$ output which is at the logic ONE level when the word A is less than the word B, an $A = B$ output which is at the logic ONE level when the words are equal, and an $A > B$ output which is a logical ONE when the word A is larger than the word B. The $A < B$ output is connected to the D input of a type D positive edge triggered flip-flop **170**, the $A = B$ output is connected to the D input of flip-flop **174**, and the $A > B$ output is connected to the D input of a flip-flop **170**. The clock inputs of these flip-flops is connected to receive clock signals $\overline{K32}$ via an inverter **176**. The Q outputs of flip-flops **170** and **172** are connected to indexer **78**, while the Q output of flip-flop **174** is connected to output terminal $\overline{EQ2}$ via inverter **178**. Output terminal $\overline{EQ2}$ provides the equality signal $\overline{EQ2}$ when the continuous advanced car position arrives at the floor level of the discrete advanced car position.

In the operation of comparator **76**, it will first be assumed that the car is travelling upwardly. Word A will thus be less than word B, and the $A < B$ output will be at the logic ONE level, while the other outputs are at the logic ZERO level. Flip-flop **172** thus outputs a logical ONE signal while the outputs of flip-flops **170** and **174** are low. When input words A and B are equal, indicating the car must now initiate slowdown if it is to stop at the floor of the discrete advanced car position according to a predetermined deceleration schedule, the $A = B$ output goes to logical ONE, flip-flop **174** outputs a logical ONE, and signal $\overline{EQ2}$ goes low or true. If deceleration is initiated, signal ACC goes low and the counter **70** remains at the count of the discrete advanced car position, and word A will continue to equal word B until the car stops, and then starts to move away from the floor. If deceleration is not initiated when the $A = B$ output is high, the first distance pulse after equality will cause the $A>B$ output of the comparator to go high, and flip-flop **170** outputs a logical ONE.

The indexer 78 is responsive to the outputs of flip-flops 170 and 172, to index the discrete advanced car position to represent the next floor at which the car can stop. Indexer 78 includes NAND gates 182, 184, 186 and 188, inverters 190 and 192, it is responsive to input terminals UP, DOWN, ACC, and S100, and it is connected to output terminals $\overline{PU}$ and $\overline{PD}$ which are connected to counter 72, and to synchronizer 94. NAND gates 182 and 184 have inputs connected to the UP and DOWN input terminals, respectively, and each have inputs connected to input terminal ACC. Thus, when the car is travelling upwardly and the car is not decelerating, NAND gate 182 outputs a ZERO, which is inverted to enable NAND gate 186. NAND gate 184 outputs a logic ONE which is inverted to block NAND gate 188. In a similar manner, when the car is travelling downwardly, NAND gate 186 is blocked and NAND gate 188 is enabled. Thus, when the car is travelling upwardly, the A <B output of comparator 176 and its associated flip-flop 172 have no circuit affect, as NAND gate 188 is blocked. As soon as the A> B output goes to the logic ONE level, the output of flip-flop 170 goes high and the S100 strobe, which occurs only during scanning interval 00 of the scan counter 80, drives the output of NAND gate 186 low, which is the true level for signal $\overline{PU}$. When signal $\overline{PU}$ goes low, it advances counter 72 to indicate the next higher floor number, and the output of memory 74 changes to indicate the floor address of that floor, which number is again higher than the continuous advanced car position. The A < B output of comparator 76 thus goes high while its other outputs are low.

When the car is travelling downwardly, the A word responsive to the continuous advanced car position is larger than the B word responsive to the discrete advanced car position, and the A<B output of comparator 76 is high, which has no circuit affect since gate 186 is blocked. When the continuous advanced car position reaches the discrete advanced car position, the A = B output goes high and signal $\overline{EQ2}$ goes low. If deceleration is initiated the counter 70 is blocked by signal ACC going low. If deceleration is not initiated, counter 70 continues to count down, and as soon as the A<B output goes high, flip-flop 172 goes high and the output of NAND gate 188 will go low upon receiving the S100 strobe during scanning slot 00, to index the counter 72 with a true or low $\overline{PD}$ signal to represent the next lower floor. When the counter 72 is indexed, the comparator 76 will output a logical ONE at the A>B output, and the above sequence is repeated.

FIGURE 6

FIG. 6 is a schematic diagram of a reversible counter, a top/bottom reset, and a comparator, which may be used for counter 72, top/bottom reset 86, and comparator 82 shown in FIG. 3. Like reference numerals in FIGS. 6 and 3 indicate like components.

Counter 72 includes the necessary number of cascaded synchronous 4-bit binary counters required to represent the number of the floors in the associated structure, with two counters 194 and 196 being illustrated. The count-up input of counter 194 is connected to input terminal $\overline{PU}$, which receives index pulses from indexer 78, and the count-down input of counter 194 is connected to input terminal $\overline{PD}$, which receives index pulses from indexer 78. Th output of counter 72 is connected to memory 74, hereinbefore described, via output terminals AVPO, AVP1, AVP2, AVP3 and AVP4, and to one input of comparator 82. Comparator 82 is a bit-by-bit comparator, which has its other input connected to the scan counter 80. Comparator 82 has three outputs, an A<B output which is high when the output of scan counter 80 is less than the binary output word of counter 72, an A = B output which is high when the scan counter is at the time slot of the discrete advanced car position, and an A > B output which is high when th output word of the scan counter 80 exceeds the output word of counter 72.

The outputs of comparator 82 are used to develop the serial advanced car position signal EQ1Z, the scanning below the discrete advanced car position signal SBC, and the scanning above the discrete advanced car position signal SAC. These signals are developed by a circuit which includes an input terminal $\overline{STC}$, which receives a strobe signal $\overline{STC}$ which occurs during each scanning slot of scan counter 80, as represented in FIG. 4, an input terminal $\overline{PCR}$, which receives a $\overline{PCR}$ signal which is low or true each time the indexer 78 provides an index signal $\overline{PU}$ or $\overline{PD}$, as will be explained when the synchronizer 94 is described, NAND gates 198, 200 and 202, inverters 204, 206 and 208, and output terminals SBC, EQ1Z and SAC.

In the operation of comparator 82, when the scan counter 80 is scanning (counting) below the floor of the discrete advanced car position, the A<B output is high, which is strobed by signal $\overline{STC}$ during each scanning slot to provide a low output from NAND gate 198, which is inverted by inverter 204 to provide a high or true SBC signal.

When the scan counter 80 reaches the count which represents the floor of the advanced car position, the A = B output goes high, and the output of NAND gate 200 goes low when $\overline{STC}$ goes high, as long as the counter 72 is enabled by a high $\overline{PCR}$ signal (counter 72 not being indexed). The low output of NAND gate 200 is inverted by inverter 206 to provide a true EQ1Z serial advanced car position signal in the proper scanning slot of scan counter 80. When the scan counter 80 passes the count of the discrete advanced car position, the A > B output goes high and NAND gate 202 outputs a logical ZERO when strobe $\overline{STC}$ goes high during each scanning slot. The low output of NAND gate 202 is inverted by inverter 208 to provide a high or true SAC signal, which indicates scanning above the discrete advanced car position.

The top/bottom reset 86 resets both of the reversible counters 70 and 72 with the proper count at both the top and bottom floors, to start the elevator car from either terminal with the proper count, prior to a run which is initiated from these floors.

The top/bottom reset 86 includes NAND gates 210, 212, 214, 216, 218 and 220, a read only memory 222, inverters 224, 226, 228, 230, 232 and 234, input terminals TOP, BOTTOM, MAIN, DL2, Z02 and S100, and an output terminal $\overline{LOAD\ N}$.

NAND gate 210 has its inputs connected to input terminals $\overline{DL2}$ and Z02, with signal $\overline{DL2}$ being a signal developed by the speed pattern generator 48 when the car is going to stop at a landing. When $\overline{DL2}$ is at the logic ZERO level, it corresponds to "run," and when $\overline{DL2}$ is at the logic ONE level it corresponds to "land." Signal ZO2 is developed by a limit switch in the hatchway, with signal ZO2 being a logic ONE when the car is within 2 inches of the landing level. The signals TOP,

BOTTOM and MAIN are developed by switches in the hatchway, and are at the logic ONE level when the car is within 18 inches of the top, bottom and main floors, respectively. If the bottom floor is the main floor, the MAIN input terminal and NAND gate 214 may be eliminated. The S100 input terminal receives clock pulse S100 generated during scan slot 00 of the scan counter 80. The output of NAND gate 218 is connected to counter 72, and also to the $\overline{\text{LOAD N}}$ output terminal, which terminal is connected to counter 70 shown in FIG. 5.

Read-only memory 22 is set to output the floor number in binary of the specific floor addressing the memory. For example, when the output of NAND gate 212 goes low, memory 222 will output the floor number of the bottom floor, which is 00001. When the output of NAND gate 216 goes low, memory 222 will output the number of the top floor, which in our 30 floor example, would be 11110.

When the elevator car is at a floor other than a floor at which the counters are reset, the inputs to NAND gate 220 will all be high and its output will be low, blocking NAND gate 218. When the car arrives at one of the reset floors, NAND gate 210 enables the NAND gates 212, 214, and 216, and depending upon which reset floor the car is located at, one of these NAND gates addresses the read-only memory 222 and enables NAND gate 220. Clock signal S100 in scanning slot 00 of the scan counter drives the output of NAND gate 218 low, which loads the proper floor number into counter 72. Counter 72 is thus forced to the correct output number, and this output addresses memory 74 of FIG. 5. Memory 74 provides the exact location of the floor relative to the structure, in terms of the standard increment. In addition to the output of memory 74 being used by comparator 76, the output of memory 74 is also connected to the load input of counter 70, as illustrated in FIG. 5. The $\overline{\text{LOAD N}}$ signal from the top/bottom reset 86 is connected to the $\overline{\text{LOAD N}}$ input of terminal 70, and when the $\overline{\text{LOAD N}}$ signal goes low, the output of memory 74 is loaded into counter 70, to always start counter 70 with the correct count at each reset floor. This resetting of counters and memories at the selected reset floors occurs automatically during the operation of the elevator car. If power is lost during the operation of the elevator, causing the counters to lose their count, normal system operation is achieved, following power return, by running the car manually to one of the reset floors.

FIG. 7

FIG. 7 is a timing diagram for a thirty floor building, illustrating the various scanning slots or intervals of the scan counter 80, and the relationship of selected signals thereto, such as car calls and up and down corridor calls. Since the building of the example has thirty floors, the scan counter 80 may be a 5-bit counter, which provides 32 intervals or slots for each scan. Since it is assumed that each interval is 2 milliseconds, the scan time for each scanning period is 64 milliseconds. If the building has more than thirty-two floors, a 6-bit counter would be used to handle structures with 33 through 64 floors, and a 7-bit scan counter would handle structures with 65 through 128 floors. The other counters and memories would be selected accordingly.

The car calls, referred to as signals 3Z are serialized and synchronized with the scan counter 80 to appear in the time slot for the floor which they request the car to travel to. For example, each of the car pushbuttons may be connected by a wire to a gate, with the gates being sequentially enabled by the output of the scan counter, such that scanning slot 00 would enable the gate associated with the first floor, etc. The outputs of the gates would be collected to present the car call information in serial form. For purposes of example, it will be assumed that the car is travelling downwardly, the discrete advanced car position, represented by signal EQ1Z, is at the 20th floor, and the car has car calls (signal 3Z) for the 19th, 15th, 11th, 10th and fourth floors.

The up and down corridor calls, represented by signals 1Z and 2Z, respectively, may also be gated by the scan counter 80 to serialize and synchronize the calls into the scanning slots associated with the floor number from which they are registered. As illustrated in FIG. 7, up corridor calls 1Z are separately serialized, with calls for up service being registered from the 10th and 13th floors. Down corridor calls 2Z are registered for the seventh and 22th floors.

Signals MTOO and MTO1 shown in FIG. 7 are provided by read-only memory 90 shown in FIG. 3, and are used as enabling signals to insure that the scanning slots of the scan counter not used to represent floors are disregarded, as well as disregarding the scanning slots for the uppermost and lowermost floors when considering up and down corridor calls, respectively. Thus, memory track MTOO, which is used to enable up corridor calls 1Z, is a logic ONE for scanning slots 00 through 28, representing floors 1 through 29, and a logic ZERO for scanning slots 29, 30 and 31. Memory track MTO1 is used to enable down corridor calls 2Z, and is thus a logic ONE for scanning slots 01 through 29, representing floors 2 through 30, and a logic ZERO for scanning slots 00, 30 and 31.

Signal CEN is a call enable signal, for car calls, provided by a read-only memory track, such as from read-only memory 90. Signal CEN may simply be used to insure that the scanning slots not used to represent floors are disregarded by the car call circuits; or, as illustrated by the alternate CEN signal in FIG. 7, it may be used to prevent the car from going to specific floors in response to a car call, such as floors 15, 20 and 30.

The remaining signals shown in FIG. 7 are clock signals developed in FIG. 4, and hereinbefore described.

In the timing diagram of FIG. 7, the car, which is travelling downwardly, would stop at the floors for which car calls 3Z are registered, and it would stop at the seventh floor to serve the registered down call 2Z for that floor. When the car has served its last call in the down direction, it will proceed to the lowest registered up corridor call, and then handle all of the registered up calls. Upon handling the last call for service in the up direction, the car will proceed to the highest registered down call. The circuitry for operating the car in this manner will be hereinafter described.

FIG. 8

FIG. 8 is a schematic diagram of a call selector which may be used for the call selector 92 shown in FIG. 3. The primary function of the call selector 92 is to detect coincidence between the floor of the discrete advanced car position signal EQ1Z and a request for service for that floor, and to provide a request to stop signal $\overline{\text{EIX}}$ when such coincidence is detected. Auxiliary functions

of the call selector **92** are the resetting of corridor calls, the enabling of the hall lanterns, providing the door open request, and detecting a call at the floor at the start of each run.

More specifically, call selector **92** includes input terminals $\overline{1Z}$, $\overline{2Z}$ and $\overline{3Z}$ for receiving the serial up and down corridor calls and car calls, respectively, input terminals TM00, MT01 and $\overline{CEN}$ for receiving the memory track signals MT00, MT01 and $\overline{CEN}$, respectively, input terminals UCE and DCE for receiving up and down call enable signals, respectively, for logic circuit **96**, input terminals DCL, DO and $\overline{DORR}$ for receiving door closed, door open enable, and door reset signals, respectively, input terminal UPTR which receives a signal from logic circuit **96** which indicates direction of car travel, input terminal $\overline{FSC}$ which receives a signal from logic circuit **96** when the first scan is initiated at the start of a run, and input terminal S4 for receiving timing pulses during each scanning slot.

The serial advanced car position signal EQ1Z appears at input terminal EQ1Z in the scanning slot allocated to its specific floor position, and it is strobed by clock signal S4 through NAND gate **240**, inverted by inverter **242**, to appear at the logic ONE level at the input of each of the NAND gates **244, 246** and **248.**

Serial up corridor calls which appear at input terminal $\overline{1Z}$ are inverted by inverter **250**, screened by memory track signal MT00 through NAND gate **252**, inverted to the logic ONE level by inverter **254**, applied to an input of each of the NAND gates **244, 256**, and also via inverter **258** to output terminal $\overline{UCY}$, which provides serial up corridor calls as screened by memory track $\overline{MT00}$.

Serial down corridor calls which appear at input terminal $\overline{2Z}$ are inverted by inverter **260**, screened by memory track signal MT01 through NAND gate **262**, inverted to the logic ONE level by inverter **264**, applied to an input of each of the NAND gates **246** and **266**, and also via inverter **268** to output terminal $\overline{DCY}$, which provides serial down corridor calls, as screened by memory track MT01.

Serial car calls which appear at input terminal $\overline{3Z}$ are inverted by inverter **270** and applied to an input terminal of each of the NAND gates **272** and **248.** The car call enable signal applied to input terminal $\overline{CEN}$ is inverted by inverter **274** and applied to another input on each of the NAND gates **272** and **248.** Car calls for floors for which the car is enabled appear at the output of NAND gate **272** and at the output terminal $\overline{CCY}$.

When the up call enable signal at input terminal UCE, which is received from logic circuit **96**, is at the logic ONE level, NAND gates **244, 256** and **276** are enabled. At this time, the down call enable signal at input terminal DCE will be at the logic ZERO level, blocking NAND gates **246, 266** and **278.** When the down call enable signal at input terminal DCE, which is also received from logic circuit **96**, is at the logic ONE level, signal UCE will be at the logic ZERO level, NAND gates **246, 266** and **278** will be enabled, and NAND gates **244, 256** and **276** will be blocked.

The outputs of NAND gates **244, 246** and **248** are normally high when no coincidence of the discrete advanced car position and a call for service for that floor is detected, and since these outputs are all connected to an input of NAND gate **280**, the NAND gate **280** outputs a logic ZERO in the absence of coincidence, which is inverted to the logic ONE level by inverter **282.** Thus, the signal at output terminal $\overline{EIX}$, which is the request to stop signal, is false or at the ONE logic level in the absence of coincidence.

When a corridor or car call is registered for the floor of the discrete advanced car position, signal $\overline{EIX}$ goes true or low in the following manner. If the coincidence detected is an up corridor call, and the car is enabled for up calls, the input signals to NAND gate **244**, i.e., UCE, strobed EQ1Z, and UCX, with the latter indicating screened up corridor calls, will all be at the logic ONE level simultaneously during the scan slot of the floor of the discrete advanced car position, driving the output of NAND gate **244** low, the output of NAND gate **280** high, and the output terminal $\overline{EIX}$ low via inverter **282.**

If the coincidence detected is a down corridor call, and the car is enabled for down calls, the input signals for NAND gate **246**, i.e., DCE, strobed EQ1Z and DCX, the latter indicating screened down corridor calls, will all be at the logic ONE level simultaneously during the scan slot of the floor of the discrete advanced car position, driving the output of NAND gate **246** low, the output of NAND gate **280** high, and the output terminal $\overline{EIX}$ low.

If the coincidence detected is a car call, and the car is enabled for the floor of the discrete advanced car position signal, the input signals CEN, strobed EQ1Z, and 3Z for NAND gate **248** will all be at the logic ONE level simultaneously during the scan slot of the floor of the discrete advanced car position, driving the output of NAND gate **248** low, the output of NAND gate **280** high, and output terminal $\overline{EIX}$ low.

When the elevator car starts a run, the logic circuit **96** provides a true or low $\overline{FSC}$ signal during the first complete scan of scan counter **80**, starting at timing signal **S200** and ending at timing signal **S100**, which is applied to input terminal $\overline{FSC}$ of call selector **92.** This true or low $\overline{FSC}$ signal is inverted by inverter **284**, applying a logic ONE to an input of NAND gate **286.** Since the discrete advanced car position and the actual car position are the same at the start of a run, signal EQ1Z will appear in the time slot for the floor where the car is located. If there is an up corridor call at the floor where the car is located, a true corridor signal UCX will be applied to an input of AND gate **256.** If the car is enabled for up calls, signal UCE will be true, and if the car is set for up travel, signal UPTR will be true, driving the output of NAND gate **256** low.

In a similar manner, if there is a down corridor call at the floor where the car is located, a true down corridor signal DCX will be applied to an input of NAND gate **266.** If the car is enabled for down calls, signal DCE will be true, and if the car is set for down travel signal $\overline{UPTR}$ will be false or high, driving the output of NAND gate **256** low.

The outputs of NAND gates **256** and **266** are connected to inputs of NAND gate **288.** If there is no call at the floor, these outputs will be high and the output of NAND gate **288** will be low. If one of the outputs of the NAND gates **256** or **266** goes low, indicating a call at the floor, the output of NAND gate **288** will go high. When the output of NAND gate **288** goes high during the first scan, the output of NAND gate **286** goes low, which is inverted by inverter **290** and applied to an input of a NAND gate **292.** The other input of NAND gate **292** is connected to receive clock signal **S4**, which signal strobes the call at the floor through NAND gate

292 where it is applied to an input terminal $\overline{CFLY}$, which indicates a call at the floor. The output of NAND gate 292 is also applied to one of the set inputs of a first door flip-flop 294. Flip-flop 294 may be of the cross-coupled NAND gate type, having NAND gates 295 and 297.

Set inputs of the first door flip-flop 294, i.e., the inputs of NAND gate 295, are also connected to be responsive to the outputs of NAND gates 244, 246 and 248. Thus, a call at the floor, or a request to stop for a car call or a corridor call, will set the first door flip-flop 294, providing a logic ONE at the output of NAND gate 295, and a logic ONE at the input of NAND gate 296. The other input of NAND gate 296 is connected to input terminal DO, which is at the logic ONE level when the door open request is enabled. Thus, when NAND gate 296 is enabled by a high DO signal and flip-flop 294 is set, a second door flip-flop 298 will be set. Flip-flop 298 may be of the cross-coupled NAND gate type, having NAND gates 299 and 301. NAND gate 299 provides a logic ONE at its output, which is inverted by inverter 300 and applied to output terminal $\overline{DOR}$. A low $\overline{DOR}$ signal is a request to open the doors of the car, which request is directed to door operator circuits 52 shown in FIG. 1. The door operator circuits may be conventional. When the non-interference or normal door open time times out, the door operator circuits 52 provide a low $\overline{DORR}$ signal at input terminal $\overline{DORR}$, which resets the second door flip-flop 298. When the doors actually close, a low DCL signal, applied to input terminal DCL, initiated by a limit switch associated with the car and hatch doors, resets the first door flip-flop 294.

It will be noted that the second door flip-flop 298 may be set, initiating a door open request, by a low terminal slowdown signal $\overline{TSD}$, applied to input terminal $\overline{TSD}$, and connected to one of the set inputs of flip-flop 298. Thus, terminal slowdown, initiated by the speed pattern generator 48, as will be hereinafter described, will also initiate the opening of the car and hatch doors.

The output of inverter 300 is inverted by inverter 302 and connected to an input of each of the NAND gates 276 and 278, which also have inputs connected to receive up call enable and down call enable signals UCE and DCE, respectively. Thus, when the car is enabled for up calls and a door open request is initiated, the output of NAND gate 276 goes low, and this signal is inverted by inverter 304 and applied to an input of NAND gate 306. NAND gate 306 also has an input connected to receive the serial advanced car position signal EQ1Z. When the serial advanced car position signal EQ1Z goes high, the output of NAND gate 306 goes low, and this output is connected to output terminal $\overline{HLU}$, which enables the up hall lantern for the floor of the serial advanced car position, and to output terminal $\overline{UPRZ}$, which resets the up corridor pushbutton for the floor of the serial advanced car position. The hall lantern control 54 and corridor call control 46 shown in FIG. 1, which receives these enabling and reset signals, may be conventional.

In a similar manner, when the car is enabled for down calls, and a door open request is initiated, the output of NAND gate 278 goes low, and this signal is inverted by inverter 308 and applied to an input of NAND gate 310. The serial advanced car position signal EQ1Z is connected to another input of NAND gate 310, and when it is received, the output of NAND gate 310 goes low, providing a low down hall lantern enable signal $\overline{HLD}$, and a low or true down corridor reset signal $\overline{DNRZ}$.

FIG. 9

FIG. 9 is a schematic diagram of a logic circuit which may be used for the logic circuit 96 shown in FIG. 3. The function of the logic circuit 96 is to receive the serial calls $\overline{UCY}$, $\overline{DCY}$ and $\overline{CCY}$ for the call selector 92, determine where a call is relative to the serial advanced car position EQ1Z, determine in which direction the car should travel and provide travel direction signal UPTR in response thereto, enable the car for up or down calls with enable signals UCE and DCE, respectively, request starting of the car with a true $\overline{ACCX}$ signal when it is idle, in response to a call for service, provide the first scan signal $\overline{FSC}$ for the call selector 92, provide a high or true EI signal when there is a call at the floor of the serial advanced car position, provide a true or low $\overline{ACCX}$ signal when a deceleration request is made by the synchronizer 94, and enable the hall lantern control with a true $\overline{HLX}$ signal.

More specifically, car and corridor calls are connected to selected inputs of NAND gates 320, 322, and 324, with the serial car calls, which are received at input terminal $\overline{CCY}$ being connected to an input terminal on all three of these NAND gates, the serial up corridor calls, which are received at input terminal $\overline{UCY}$, are connected to input terminals of NAND gates 322 and 324, and the serial down corridor calls, applied to input terminal $\overline{DCY}$, are connected to input terminals of NAND gates 320 and 324. In the absence of any calls, the outputs of all three of these NAND gates will be low. A car call $\overline{CCY}$ will drive the outputs of all three of these NAND gates high. An up corridor call $\overline{UCY}$ will drive the outputs of NAND gates 322 and 324 high. A down call $\overline{DCY}$ will drive the outputs of NAND gates 320 and 324 high.

The outputs of NAND gates 320, 322, and 324 are connected to selected inputs of NAND gates 326, 328, 330 and 332, with the output of NAND gate 320 being connected to an input of NAND gate 330, the output of NAND gate 322 connected to an input of NAND gate 328, and the output of NAND gate 324 connected to inputs of NAND gates 326 and 332.

NAND gate 326 also has an input connected to input terminal SAC, which receives a high or true SAC signal from comparator 82 in FIG. 6 when the scan counter 80 is scanning above the floor position of the serial advanced car position.

NAND gate 328 also has inputs connected to input terminal S4, which receives clock signals during each scanning slot, as shown in FIG. 7, to input terminal EQ1Z from comparator 82 which provides the serial advanced car position in the appropriate scanning slot, and to the output of a NAND gate 374 via inverter 323. The output of inverter 323 is high when a request is made to accelerate the car, as will be hereinafter explained.

NAND gate 330 also has inputs connected to the output of inverter 323, to input terminal EQ1Z, and to input terminal S4.

NAND gate 332 also has an input connected to input terminal SBC, which is true when comparator 82 indicates the scan counter 80 is scanning below the floor of the serial advanced car position signal EQ1Z.

The outputs of NAND gates **326, 328, 330** and **332** are connected to selected inputs of a "call above" flip-flop **333**, and a "call below" flip-flop **335**. The call above flip-flop **333** includes two cross-coupled NAND gates **334** and **336**, with inputs of NAND gate **334** being connected to outputs of NAND gates **326** and **328**. An input of NAND gate **336** is connected to input terminal **S300** via inverter **342**, which resets the call above flip-flop **330** during scanning slot **00** of the scan counter **80**.

The call below flip-flop **335** includes two cross-coupled NAND gates **338** and **340**, with inputs of NAND gate **338** being connected to outputs of NAND gates **330** and **332**. An input of NAND gate **340** is connected to input terminal **S300** via inverter **342**, to also reset the call below flip-flop **335** during scanning slot **00**.

The call above flip-flop **333** is set, triggering the output of NAND gate **334**, referred to as signal CA, to a logic ONE level, by the output of NAND gate **326** going low, which indicates the scan counter **80** is scanning above the floor of the serial advanced car position, and while scanning there an up or down corridor call or car call was detected. When the output signal CA of NAND gate **334** goes high, the output of NAND gate **336**, referred to as signal $\overline{CA}$, goes low. The call above flip-flop may also be set by the output of NAND gate **328** going low, which indicates that there is a request to accelerate, and a car or up corridor call at the floor of the car (the floors of the serial advanced car position and the actual car position are the same). When the call above flip-flop is set during the scan cycle of scan counter **80**, it is reset by signal $\overline{S300}$ during scanning slot **00**.

The call below flip-flop **335** is set, triggering the output of NAND gate **338**, referred to as signal CB, to a logic ONE level, and the output of NAND gate **340**, referred to as $\overline{CB}$, to a logic ZERO level, by the output of NAND gate **332** going low. This indicates that the scan counter **80** is scanning below the floor position of the serial advanced car position, and while scanning there an up or down corridor call, or car call, was detected. The call below flip-flop **335** may also be set by the output of NAND gate **330** going low, indicating that there is a request to accelerate the car, and that there is a down corridor or car call at the floor where the car is located.

The CA and $\overline{CA}$ outputs of the call above flip-flop **333** are connected to inputs of NAND gates **344** and **346**, respectively, and the $\overline{CB}$ and CB outputs of the call below flip-flop **335** are connected to inputs of NAND gates **334** and **346**, respectively. Inputs of NAND gates **344** and **346** are also connected to input terminal **S200**, which provides a clock pulse during scanning slot **00**, and also to input terminal $\overline{DOR}$, which is high when there is no request to open the car door by the call selector **92**. Thus, when the call above flip-flop **333** is set, signal CA is at the ONE logic level, the call below flip-flop **335** is not set, signal $\overline{CB}$ is at the ONE logic level, and there is no request to open the car door, signal $\overline{DOR}$ is at the ONE logic level, and the output of NAND gate **344** will go low when the clock signal **S200** is received during scanning slot **00**.

In a similar manner, when the call below flip-flop **335** is set, signal CB will be at the ONE logic level, the call above flip-flop **333** is not set, signal $\overline{CA}$ will be at the ONE logic level, and there is no request to open the car door, signal $\overline{DOR}$ will be at the ONE logic level, and the output of NAND gate **346** will go low when the clock signal **S200** is received.

If there are calls above and below the car, neither of the NAND gates **344** and **346** will switch to the low output level, as $\overline{CB}$ and $\overline{CA}$ will both be ZERO.

The outputs of NAND gates **344** and **346** are connected to selected inputs of a travel direction flip-flop **350**. Travel direction flip-flop **350** includes cross-coupled NAND gates **352** and **354**, with NAND gate **352** having an input connected to the output of NAND gate **344**, and NAND gate **354** having an input connected to the output of NAND gate **346**.

NAND gate **352** also has inputs connected to input terminals $\overline{SUT}$ and BOTTOM. Input terminal $\overline{SUT}$, for example, may be responsive to an attendant pushbutton which when depressed to indicate that up travel is desired, will provide a signal $\overline{SUT}$ at the logic ZERO level. Input terminal BOTTOM is responsive to a limit switch in the hatchway which provides a signal at the logic ONE level when the car is within 18 inches of the bottom landing. An inverter **356** inverts the BOTTOM signal before it is applied to NAND gate **352**.

NAND GATE **354** also has inputs connected to input terminals $\overline{SDT}$ and TOP. Input terminal $\overline{SDT}$, for example, may be responsive to an attendant pushbutton, which is depressed when down travel is desired, to provide a signal $\overline{SDT}$ at the logic ZERO level. Input terminal TOP is responsive to a limit switch in the hatchway which provides a signal at the logic ONE level when the car is within **18** inches of the top landing. An inverter **358** inverts the signal TOP before it is applied to NAND gate **354**.

The output of NAND gate **352** of the travel direction flip-flop **350**, which is termed signal **81U**, is connected to one input of a two input NAND gate **360**. The remaining input of NAND gate **360** is connected to the output of inverter **358**. The output of NAND gate **360**, termed $\overline{UPTR}$, is inverted by an inverter **362** and applied to an output terminal UPTR. Output terminal UPTR, which is connected to the speed pattern generator **48**, is high when up travel is requested, and low when down travel is requested.

In the operation of the travel direction circuits of FIG. **9**, it will be noted that the travel direction flip-flop **350** will be set to provide a true **81U** signal by either the attendant pushbutton signal $\overline{SUT}$, or when the car is within 18 inches of the bottom landing, or when the output of NAND gate **344** goes low. Further, the travel direction flip-flop **350** will be set to provide a low **81U** signal by the attendant pushbutton $\overline{SDT}$, or when the car is within **18** inches of the top landing, or when the output of NAND gate **346** goes low.

If there are calls below and above the car location, or a call at the floor during first scan, neither of the NAND gates **344** or **346** can go low, as $\overline{CA}$ and $\overline{CB}$ will both be at the logic ZERO level. Thus, the travel direction flip-flop **350** will not be triggered, and the car will maintain the travel direction it is presently taking. If we assume the car is travelling upwardly, it will continue in the upward direction until (a) there are no further calls for service ahead of its travel direction, or (b) it reaches the top landing. When the car reaches a top landing, the input terminal TOP will go high, flip-flop **350** will trigger, and the output of NAND gate **360** will go high. The output of NAND gate **360** will go high even though flip-flop **350** does not trigger for some rea-

son, due to an input of NAND gate **360** being connected to input terminal TOP via inverter **358.** If the car is not at the top landing and there are no calls ahead of its upward travel, but there are calls below, the output of NAND gate **346** will go low, triggering flip-flop **350** to provide a low **81U** signal, and driving the output of NAND gate **360** high.

If we assume the car is travelling downwardly, it will continue in the downward direction until (a) there are no further calls for service ahead of its travel direction, or (b) it reaches the bottom landing. When the car reaches the bottom landing, input terminal BOTTOM will go high, triggering flip-flop **350** to provide a true **81U** output signal, and the output of NAND gate **360** will be driven low. If there are no calls ahead of its downward travel direction and it is not at the bottom landing, but there are calls above, the output of NAND gate **344** will go low, triggering flip-flop **350** to provide a true **81U** signal, which drives the output of NAND gate **350** low.

The up and down corridor call enabling circuits of logic circuit **96** include NAND gates **364** and **366,** and inverters **368** and **370,** which circuits are responsive to an input terminal $\overline{\text{BYPS}}$, which is responsive to car weight. When the car weight exceeds a predetermined amount, a true or low signal is applied to input terminal $\overline{\text{BYPS}}$.

NAND gates **364** and **366** each have an input connected to input terminal $\overline{\text{BYPS}}$. NAND gate **364** also has an input connected to the output terminal UPTR, while NAND gate **366** also has an input terminal connected to the output $\overline{\text{UPTR}}$ of NAND gate **360.** If the car weight is below the predetermined magnitude, and the signal UPTR is high, the output of NAND gate **364** will go low, which is inverted by inverter **368** and applied to output terminal UCE as a high or true signal, indicating the car is enabled for up corridor calls. In a similar manner, if the car weight is below the predetermined magnitude and the signal $\overline{\text{UPTR}}$ is low or true, the output of NAND gate **366** will go low, which is inverted by inverter **370** and applied to output terminal DCE as a high or true signal, indicating the car is enabled for down corridor calls.

If the car weight exceeds the predetermined magnitude, signal $\overline{\text{BYPS}}$ will go low, and both NAND gates **364** and **366** will be blocked, and output terminals UCE and DCE will both be at the ZERO logic level. As hereinbefore explained, output terminals UCE and DCE are connected to the call selector circuit **92** shown in detail in FIG. **8.**

When the elevator car is idle, a call in the system will initiate a true request to accelerate signal $\overline{\text{ACCX}}$, in the direction requested by the travel direction circuits just described. The circuits which generate the $\overline{\text{ACCX}}$ signal include flip-flops **380, 383** and **384,** NAND gates **374, 386, 388, 390, 391, 392** and **394,** and inverters **396, 398** and **400.**

Flip-flop **380** includes cross-coupled NAND gates **402** and **404** with inputs of NAND gate **402** being connected to the $\overline{\text{CA}}$ and $\overline{\text{CB}}$ outputs of the call above and call below flip-flops **333** and **335,** respectively. NAND gate **402** also has an input connected to the output of NAND gate **391.** NAND gate **391** has one input connected to input terminal EQ1Z, and another input connected to input terminal $\overline{\text{CEN}}$. Any call will set flip-flop **380** to provide a logic ONE at the output of NAND gate **402,** which output signal will be referred to as signal NCS. Also, since signal $\overline{\text{CEN}}$ is a logic ONE for a floor for which the car is not enabled, as described relative to call selector **92,** if the floor of the serial advanced car position indicated by signal EQ1Z and a floor for which the car is not enabled coincides, it appears that there is a call in the system and the flip-flop **380** will also be set. This prevents the car from accidentally stopping at a floor for which it is not enabled. The flip-flop **380** is reset during scanning slot **00** by clock signal $\overline{\text{S300}}$ which is connected to an input of NAND gate **404.**

The NCS output signal of NAND gate **402** is connected to inputs of NAND gates **386** and **392.** The output of NAND gate **404** is connected to an input of NAND gate **388.** When a call is detected in the system and flip-flop **380** is set, the true NCS signal is gated through NAND gate **386** during scan slot **00** by clock signal **S200,** which is connected to the other input of NAND gate **386.** The output of NAND gate **386** goes low when the S200 clock pulse is received, setting flip-flop **382** to provide a logic ONE signal NC at the output of NAND gate **406.** The reset input of flip-flop **382,** i.e., an input terminal of NAND gate **408,** is connected to the output of NAND gate **388.** The inputs of NAND gate **388** are connected to the output of NAND gate **404** of flip-flop **380,** to the input terminal S200 to receive the S200 clock pulse, and input terminal $\overline{\text{DOR}}$ which is high in the absence of a request to open the car door. Thus, flip-flop **382** is reset by NAND gate **388,** in the absence of a door open request $\overline{\text{DOR}}$, but not until flip-flop **380** has been reset by clock signal $\overline{\text{S300}}$.

The set output NC of flip-flop **382** is connected to an input of NAND gate **410** of flip-flop **384,** to an input of NAND gate **390,** and also to an input of a NAND gate **414** which is associated with the first scan function, as will be hereinafter explained. When the NC signal goes high at clock signal **S200** it enables flip-flop **384,** and it enables NAND gate **390.** NAND gate **390** also has an input connected to input terminal **S100,** to receive a clock pulse during scanning slot **00.** Clock signal **S100,** which appears a full scan period after flip-flop **382** is triggered at clock signal **S200,** triggers NAND gate **390** to provide a low output, triggering flip-flop **384** to drive the $\overline{\text{RUN}}$ output of NAND gate **410** low, and the RUN output of NAND gate **412** high. The $\overline{\text{RUN}}$ output of flip-flop **384** is connected to an input of NAND gate **414,** and the RUN output of flip-flop **384** is connected to an input of NAND gate **392.**

Flip-flop **380** is not reset at the clock pulse $\overline{\text{S300}}$, due to the call in the system so the NCS input to NAND gate **392** is high when the RUN output of flip-flop **384** goes high at **S100.** Inputs of NAND gate **392** are also connected to input terminal **S100** and IDLE. Therefore, when signals NCS, RUN and **S100** are all high when the car is idle, the output of NAND gate **392** goes low, forcing the output of NAND gate **394** high, which is inverted by inverter **398** to a low or true signal $\overline{\text{ACCX}}$. Signal $\overline{\text{ACCX}}$ which is a request to accelerate, is applied to the speed pattern generator **48.**

The output of NAND gate **394** is also connected to an input of NAND gate **374,** and the output of NAND gate **374** is also connected to an input of NAND gate **394,** providing a low $\overline{\text{ACCY}}$ output signal from NAND gate **374,** in the absence of a deceleration request signal $\overline{\text{DEC}}$. Thus, NAND gate **374** maintains the low $\overline{\text{ACCX}}$ signal, even though NAND gate **392** goes high

at the termination of clock pulse S100 until signal $\overline{DEC}$ goes low.

The first scan signal $\overline{FSC}$ is provided for a complete scan period at the start of a run, just prior to the setting of the run flip-flop **384.** When the NC output of flip-flop **382** goes high, enabling the run flip-flop **384,** $\overline{RUN}$ is high which signal is applied to an input terminal of NAND gate **414,** and since the high NC signal is also applied to an input of NAND gate **414,** the $\overline{FSC}$ signal immediately goes low and remains low from clock signal **S200,** which triggered flip-flop **382,** until clock signal **S100,** which triggers the run flip-flop **384,** driving RUN low, and $\overline{FSC}$ high. At clock signal **S200,** flip-flop **382** is reset by NAND gate **388,** and the resetting of flip-flop **382** resets flip-flop **384.**

Another function of logic circuit **96** is to provide an EI signal indicating a call at the floor of the serial advanced car position, when a request for stop signal $\overline{EIX}$ is generated by the call selector **92.** The circuit for generating signal EI includes input terminals $\overline{EIX}$, $\overline{CEN}$, **S4,** EQ1Z, **S200,** $\overline{PCR}$ and $\overline{DECS}$, flip-flops **420, 422** and **424,** inverters **400, 426, 428** and **430,** and NAND gate **432.** Flip-flop **420** includes cross-coupled NAND gates **434** and **436,** with an input of NAND gate **434** being connected to input terminal $\overline{EIX}$. An input terminal of NAND gate **434** is also connected to the output of NAND gate **432.** An input of NAND gate **436** is connected to input terminal **S200** via inverter **426.** An input of NAND gate **436** is also connected to flip-flop **424.**

Flip-flop **422** is of the JK type, which has its J input connected to the output of NAND gate **436** via inverter **436,** its clock input C connected to receive clock signals **S100,** its K input grounded, and its $\overline{Q}$ output connected to output terminal EI via inverter **430.**

Flip-flop **424** includes cross-coupled NAND gates **438** and **440,** with an input of NAND gate **424** connected to input terminal $\overline{PCR}$, an input of NAND gate **440** connected to input terminal $\overline{DECS}$, and the output terminal of NAND gate **438** connected to the CLEAR input of flip-flop **422** and an input of NAND gate **436** of flip-flop **420.**

NAND gate **432** has inputs connected to the RUN output of flip-flop **384,** to input terminal EQ1Z, to input terminal **S4,** and to input terminal $\overline{CEN}$ via inverter **400.** Thus, a true RUN signal which coincides with a high serial advanced car position signal EQ1Z, for a floor for which the car is enabled (CEN = 1) results in the output of NAND gate **432** going low at clock signal **S4.** The output of NAND gate **432** is connected to an input of NAND gate **434** of flip-flop **420.**

When input terminal $\overline{EIX}$ goes low, flip-flop **420** is set, providing a logic ONE at the output of inverter **428** and at the J input of flip-flop **422.** At clock signal **S100,** the $\overline{Q}$ output of flip-flop **422** will go low, and the inverter **430** inverts this low signal to a true EI signal. The EI signal is applied to synchronizer **94,** which will be hereinafter explained.

The reset flip-flop **424,** which includes cross-coupled NAND gates **438** and **440,** resets flip-flops **420** and **422** when a request is made to decelerate the car, i.e., signal $\overline{DECS}$ goes low. The reset flip-flop **424** is reset when the floor of the serial advanced car position is changed, indicated by signal $\overline{PCR}$ going low. Flip-flop **420** may also be reset by clock signal **S200.**

In addition to flip-flop **420** being set by a true $\overline{EIX}$ request for stop, the output of NAND gate **432** going low has the same effect, and this occurs, as hereinbefore stated, when a true or high RUN signal coincides with the serial advanced car position signal for a floor which the car is enabled.

A hall lantern enable signal $\overline{HLX}$ is provided by a circuit which includes NAND gates **441, 443, 445** and **447.** NAND gate **441** has inputs connected to the output of NAND gate **324,** the output of NAND gate **360,** and input terminal SBC. The output of NAND gate **441** is connected to an input of NAND gate **445.** NAND gate **443** has inputs connected to the output of NAND gate **324,** output terminal UPTR, and input terminal SAC. The output of NAND gate **443** is connected to an input of NAND gate **445.** NAND gate **447** has an input connected to the output of NAND gate **445** and to the input terminal $\overline{DOR}$. The output of NAND gate **447** is connected to output terminal $\overline{HLX}$.

In the operation of the hall lantern enable circuit, if there are no calls in the system, the output of NAND gate **324** will be low, forcing the outputs of NAND gates **441** and **443** high. This forces the output of NAND gate **445** low and the output of NAND gate **447** high, providing a high $\overline{HLX}$ signal which may be used to suppress the hall lantern circuits. If there is any call in the system, the output of NAND gate **324** will be high. If the scan counter is scanning below the position of the advanced car position, signal SBC will be high, and if the car is set for down travel signal $\overline{UPTR}$ will be high, and the output of NAND gate **441** will go low. This forces the output of NAND gate **445** high, and if there is no request to open a door, signal $\overline{DOR}$ will also be high, forcing the output of NAND gate **447** low, which provides a low $\overline{HLX}$ which may be used to enable the hall lantern circuits. If there is a call in the system, NAND gate **324** will be high, and if the scan counter is scanning above the car, signal SAC will be high, and if the car is set for up travel signal UPTR will be high. This forces the output of NAND gate **443** low, and the output of NAND gate **445** goes high. In the absence of a request to open the door, signal $\overline{DOR}$ will be high, and NAND gate **447** will have a low output, providing a low output signal $\overline{HLX}$, which again may be used to enable the hall lantern circuits.

FIGURE 10

FIG. **10** is a schematic diagram of a synchronizer circuit which may be used for the synchronizer **94** shown in FIG. **3.** The function of the synchronizer circuit **94** is to receive the signal EI from the logic circuit **96,** which indicates that there is a call at the floor of the advanced car position, and the signal $\overline{EQ2}$ from comparator **76** in FIG. **5,** which indicates when the advanced car position is equal to the floor level. If the signal $\overline{EQ2}$ is received by the synchronizer and no call for that floor has been registered, i.e., the synchronizer has not received a high EI signal from the logic circuit **96,** the signal $\overline{EQ2}$ blocks a later arriving EI signal from having any circuit effect. The car thus continues to travel at the same rate, and the indexer **78** provides a pulse up or pulse down signal $\overline{PU}$ or $\overline{PD}$ for the reversible counter and for the synchronizer, which pulse resets the synchronizer and enables it to register an EI signal for the next discrete advanced car position up until the time the next $\overline{EQ2}$ pulse is received. When a signal EI has been registered when the $\overline{EQ2}$ pulse is received, the $\overline{EQ2}$ pulse initiates the deceleration request signal DEC.

More specifically, FIG. 10 includes a circuit for providing a single pulse E2 in response to the equality pulse $\overline{EQ2}$. This one-shot type circuit includes NAND gates 450 and 452, and flip-flops 454, 456 and 458. The flip-flops may be of the cross-coupled NAND gate type, with flip-flop 454 having NAND gates 460 and 462, flip-flop 456 having NAND gates 464 and 466, and flip-flop 458 having NAND gates 468 and 470.

Input terminal $\overline{EQ2}$ is connected to an input of NAND gate 450 and to an input of NAND gate 462 of flip-flop 454. The output of NAND gate 450 is connected to an input of NAND gate 460. The output of NAND gate 462 is connected to an input of NAND gate 466 of flip-flop 456, and also to an input of NAND gate 452. The output of flip-flop 456 is connected to another input of NAND gate 452. The output of NAND gate 452 is connected to an input of NAND gate 470 of flip-flop 458. Another input of NAND gate 470 is connected to receive a signal $\overline{DECS}$, which, as will be hereinafter explained, is a request to decelerate. The output of flip-flop 458 is connected to inputs of NAND gate 450, NAND gate 464 of flip-flop 456, and to an input of NAND gate 452. An input of NAND gate 452 is also connected to receive the deceleration request signal $\overline{DECS}$. The output of NAND gate 452 provides the signal E2 when the equality signal $\overline{EQ2}$ is received.

Flip-flop 458 is reset by either of the terminal slowdown signals $\overline{TDS}$ or $\overline{TSD}$ via an AND gate 472 which has inputs connected to input terminals $\overline{TDS}$ and $\overline{TSD}$, and an output terminal connected to an input terminal of NAND gate 468. Terminal slowdown signal $\overline{TDS}$ is generated by the min/max decoder 88 shown in FIG. 5, and terminal slowdown signal $\overline{TSD}$ is generated by the speed pattern generator 48, as will be hereinafter explained.

Flip-flop 458 may also be reset by a signal $\overline{PU}$ or $\overline{PD}$ from the indexer 78. This reset circuit includes input terminals $\overline{PU}$, $\overline{PD}$ and S200, inverters 476, 478 and 480, flip-flop 482, NAND gate 484, and an output terminal $\overline{PCR}$. Flip-flop 482 may be of the cross-coupled NAND gate type including NAND gates 486 and 488.

An input of NAND gate 488 of flip-flop 482 is connected to input terminal S200 via an inverter 476, which provides a clock pulse during scanning slot 00. Inputs of NAND gate 486 are connected to input terminals $\overline{PU}$ and $\overline{PD}$. The output of NAND gate 486 of flip-flop 482 is connected to an input of NAND gate 484, and via inverter 480 to output terminal $\overline{PCR}$. Since $\overline{PU}$ or $\overline{PD}$ occurs at clock pulse S100, setting flip-flop 482, and clock pulse S200 resets flip-flop 482, signal $\overline{PCR}$ is low or true each time the indexer 78 provides an output, with signal $\overline{PCR}$ being true from clock pulse S100 to clock pulse S200.

NAND gate 484 also has an input connected to input terminal S100 via inverter 478. The output of NAND gate 484 is connected to an input of NAND gate 468 of flip-flop 458.

The operation of the circuit which provides a signal EI pulse for each equality signal $\overline{EQ2}$ is as follows. The various logic levels indicated in FIG. 10 are those just prior to receiving a true or low $\overline{EQ2}$ signal. When $\overline{EQ2}$ goes low, the $\overline{EQ2}$ input to NAND gate 450 goes low and the output of NAND gate 450 goes high, enabling flip-flop 454. The low $\overline{EQ2}$ input to NAND gate 462 of flip-flop 452 triggers flip-flop 454, thus "remembering" that the circuit received an equality signal $\overline{EQ2}$. When flip-flop 454 triggers, NAND gate 462 of flip-flop 454 outputs a logic ONE signal which enables flip-flop 456 and drives the output of NAND gate 452 low. The low output of NAND gate 452 triggers flip-flop 458, driving the output of NAND gate 468 low. The output of NAND gate 468 is connected to an input of NAND gate 452, driving the output of NAND gate 452 high, which is a true E2 signal. The low output of NAND gate 468 also triggers flip-flop 456, which "remembers" flip-flop 458 was triggered, and the output of NAND gate 452 is driven high to enable flip-flop 458. The low output of flip-flop 458 also blocks NAND gate 450.

If deceleration is requested, the $\overline{DECS}$ input to NAND gate 470 of flip-flop 458 will go low, blocking flip-flop 458 from being reset. If deceleration is not requested, $\overline{EQ2}$ will go back to the logic ONE level. A true or low signal $\overline{PU}$ or $\overline{PD}$ will be provided when clock pulse S100 occurs, and flip-flop 482 will be set, changing the output of NAND gate 486 to a logic ONE. NAND gate 484 is thus driven low at the end of clock pulse $\overline{S100}$, which resets flip-flop 458 and the E2 output of NAND gate 452 goes back to logic ZERO level. As hereinbefore stated, terminal slowdown, as evidenced by a low or true $\overline{TDS}$ or $\overline{TSD}$ signal, will also reset flip-flop 458.

When flip-flop 458 resets, it also enables flip-flop 456, and since $\overline{EQ2}$ is back to the logic ONE level, NAND gate 450 is driven low by the high input from flip-flop 458. This resets flip-flop 454, and flip-flop 454 resets flip-flop 456, maintaining the logic ONE output of NAND gate 452 since the input from flip-flop 454 is now at the logic ZERO level. Flip-flop 482 resets at clock pulse S200, terminating the true $\overline{PCR}$ signal. The circuit is back to its original status, awaiting another true $\overline{EQ2}$ signal.

Synchronizer 94 also includes input terminals IDLE, S4, D45, $\overline{CFLY}$ and EI, output terminals DEC, $\overline{DECS}$, and DO, flip-flops 490 and 492, NAND gates 494, 496, 498, 500, 502, 504, 506 and 508, and inverters 510, 512 and 514. Flip-flops 490 and 492 may be of the cross-coupled NAND gate type, with flip-flop 490 having NAND gates 516 and 518, and flip-flop 492 having NAND gates 520 and 522.

Input terminals IDLE, S4 and D45 are connected to input terminals of NAND gate 494. Input terminal IDLE is a logic ONE when the car is idle with the brakes applied, S4 is a clock pulse which occurs during each scanning slot, and a high D45 signal indicates that the doors should close. Input terminal D45 is also connected to an input of NAND gate 516 of flip-flop 490. An input of NAND gate 518 of flip-flop 490 is connected to input terminal $\overline{CFLY}$, which is low when there is a call at the floor during the first scan, as described relative to the call selector 92 shown in FIG. 8. The output of flip-flop 490 is connected to inputs of NAND gate 494 and NAND gate 508.

Input terminal EI is connected to an input of NAND gate 496, to an input of NAND gate 500, and via inverter 510, to an input of NAND gate 506. The remaining input of NAND gate 500 is connected to the output of NAND gate 502, and the output of NAND gate 500 is connected to an input of NAND gate 502. Other inputs of NAND gate 502 are con-nected to the output of AND gate 472, to the output of NAND gate 452, and to the output of NAND gate 504. The output of NAND gate 504 is also connected to an input of NAND gate 506. NAND gate 504 also has inputs connected to the

output of AND gate **472**, to the output of NAND gate **452**, and to the output of NAND gate **506**.

NAND gate **496**, which as already described, has inputs connected to the output of NAND gate **502** and to the input terminal EI, also has an input connected to the output of NAND gate **452**. The output of NAND gate **496** is connected to an input of NAND gate **508**. NAND gate **508** also has inputs connected to the output of AND gate **472**, to the output of NAND gate **516** of flip-flop **490**, and to the output of inverter **512**. The output of NAND gate **508** is connected to output terminal DEC, which is the request to decelerate signal, and to an input terminal of NAND gate **498**. NAND gate **498** also has an input connected to input terminal **S100**. The output of NAND gate **498** is thus the deceleration request synchronized with the clock pulse **S100**, and it is connected to an input of NAND gate **522** of flip-flop **492**. The output of NAND gate **522** of flip-flop **492** is connected to output terminal $\overline{DECS}$ via inverter **512**, which is the synchronized deceleration request. The output of inverter **512** is connected to output terminal DO via inverter **514**, which is the door open request enable signal.

In describing the operation of synchronizer **94** it will be assumed that the car is moving, with the logic levels shown in FIG. **10** being those prior to receiving true $\overline{EQ2}$ and EI signals. When signal EI goes high or true before signal $\overline{EQ2}$ goes low or true, the EI input to NAND gate **496** goes high, the EI input to NAND gate **500** goes high, driving the output of NAND gate **500** low, which blocks NAND gate **502** in its present state of providing a high output. The $\overline{EI}$ output to NAND gate **506** goes low, switching NAND gate **506** to provide a high output, which provides a high input to NAND gate **504**.

Now, when signal E2 goes high upon receiving the equality signal $\overline{EQ2}$, NAND gate **496** has all high inputs, switching its output low, which causes NAND gate **508** to switch to a high output. The output of NAND gate **508** is connected to output terminal DEC, which is thus high, providing a true request to decelerate signal DEC. The high output of NAND gate **508** is also applied to NAND gate **498**, and when clock pulse **S100** is received, the output of NAND gate **498** goes low to set flip-flop **492**, providing a true $\overline{DECS}$ output signal, and a true DO output signal, which are synchronized deceleration and door open enable requests, respectively. When the car stops and opens its door in response to the deceleration request and door open enable request, the IDLE signal goes to a logic ONE, and when the non-interference time expires and signal D45 goes to a logic ONE requesting the door to close, NAND gate **494** provides a low output which resets flip-flop **492**.

When signal $\overline{EQ2}$ goes low before signal EI goes high, E2 goes high applying a logic ONE to the inputs of NAND gates **502**, **504** and **496**. NAND gate **502** switches its output low, which blocks NAND gate **496**, and NAND gate **500**. Thus, if signal EI were to occur in the short time between timing signals **S100** and **S200** (the indexer **78** operates at **S200** if no EI signal by the time of **S100**), it would have no circuit affect, as NAND gate **500** is blocked, and NAND gate **496** is blocked.

If there is a call at the floor during the first scan prior to the car making a run, as hereinbefore explained, signal $\overline{CFLY}$ will be true, and this prevents acceleration and issues a door open request by a circuit which includes flip-flop **490**. The low or true $\overline{CFLY}$ signal sets flip-flop **490**, enabling flip-flop **492** by switching the output of NAND gate **494** high, and switching the output of NAND gate **508** high, which, as hereinbefore explained, provides a high DEC signal, a low $\overline{DECS}$ signal, and a high DO signal.

FIGURE 11

FIG. **11** is a diagram which illustrates the corridor calls that the floor selector **34** allows the car to consider. Each of the floors of a 30 floor building are shown, with blocks associated with the floors **2** through **30** for receiving down calls, and with blocks associated with the floors **1** through **29** for receiving up calls. The blocks for the up and down calls are shown twice, with the first showing being associated with a car **530** travelling downwardly (UPTR=0), which has an advanced car position at the 17th floor, and the second showing being associated with a car **530'** travelling upwardly (UPTR=1), which has an advanced car position at the 17th floor.

In the case of car **530** travelling downwardly, the car can consider down calls at the 17th floor and below it through the second floor, while it may consider up calls from the 16th floor to the first floor. The blocks associated with the floors and direction of the calls which the car may consider are cross-hatched, As explained relative to logic circuit **96**, the car **530** will answer all down calls ahead of it, and if there are no down calls it will travel to the lowest registered up call. Thus, the car **530** is considering the down calls ahead of it, and when there are no further down calls, it considers the up calls for the floors below its advanced car position.

When the car **530'** is travelling upwardly, it considers all up calls ahead of it, including the floor of its advanced car position, and when there are no further up calls, it considers all down calls for all of the floors ahead of it, and it travels to the highest requested down call before stopping and reversing its travel direction.

FIGURE 12

FIG. **12** is a block diagram of a speed pattern generator which may be used for the speed pattern generator **48** shown in FIG. **1**. The speed pattern generator **48** provides a signal for the motor controller **50** which controls the speed of the drive motor **20**, and thus the movement of the car **12**. In elevator systems, the speed and position of the car must be precisely controlled for the safety and comfort of the passengers, while being responsive to calls for service at any time.

The speed pattern generator **48** shown in FIG. **12** continues the concept of the floor selector **34**, hereinbefore described, in that the prior art electromechanical model of the elevator system is not required in order to provide signals for the operation thereof. As will be hereinafter explained, the speed pattern generator of FIG. **12** is a time optimum control system, moving the elevator car from one point to another in minimum time, while directly controlling the rate of change of acceleration, commonly called jerk, subject to maximum limitations placed on acceleration and speed.

The speed pattern generator **48** receives signals $\overline{ACCX}$ and UPTR from the floor selector **34**, responsive to a request for acceleration, and travel direction request, respectively, which signals are processed in logic circuit **540** to provide signals $\overline{DGU}$ and $\overline{DGD}$ for

the car direction relays, acceleration signal ACC, speed signals $\overline{SPS1}$ or $\overline{SPS2}$ for a time ramp generator circuit **542**, and a start signal START for a driver circuit **552**.

The time ramp generator **542** provides a time dependent signal TRAN which for elevator systems having a maximum car speed of about 500 feet/min. may be used to control the acceleration, full speed, deceleration and landing phases of a car. For elevator systems which operate the cars above this speed, the time dependent speed reference signal TRAN is used only for the acceleration, full speed and transition between full speed and maximum deceleration phases of the run, with the speed pattern generator **48** automatically switching to distance dependent signals for the maximum deceleration and landing phases of the run.

A reversible counter **544** receives the distance pulses NLC from counter **70** shown in FIG. **5**. Counter **544** is responsive to signal $\overline{MXVM}$ from the time ramp generator, which goes to logic zero when maximum speed of the car is reached, and signal ACC from logic circuit **540** goes to the logic ZERO level when deceleration is requested. These signals program counter **544** to (a) count up in response to the NLC distance pulses while the car is accelerated, to (b) stop counting when the car reaches maximum speed ($\overline{MXVM}$ goes to ZERO), which thus stores the distance to go to a landing, and to (c) count down when the deceleration is initiated (ACC goes to ZERO).

The output of counter **544** is applied to a distance slowdown circuit **546**, which provides a speed reference signal DSAN proportional to the square root of the distance to go to the landing. The square root of the distance to go to the landing provides constant deceleration for the elevator car, with the switching from the time dependent signal TRAN to the distance dependent signal DSAN being accomplished by switches **548** and **550** and a driver circuit **552** which provides switching signals $\overline{TRSW}$ and $\overline{DSSW}$ at the proper time for operating switches **548** and **550**, respectively. The switching between the speed reference signals will be described in this application as a direct and complete switch from one signal to the other. However, it is preferable that transitional switching be used, which progressively mixes or blends the signals to be switched to provide a smooth transition between the signals and limit jerk in the event of a mismatch between them. Apparatus for performing this transitional switching of signals is disclosed in copending application Ser. No. 13,660, filed Feb. 24, 1970, now U.S. Pat. No. 3,651,892 which is assigned to the same assignee as the present application.

When the car is within a predetermined distance of the floor at which it is to stop, such as 10 inches, a signal HT1 from a hatch transducer is applied to a switching arrangement **554**, which is also responsive to the car travel direction, signals UP and DOWN. Signal UP is true when the car is travelling upwardly, and signal DOWN is true when the car is travelling downwardly. Switching arrangement **554** provides a speed reference signal HTAN for a switch **556**, which receives a switching signal $\overline{HTS}$ from driver **552** at the proper time to switch from the distance speed reference signal DSAN to the distance speed reference signal HTAN. Again, transitional switching is preferably used, using analog switches to switch between the two speed reference signals. The development of the hatch transducer signal HT1 is described in the hereinbefore mentioned U.S. Pat. No. 3,207,265.

The pulse detector **64** shown in FIG. **1** generates pulses in response to pickup **60** on the elevator car and slowdown blades **62** mounted in the hatch near the terminals. These pulses, referred to as PLSDP pulses, along with a signal from a tachometer on the drive motor **20**, are applied to a terminal slow down circuit **558**. Terminal slowdown circuit **558** detects car overspeed near a terminal, nd when overspeed is detected, it provides a speed reference signal TSAN for stopping the car at the terminal the car is approaching. Signal TSAN is switched into circuit effect by switch **560**, which receives a switching signal $\overline{TSD}$ from driver **552**. If the overspeed condition detected by terminal slowdown circuit **558** exceeds a predetermined magnitude, a signal TOVSP is generated which is applied to emergency stopping control (not shown), which may be conventional.

The signals from the analog switches driven by the driver **552** are applied to a summing amplifier **562**, which provides a speed reference signal SRAT for the motor controller **50**, shown in FIG. **1**, which may be conventional.

FIG. 13

FIG. **13** is a schematic diagram of a logic circuit that may be used for the logic circuit **540** shown in FIG. **12**. Logic circuit **540** includes input terminals UPTR, $\overline{ACCX}$, $\overline{A}$, and SPSL. Input termianls UPTR receives a signal from logic circuit **96** responsive to travel direction of the car, with the signal UPTR being a logic ONE for up travel, and a logic ZERO for down travel. Input terminal $\overline{ACCX}$ receives a signal from logic circuit **96** responsive to a request for acceleration. Signal $\overline{ACCX}$ is true or at the logic ZERO level as soon as the brake relay A (not shown) is picked up, and it remains true until the car is requested to initiate slowdown. Input terminal $\overline{A}$ is connected to be responsive to the brake relay A, and is at the logic ZERO level when the brake is set, and at the logic ONE level when the brake is picked up. Input terminal SPSL may simply be a manual selector switch, which is set to select a desired maximum car speed, or it may be an automatic switch which, for example, is in one position during the high speed part of a run, and in a second position to select a lower car speed prior to landing.

Logic circuit **540** also includes output terminals $\overline{DGU}$, $\overline{DGD}$, ACC, SPS1 and SPS2. Output terminals $\overline{DGU}$ and $\overline{DGD}$ are connected to the "go up" and "go down" interface relays, respectively, which set the travel direction preference for the car, output terminal ACC is connected to the reversible counter **70** in floor selector **34**, to the time ramp generator **542**, to reversible counter **544**, and to the distance slowdown circuit **546**. Output terminals SPS1 and SPS2 are connected to the time ramp generator **542**.

Logic circuit **540** also includes NAND gates **564**, **566** and **570**, AND gates **576** and **578**, inverters **568**, **572** and **574**, and a flip-flop **580**.

Input terminal UPTR is connected directly to an input of NAND gate **564**, and via inverter **568** to an input of NAND gate **566**. Input terminal $\overline{ACCX}$ is connected, via inverter **572**, to inputs of NAND gates **564**, **566** and **570**. Input terminal $\overline{A}$ is connected, via inverter **574** to an input of NAND gate **570**. The outputs

of NAND gates 564, 566 and 570 are connected to output terminals $\overline{DGU}$, $\overline{DGD}$ and ACC.

Input terminal SPSL is connected to the D input of flip-flop 580, which may be of the positive edge triggered D type. The clock input of flip-flop 580 is connected to output terminal ACC. The Q and $\overline{Q}$ outputs of flip-flop 580 are connected to inputs of AND gates 576 and 578, respectively. The output terminal ACC is connected to input terminals of AND gates 576 and 578.

In the operation of logic circuit 540, a true UPTR signal enables NAND gate 564, while a false or low UPTR signal enables NAND gate 566. When a request for the car to accelerate is made, signal $\overline{ACCX}$ goes low, which is inverted to a logic ONE by inverter 572, and either NAND gate 564 or NAND gate 566, depending upon which one has been enabled by signal UPTR, outputs a logic ZERO or true signal to its associated output terminal. Assuming that the car is set for up travel, UPTR will be high, enabling NAND gate 564. When the request is made to accelerate the car, NAND gate 564 will provide a logic ZERO to output terminal $\overline{DGU}$, which drives the specific interface relay which sets the car for up travel.

When a request is made by the floor selector 34 to start and accelerate the car, signal $\overline{ACCX}$ goes low, and if the brake A is set, signal $\overline{A}$ will be low. Inverters 572 and 574 invert the low $\overline{ACCX}$ and $\overline{A}$ signals to switch NAND gate 570 to provide a low output, driving output terminal ACC high via inverter 575. A true ACC signal indicates a request has been made to accelerate the car, and the car is available, i.e., idle with the brake applied.

When signal ACC goes high it enables AND gates 576 and 578, and clocks the setting selected by the speed selector switch SPSL to the outputs of flip-flop 580, which "remembers" the speed selection. If the Q output is high, AND gate 576 outputs a high signal to its output terminal SPS1. If the $\overline{Q}$ output is high, AND gate 578 outputs a true signal to its output terminal SPS2.

Output terminal START is connected to the output of inverter 572, which, when terminal START goes high indicates a request to start the car has been made. Output terminal START is connected to the driver circuit 552.

FIG. 14

FIG. 14 is a schematic diagram of a time ramp generator which may be used for the time ramp generator 542 shown in FIG. 12. Time ramp generator 542 is a new and improved arangement for providing at least the speed reference pattern for the acceleration and full speed phases of the run, and in relatively low speed elevator systems it may be used to provide the speed reference pattern for a complete run.

The time ramp generator 542 provides a speed reference signal which includes control over the maximum rate of change of acceleration, hereinafter termed "jerk," in the pattern itself. Regardless of how fast the car responds to the reference speed signal, the jerk in the car speed cannot exceed the maximum jerk built into the reference pattern.

Basically, the time ramp generator 542 generates a speed reference pattern which is jerk controlled, by double integration of a current signal which is representative of the jerk itself. With this arrangement, jerk, which passengers are more aware of than acceleration or speed, is directly controlled, and is not subject to inaccuracies due to tolerances and drift in the circuit components used to perform mathematical calculations. The acceleration is indirectly controlled by integrating the jerk signal, and the car speed is indirectly controlled by integrating the acceleration signal, but small errors in acceleration and car speed due to circuit inaccuracies do not result in passenger discomfort, as might errors in control of jerk.

The measure of jerk for acceleration and deceleration is provided by positive and negative currents, respectively, with these currents being subject to an analog switch, which is switched in response to a feedback circuit which controls maximum acceleration and deceleration, as well as maximum speed. The switching rate of the analog switch when maximum acceleration or deceleration, or maximum speed, is reached, is too rapid for the car to respond thereto, and this switching averages the jerk to ZERO during these periods. During the transition periods between zero speed and maximum acceleration, between maximum acceleration and maximum speed, between maximum speed and maximum deceleration, and between maximum deceleration and zero speed, the analog switch is set by the feedback signal to apply the positive or negative current to the first integrator without switching, to provide a speed pattern reference during these transitional periods with an accurate directly controllable amount of jerk built into the speed pattern by the magnitudes of the positive and negative currents.

More specifically, the time ramp generator 542 includes input terminals SPS1, SPS2 and ACC, being output terminals TRAN, $\overline{MINA}$, and $\overline{MXVM}$. Input terminals SPS1, SPS2 and ACC are connected to logic circuit 540. Output terminal TRAN provides at least the acceleration and full speed portions of the speed pattern for the motor controller, output terminal $\overline{MINA}$, which provides a true signal during maximum deceleration, is connected to the driver circuit 552, and output terminal $\overline{MXVM}$, which provides a true signal when the speed pattern is at its maximum value, is connected to the counters 544 and 70, with the latter counter being hereinbefore described and shown in FIG. 5. FIG.

Time ramp generator 542 includes means 582 for directly representing jerk or rate of change of acceleration, such as adjustable positive and negative voltage sources 584 and 586, and an analog switch 587. The positive voltage source 584 is connected to a terminal 588 through the switch 587 and a voltage 589, and a negative voltage source 586 is connected to terminal 588 via a resistor 591. Thus, the value and direction of the current at terminal 588 may be controlled by opening and closing switch 587. The operation of switch 587 is controlled by a feedback circuit which includes conductor 590, with the switch 587 closing when the conductor 590 is at the logic ONE level, and opening when the conductor 590 is at the logic ZERO level.

The current at terminal 588 is a direct representation of jerk, and since its magnitude is set by the adjustable voltage sources 584 and 486, the jerk in the speed reference pattern to be developed will not exceed the preset jerk magnitude.

Terminal 588 is connected to first integrating means 592, such as an operational amplifier having a capacitor 593 in its feedback loop. If an operational amplifier is used, as illustrated in FIG. 14, terminal 588 is connected to its inverting input, and the non-inverting

input is grounded. Since the integral of jerk or rate of change of acceleration is acceleration, or deceleration, the output of the first integrator **592**, at terminal **594**, is representative of acceleration or deceleration.

Terminal **594** is connected to second integrating means **596**, which may be an operational amplifier having an capacitor **595** in its feedback circuit, with terminal **594** connected to the inverting input thereof via resistor **597**. The non-inverting input is grounded. The integral of acceleration or deceleration is speed, and thus the output of the second integrating means is representative of the speed. The output terminal **598** of the second integrating means **596** is connected to the output terminal TRAN.

Limits on acceleration, deceleration and speed with the direct and automatic control of jerk, are built into the speed reference pattern TRAN by acceleration and speed feedback circuits which control the switching of switch **587**.

The speed feedback circuit compares the signal at the output terminal **598** of the second integrator **596** with a reference signal. The speed signal from terminal **598** is inverted by inverting means **600**, which may be an operational amplifier with a resistor **606** in its feedback loop. Terminal **598** is connected to the inverting output of the operational amplifier via the resistor **608**, and the non-inverting input is grounded through a resistor **604**. The feedback and input resistors **606** and **608**, respectively, are of like value, to provide an amplifier having a gain of -1.

The output terminal **602** of inverting means **600** is connected to first comparator means **610**, which may be an operational amplifier, with output terminal **602** connected to the inverting input of the operational amplfiier. The non-inverting input of the first comparator **610** is conncted to a reference voltage via inverting means **612**, speed demand selector means **614**, and an analog switch **616**.

Analog switch **616** includes first and second switches **618** and **620** driven by signals applied to input terminals SPS1 and SPS2, respectively. The signals SPS1 and SPS2 are provided by logic circuit **540**, hereinbefore described. The outputs of the first and second switches **618** and **620** are connected to selected inputs of the speed demand selector **614**, with each being connected to one end of a predetermined resistor thereof, such as resistors **622** and **624**, respectively, which have a magnitude selected to provide predetermined car speeds. The other ends of the speed selector resistors, including a conductor **625** which has no additional resistance added thereto, and therefore represents the maximum speed selection, are connected in common to output terminal **628** of the speed demand selector **614**. Output terminal **628** of the speed demand selector **614** is connected to the input of inverter means **612**. Inverter means **612** may be an operational amplifier having a feedback resistor **630**, with terminal **628** of speed demand selector **614** connected to the inverting input of the operational amplifier via a resistor **632**. The feedback and input resistors **630** and **632**, respectively, are of like value to provide a gain of -1. The non-inverting input of the operational amplifier is grounded via resistor **634**. The output of inverter **612** appears across resistor **638** at terminal **636**. Terminal **636** is connected to the non-inverting input of comparator **610**. When the speed input to comparator **610** from terminal **602** is less than the reference input at input terminal **636**, the output of comparator **610** is positive, and this output is inverted by inverter **638** to appear at terminal **640** at the logic ZERO level. When the speed input to comparator **610** from terminal **602** exceeds the reference input at input terminal **636**, the output of comparator **610** is negative, and this output is inverted by inverter **638** to appear at terminal **640** at the logic ONE level. Thus, terminal **640** is a logic ONE when the speed input exceeds the reference input and a logic ZERO when the reference input exceeds the speed input.

The acceleration feedback circuit from terminal **594** consists of two separate loops or circuits, one for acceleration, and one for deceleration. The circuit for acceleration includes inverter means **642** and comparator means **644**. Inverter means **642** may be an operational amplifier having a feedback resistor **646**, with the inverting input connected to terminal **594** via resistor **648**. The non-inverting input is connected to ground via resistor **650**. The feedback and input resistors **646** and **648**, respectively, are of like value, to provide a gain of -1.

Output terminal **652** of inverter **643** is connected to the inverting input of inverter **600** through a resistor **653**, which is large compared with the value of resistor **608**, such as about 10 times larger. Thus, the acceleration and speed feedback loops are interconnected, with the value of the connecting resistor **653** being selected to prevent overshoot of the maximum speed during the transition from maximum acceleration to zero acceleration and maximum speed.

Output terminal **652** of inverter means **642** is also connected to the non-inverting input of comparator **644**, and the inverting input of comparator **644** is connected to the selector arm **654** of an acceleration demand selector **656**. Selector arm **654** is connected to a predetermined resistor of the acceleration demand selector, such as resistor **658**, which has a value which provides the desired acceleration. When the acceleration input to comparator **644** from terminal **652** exceeds the reference input from the acceleration demand selector **656**, the output of comparator **644** is positive, which is inverted by inverter **660** to appear at terminal **662** at the logic ZERO level. When the reference input exceeds the acceleration input, the output of comparator **644** is negative, which is inverted by inverter **660** to appear at terminal **662** at the logic ONE level. Thus, terminal **662** is at the logic ONE level when the reference exceeds the acceleration input, and at the logic ZERO level when the acceleration input exceeds the reference level.

Terminals **640** and **662**, responsive to speed and acceleration, respectively, are connected to inputs of a NAND gate **664**. Thus, either speed or acceleration, by providing a logic ZERO at terminals **640** and **662**, respectively, can force the output of NAND gate **664** to the logic ONE level. The output of NAND gate **664** is connected to an input of NAND gate **666**. The other input of NAND gate **666** is responsive to the deceleration feedback loop, as will be hereinafter explained, while the output of NAND gate **666** is connected to the feedback conductor **590**, and thus the switching of NAND gate **666** controls the ON-OFF state of analog switch **582**.

The feedback loop responsive to deceleration includes a comparator **668**, which may be an operational amplifier having its non-inverting input connected to

terminal **594**, and its inverting input connected to the selector arm **654** of the acceleration demand selector **656**. Thus, during deceleration, the acceleration demand selector **656** controls the deceleration portion of the speed pattern. The output of comparator **668** is inverted by inverter **670**, and the output of inverter **670** is connected to a terminal **672** which is connected to an input of NAND gate **666** and to output terminal $\overline{\text{MINA}}$. Signal $\overline{\text{MINA}}$ is true during maximum deceleration.

The output of comparator **668** is positive when the deceleration input from terminal **594** exceeds the reference input, and negative when the reference input exceeds the deceleration input. Thus, terminal **672** is at the logic ONE level when the reference exceeds the deceleration input, and at the logic ZERO level when the deceleration input exceeds the reference input. As will be hereinafter explained, terminal **672** will be at the logic ONE level, except during deceleration. Thus, except during deceleration, NAND gate **666** acts as an inverter for the output of NAND gate **664**, with the acceleration or speed inputs to NAND gate **664** controlling the switching of the feedback switch **587**. Once deceleration is initiated, the output of NAND gate **664** is at the logic ONE level, enabling the NAND gate **666** to be controlled by the deceleration feedback from terminal **672**.

As will be explained during the description of the operation of the time ramp generator **542**, the output of comparator **610** switches rapidly during the maximum speed portion of the speed reference signal. In order to provide a definite signal which indicates that the maximum speed phase of the speed reference signal is taking place, a memory circuit **670** is provided which is connected to input terminal ACC and to terminals **662** and **640** which are responsive to the acceleration and speed feedback, respectively. The output of memory circuit **670** is connected to output terminal $\overline{\text{MXVM}}$, which provides a low or true signal only during the maximum speed phase of the speed reference signal TRAN.

Memory circuit **670** includes a NAND gate **672** which has an input connected to terminal **640** via an inverter **674**, and an input connected to an output from a flip-flop **676** via an inverter **678**. Flip-flop **676** may be of the cross-coupled NAND gate type, having NAND gate **680** and **682**. NAND gate **680** has an input connected to terminal **662**, and NAND gate **682** has an input connected to input terminal ACC.

The output of NAND gate **672** is connected to a flip-flop **684**. Flip-flop **684** may be of the J–K type, which, with positive logic, operates to set Q to the logic ONE level with a low input to the PRESET terminal, and sets Q to the logic ZERO level with a low input to the CLEAR terminal. The output of NAND gate **672** is connected to the PRESET input, the input terminal ACC is connected to the CLEAR input, the J, C and K inputs are grounded, and the Q output is connected to output terminal $\overline{\text{MXVM}}$ via inverter **686**. The operation of the memory circuit **670** will be described after the operation of the time ramp generator in developing the speed reference pattern is described.

FIG. 15

FIG. **15**, which includes FIGS. **15A** and **15B**, is a graph which illustrates waveforms at various circuit points of the time ramp generator **542** shown in FIG. **14**. FIG. **15** will be referred to while describing the circuit operation of the time ramp generator **542**.

It will first be assumed that the elevator car is at rest and there is no demand for service. Thus, signals SPS1, SPS2 and ACC will be at the logic ZERO level. With zero volts into operational amplifier **612**, there will be zero volts at its output **636**, as indicated in FIG. **15B** at **689** of the waveform for operational amplifier **612**. If switch **587** is open, as indicated at **690** on the "open-closed" graph of switch **587** in FIG. **15A**, current will flow out of the inverting input of the first integrator **592** and the output of the first integrator **592** will start to go positive, as indicated at **692** of the waveform for the output of the first integrator **592**. When the output of the first integrator **592** goes positive, the output of the second integrator **596** will go negative, as indicated at **694** of the curve for the second integrator **596**. The output of the operational amplifier **600** will thus go positive, as indicated at **696**. The positive output of operational amplifier **600** is applied to the inverting input of comparator **610** (FIG. **15B**), and it is compared with the ZERO input at the non-inverting input from operational amplifier **612**. Since the speed signal from operational amplifier **600** exceeds the speed reference signal from operational amplifier **612**, the output of comparator **610** goes negative, as indicated at **698** on the curve for comparator **610**. The negative output of comparator **610** is inverted to the logic ONE level by inverter **638**, indicated at **700** for the graph for inverter **638**, which is applied to an input of NAND gate **664**.

The acceleration demand selector **656** is providing a positive voltage at the inputs of comparators **668** and **644**. Since the car is not accelerating or decelerating at this time, the reference voltage exceeds the acceleration and deceleration signals and the outputs of comparators **668** and **644** are negative, as indicated at **702** and **704**, respectively, on the graphs associated with these comparators. The negative output of comparator **668** is inverted to the logic ONE level by inverter **670**, as indicated at **706** of the graph for inverter **670**, and the negative output of comparator **644** is inverted by inverter **660** to the logic ONE level, indicated at **708** of the graph for inverter **660**. The logic ONE output of inverter **660** is applied to the other input of NAND gate **664**, and the logic ONE output of inverter **670** is applied to an input of NAND gate **666**.

Thus, when the car is at rest and switch **587** is open, both inputs of NAND gate **664** go high, driving the output of NAND gate **664** from the logic ONE level, indicated at **710**, to the logic ZERO level, indicated at **712**. When the output of NAND gate **664** goes low, the output of NAND gate **666** is switched from the logic ZERO level, indicated at **714**, to the logic ONE level, indicated at **716**. When the output of NAND gate **666** goes high, analog switch **587** closes, as indicated at **718** (FIG. **15A**).

When the analog switch **587** closes, the jerk current will flow into the inverting input of the first integrator **592**, driving the output of the first integrator **592** negative, as indicated at **720**. The output of the second integrator **596** thus starts to go positive, indicated at **722**, and the output of operational amplifier **600** starts to go negative, as indicated at **724**. The inverting input of speed comparator **610** will thus become less than the ZERO input from the speed reference circuit, and the output of comparator **610** will go positive, indicated at **726** (FIG. **15B**). This positive output of comparator

610 is inverted to the logic ZERO level by inverter 638, indicated at 728, the output of NAND gate 664 is driven high at 730, the output of NAND gate 666 is driven low by the two high inputs, indicated at 732, and the analog switch 587 opens as indicated at 734 (FIG. 15A). This switching of the analog switch 587 occurs at a very rapid rate which is determined by the threshold of comparator 610 and the characteristics of the integrators 592 and 596. The switching rate, which will usually be greater than 1 Khz., is much too fast for the car to respond thereto, so it has no adverse affect on the car movement. The rapid switching of switch 587 is illustrated in the waveforms of FIGS. 15A and 15B as being a low rate in order to more clearly illustrate how the condition of switch 587 affects the various circuit actions.

The rapid switching of analog switch 587 continues, due to the speed feedback and comparator 610, while the car is at rest with no request to accelerate, which phase of the car operation will be referred to as phase I. The various phases of a complete run are indicated at the top of FIG. 15A.

Phase II is initiated when there is a request to accelerate the car, signalled by ACC and either SPS1 or SPS2 switching from a logic ZERO level to a logic ONE level at 736. For purposes of example, it will be assumed that the speed selector switch is set to provide a true SPS1 signal when the ACC signal does true. A true SPS1 signal closes analog switch 618 and the output of operational amplifier 612 goes negative at 738 (FIG. 15B). Since the output of operational amplifier 600 is near ZERO, it is more positive than the negative output of operational amplifier 612, and the output of comparator 610 goes negative, indicated at 740. The output of inverter 638 goes to a logic ONE level, indicated at 742, the output of NAND gate 664 goes to the logic ZERO level, indicated at 744, the otuput of NAND gate 666 goes to the logic ONE level, indicated at 746, and the analog switch 587 closes, indicated at 748 (FIG. 15A).

The rapid switching of analog switch 587 which averaged jerk to ZERO and also maintained the acceleration and speed signals at ZERO, now ceases, and switch 587 remains closed until the selected acceleration demand is reached. When switch 587 closes, the positive input to the inverting input of operational amplifier 592 drives the output of the operational amplifier negative with a slope 750 determined by the pre-selected jerk magnitude. Thus, the output of operational amplifier 592, which is the first integral of jerk, provides the acceleration pattern, and the rate of change of this acceleration pattern cannot exceed the preselected valve.

The linearly decreasing output of operational amplifier 592 is integrated by the second integrator or operational amplifier 596, to provide a smooth curved transition 751 from zero to a predetermined speed when maximum acceleration is reached.

Operational amplifier 642 inverts the output of the second integrator 592, and applies a positive signal, indicated at 752, to the non-inverting input of comparator 644. The increasing magnitude of the positive signal 752 is compared with the constant positive acceleration demand signal applied to the other input of comparator 644, and when the acceleration signal 752 exceeds the acceleration reference, at point 754, the output of comparator 644 switches from the negative voltage level 704 to a positive voltage level 756. Inverter 660 switches from the logic ONE level 708 to the logic ZERO level 758. The output of NAND gate 664 thus goes from the logic ZERO level to the logic ONE level at 760, the output of NAND gate 666 goes low at 762, and switch 587 opens at 764. This ends phase II and initiates phase III of the run.

In phase III, the acceleration is held constant by rapid switching of switch 587 due to comparator 644. The car speed, indicated by the output of the second integrator 596, however, is increasing due to the constant acceleration. When the car speed reaches the selected speed demand, phase III is terminated and phase IV is initiated.

More specifically, when switch 587 opens at 764, operational amplifier 592 starts to go less negative, operational amplifier 642 starts to go less positive, dropping below the acceleration demand reference level, and the output of comparator 644 goes negative. The output of inverter 660 goes to a logic ONE, NAND gate 664 goes low, and the output of NAND gate 666 goes high to close switch 587. This drives the acceleration signal higher than the acceleration reference signal, again opening the switch 587. This rapid switching of switch 587 continues, holding the output of operational amplifier 592 at a predetermined maximum negative level 766, and the output of operational amplifier 642 at the predetermined positive level 754. The constant negative input into the second integrator 596 causes the output of the second integrator 596 to increase linearly during phase III, indicated at 768, although switching at the same rapid rate as switch 587. Inverter 600 inverts the output of the second integrator 596, and applies a negative signal 770 to comparator 610. When the decreasing signal 770 reaches the negative speed reference level at the other input to comparator 610, indicated at point 771 on the graph for inverter 600, the output of comparator 610 switches from a negative to a positive level at 772. The output of inverter 638 switches to a logic ZERO level at 774, the output of NAND gate 664 goes high at 776, the output of NAND gate 666 goes low at 778, and the analog switch 587 opens at 780. This ends phase III.

It will be noted that the positive input to inverter 600 in the speed feedback circuit from the second integrator 596 is aided during phase III by the positive output from inverter 642 in the acceleration feedback circuit. This interaction of the acceleration and speed feedback circuits causes the output of inverter 600 to reach the speed demand level at 771 slightly faster than it would without such interaction, and while it overshoots the speed reference level, it prevents overshoot of the speed reference pattern 596 during the transition from the period of increasing car speed to the period of constant car speed during phase IV.

When switch 587 opens at 780 to end phase III and start phase IV, the output of the first integrator 592 linearly increases from the constant negative level 766 towards zero along line 782. The slope of line 782, and thus the rate of change of acceleration is determined by the preselected jerk setting.

The second integrator 596 provides a smooth, curved transition 784 from the linearly increasing portion 768 to a constant portion 786. As the output from the second integrator 596 smoothly flattens out, the aid from inverter 642 received by inverter 600, determined by the value of resistor 653, is reduced to zero along line 788, enabling the output of inverter 600 which over-

shoots the speed reference level, to return to the speed demand level at the time the speed pattern **596** is arriving at the speed reference level. Thus, during phase IV, the portion **790** of the output of inverter **600** is slightly below the reference level. When the output of inverter **600** increases to the reference level, comparator **610** switches from a positive to a negative output at **792** which in turn drives inverter **638** high, NAND gate **664** low, and NAND gate **666** high, to close switch **587** and end phase IV.

Phase V consists of rapid switching of analog switch **587** in response to comparator **610**, to maintain the output of the second integrator **596** constant at the level **786.** When the switch **587** closes at the start of phase V, the output of the first integrator **592** becomes negative, the output of the second integrator **596** becomes more positive, the output of inverter **600** becomes more negative, and when it reaches the speed reference level, the output of comparator **610** goes positive, inverter **638** goes to logic ZERO, the outputs of NAND gates **664** and **666** go high and low, respectively, and gate **587** opens at **796.** This starts the chain of events which closes switch **587,** causing a rapid switching of analog switch **587** during phase V, which maintains the car speed constant.

Phase V is terminated when a request is made by the floor selector to stop the car at the floor of the advanced car position, signified by signals ACC and SPS1 going to the logic ZERO level at **800.** This starts phase VI, which is a smooth transition from a maximum constant speed to maximum deceleration. When signal SPS1 goes to ZERO, the speed demand input to operational amplifier **612** goes to ZERO, and the output of operational amplifier **612** switches from the speed demand reference level **738** to zero at **802.** Since the car speed is above the reference level, the output of comparator **610** goes positive at **804,** driving the output of inverter **638** low at **806,** and the output of NAND gate **664** high at **808.** The other input to NAND gate **666,** from the deceleration feedback circuit is still a logic ONE, and NAND gate **666** switches low at **810** to open switch **587** at **812.**

When switch **587** opens at **812,** the output of the first comparator increases from zero along a curve **814,** which has a slope determined by the jerk setting. The output of the second integrator **596** smoothly drops from the maximum speed level **786** to a slower speed along curve **816.** When the deceleration of the car reaches the deceleration demand level, signified by portion **814** of the acceleration signal at the output of the first integrator **592** reaching the magnitude of the acceleration demand reference, comparator **668** switches its output from a negative level **702** to a positve level **818.** Inverter **670** switches to the logic ZERO level at **820,** the output of NAND gate **666** goes high at **822,** and switch **587** closes at **824.** This ends phase VI, and starts phase VII, which is the constant deceleration phase of the run.

When switch **587** closes at the start of phase VII, the output of the first integrator **592** drops, and when it drops below the deceleration reference level, the output of comparator **668** switches to a negative output, inverter **670** goes to a logic ONE, the output of NAND gate **666** goes to logic ZERO, and switch **587** opens. This then starts the chain of events which recloses the switch **587,** and switch **587** switches rapidy between its open and closed states to maintain the output of the first integrator at the selected maximum positive value **826.** The constant positive output of the first integrator **592** causes the second integrator **596** to decrease linearly along a curve **828,** and inverter **600** increases towards zero. The increase in the output of inverter **600** towards zero along curve portion **830** is aided by the negative portion **832** of the output of inverter **642,** causing the curve **830** to reach the ZERO level ahead of the output of the second integrator **596,** preventing overshoot of the speed pattern beyond the reference level in the same manner hereinbefore described relative to phase IV. When curve portion **830** reaches the threshold of comparator **610,** at point **834,** the output of comparator **610** switches from a positive to a negative level at **836,** the output of inverter **638** switches to a logic ONE level at **838,** the output of NAND gate **664** goes to logic ZERO at **840,** the output of NAND gate **666** goes high at **842,** and the feedback switch **587** closes at **844,** to end phase VII and initiate phase VIII.

Phase VIII is the transition from maximum deceleration to zero car speed. When switch **587** closes at the start of phase VIII, the output of the first integrator **592** decreases along curve **846,** with a constant slope determined by the jerk setting, the second integrator provides a smooth curved transition **848** from maximum deceleration towards zero car speed, and the combination of the outputs of the second comparator and operational amplifier **642,** the latter of which is increasing towards ZERO along curve **850,** prevents operational amplifier **600** from dropping back to the reference level until the car comes to a smooth stop at **852.** When the car stops, phase VIII is terminated, and phase I is initiated.

The memory circuit **670** provides a false or high $\overline{\text{MXVM}}$ signal until comparator **610** indicates maximum velocity has been reached, at which time, as indicated in FIG. 15B, signal $\overline{\text{MXVM}}$ switches true or low at point **854.** When the car is at rest, the output of inverter **660** is high, which enables flip-flop **676,** and the signal ACC is low, which sets flip-flop **676** to provide a logic ONE level at the output of NAND gate **682,** which is inverted to the logic ZERO level by inverter **678.** NAND gate **672** thus supplies a logic ONE to the PRESET input of flip-flop **684.** The low ACC signal applied to the CLEAR input of flip-flop **684** sets flip-flop **684** to provide a logic ZERO at the Q output, which is inverted to a logic ONE at output terminal $\overline{\text{MXVM}}$. When acceleration is requested, signal ACC goes to logic ONE, enabling flip-flops **676** and **684.** When maximum acceleration is reached, inverter **660** goes low at **758** to switch flip-flop **676,** and inverter **678** now provides a logic ONE to one of the inputs of NAND gate **672.** When the comparator **610** switches positive to indicate maximum speed has been reached, inverters **638** and **674** apply a logic ONE to the other input of NAND gate **672,** and the output of NAND gate **672** goes low, switching flip-flop **684** to provide a high Q output, which is inverted to a low or true $\overline{\text{MXVM}}$ signal. When signal ACC goes to ZERO, flip-flop **676** is switched again, to cause NAND gate **672** to output a logic ONE, and the logic ZERO at the CLEAR input switches flip-flop **684** to provide a low Q output, which is inverted to provide a high $\overline{\text{MXVM}}$ signal, as indicated at **856** in FIG. 15B.

FIG. 16

FIG. **16** is a graph which presents the jerk, accelera-

tion and speed curves shown in FIG. 15, except without the rapid switching shown in FIG. 15. The jerk curve represents the input to the first comparator 592 from terminal 588. During the rapid switching of the switch 587, the jerk is averaged to zero. When the switch is closed, positive jerk restraint is applied, and when it is open negative jerk restraint is applied.

The speed curve, i.e., the output of the second comparator 596, may be used for the complete run of the car for relatively low speed elevator systems, as it provides a speed pattern for all phases of a run. On high speed elevator systems, above about 500 ft./min., the speed pattern provided by the time ramp generator would not be accurate enough during the deceleration and landing phases of the run. Thus, as shown in FIG. 12, the speed pattern generator 58 includes, in addition to the time ramp generator 542, a distance slowdown circuit 546, and a hatch transducer circuit 554. As shown in FIG. 16, the speed pattern signal SRAT from the speed pattern generator 48 may be a composite signal, including a portion 860 from the time ramp generator which includes phases I through VI, a portion 862 from the distance slowdown circuit 546, which includes phase VII, and a portion 864 from the hatch transducer circuit 554, which includes phase VIII.

FIGURE 17

FIG. 17 is a schematic diagram of a reversible counter and a distance slowdown circuit which may be used for the reversible counter 544 and distance slowdown circuit 546 shown in block form in FIG. 12. The distance slowdown circuit shown in FIG. 17 is a new and improved arrangement for accurately bringing the car to the landing or leveling zone, despite long term drift of circuit constants. The driver circuit 552 switches the source of the speed pattern from the time ramp generator 542 to the distance slowdown circuit 546 when signal $\overline{\text{MINA}}$ goes to ZERO, indicating that maximum deceleration has been reached. Just prior to this time, the distance slowdown circuit shown in FIG. 17 is automatically calibrated, but not for the position of the car at that time. The distance slowdown circuit is calibrated for the count which represents the point where the car will be when the speed pattern should transfer from the distance slowdown circuit to the hatch transducer circuit. This is the only point that extreme accuracy is required, and by calibrating the distance slowdown circuit for this specific diatance to the floor, which calibration occurs just before the circuit is utilized, the distance slowdown circuit need not be designed to maintain freedom from drift over a long period of time, and the resulting apparatus may therefore be constructed more economically.

More specifically, the counter 544 shown in FIG. 17 includes input terminals IDLE, $\overline{\text{MXVM}}$, ACC, and NLC, and output terminals NL1 through NL12, and $\overline{\text{NL16}}$. Input terminal IDLE receives a high or true signal when the car is idle, ready to make a run, input terminal $\overline{\text{MXVM}}$ receives a low or true signal from the time ramp generator 542, when the car is in the maximum speed portion of its run, input terminal ACC receives a high or true signal when a request is made to accelerate the car and the brake relay is picked up, and it remains true until the car is requested to slow down, and input terminal NLC receives distance pulses, such as one distance pulse for each one-half inch of car travel, from the reversible counter 70 in the floor selector 34.

Counter 544 includes reversible counting means 870, such as a binary counter, having a sufficient bit capacity to count to the maximum distance in terms of the standard increment, over which the elevator car is accelerated. For example, three synchronous 4-bit UP/-DOWN binary counters 872, 874 and 876 may be cascaded to provide a 12-bit counter sufficient to count to about 170 feet, using 0.5 inch for each pulse, but any number of bits may be used, depending upon the requirements of the specific application.

The CARRY and BORROW outputs of counter 872 are connected to the UP and DOWN inputs of counter 874. respectively, and the CARRY and BORROW outputs of counter 874 are connected to the UP and DOWN inputs of counter 876. The CLEAR inputs of counters 872, 874 and 876 are connected to the input terminal which receives the IDLE signal. When the IDLE signal is true or high, all outputs are forced to the low level.

The UP and DOWN inputs of counter 872 are connected to receive NLC pulses via a circuit which includes input terminals NLC and $\overline{\text{MXVM}}$, inverters 902 and 904, and NAND gates 906, 908, 910 and 912.

NAND gate 906 has an input connected directly to input terminal $\overline{\text{MXVM}}$, and another input connected to input terminal NLC via inverter 902. NAND gate 908 has an input connected to input terminal NLC via inverter 902, and another input connected to the BORROW output terminal of counter 876, which output terminal is at the logic ONE level, except when the counter 876 counts down and reaches zero. The outputs of NAND gates 906 and 908 are connected to inputs of NAND gates 910 and 912, respectively. NAND gate 910 also has an input connected to input terminal ACC, and NAND gate 912 has an input connected to input terminal ACC via an inverter 904. The outputs of NAND gates 910 and 912 are connected to the UP and DOWN inputs, respectively, of counter 872.

The A, B, C and D outputs of counter 872 are connected to inputs of NAND gates 878, 880, 882 and 884, respectively, the A, B, C and D outputs of counter 874 are connected to inputs of NAND gates 886, 888, 890 and 892, respectively, and the A, B, C and D outputs of counter 876 are connected to NAND gates 894, 896, 898 and 900, respectively. The B, C and D outputs of counter 874 and the A, B, C and D outputs of counter 876 are also connected to inputs of a NAND gate 948 via inverters 950, 951, 952, 953, 954, 955 and 956, respectively. The output of NAND gate 948 is connected to an output terminal $\overline{\text{NL16}}$.

NAND gates 878, 880, 882, 884, 886, 888, 890, 892, 894, 896, 898 and 900 also each have an input connected to the output terminal 999 of a circuit which includes input terminal ACC, the BORROW output of counter 876, inverters 914 and 916, an AND gate 918, a NAND gate 920, and a monostable multivibrator 922. The AND gate 918 has one input connected to input terminal ACC via inverter 914, and another input connected to the BORROW output of counter 876. The output of AND gate 918 is connected to inputs of the NAND gate 920 and of the monostable multivibrator 922. Another input of NAND gate 920 is connected to the output of the monostable multivibrator 922. The output of NAND gate 920 is connected to output terminal 999 via inverter 916.

The outputs of NAND gates **882** and **886** are connected to inputs of NAND gates **928** and **932**, respectively. NAND gates **928** and **932** also have inputs connected to terminal **999**. The outputs of NAND gates **928** and **932** are connected to output terminals NL3 and NL5, respectively. The remaining NAND gates **878, 880, 884, 888, 890, 892, 894, 896, 898** and **900** are connected to output terminals NL1, NL2, NL4, NL6, NL7, NL8, NL9, NL10, NL11 and NL12, respectively, via inverters **924, 926, 930, 934, 936, 938, 940, 942, 944** and **946**, respectively.

In the operation of counter **544** it will be assumed that the elevator car is idle and ready to make a run, in which case input terminal IDLE receives a true or high signal which forces the 12 outputs of counter **870** to the logic ZERO level. When the car is requested to accelerate, the signal IDLE goes to logic ZERO, enabling counter **870**, the accelerate signal ACC goes to the logic ONE level, and the time ramp generator **542** provides the speed pattern which initiates car movement. When the car starts to move, an NLC pulse is provided at input terminal NLC for each standard increment of car travel, such as 0.5 inch. Input terminal $\overline{\text{MXVM}}$ is at the logic ONE level, since the car is not at maximum speed, and the BORROW output B of counter **876** provides a signal which is at the logic ONE level. Thus, both NAND gates **906** and **908** are gated by the NLC pulses. During acceleration, signal ACC is at the logic ONE level, which gates the NLC pulses through NAND gate **910** to the count up input of counter **872**. The inverter **904** inverts the true ACC signal to block NAND gate **912**. When the car reaches maximum speed, $\overline{\text{MXVM}}$ goes to logic ZERO, as hereinbefore described and shown in the graph of FIG. **15**, which blocks NAND gate **906** and prevents the NLC pulses from reaching the counter **870**.

When signal ACC goes to logic ZERO, requesting deceleration, signal $\overline{\text{MXVM}}$ goes back to logic ONE but NAND gate **910** is now blocked by the low ACC signal. The inverter **904** inverts the low ACC signal and passes the NLC pulses through NAND gate **912** to the count down input of counter **872**. Thus, the output of counter **870** has a count at its output terminals which continuously registers the distance to go to the floor. It stops counting the NLC pulses when the car stops accelerating, and it counts down when the car starts decelerating. With like rates of acceleration and deceleration, the counter accurately registers the distance to go to the floor of the advanced car position when the signal ACC goes to logic ZERO.

When the counter **870** counts down to the binary number representing **32**, which indicates the car is **16** inches from the floor at which it is to land, the B, C and D outputs of counter **874** and the A, B, C and D outputs of counter **876** will be at the logic ZERO level. These ZERO outputs are inverted by inverters **950, 951, 952, 953, 954, 955** and **956** to switch NAND gate **948** and provide a low $\overline{\text{NL16}}$ signal, indicating the car is within **16** inches of the floor at which it is to stop.

When slowdown is initiated, the distance slowdown circuit **546** shown in FIG. **17** provides a speed pattern responsive to the square root of the signal having the magnitude proportional to the distance to go to the floor, with the speed pattern transferring from the time ramp generator **542** to the distance slowdown circuit **546** through the operation of analog switches **548** and **550** and driver **552** shown in FIG. **12**. Thus, the output of counter **870** is not used until slowdown is initiated, and it is then used until the speed pattern switches from the output of the distance slowdown circuit **546** to the output of the hatch transducer circuit **554** when the car is a predetermined distance from the floor, which for purposes of example will be assumed to be 10 inches. When the car is slowing down to land and it is 10 inches from the floor, it is important, in order to avoid a jerky landing, that the output voltages of the distance slowdown circuit **546** and the hatch transducer circuit **554** match when the transfer is made at the 10 inch point by the analog switches **550** and **556**. In order to insure a good match, the square root device used in the distance slowdown circuit would have to have an accuracy of $\pm$ 0.05 percent. A square root device with this accuracy, however, would be relatively costly to manufacture.

FIG. **17** illustrates a new and improved distance slowdown circuit which provides the necessary accuracy at the 10 inch transfer point, without the necessity of using a highly accurate, high cost square root device. An inexpensive square root device, such as an operational amplifier with a low cost analog multiplier in its feedback loop, will hold its calibration over the period of time that it takes to decelerate an elevator car and bring it to a stop at a landing. This characteristic, along with the fact that the output of the reversible counter **870** is only used during the slowdown phase of the elevator run, is used to provide a low cost distance slowdown circuit which will give the required 0.05 percent accuracy at the 10 inch transfer point when the transfer is made.

More specifically, the reversible counter **544** is modified to output the binary signal 10100 for number 20, which represents the transfer distance 10 inches, prior to the deceleration stage of the run, and then switch over to provide the actual count of the counter **870** when deceleration is requested.

When the signal ACC is low, AND gate **918** has two logic ONE inputs, one from the BORROW output of counter **876**, and one from input terminal ACC via inverter **914**. The monostable multivibrator **922**, such as Texas Instrument SN **74121**, has its $\overline{\text{Q}}$ output connected to an input of NAND gate **920**, and thus is providing an output at the logic ONE level. The two logic ONE inputs to NAND gate **920** provide a logic ZERO output, which is inverted to the logic ONE level by inverter **916**. Thus, terminal **999** is at the logic ONE level, which enables NAND gates **873** through **900** and NAND gates **928** and **932**.

When the car is requested to accelerate, signal ACC goes high, AND gate **918** switches low, NAND gate **920** switches high, and inverter **916** provides a logic ZERO at terminal **999**. NAND gates **878** through **900** all provide a logic ONE at their outputs, which signals are inverted by inverters **924, 926, 930, 934, 936, 938, 940, 942, 944** and **946** to the logic ZERO level. NAND gates **928** and **932**, however, provide outputs at the logic ONE level. Thus, when signal ACC is high, output terminals NL1 through NL12 output the binary number for 20 or 10100, representing the 10 inch transfer point. When the signal ACC goes low, the output of AND gate **918** again goes high, which triggers the monostable multivibrator **922** to provide a low pulse of predetermined duration, which thus holds NAND gate **920** high and terminal **999** low for the duration of the

monostable pulse, for reasons which will be hereinafter explained.

Should the counter **870** for some reason count down to ZERO before reaching the 10 inch transfer point, the distance slowdown circuit would take the square root of ZERO, which is ZERO, and the speed pattern would be at ZERO voltage and the car would not run. However, with the arrangement shown in FIG. **17**, wherein the BORROW output of counter **876** is connected to an input of AND gate **918**, the counter **544** will be forced to output a binary count of **20** when the counter **870** counts down to and reaches zero. If the car has not reached the **10** inch transfer point, this count will provide a voltage output from the distance slowdown circuit, running the car in the same direction as its previous travel direction until the transfer point or the floor is reached. The BORROW output of counter **876** goes to ZERO when the counter **876** counts down to zero, which starts the same sequence described when the signal ACC went to ZERO.

The distance slowdown circuit **546** shown in FIG. **17** includes a digital to analog converter **960**, inverter means **962**, a square root device **964**, inverter means **966** and **968**, and a sample and hold circuit **970**.

The digital to analog converter **960** is a linear converter which provides a predetermined unidirectional output voltage when its input terminals NL1 through NL12, which are connected to the like numbered output terminals of counter **544**, are all at the logic ONE level, and proportionally less voltage as the binary count is reduced.

The output of converter **960** is applied to inverter means **962**, which may be an operational amplifier having a resistor **972** in its feedback loop. The output of converter **960** is connected to the inverting input of operational amplifier **962** via resistor **973**, and its non-inverting input is connected to ground via a resistor **974**. The output of operational amplifier **962** is connected to square root device **964** via a selector **976**, which includes a selector arm **978** and a plurality of resistors **980**. Selector **976** is used to provide a choice in deceleration characteristics.

The square root device **964** may be of any suitable type, such as an operational amplifier **982** having an analog multiplier **984** and resistor **986** in its feedback loop. The selector **976** is connected to the inverting input of operational amplifier **982**, and the non-inverting input is connected to an adjustable voltage source **988**. Thus, if the source **988** is adjusted to zero, in the absence of a voltage from operational amplifier **962**, the output of operational amplifier **982** and the output of multiplier **984** will be zero, as the inputs are balanced. If the output of operational amplifier **962** increases from zero to $-X$ volts, the output of the multiplier **984** will be $+X$ volts, in order to keep the inputs of operational amplifier **982** balanced, and the input to the multiplier **984** must therefore be the $\sqrt{X}$ volts. If the source **988** is not adjusted to ZERO, the output of the operational amplifier **982** will be proportional to the square root of the input from the operational amplifier **962**, with a bias added thereto depending upon the setting of the adjustable voltage source **988**.

The output from operational amplifier **982**, which as hereinbefore stated is proportional to the square root of the input thereto, is applied to inverter means **966** via resistor **989**. Inverter means **966** may be an operational amplifier having its inverting input connected to resistor **989**, a resistor **990** in its feedback loop which is equal to resistor **989** in magnitude in order to provide a gain of -1, and its non-inverting input connected to ground via resistor **992**.

The output of operational amplifier **966** is connected to inverting means **968** via resistor **994**. Inverting means **968** may be an operational amplifier having its inverting input connected to resistor **994**, its non-inverting input connected to ground via resistor **996**, and a resistor **998** in its feedback loop which is equal in magnitude to resistor **994**, to provide a gain of -1. The output of operational amplifier **968** provides the speed pattern voltage during slowdown, and is thus connected to output terminal DSAN.

A selector **1000** may be provided to add a bias voltage to the input of operational amplifier **968**, to select different deceleration characteristics. Selector **1000**, for example, may include a source voltage **1002** selectively connected to one of the plurality of resistors **1004** via a selector arm **1006**.

The sample and hold circuit **970** includes comparator means **1008**, which may be an operational amplifier having Zener diodes **1010** connected in its feedback loop, and its inverting input connected to a reference voltage which includes a source **1012** of unidirectional potential and a resistive divider circuit **1014**. The reference voltage is selected to be equal to the desired value of the output voltage DSAN when the count of the counter **544** reaches the magnitude which indicates the car is at the distance to the floor where the hatch transducer takes over in supplying the speed reference pattern. As hereinbefore used as an example, the reference voltage would be the voltage which should appear at the output terminal DSAN when the count of counter **870** is the binary number for 20, representing a distance of 10 inches from the floor. The non-inverting input of operational amplifier **1008** is connected to the output terminal DSAN, via resistor **1016**, which provides the necessary feedback information as to the value of the signal DSAN, and the affect of the sample and hold circuit on the signal DSAN.

Any deviation of the output voltage at terminal DSAN from the reference voltage provided by source **1012** and divider **1014**, results in the output of operational amplifier **1008** changing in the direction necessary to balance the inputs. The sample and hold circuit **970** is operatively connected to sample the voltage appearing at terminal DSAN, when the car is accelerating and during the constant speed portion of its run. This is the time that the counter **544** is outputting the binary number for 20 representing the switchover distance from the distance slowdown circuit **546** to the hatch transducer circuit **554**. During this time, the calibration voltage necessary to force the voltage at output terminal DSAN to equal the reference voltage is developed and stored. Just prior to the counter **544** changing from the forced output count to the actual count of counter **870**, the feedback portion of the sample and hold circuit is disconnected from the storage portion, such that the calibration voltage for the switchover point may be maintained during the distance slowdown without being affected by the output of counter **544** when is switches to the count of counter **870**. This bias or calibration voltage for the switchover point between the distance slowdown signal DSAN and the hatch transducer signal HTAN has no adverse affect on the operation of the car while it is decelerating from its maxi-

mum speed to the switchover point, as its value is insignificant when the output count of counter **544** is relatively high. The calibration voltage only becomes important when the countdown nears the switchover distance, and it assures transfer between the distance slowdown and hatch transducer signals without a discontinuity which would cause a jerky landing.

The proper sequencing of the sample and hold circuit **970** with the output of counter **544** may be accomplished by using a high ACC signal to activate the sample and hold circuit, and to disconnect the feedback portion of the sample and hold circuit from the storage portion when the ACC signal goes low at the time deceleration is requested. This is when the monostable multivibrator **922** becomes important, as it delays the switching of the counter **544** from its forced to its actual count when the ACC signal goes low, for a time sufficient for the sample and hold, in response to the low ACC signal, to disconnect the sampling function from its holding function.

The circuit functions of the sample and hold circuit **970** may be provided by an inverter **1018**, a PNP transistor **1020**, an NPN transistor **1022**, two N-channel field effect transistors **1024** and **1026**, and a capacitor **1028**. The emitter electrode of transistor **1020** is connected to input terminal ACC via the inverter **1018** and a resistor **1030**, the base of transistor **1020** is connected to ground, and its collector electrode is connected to the base electrode of transistor **1022**. The emitter electrode of transistor **1022** is connected to its base electrode via resistor **1032** and to a source **1033** of negative unidirectional potential. The collector of transistor **1022** is connected to the gate electrode G of field effect transistor **1024**. The gate electrode G of field effect transistor **1024** is also connected to the output of comparator **1008** via resistor **1036**. The source S of transistor **1024** is connected to the output of comparator **1008**, and its drain D is connected to the gate of transistor **1026**. The capacitor **1028** is connected from the interconnected drain and gate electrode of transistors **1024** and **1026** to ground. The drain of transistor **1026** is connected to a source **1037** of positive unidirectional potential, and its source is connected to the inverting input of operational amplifier **986** via resistor **1038**, and to the source **1033** of negative unidirectional potential via resistor **1034**.

When input terminal ACC goes high, counter **544** switches to its forced count, as hereinbefore described, and inverter **1018** cuts off transistors **1020** and **1022**, providing a zero voltage between the source and gate of transistor **1024**, switching the channel of transistor **1024** to its low impedance condition. Thus, the output of comparator **1008**, which goes to the value necessary to balance its inputs, is effectively connected to charge capacitor **1028**. Capacitor **1028**, connected to the gate of transistor **1026**, causes transistor **1026** to conduct in accordance with the magnitude of the charge on capacitor **1028**, and apply a calibration voltage to the inveting input of operational amplifier **968**. When the output of operational amplifier **968** is equal to the reference voltage at the inverting input of comparator **1008**, the charge on capacitor **1028** becomes stabilized, as does the calibration voltage applied to the inverting input of operational amplifier **968**.

When the signal ACC goes low when deceleration is requested, inverter **1018** applies a positive voltage to transistor **1020**, causing it to conduct and provide base drive for transistor **1022**. Transistor **1022** conducts and connects the gate of transistor **1024** to the source **1033** of negative unidirectional potential, switching transistor **1024** to its high impedance condition, and effectively disconnecting the output of comparator **1008** from the capacitor **1028**. The monostable multivibrator **922** holds the counter **544** at its forced count for a time sufficient to enable the capacitor **1028** to become isolated from the output of comparator **1008**. The capacitor **1028** remains charged during slowdown, with very little leakage due to the high input impedance of transistor **1026**, while biasing transistor **1026** to provide the calibration voltage necessary to match the output of operational amplifier **968** with the output of the hatch transducer at the distance from the floor where the speed pattern switches from the distance slowdown circuit to the hatch transducer circuit.

This calibration of the distance slowdown circuit, prior to each slowdown of the elevator car, enables a low cost square root device **964** to be used, as the intermittent calibration takes care of long term drift associated with the lower cost square root devices. These lower cost square root devices are very stable for short periods of time, such as the time required to decelerate a high speed elevator car from its maximum speed to rest. Further, the calibration of the distance slowdown circuit is made in the low range of the output voltage, the least accurate region for a square root computing device.

The calibration of the distance slowdown circuit prior to each deceleration phase of a run of an elevator car, while primarily to reduce the cost of the square root device, has other advantages, as it allows the accuracy of the analog to digital converter to be relaxed. At the larger signal values, the error of the digital to analog converter **960** is roughly halved by taking the square root of its output, and at the lower signal values the calibration compensates for drift in the digital to analog converter. Special recalibration of the distance slowdown circuit **546** after the initial factory calibration, is eliminated, since recalibration occurs automatically during each run of the elevator car.

FIG. 18

Elevator safety codes require that a redundant and independent means be provided for slowdown of the car in the vicinity of the terminal floors. This terminal slowdown means provides the functions of monitoring for possible loss of control, and in the event loss of control is detected, it provides an auxiliary speed pattern for the motor controller which brings the car to a stop. The prior art terminal slowdown devices commonly utilize two series of cam actuated switches, one series located on the selector carriage, and the other series on the elevator car. As the elevator car moves towards a terminal floor, a cam located in the shaft opens the switches on the car in sequence. If the selector carriage is moving properly, as required for normal car slowdown, there is a corresponding contact closing on the selector. Should the selector fail to move, a monitoring circuit initiates terminal slowdown. An auxiliary slowdown pattern is generated by a cam driven distance sensor located on the top of the car. While this prior art arrangement is effective, it requires a delicate adjustment of the slanted cam which drives the switches and distance sensors on the car. The deflection of the sensors arm is small compared with the very long distances

required to slow the car, making it necessary to use two cams and two sensors in some high speed elevator systems.

FIG. 18 is a schematic diagram of a terminal slowdown circuit which may be used for the terminal slowdown circuit 558 shown in block form in FIG. 12, which circuit eliminates the series of cam operated switches and distance sensor used in the prior art. In general, the terminal slowdown circuit 558 shown in FIG. 18 utilizes notched plates disposed in the hatchway, one near each terminal, such as the notched plate 62 shown in FIG. 1, and the notched plate 1040 shown in FIG. 19. Plate 1040 has a series of holes or openings 1042 spaced such that a photoelectric or magnetic detector located on the car can detect their presence and initiate pulses for the terminal slowdown circuit 558. The holes or openings 1042 are spaced such that if the car is slowing down with a constant rate of deceleration, the time elapsed as the car travels from one opening to the next stays constant. If the car is not decelerating, or the deceleration rate of the car is not within acceptable limits, the time between the spaced openings will be shorter than normal, and a monitoring circuit in the terminal slowdown circuit 558 will detect this overspeed condition and cause the car to initiate terminal slowdown.

The same blade 1040 used to detect overspeed is used to generate the auxiliary speed pattern when an overspeed condition is detected. The difference between the rate at which the pulses are provided in response to a detector passing the blade 1040, and a predetermined rate corresponding to the maximum allowable slowdown rate, gives the speed error. The spacing of the openings in the blade sets the predetermined slowdown rate, with any deviation from the slowdown rate automatically providing an unbalance which is converted to a unidirectional speed error signal. This speed error signal may be used to directly feed the motor controller. Alternatively, the speed error signal may be added to the actual speed of the car, measured by such means as a conventional tachometer, to obtain a speed pattern which may be directly substituted for the normal speed pattern.

More specifically, the terminal slowdown circuit 558 shown in FIG. 18 includes a slowdown blade 1040 having spaced notches or openings 1042 therein, with the spacing between successive openings being selected to provide a predetermined speed profile which substantially matches the normal deceleration rate of the elevator car. FIG. 19 illustrates a typical speed profile curve 1043.

While it is preferable that the slowdown blade 1040 be mounted in the hatchway near the terminal which it is to monitor for overspeed, with the pick-up device on the car, it would also be suitable to mount the blade on the car with a pick-up device disposed adjacent to the terminal to be monitored.

Pick-up means 1044 is provided for detecting the presence of the notches or holes 1042. Pick-up means 1044 may be of any suitable type, such as the photoelectric device illustrated in FIG. 18 which includes a source 1046 of electromagnetic radiation directed towards and spaced from a detector 1048, such that the discontinuities of the blade 1040 pass therebetween when the car is travelling in the hatchway. The source 1046, for example, may be a light emitting diode, a glow lamp, a neon lamp, or the like, and the detector 1048 may be a phototransistor, a photodiode, a photoresistor, or the like. The pick-up means 1044 may also be of the magnetic type, using proximity detector principles, which requires a single coil, or transformer principles which uses two coils.

Detector 1048 includes means for generating pulses as the discontinuities of the blade 1040 and detector 1048 move relative to one another, which pulses are applied to input terminal PLSDP of the terminal slowdown circuit 558. The PLSDP pulses are amplified in amplifier 1050 and applied to a monostable multivibrator 1052. The output of the monostable multivibrator 1052 is a series of constant width pulses spaced according to the rate pulses are received from the amplifier 1050. The pulses from the monostable multivibrator 1052 are used to gate a switch 1053, which has one side connected to a positive source 1055 of unidirectional potential via resistor 1057, and its other side is connected to ground. Switch 1053 may be a transistor, or the like. A low pass filter amplifier 1054 is connected to the junction 1051 between the switch 1053 and resistor 1057. The filter amplifier 1054 may be an operational amplifier having its inverting input connected to junction 1051 via resistor 1059. Its non-inverting input is connected to a source 1061 of positive unidirectional potential via an adjustable resistor 1063. Parallel connected capacitor 1065 and resistor 1067 are connected in the feedback loop of the operational amplifier.

In the absence of a pulse from the monostable multivibrator 1052, switch 1053 is open, and the positive source 1055 is connected to the inverting input of filter amplifier 1054. When a pulse is received from the monostable multivibrator 1052, switch 1053 closes to connect the inverting input of filter amplifier 1054 to ground. When the slowdown of the car is normal, the low pass filter amplifier provides a constant unidirectional output voltage which is adjusted to zero, as there is no speed error. If the speed of the car exceeds the predetermined speed profile, the pulse rate applied to switch 1053 increases, which increases the relative time the switch 1053 is connected to ground, making the effective input voltage less positive and the output voltage of the filter amplifier 1054 more positive.

The output of the low pass filter amplifier 1054 is applied to comparator means 1056, such as an operational amplifier, with the output of the low pass filter 1054 being connected to the non-inverting input of the operational amplifier 1056. A reference voltage V_1 comprising a source 1058 of unidirectional voltage and a voltage divider 1060, is applied to the inverting input of operational amplifier 1056. The magnitude of the reference voltage V_1 is the magnitude which would be developed by the low pass filter when the elevator car is exceeding a selected maximum allowable speed as it approaches the terminal. Thus, when the output of the low pass filter 1054 is below the reference voltage, the output of the operational amplifier 1056 will be negative, or at the logic ZERO level. When the output of the low pass filter reaches the magnitude of the reference voltage, the output of the operational amplifier 1056 will switch to a positive polarity, or logic ONE level, which is inverted by inverter 1049, providing a low or true signal at output terminal $\overline{\text{SPSW}}$, which terminal is connected to the driver circuit 552 shown in FIG. 12. A true $\overline{\text{SPSW}}$ signal indicates an overspeed condition near a terminal.

The output of low pass filter amplifier **1054** is connected to a second comparator **1062,** which may be an operational amplifier, with the output of filter amplifier **1054** connected to the non-inverting input of operational amplifier **1062.** The inverting input of operational amplifier **1062** is connected to a reference voltage V_2 which includes a source **1064** of unidirectional potential and a voltage divider **1066.** The reference voltage V_2 applied to the operational amplifier **1062** is higher than the reference voltage V_1 applied to operational amplifier **1056,** with its magnitude being selected to represent the car speed at which an emergency stop of the elevator car should be initiated. In the event of an emergency stop, the elevator car should not be restarted until maintenance personnel have had an opportunity to check the installation. Therefore, if comparator **1062** is switched to a positive output by the output of the filter amplifier **1054** reaching the reference voltage level of comparator **1062,** a memory circuit **1068** may be triggered to retain the emergency stop signal until it is reset by maintenance personnel. A memory circuit which may be used includes a flip-flop **1070** having cross-coupled NAND gates **1072** and **1074,** an inverter and a normally open reset pushbutton **1082.** The output of comparator **1062** is applied to an input of NAND gate **1072** via inverter **1076,** the output of NAND gate **1072** is connected to an output terminal TOVSP, which is connected to emergency stop means (not shown), and an input of NAND gate **1074** is connected to ground **1080** via pushbutton **1082.**

Under normal circuit conditions, flip-flop **1070** is enabled with a logic ONE at the input of NAND gate **1074,** due to the open pushbutton, and the output of comparator **1062,** being low, applies a logic ONE to the input of NAND gate **1072** via inverter **1076.** The output terminal TOVSP is thus at the logic ZERO level. If an emergency overspeed condition is detected by comparator **1062,** switching its output positive or high, flip-flop **1070** is triggered to provide a high or true signal at output terminal TOVSP. The flip-flop will remain in this condition until pushbutton **1082** is manually actuated to reset the flip-flop **1070.**

FIGS. **20A** and **20B** are graphs which plot voltage versus time and illustrate the operation of terminal slowdown circuit **558** during a normal approach to a terminal, and during an overspeed approach, respectively. In FIG. **20A,** the square wave **1084** represents the voltage input to the filter amplifier **1054,** and the line **1086** represents the output voltage of the filter amplifier **1054.** As illustrated, the square pulses **1084,** which are the complement of the square wave output of the monostable multivibrator **1052,** are being produced by the monostable multivibrator at a constant rate, which when passed through filter **1054** provides a unidirectional signal **1086** having a magnitude of substantially zero volts. The magnitudes of the reference voltages V_1 and V_2 applied to comparators **1056** and **1062** are indicated in FIG. **20,** but the slowdown, being normal, provides a voltage **1086** which is below these reference levels.

FIG. **20B,** on the other hand, illustrates an overspeed condition near the terminal. Instead of the PLSDP pulses being generated at a predetermined constant rate, the rate is too fast, or increasing which results in the square wave input voltage to the filter amplifier, represented by curve **1084'**, being at zero or ground for successively greater periods of time. This results in a lower average input voltage, which increases the output voltage of the filter amplifier along curve **1086'**. When the overspeed condition, compared with the built in speed profile of the slowdown blade **1040,** is great enough, the output voltage of the filter amplifier **1054,** which is the speed error voltage V_{SE}, reaches the magnitude of the reference voltage V_1, which generates a true $\overline{SPSW}$ signal for driver **552.** If the overspeed condition is such that the speed error signal V_{SE} reaches the magnitude of the reference voltage V_2, the emergency terminal overspeed signal TOVSP becomes true, which is used to initiate an emergency stop of the elevator car.

An important feature of the terminal slowdown circuit **558** is the fact that the same blade **1040** which is used to monitor and detect an overspeed condition near the terminal, is also used to generate the auxiliary speed pattern when an overspeed condition is detected. The output of the low pass filter amplifier **1054** is the speed error, and while it may be applied to the motor controller, it is preferable to independently develop an auxiliary speed pattern signal TSAN, by adding the speed error voltage V_{SE} to a voltage representing the actual speed of the car, such as the output voltage of a tachometer, which may be called signal V_{TACH}. Since the speed error is equal to the speed pattern reference voltage minus the tach voltage, an auxiliary speed pattern reference voltage may be developed by adding the speed error voltage V_{SE} to the tach voltage V_{TACH}.

As illustrated in FIG. **18,** the development of an auxiliary speed reference signal TSAN is accomplished by summing the speed error voltage V_{SE} with the tach voltage V_{TACH} in a summing amplifier **1090.** Summing amplifier **1090** may be an operational amplifier having its non-inverting input connected to ground via resistor **1092,** its inverting input connected to the speed error signal and tach signal via resistors **1094** and **1096,** respectively. The tach output includes rectifier means **1098,** such as a bridge rectifier, for providing a unidirectional voltage which may be summed with the unidirectional speed error voltage V_{SE}. The tach voltage V_{TACH} is negative, i.e., tied to the negative side of the bridge **1098.** The speed error voltage V_{SE} will not exceed the tach voltage V_{TACH}, and thus the output signal TSAN will be positive.

FIG. 21

FIG. **21** is a schematic diagram of a driver circuit which may be used for the driver circuit **552** shown in block form in FIG. **12.** While it is preferable that the speed pattern signals from the different sources hereinbefore described be mixed or blended together at the transition point between the signals, as disclosed in the hereinbefore mentioned U.S. Pat. No. 3,651,892, this blending or programmed transition between signals is not essential to the present invention and the driver **552** will be described without this feature. The calibration circuit hereinbefore described relative to the distance slowdown circuit **546** insures that the distance slowdown speed pattern signal DSAN will match the hatch transducer signal HTAN at transfer, without signal mixing, and this matching of signals occurs during landing where dissimilarities in the signals being switched would be the most noticeable to the passengers. Therefore, signal mixing is not essential in order to achieve comfortable operation of the elevator system described in this application.

More specifically, driver circuit 552 includes input terminals $\overline{NL16}$, $\overline{LAZO}$, $\overline{MINA}$, START, $\overline{TOP}$, $\overline{BOTTOM}$, $\overline{SPSW}$, and DCL, and output terminals $\overline{DL2}$, $\overline{TRSW}$, $\overline{DSSW}$, $\overline{HIS}$ and $\overline{TDS}$. Input terminal $\overline{NL16}$ is connected to reversible counter 544, and, as hereinbefore described, signal $\overline{NL17}$ is low or true when the car is landing and within 16 inches of the floor at which it is to stop. Input terminal $\overline{LAZO}$ is connected to a switch in the hatchway, which switch provides a low signal when the car is within 10 inches of a floor. Input terminal $\overline{MINA}$ is connected to the time ramp generator 542, and signal $\overline{MINA}$ goes low when the car reaches maximum deceleration during the slowdown portion of a run. Input terminal START is connected to logic circuit 540. The START signal, which is the same as ACCX, is high or true when a request is made to accelerate the car, and it remains true until the car is requested to stop at a floor. The $\overline{TOP}$ and $\overline{BOTTOM}$ input terminals are connected to switches in the hatchway, which provide high signals except when the car is within 18 inches of the top and bottom terminals, respectively. Input terminal $\overline{SPSW}$ is connected to the terminal slowdown circuit 558, with the $\overline{SPSW}$ signal being high except when car overspeed is detected near a terminal. Input terminal DCL is responsive to limit switches on the car and hatch doors, with signal DCL being high when both the car and hatch doors are closed.

Output terminal $\overline{DL2}$ provides a low signal when the car is running, and a high signal when the car is landing and is in the landing zone, i.e., plus or minus 10 inches from the floor at which it is to stop.

Output signals $\overline{TRSW}$, $\overline{DSSW}$, and $\overline{HIS}$, provide low or true signals at the appropriate times during a normal run in order to switch analog switches 548, 550 and 556, respectively, shown in FIG. 12, to provide the proper speed pattern signal for each portion of a car run. Output terminal $\overline{TSD}$ provides a low signal when an overspeed condition is detected near a terminal. Output terminal $\overline{TSD}$ is connected to analog switch 560 shown in FIG. 12, and also to various circuit points in the floor selector, hereinbefore described.

Driver circuit 552 includes NAND gates 1102, 1104, 1106, 1108, 1110, 1112, 1114 and 1116, inverters 1118, 1120, 1122, 1124, 1126 and 1128, and flip-flops 1130, 1132 and 1134. Flip-flops 1130, 1132 and 1134 may each be of the cross-coupled NAND gate type, with flip-flop 1130 including NAND gates 1136 and 1138, flip-flop 1132 including NAND gates 1140 and 1142, and flip-flop 1134 including NAND gates 1144 and 1146.

Input terminal $\overline{NL16}$ is connected to an input of NAND gate 1102 via inverter 1118, and the output of gate 1102 is connected to an input of NAND gate 1136 of flip-flop 1130. Input terminal $\overline{LAZO}$ is connected to inputs of NAND gates 1102 and 1106 via inverters 1120 and 1122, respectively. The output of NAND gate 1106 is connected to an input of NAND gate 1140 of flip-flop 1132. Input terminal $\overline{MINA}$ is connected to an input of NAND gate 1144 of flip-flop 1134. The START input terminal is connected to inputs of NAND gates 1108 and 1110, with the outputs of gates 1108 and 1110 being connected to inputs of NAND gates 1138 and 1146 of flip-flops 1130 and 1134, respectively. The $\overline{TOP}$ and $\overline{BOTTOM}$ input terminals are connected to inputs of NAND gate 1104, and the output of gate 1104 is connected to an input of NAND gate 1106. The output of NAND gate 1106 is connected to an input of NAND gate 1136 of flip-flop 1130 and to an input of NAND gate 1140 of flip-flop 1132. Input terminal $\overline{SPSW}$ is connected to an input of NAND gate 1142 of flip-flop 1132. Input terminal DCL is connected to an input of NAND gate 1110. The output of NAND gate 1140 of flip-flop 1132 is connected to inputs of NAND gates 1108, 1102, 1112, 1114 and 1116, and also to output terminal $\overline{TDS}$. The output of NAND gate 1138 of flip-flop 1130 is connected to an input of NAND gate 1144 of flip-flop 1134, to output terminal $\overline{DL2}$ and an input of NAND gate 1116 via inverter 1124, and to inputs of NAND gates 1112 and 1114 via inverters 1124 and 1126. The output of NAND gate 1146 of flip-flop 1134 is connected to an input of NAND gate 1112, and via inverter 1128 to an input of NAND gate 1114. The outputs of NAND gates 1112, 1114 and 1116, are connected to output terminals $\overline{TRSW}$, $\overline{DSSW}$ and $\overline{HIS}$, respectively.

In the operation of driver circuit 552, it will be assumed that the elevator car is at the bottom terminal with the doors closed and no request to run. Signals $\overline{NL16}$, $\overline{LAZO}$, START and $\overline{BOTTOM}$ will be low, and signals $\overline{MINA}$, $\overline{TOP}$, $\overline{SPSW}$, and DCL will be high. NAND gate 1138 of flip-flop 1130 has a low output, inverted to a logic ONE by inverter 1124 to provide a high $\overline{DL2}$ signal. NAND gate 1146 of flip-flop 1134 has a low output, and NAND gate 1140 of flip-flop 1132 has a high output to provide a high $\overline{TDS}$ signal. Combining these outputs of flip-flops 1130, 1132 and 1134 in NAND gates 1112, 1114 and 1116, results in only NAND gate 1116 having two high inputs. Thus, signals $\overline{TRSW}$ and $\overline{DSSW}$ will be high and signal $\overline{HIS}$ will be low or true. Thus, the speed pattern will be under control of the hatch transducer, as required when the car is at a floor.

When a request is made to accelerate the car, signal $\overline{ACCX}$ from the floor selector 34 goes low, and logic circuit 540 of the speed pattern generator 48 generates a high START signal. When the START signal goes high, NAND gate 1108 switches to a low output, switching the output of NAND gate 1138 of flip-flop 1130 high, and providing a a low $\overline{DL2}$ signal, which corresponds to RUN. a high START signal also switches NAND gate 1110 to a low output, triggering flip-flop 1134 to provide a high output from NAND gate 1146. NAND gate 1112 now has all high inputs, providing a low $\overline{TRSW}$ signal, while NAND gate 116 now has a low input, providing a high $\overline{HIS}$ signal. The switching of signals $\overline{TRSW}$ and $\overline{HIS}$ to their low and high states, respectively, switches analog gates 548 and 556 to their closed and open conditions, respectively, transferring the speed pattern from the hatch transducer circuit 554 to the time ramp generator circuit 542.

The car thus moves away from the bottom floor under the influence of the speed pattern from the time ramp generator, and signals $\overline{NL16}$, $\overline{LAZO}$ and $\overline{BOTTOM}$ switch high.

When a request is made by the floor selector to stop the car at a floor, signal $\overline{ACCX}$ goes high and the signal START goes low. NAND gates 1108 and 1110 switch high, enabling flip-flops 1130 and 1134, respectively. Signal $\overline{TRSW}$ remains low, as the initial slowdown of the car from maximum speed to maximum deceleration remains under control of the time ramp generator.

When maximum deceleration is reached, signal $\overline{MINA}$ produced by the time ramp generator goes low, triggering flip-flop **1134** to provide a low output from NAND gate **1146**, driving NAND gate **1112** high and NAND gate **1114** low. This operates analog switches **548** and **550** shown in FIG. **12** to transfer the speed pattern from the time ramp generator **542** to the distance slowdown circuit **546**.

When the car reaches a point **16** inches from the floor at which it is going to stop, signal $\overline{NL16}$ goes low, and when the car reaches **10** inches from the floor, signal $\overline{LAZO}$ goes low, switching NAND gate **1102** to a low output and triggering flip-flop **1130** to provide low output from its NAND gate **1138**. This switches signal $\overline{DL2}$ high, corresponding to land, and it switches NAND gates **1114** and **1116** to high and low outputs, respectively. The output signal $\overline{DSSW}$ and $\overline{HIS}$ go high and low, respectively, switching analog switches **550** and **556** to connect the hatch transducer signal HTAN to the summing circuit **562**, which brings the car into the landing.

In the event an overspeed condition is detected near a terminal, terminal slowdown circuit **558** provides a $\overline{SPSW}$ signal, as hereinbefore described, which triggers flip-flop **1132** to provide a low output from NAND gate **1140**. This provides a low $\overline{TSD}$ signal for analog switch **560**, and it drives NAND gates **1112**, **1114** and **1116** high, transferring the speed pattern from conventional control to the auxiliary speed pattern signal TSAN provided by the terminal slowdown circuit **558**.

In summary there has been disclosed a new and improved speed pattern generator for elevator systems which may be used to provide a speed reference signal for a complete run, or only for certain phases thereof, depending on the maximum car speed. Signals representing maximum jerk are developed directly, and not inferentially, and the directly developed maximum jerk signals are incorporated into a time dependent speed reference pattern. Regardless of how fast the elevator control system responds, the preselected maximum jerk cannot be exceeded.

I claim as my invention.

1. A speed pattern generator for providing a jerk controlled, time dependent speed pattern signal, comprising:

first means providing a step signal switchable between first and second magnitudes representative of maximum rate of change of acceleration,

second means integrating said step signal to provide an acceleration signal,

third means integrating said acceleration signal to provide a speed pattern signal,

and fourth means for controlling the switching of said step signal in response to said acceleration signal and said speed pattern signal.

2. The speed pattern generator of claim **1** wherein the fourth means switches the step signal to a predetermined one of its first and second magnitudes during predetermined transitions between constant speed and constant acceleration portions of the speed pattern signal, and switches back and forth between the first and second magnitudes during portions of the speed pattern which provide constant parameters.

3. The speed pattern generator of claim **1** wherein the first and second magnitudes of the step signal provide first and second currents of opposite polarity.

4. The speed pattern generator of claim **3** wherein the fourth means controls the switching of the step signal to average the first and second currents to zero during the portions of the speed pattern which represent constant parameters.

5. The speed pattern generator of claim **1** wherein the fourth means includes acceleration and speed feedback loops connected to be responsive to the second and third means, respectively.

6. The speed pattern generator of claim **5** including means interconnecting the acceleration and speed feedback loops, such that the signal in the acceleration feedback loop modifies the signal in the speed feedback loop.

7. The speed pattern generator of claim **6** wherein the acceleration and speed feedback loops each include means providing reference signals, and comparator means which com-pares the feedback signal with a reference signal, and wherein the acceleration feedback signal modifies the speed feedback signal to reduce the time required for the speed feedback signal to reach the level of its reference signal.

8. The speed pattern generator of claim **1** wherein the fourth means includes acceleration reference and speed reference signals, acceleration and speed comparator means for comparing said acceleration reference and speed reference signals with the acceleration and speed pattern signals, respectively, and means for switching the step signal in response to said acceleration and speed comparator means

9. The speed pattern generator of claim **8** wherein the speed pattern is initiated by a change in the magnitude of the speed reference signal from a first to a second magnitude.

10. The speed pattern generator of claim **9** wherein the speed pattern includes a slowdown phase, with the slowdown phase of the speed pattern being initiated by a change in the magnitude of the speed reference signal from its second to its first magnitude.

11. The speed pattern generator of claim **8** wherein the speed pattern signal includes a zero speed phase, a jerk controlled first transition phase, and a constant acceleration phase, with the first transition phase being initiated by a change in the magnitude of the speed reference signal and terminated by the acceleration comparator means when the acceleration signal reaches the level of the acceleration referenc.

12. The speed pattern generator of claim **8** wherein the speed pattern signal includes a constant acceleration phase, a jerk controlled second transition phase, and a constant spee phase, and including means modifying the speed pattern signal applied to the speed comparator means with the acceleration signal, to cause the modified speed signal to reach thelevel of the reference signal earlier than would the unmodified speed signal, to enable the second transition phase to interconnect the constant acceleration and constant speed phases without overshoot.

13. The speed pattern generator of claim **8** wherein the speed pattern signal includes a constant speed phase, a jerk controlled their transition phase, and a constant deceleration phase, and wherein the comparator means includes a deceleration comparator, with the third transition phase being initiated by a change in the magnitude of the speed reference signal and terminated by the deceleration comparator when the acceleration signal reaches the level of the acceleration reference.

14. The speed pattern generator of claim 8 wherein the speed pattern signal includes a constant deceleration phase, a jerk controlled fourth transition phase, and a zero speed phase, and including means modifying the speed pattern signal applied to the speed comparator means with the acceleration signal, to cause the modified speed signal to reach the level of the reference signal earlier than would the unmodified speed signal, to enable the fourth transition phase to smoothly interconnect the constant deceleration and zero speed phases.

15. A speed pattern generator for providing a jerk controlled, time dependent speed pattern signal for elevator motor control which controls the travel of an elevator car relative to a structure, comprising:

first means providing a step signal switchable between first and second magnitudes representing maximum jerk,

second means integrating said step signal to pro-vide an acceleration signal,

third means integrating said acceleration signal to provide a speed pattern signal,

a speed feedback loop responsive to the speed pattern signal for providing a speed feedback signal, said speed feedback loop including speed reference means switchable between predetermined magnitudes, and speed comparator means connected to compare the speed feedback and speed reference signals and provide an output indicative of their relationship,

an acceleration feedback loop responsive to the acceleration signal for providing an acceleration feedback signal, said acceleration feedback loop including acceleration reference means, and first acceleration comparator means connected to compare the acceleration feedback signal and acceleration reference signal and provide an output indicative of their relationship,

logic means providing output signals responsive to the outputs of said speed and acceleration comparators,

and switching means connected to said logic means and said first means, switching the step signal to a selected magnitude in response to the output signal of the logic means during transitions between constant speed and constant acceleration to limit jerk during such transitions, and switching the step signal between its magnitudes at a rate which exceeds the response time of the elevator car, to maintain predetermined constant parameters during portions of the speed pattern when such parameters are to be kept constant.

16. The speed pattern generator of claim 15 including means modifying the speed feedback signal with the acceleration feedback signal, to reduce the time required for the speed feedback signal to reach the selected magnitude of the speed reference, and provide a jerk limited transition from a constant acceleration phase of the speed pattern to a constant speed phase without overshoot.

17. The speed pattern generator of claim 15 wherein the speed pattern signal includes acceleration and deceleration phases, the acceleration signal is of one polarity during the acceleration phase, and of the opposite polarity during the deceleration phase, and including second acceleration comparator means in the acceleration feedback loop connected to compare the deceleration signal with the acceleration reference signal and provide an output indicative of their relationship, and means connecting the output of said second acceleration comparator means to the logic means.

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