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(54) **Title**: A VARIABLE FREQUENCY RC OSCILLATOR

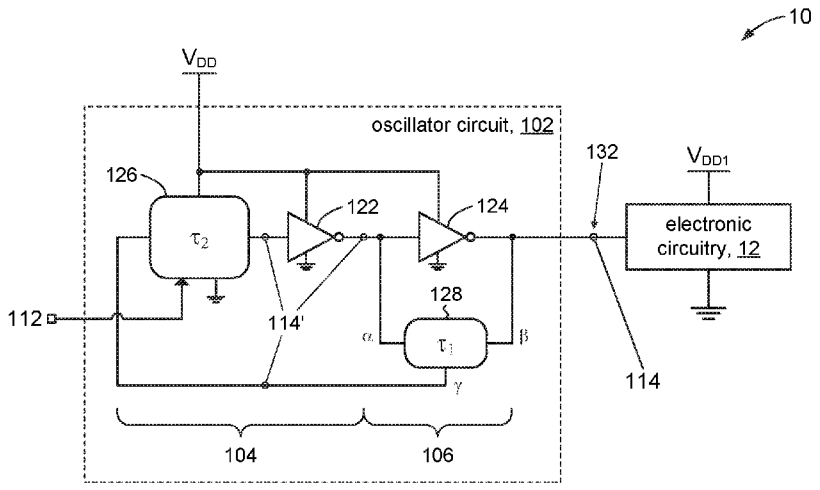


Fig. 1A

(57) **Abstract**: An oscillator circuit having a programmable output frequency may include a first delay section having a negative gain and a variable delay that is set by a control signal provided to the first delay section. A second delay section having a negative gain and a fixed delay may be connected in series with the first delay section. The oscillator circuit may include an output comprising the output of the second delay section having a frequency that is dependent on the delay of the first delay section and the delay of second delay section.

WO 2017/151295 A1

A VARIABLE FREQUENCY RC OSCILLATOR

CROSS REFERENCE TO RELATED APPLICATIONS

[0001] Pursuant to 35 U.S.C. §119(e), this application is entitled to and claims the benefit of the filing date of U.S. Provisional App. No. 62/302,735 filed March 2, 2016, the content of which is incorporated herein by reference in its entirety for all purposes.

TECHNICAL FIELD

[0002] The present disclosure relates generally to oscillators, and more particularly to an RC oscillator having a variable frequency.

BACKGROUND

[0003] In the design of digital logic circuits, large scale integration techniques have brought about the construction of large numbers of components being fabricated on a single chip of silicon. Digital circuitry typically require various clock signals to provide a time base for their operation. Such clock signals are generated by oscillator circuits, which come in a variety of designs. One such design is based on a resistor/capacitor (RC) network, referred to as an RC oscillator.

[0004] Conventional RC oscillators can provide a low-cost timing source. Furthermore, conventional RC oscillators avoid the use of inductors (see, for example, FIG. 5), which can be difficult to fabricate on integrated circuits. RC oscillators may allow for generation of variable frequencies by changing the resistance R, or capacitance C to increase their utility.

SUMMARY

[0005] In accordance with aspects of the present disclosure, an oscillator circuit having a programmable output frequency may comprise a first delay section having an input end and an output end. The first delay section may have a negative gain between the input end and the output end and a variable delay that is set by a control signal provided to the first delay section. The oscillator may further comprise a second delay section electrically connected in series with the first delay section. The second delay section may have an input end and an output end and a negative gain between the input end and the output end. The second delay section may have a fixed delay. The oscillator may further comprise a circuit output for an output signal having a

frequency that is a function of the delay due to the first delay section and the second delay section. The circuit output may comprise the output end of the second delay section.

[0006] In some embodiments, the first delay section may include a first RC network comprising a resistor and a variable capacitor, and a second RC network connected in series with the first RC network and also comprising a resistor and a variable capacitor. A delay of the first delay section may be determined based on capacitances of the variable capacitors of the first and second RC networks. The control signal may set the capacitance of the variable capacitor of the first RC network, and an additional control signal may set the capacitance of the variable capacitor of the second RC network.

[0007] In some embodiments, the first delay section may include an RC network comprising a resistor and a variable capacitor. The control signal provided to the first delay section may set a capacitance of the variable capacitor of the first RC network. A delay of the first delay section may be based on the capacitance of the variable capacitor.

[0008] In some embodiments, the first delay section may include a plurality of switched capacitors, wherein the control signal selectively sets each of the plurality of switched capacitors to an ON state or an OFF state. In some embodiments, when a switched capacitor is in the ON state, the switched capacitor has a node electrically connected to a DC voltage. In other embodiments, when a switched capacitor is in the ON state, the switched capacitor has a node electrically connected to ground potential. The control signal may be an n-bit word.

[0009] In some embodiments, the second delay section may include an RC network comprising a fixed value resistive component and a fixed value capacitive component. At least one node of the fixed value capacitive component may swing above supply voltage of the oscillator circuit. In some embodiments, the at least one node of the fixed value capacitive component may swing below ground potential.

[0010] In some embodiments, the first delay section may be electrically connected to the circuit output via the second delay section in a feedback loop.

[0011] In accordance with aspects of the present disclosure, an oscillator circuit may comprise a first delay section having an input end and an output end. The first delay section may have a

negative gain between the input end and the output end. The first delay section may include a first RC network comprising a resistor and a variable capacitor and a second RC network connected in series with the first RC network and comprising a resistor and a variable capacitor. The oscillator circuit may include at least one control signal provided to at least the variable capacitor of the first RC network to set a delay of the first delay section. The oscillator circuit may include a second delay section electrically connected in series with the first delay section. The second delay section may have an input end and an output end, and a negative gain between the input end and the output end. The second delay section may have a fixed delay. The oscillator circuit may include a circuit output for an output signal having a frequency that is a function of the delay due to the first delay section and the second delay section. The circuit output may comprise the output end of the second delay section.

[0012] In some embodiments, each of the variable capacitors in the first and second RC networks in the first delay section may comprise a plurality of switched capacitors, wherein the control signal provided to the programmable delay stage selectively sets each of the plurality of switched capacitors to an ON state or an OFF state. In some embodiments, when a switched capacitor is in the ON state, a node of the switched capacitor is electrically connected to a DC voltage. In other embodiments, when a switched capacitor is in the ON state, a node of the switched capacitor is electrically connected to ground potential.

[0013] In some embodiments, the control signal may be provided to the variable capacitor in the first RC network. The oscillator circuit may further include an additional control signal provided to the variable capacitor in the second RC network.

[0014] In some embodiments, the first delay section may further comprise at least a third RC network connected in series with the second RC network and comprising a resistor and a variable capacitor.

[0015] In some embodiments, the second delay section may comprise an RC network comprising a fixed value resistive component and a fixed value capacitive component,. At least one node of the capacitive component may swings above supply voltage of the oscillator circuit. The at least one node of the capacitive component may further swing below ground potential.

[0016] In accordance with aspects of the present disclosure, an oscillator circuit may comprise a first inverter stage and a second inverter stage having an input electrically connected to an output of the first inverter stage. The second inverter stage may have an output for an output signal of the oscillator circuit. The oscillator circuit may comprise an RC circuit comprising a resistor element connected to a capacitive element. The RC circuit may be electrically connected between the input and output of the second inverter stage. The oscillator circuit may comprise at least one variable delay stage having a delay that is set by a control signal provided to the at least one variable delay stage. The at least one variable delay stage may be electrically connected between a node in the RC circuit that connects the resistor element and the capacitor element and an input of the first inverter stage. A frequency of the output signal may be dependent on a delay of the at least one variable delay stage.

[0017] In some embodiments, the oscillator circuit may further comprise at least one additional variable delay stage connected in series with the at least one variable delay stage, and having a delay that is dependent on a control signal provided to the at least one additional variable delay stage.

[0018] In some embodiments, a voltage level at the node that connects the resistor element and the capacitor element may swings above and below a supply voltage of the oscillator circuit and above and below a ground potential during operation of the oscillator circuit.

[0019] In some embodiments, the at least one variable delay stage may comprise a resistor and a variable capacitor, wherein the control signal provided to the at least one variable delay stage sets a capacitance of the variable capacitor. The delay of the at least one variable delay stage may be dependent on the capacitance of the variable capacitor.

[0020] In some embodiments, the at least one variable delay stage may comprise a plurality of switched capacitors, wherein the control signal sets each of the plurality of switched capacitors to an ON state or an OFF state. In some embodiments, when a switched capacitor is in the ON state, a node of the switched capacitor is electrically connected to a DC voltage or to ground potential.

[0021] In some embodiments, at least one node of the capacitive element of the RC circuit swings above supply voltage of the oscillator circuit and below ground potential.

[0022] The following detailed description and accompanying drawings provide a better understanding of the nature and advantages of the present disclosure.

BRIEF DESCRIPTION OF THE DRAWINGS

[0023] With respect to the discussion to follow and in particular to the drawings, it is stressed that the particulars shown represent examples for purposes of illustrative discussion, and are presented in the cause of providing a description of principles and conceptual aspects of the present disclosure. In this regard, no attempt is made to show implementation details beyond what is needed for a fundamental understanding of the present disclosure. The discussion to follow, in conjunction with the drawings, makes apparent to those of skill in the art how embodiments in accordance with the present disclosure may be practiced. Similar or same reference numbers may be used to identify or otherwise refer to similar or same elements in the various drawings and supporting descriptions. In the accompanying drawings:

[0024] FIGs. 1A and 1B show oscillator circuits in accordance with the present disclosure.

[0025] FIG. 2 shows an oscillator circuit in accordance with the present disclosure.

[0026] FIG. 2A shows details of a variable capacitor in accordance with the present disclosure.

[0027] FIG. 3 shows an oscillator circuit in accordance with the present disclosure.

[0028] FIG. 3A shows details of a variable capacitor in accordance with the present disclosure.

[0029] FIGs. 4A and 4B illustrate alternate embodiments in accordance with the present disclosure.

[0030] FIG. 5 shows an example of a conventional RC oscillator.

DETAILED DESCRIPTION

[0031] In the following description, for purposes of explanation, numerous examples and specific details are set forth in order to provide a thorough understanding of the present disclosure. It will be evident, however, to one skilled in the art that the present disclosure as expressed in the claims may include some or all of the features in these examples, alone or in combination with other features described below, and may further include modifications and equivalents of the features and concepts described herein.

[0032] FIG. 1A shows an electronic circuit 10 in accordance with an embodiment of the present disclosure. The electronic circuit 10 may include an oscillator circuit 102 and electronic circuitry 12. The oscillator circuit 102 may have an output 114 for an output signal (e.g., a clock signal 132), which for example, may be used by the electronic circuitry 12. The electronic circuit 10 may be a component in an electronic device (not shown). The oscillator circuit 102 may be powered by a source V_{DD} and the electronic circuitry 12 may be powered by a source V_{DD1}. In some embodiments, V_{DD} may be the same as V_{DD1}, and in other embodiments V_{DD} may be different from V_{DD1}.

[0033] The oscillator 102 may comprise a first delay section 104 and a second delay section 106 electrically connected in series with the first delay section 104. In accordance with the present disclosure, the first delay section 104 may be characterized by a negative gain between the input end of the first delay section 104 and the output end of the first delay section 104. With reference to FIG. 1A, for example, in some embodiments the first delay section 104 may include a delay stage 126 connected in series with an inversion stage 122. As discussed in more detail below, the first delay section 104 may be further characterized by having a variable delay. Further, by negative gain, we mean that a given positive change (say of the voltage) at the input end produces a negative change (of the voltage) at the output end.

[0034] The input end of the first delay section 104 may be defined by the input side of delay stage 126. The output end of the first delay section 104 may be defined by the output of the inversion stage 122. It will be clear from the discussion below that the gain of delay stage 126 is positive. The inversion stage 122 has a negative gain, and so the first delay section 104 has a negative gain. In some embodiments, the inversion stage 122 may comprise a single inverter as shown in FIG. 1A. In other embodiments, the inversion stage 122 may comprise any odd number of inverters, and in general any suitable circuitry that can provide a negative gain.

[0035] The second delay section 106 may likewise be characterized by a negative gain between its input end and its output end. In some embodiments, the second delay section 106 may include an inversion stage 124 connected across (in parallel with) a delay stage 128; for example, at terminals α and β of delay stage 128. The input and output ends of the second delay section 106 may be the input and output, respectively, of the inversion stage 124. The inversion

stage 124 has a negative gain, and so the second delay section 106 has a negative gain. In some embodiments, the inversion stage 124 may comprise a single inverter as shown in FIG. 1A. In other embodiments, the inversion stage 124 may comprise any odd number of inverters, and in general any suitable circuitry that can provide a negative gain.

[0036] The first delay section 104 may be connected to the output 114 via the second delay section 106 to define a feedback loop around which oscillations can propagate to produce the clock signal 132. The frequency f_{CLOCK} of the clock signal 132 is generally a function of the delay τ_1 of the delay stage 128 and the delay τ_2 of the delay stage 126. The clock signal 132 may be tapped out or otherwise produced at the output of the second inversion stage 124, as depicted in FIG. 1A. However, it is understood that the clock signal 132 may be obtained at other points 114' within the loop.

[0037] Referring to FIG. 1B, in some embodiments the delay stage 128 may comprise an RC network comprising a resistor R and a capacitor C. Terminal α of the delay stage 128 may be connected to the resistor R and capacitor C may be connected to terminal β. Terminal γ of the delay stage 128 may be connected to a node V_X to which resistor R and capacitor C are connected. The delay τ_1 of the RC network is generally a function of a time constant (sometimes referred to as the RC time constant) defined as $R \times C$, which represent respective element values of resistor R and capacitor C. In some embodiments, resistor R and capacitor C may be fixed-value elements. Accordingly, the delay stage 128 may provide a fixed delay.

[0038] It is noted that node V_X is not connected to ground potential, as compared to other elements in the oscillator circuit 102 (e.g., inversion stages 122, 124, delay stage 126). Rather, node V_X is a "floating" node, which means that the potential at node V_X may vary as the voltage across capacitor C varies during operation of the oscillator circuit 102. For example, during operation the voltage at node V_X may swing above and below the supply voltage in one half of a cycle of the clock signal 132 at the output 114, and may swing above and below ground potential in the other half of the cycle. This aspect of the present disclosure is discussed below.

[0039] Returning to FIG. 1A, in accordance with some embodiments, the delay stage 126 may have a variable (tunable, programmable) delay. The delay stage 126 may receive a selector input signal 112 to select or otherwise set the delay τ_2 of the delay stage 126. In some embodiments,

the selector input 112 may be a digital code. In accordance with the present disclosure, the selector input 112 may change in order to select a different delay τ_2 for the delay stage 126 during operation of the electronic circuit 10. For example, the selector input 112 may provide different digital codes to the delay stage 126, thus allowing for on-the-fly selection of a delay τ_2.

[0040] The frequency of oscillation in oscillator circuit 102 may be controlled according to the delays τ_1 and τ_2. The delay τ_1 may be determined, for example, during the design phase by selecting appropriate element values for resistor R and capacitor C in the delay stage 128. The delay of τ_2 may be set by providing a suitable selector input 112 to the delay stage 126. Since the delay τ_2 of the delay stage 126 may be set on-the-fly, the frequency of clock signal 132 produced by oscillator circuit 102 may likewise be set on-the-fly, namely by providing a suitable selector input 112 to the delay stage 126.

[0041] FIG. 2 shows additional details for delay stage 126 of the first delay section 104 in accordance with some embodiments of the present disclosure. In some embodiments, for example, the delay stage 126 may comprise a high input impedance non-inverting input buffer 202 and a variable RC network 204. The supply (not shown) for input buffer 202 may be the V_{DD} supply provided to the delay stage 126, as illustrated in FIG. 1A for example.

[0042] The variable RC network 204 may comprise a resistor R_1 and a variable capacitor C_1. The selector input 112 may be an n-bit signal bus that can be provided to the variable capacitor C_1 to select or otherwise set a capacitance for the variable capacitor C_1. The delay τ_2 of delay stage 126 may be determined based on a time constant defined as $R \times C$, which are respective values of resistor R_1 and variable capacitor C_1. The delay τ_2 may therefore be set depending on the capacitance setting of variable capacitor C_1.

[0043] One of ordinary skill will appreciate that any suitable delay circuitry may be used for the delay stage 126. Merely to illustrate the point, in other embodiments for example, the delay stage 126 may employ a tunable current source to charge a fixed capacitor. The delay stage 126 may use a current starved inverter with a tunable current source and/or a tunable capacitor, and so on.

[0044] FIG. 2A shows additional details of the variable capacitor C_1. In accordance with some embodiments, the variable capacitor C_1 may include a set of *n* fixed value switched capacitive elements C_x. The capacitive elements C_x may be connected in parallel with each other. For example, each capacitive element C_x may have a connection between resistor R_1 and a ground potential connection via a corresponding switch $M_0 - M_{n-1}$. It will be appreciated that in other embodiments, the capacitive elements C_x may be arranged in connection topologies other than in parallel.

[0045] The capacitive elements C_x may be realized using any semiconductor technology suitable for a given application of the oscillator circuit 102. Merely to illustrate this point, in various embodiments, capacitive elements C_x may be PN junction capacitors, MOSFET gate capacitors, metal-insulator-metal (MIM) capacitors, metal-oxide-metal (MOM) capacitors, and so on. The capacitive elements C_x may be based on the same semiconductor technology, or they may be based on different technologies. In some embodiments, each of the capacitive elements C_x may have the same capacitance. In other embodiments, the capacitive elements C_x may have different capacitances.

[0046] The capacitive elements C_x may be selectively switched to ground potential via a set of corresponding switches $M_0 - M_{n-1}$. The switches $M_0 - M_{n-1}$ may be any suitable switching device. In some embodiments, for example, the switches $M_0 - M_{n-1}$ may be semiconductor switches such as NMOS transistors shown in FIG. 2A, for instance; although in other embodiments other transistor technologies or designs may be used, such as NFETs for example. In some embodiments, all the switches $M_0 - M_{n-1}$ may be based on the same technology, or they may be based on several different technologies. Each of the *n* signal lines that comprise the selector input 112 may be connected to a respective one of the switches $M_0 - M_{n-1}$. For example, in FIG. 2A, each signal line of the selector input 112 is connected to a respective gate terminal of the switches $M_0 - M_{n-1}$. The input to selector input 112 may be generated by digital logic or other suitable circuitry associated with the oscillator circuit 102 or with electronic circuit 10 (FIG. 1A).

[0047] In accordance with the present disclosure, the nodes of capacitive elements C_x in FIG. 2A are not floating nodes as explained above in connection with node V_X. Rather, in some embodiments, the nodes of capacitive elements C_x may be electrically connected to or otherwise

referenced to ground potential. In other embodiments, the capacitive elements C_x may be electrically connected to or otherwise referenced to a DC voltage; e.g., a supply voltage such as V_{DD}. More generally, one of skill in the art will appreciate that the capacitive elements C_x may be electrically connected to any suitable low impedance node.

[0048] In operation, any one or more of the *n* signal lines in the selector input 112 may be asserted to turn ON their corresponding switches $M_0 - M_{n-1}$, and hence the corresponding capacitive element C_x. A switch (e.g., M_0) that is in the ON state connects its corresponding capacitive element C_x to the RC network 204 (switched on), and conversely a switch that is in the OFF state disconnects its corresponding capacitive element C_x from the RC network 204 (switched off). If the capacitive elements C_x are connected in parallel, as shown in FIG. 2A for example, the capacitance of variable capacitor C_1 may be computed as the sum of the switched-on capacitive elements. Thus, the delay τ_2 of the delay stage 126 may be set depending on which capacitive elements are switched on or switched off in the RC network 204.

[0049] In some embodiments, resistor R_1 may be a fixed value element such as shown in FIG. 2A. In other embodiments (not shown), resistor R_1 may be a variable resistor and capacitor C_1 may be a fixed value element. In still other embodiments, resistor R_1 may be a variable resistor and capacitor C_1 may be a variable capacitor.

[0050] Referring to FIG. 3, in some embodiments in accordance with the present disclosure the first delay section 104 may comprise an additional delay stage 326 connected in series with the delay stage 126. An input inverter 322 may be provided to couple the oscillations produced at the output of delay stage 126 to the input of the additional delay stage 326; in other words, the inverter 322 keeps the oscillations going. An output inverter 324 may be provided to maintain a net negative gain between the input end and the output end of the first delay section 104. The supply (not shown) for input inverter 322 and output inverter 324 may be the same V_{DD} supply provided to the delay stage 126, as illustrated in FIG. 1A for example. In some embodiments, the additional delay stage 326 can improve the noise performance of oscillator circuit 102.

[0051] The additional delay stage 326 may include a variable RC network 304 comprising a resistor R_2 and a variable capacitor C_2. A selector input 312 may comprise an m-bit signal bus that can be provided to the variable capacitor C_2 to select or otherwise set a capacitance for the

variable capacitor C_2. The additional delay stage 326 may provide a delay τ_3 that may be determined based on a time constant defined as $R \times C$, which are respective values of resistor R_2 and variable capacitor C_2. The delay τ_3 provided by additional delay stage 326 may therefore be set depending on the capacitance setting of variable capacitor C_2.

[0052] FIG. 3A shows additional details of the variable capacitor C_2. In accordance with some embodiments, variable capacitor C_2 may comprise a set of m fixed value switched capacitive elements C_y. The capacitive elements C_y may be connected in parallel with each other. In other words, each capacitive element C_y may have a connection between resistor R_2 and a ground potential connection via a corresponding switch $M_0 - M_{m-1}$. It will be appreciated that in other embodiments, the capacitive elements C_y may be connected in connection topologies other than in parallel.

[0053] The capacitive elements C_y may be realized using any semiconductor technology suitable for a given application of the oscillator circuit 102. Merely to illustrate this point, in various embodiments, capacitive elements C_y may be PN junction capacitors, MOSFET gate capacitors, metal-insulator-metal (MIM) capacitors, metal-oxide-metal (MOM) capacitors, and so on. The capacitive elements C_y may be based on the same semiconductor technology, or they may be based on different technologies. In some embodiments, each of the capacitive elements C_y may have the same capacitance. In other embodiments, the capacitive elements C_y may different capacitances.

[0054] The capacitive elements C_y may be selectively switched to ground potential via a set of corresponding switches $M_0 - M_{m-1}$. The switches $M_0 - M_{m-1}$ may be any suitable switching device. In some embodiments, for example, the switches $M_0 - M_{m-1}$ may be semiconductor switches such as PNP transistors shown in FIG. 3A, for example. In some embodiments, all the switches $M_0 - M_{m-1}$ may be based on the same technology, or may they may be based on different technologies. Each of the m signal lines that comprise the selector input 312 may be connected to a respective one of the switches $M_0 - M_{m-1}$. The input to selector input 312 may be generated by digital logic or other suitable circuitry associated with the oscillator circuit 102 or with electronic circuit 10 (FIG. 1A).

[0055] In accordance with the present disclosure, the nodes of capacitive elements C_y in FIG. 3A are not floating. Rather, the nodes of capacitive elements C_y may be electrically connected to ground potential. One of skill in the art will appreciate that in other embodiments, the capacitive elements C_y may be electrically connected to a DC voltage; (e.g., supply V_{DD}). More generally, the capacitive elements C_y may be electrically connected to any suitable low impedance node.

[0056] In operation, any one or more of the m signal lines in the selector input 312 may be asserted to turn ON their corresponding switches $M_0 - M_{m-1}$. A switch (e.g., M_0) that is in the ON state connects its corresponding capacitive element (switched on) to the RC network 304, and conversely a switch that is in the OFF state disconnects its corresponding capacitive element (switched off) from the RC network 304. If the capacitive elements C_y are connected in parallel, as shown in FIG. 3A for example, the capacitance of variable capacitor C_2 may be computed as the sum of the switched-on capacitive elements. Thus, the delay τ_3 of the additional delay stage 326 may be set depending on which capacitive elements C_y are switched on or switched off in the RC network 304.

[0057] In some embodiments, resistor R_2 may be a fixed value element such as shown in FIG. 3A. In other embodiments (not shown), resistor R_2 may be a variable resistor and capacitor C_2 may be a fixed value element. In still other embodiments (not shown), resistor R_2 may be a variable resistor and capacitor C_2 may be a variable capacitor.

[0058] In some embodiments, the selector inputs 112, 312 of respective delay stages 126, 326 may receive the same selection input; e.g., the same n-bit code may be provided to each selector input 112, 312. In other embodiments, each selector input 112, 312 may receive different selection inputs.

[0059] The frequency of oscillation in oscillator circuit 102 may be controlled according to the delays τ_1, τ_2, and τ_3. As explained above, the delay τ_1 in delay stage 128 may be fixed for resistor R and capacitor C. The delay τ_2 of the delay stage 126 may be set by asserting appropriate bit lines that comprise selector input 112 for the delay stage 126. Likewise, the delay τ_3 in delay stage 326 may be set by asserting appropriate bit lines that comprise selector signal 312. Accordingly, the frequency of the clock signal 132 may be selected as a function of the variable delays τ_2 and τ_3.

[0060] In some embodiments in accordance with the present disclosure, the first delay section 104 may comprise several additional delay stages connected in series. FIG. 4A, for example, is a schematic representation of an oscillator circuit 102a in accordance with some embodiments of the present disclosure. The first delay section 104 may comprise delay stage 126 and two additional delay stages 426a, 426b. Inverters 422a, 422b may be provided to couple the signal between delay stages. For example, inverter 422a may couple the signal between delay stage 126 and delay stage 422a, and likewise inverter 422b may couple the signal between delay stage 422a and delay stage 422b. Note that inverters 422a, 422b, 122 that comprise the first delay section 104 provide a net negative gain.

[0061] FIG. 4B is a schematic representation of an oscillator circuit 102b comprising a first delay section 102 that has three additional delay stages 426a, 426b, 426c and inverters 422a, 422b, 422c, 422d. The inverters 422a – 422c couple the signal among delay stages 126 and 426 – 426c. It can be seen that the inverter 424 provides the first delay section 104 with a net negative gain.

Technical Effect and Advantages

[0062] A conventional RC oscillator design, such as shown in FIG. 5, has many desirable properties. Such designs are generally insensitive to variations in supply voltage. The design is relatively simple, having few components. As a results these RC oscillators can achieve low noise performance. Some designs, for example, may achieve noise levels only 3dB above the theoretical low limit. Because of their relatively simple designs, RC oscillators have smaller footprints on the IC chip.

[0063] The present disclosure provides an oscillator circuit having the capability of a programmable frequency to further improve the utility of RC oscillators. As shown in FIG. 5, for example, a basic RC oscillator design comprises two inverters (e.g., inversion stages 122, 124) and an RC network comprising a resistor R and a capacitor C. The RC network provides a delay that sets an operating frequency of the RC oscillator. Accordingly, varying the elements values of either R or C can serve to provide programmability in the operating frequency of the RC oscillator.

[0064] However, the method of making R or C may not be practical. Programmable resistors can be difficult to provide. High programmability requires the ability to modify the total R in small increments. This necessitates a large network of resistors and a large number of switches that have low ON resistance. Furthermore, the voltage across a switch can vary over the oscillation cycle thereby complicating the switch design. Using switched resistors to build a variable resistor may not practical.

[0065] Programmable capacitors can be difficult, since the capacitor C is a "floating" capacitor because of the behavior at node V_X. As explained above, the node V_X is a floating node because the voltage at node V_X may swing above and below the supply voltage in one half of a cycle of the output and above and below ground potential in the other half of the cycle. Programmable capacitors typically comprise a bank of switched capacitor elements. When the source (or drain) of a switch is connected at the node V_X, the state of the switch can become forward biased during portions of the cycle and conduct when it is supposed to be in an OFF (non-conducting) state. The presence of the floating node V_X presents a challenge in using a variable capacitor at this location to provide a variable delay RC network and hence a variable frequency oscillator circuit. Thus, replacing C with a bank of switched capacitors to build a variable capacitor may not be easily accomplished.

[0066] Oscillator circuits in accordance with the present disclosure can overcome this challenge. As shown in FIG. 1B, a delay stage 126 can be provided separately from the RC network 128. The delay stage 126 may be grounded so that operation of the delay stage 126 is significantly less affected by voltage swings in the circuit.

[0067] The above description illustrates various embodiments of the present disclosure along with examples of how aspects of the particular embodiments may be implemented. The above examples should not be deemed to be the only embodiments, and are presented to illustrate the flexibility and advantages of the particular embodiments as defined by the following claims. Based on the above disclosure and the following claims, other arrangements, embodiments, implementations and equivalents may be employed without departing from the scope of the present disclosure as defined by the claims.

CLAIMS

What is claimed is:

1. An oscillator circuit having a programmable output frequency comprising:

a first delay section having an input end and an output end, the first delay section having a negative gain between the input end and the output end, the first delay section having a variable delay that is set by a control signal provided to the first delay section;

a second delay section electrically connected in series with the first delay section, the second delay section having an input end and an output end, the second delay section having a negative gain between the input end and the output end, the second delay section having a fixed delay; and

a circuit output for an output signal having a frequency that is a function of the delay due to the first delay section and the second delay section, the circuit output comprising the output end of the second delay section.

2. The circuit of claim 1, wherein the first delay section comprises: a first RC network comprising a resistor and a variable capacitor; and a second RC network connected in series with the first RC network and comprising a resistor and a variable capacitor, a delay of the first delay section determined based on capacitances of the variable capacitors of the first and second RC networks.

3. The circuit of claim 2 wherein the control signal sets the capacitance of the variable capacitor of the first RC network, and an additional control signal sets the capacitance of the variable capacitor of the second RC network.

4. The circuit of claim 1, wherein the first delay section comprises an RC network comprising a resistor and a variable capacitor, wherein the control signal provided to the first delay section sets a capacitance of the variable capacitor of the first RC network, a delay of the first delay section determined based on the capacitance of the variable capacitor.

5. The circuit of claim 1, wherein the first delay section comprises a plurality of switched capacitors, wherein the control signal selectively sets each of the plurality of switched capacitors to an ON state or an OFF state.

6. The circuit of claim 5, wherein when a switched capacitor is in the ON state, the switched capacitor has a node electrically connected to a DC voltage.

7. The circuit of claim 5, wherein when a switched capacitor is in the ON state, the switched capacitor has a node electrically connected to ground potential.

8. The circuit of claim 5, wherein the control signal is an n-bit word.

9. The circuit of claim 1, wherein the second delay section comprises an RC network comprising a fixed value resistive component and a fixed value capacitive component.

10. The circuit of claim 9, wherein at least one node of the fixed value capacitive component swings above supply voltage of the oscillator circuit.

11. The circuit of claim 10, wherein the at least one node of the fixed value capacitive component swings below ground potential.

12. The circuit of claim 1, wherein the first delay section is electrically connected to the circuit output via the second delay section in a feedback loop.

13. An oscillator circuit comprising:

a first delay section having an input end and an output end, the first delay section having a negative gain between the input end and the output end, the first delay section comprising a first RC network comprising a resistor and a variable capacitor and a second RC network connected in series with the first RC network and comprising a resistor and a variable capacitor;

at least one control signal provided to at least the variable capacitor of the first RC network to set a delay of the first delay section;

a second delay section electrically connected in series with the first delay section, the second delay section having an input end and an output end, second delay section having a negative gain between the input end and the output end, the second delay section having a fixed delay; and

a circuit output for an output signal having a frequency that is a function of the delay due to the first delay section and the second delay section, the circuit output comprising the output end of the second delay section.

14. The circuit of claim 13, wherein each of the variable capacitors in the first and second RC networks in the first delay section comprises a plurality of switched capacitors, wherein the control signal provided to the programmable delay stage selectively sets each of the plurality of switched capacitors to an ON state or an OFF state.

15. The circuit of claim 14, wherein when a switched capacitor is in the ON state, a node of the switched capacitor is electrically connected to a DC voltage.

16. The circuit of claim 14, wherein when a switched capacitor is in the ON state, a node of the switched capacitor is electrically connected to ground potential.

17. The circuit of claim 13, wherein the control signal is provided to the variable capacitor in the first RC network, the circuit further comprising an additional control signal provided to the variable capacitor in the second RC network.

18. The circuit of claim 13, wherein the first delay section further comprises at least a third RC network connected in series with the second RC network and comprising a resistor and a variable capacitor.

19. The circuit of claim 13, wherein the second delay section comprises an RC network comprising a fixed value resistive component and a fixed value capacitive component, wherein at least one node of the capacitive component swings above supply voltage of the oscillator circuit.

20. The circuit of claim 19, wherein the at least one node of the capacitive component swings below ground potential.

21. An oscillator circuit comprising:

a first inverter stage;

a second inverter stage having an input electrically connected to an output of the first inverter stage, the second inverter stage having an output for an output signal of the oscillator circuit;

an RC circuit comprising a resistor element connected to a capacitive element, the RC

circuit electrically connected between the input and output of the second inverter stage; and

at least one variable delay stage having a delay that is set by a control signal provided to the at least one variable delay stage, the at least one variable delay stage electrically connected between a node in the RC circuit that connects the resistor element and the capacitor element and an input of the first inverter stage,

a frequency of the output signal being dependent on a delay of the at least one variable delay stage.

22. The circuit of claim 21, further comprising at least one additional variable delay stage connected in series with the at least one variable delay stage, and having a delay that is dependent on a control signal provided to the at least one additional variable delay stage.

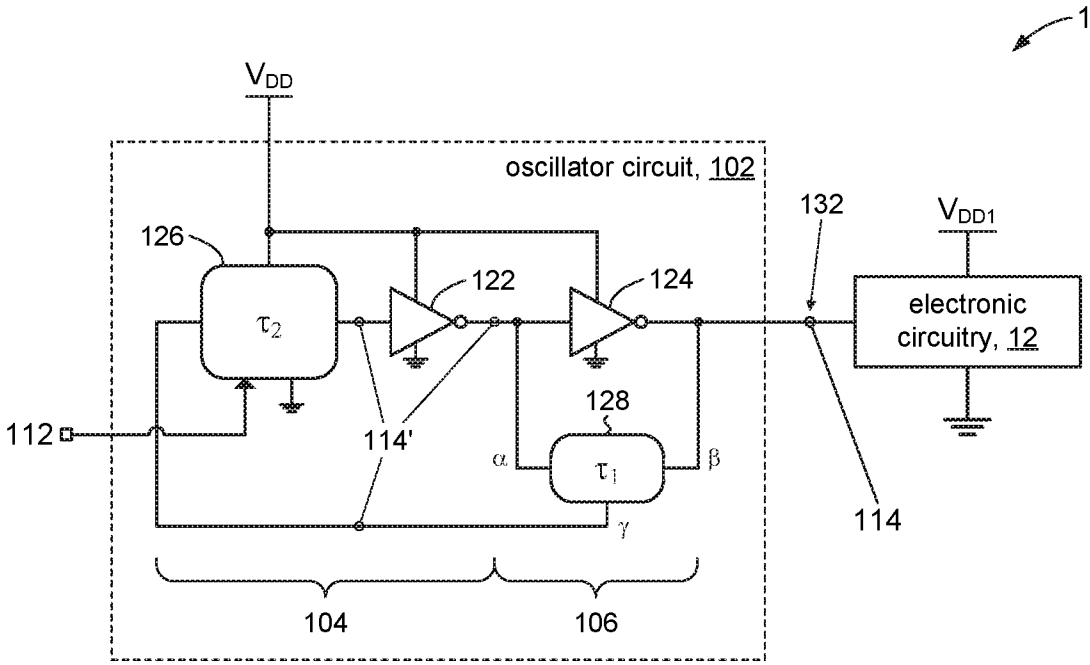
23. The circuit of claim 21, wherein a voltage level at the node that connects the resistor element and the capacitor element swings above and below a supply voltage of the oscillator circuit and above and below a ground potential during operation of the oscillator circuit.

24. The circuit of claim 21, wherein the at least one variable delay stage comprises a resistor and a variable capacitor, wherein the control signal provided to the at least one variable delay stage sets a capacitance of the variable capacitor, wherein the delay of the at least one variable delay stage is dependent on the capacitance of the variable capacitor.

25. The circuit of claim 21, wherein the at least one variable delay stage comprises a plurality of switched capacitors, wherein the control signal sets each of the plurality of switched capacitors to an ON state or an OFF state.

26. The circuit of claim 25, wherein when a switched capacitor is in the ON state, a node of the switched capacitor is electrically connected to a DC voltage or to ground potential.

27. The circuit of claim 21, wherein at least one node of the capacitive element of the RC circuit swings above supply voltage of the oscillator circuit and below ground potential.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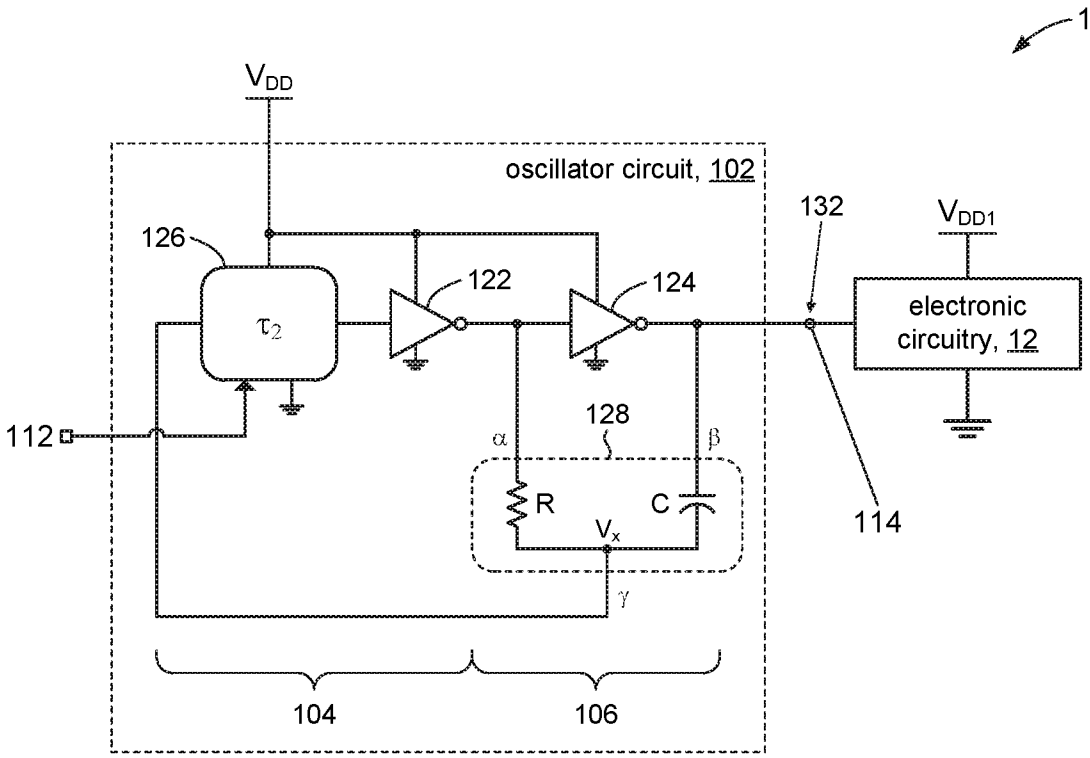
oscillator circuit, 102
126
τ_2
122
124
132
V_{DD1}
electronic circuitry, 12
112
114'
128
τ_1
α
β
γ
114
104
106

Fig. 1A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τ_2
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electronic circuitry, 12
112
128
α
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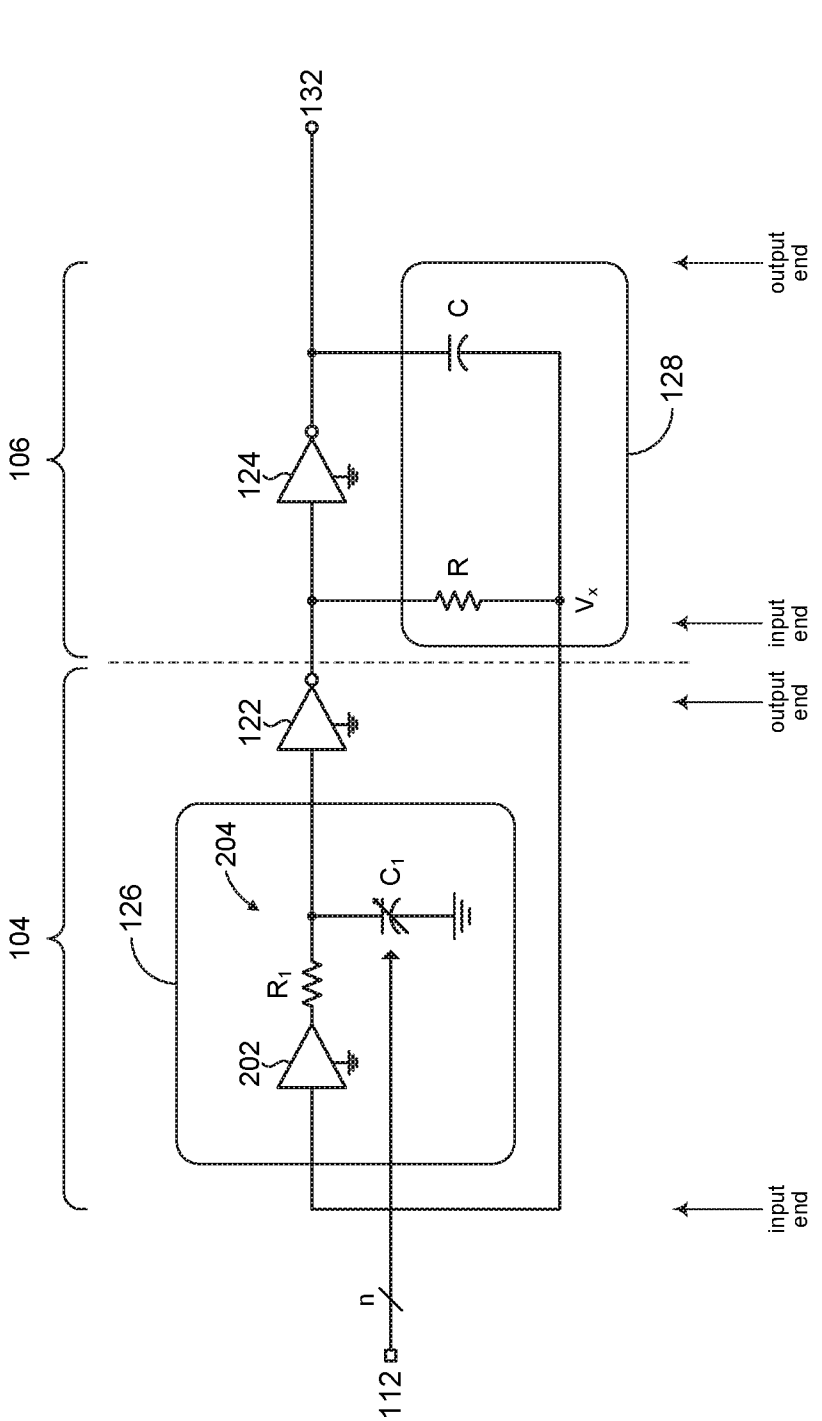
R
C
V_x
γ
114
104
106

Fig. 1B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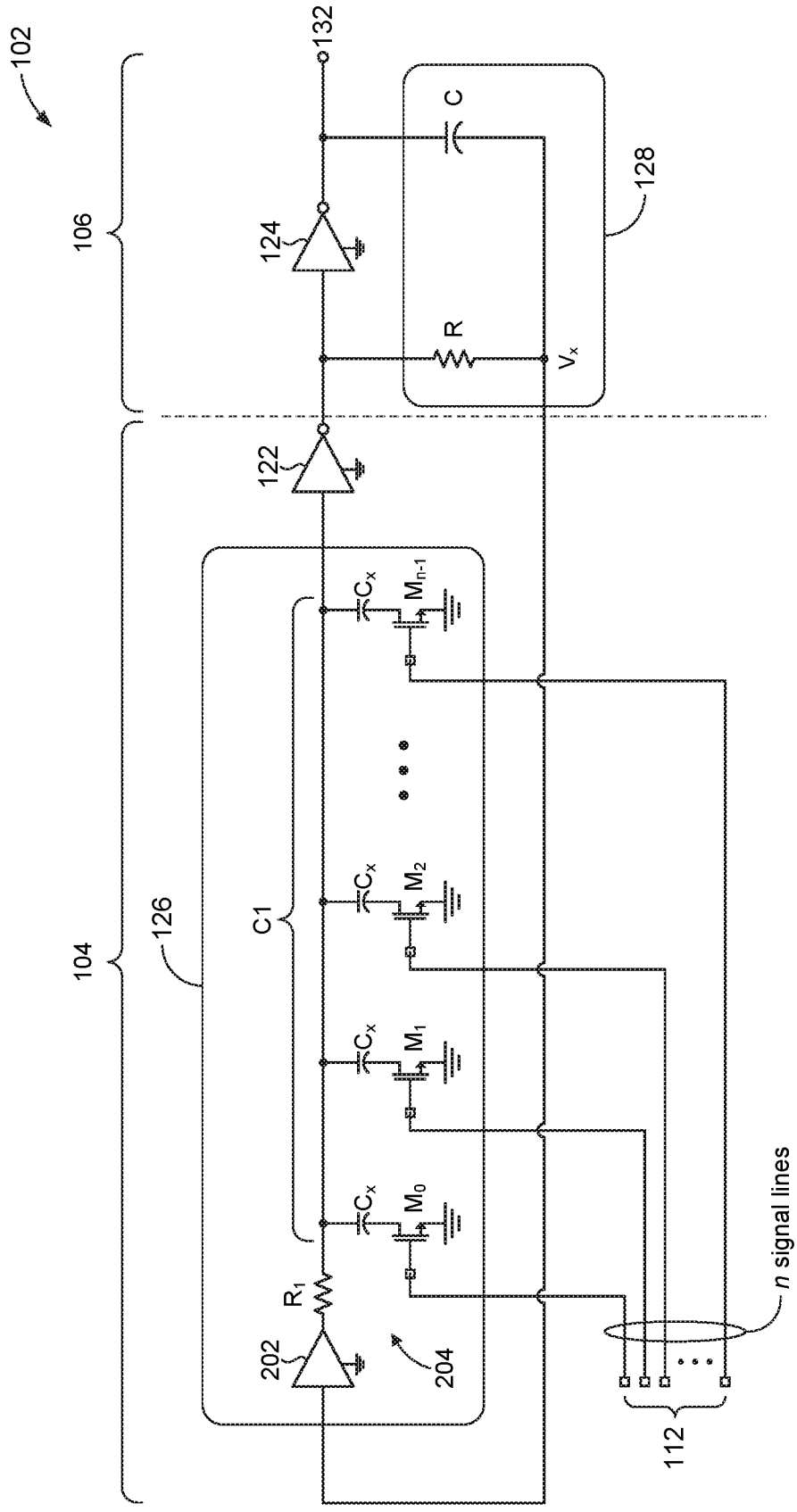
132
106
104
124
122
202
204
126
128
C
R
V_x
R_1
C_1
n
112
output end
input end
output end
input end

Fig. 2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106
104
126
132
124
122
202
204
128
C
R
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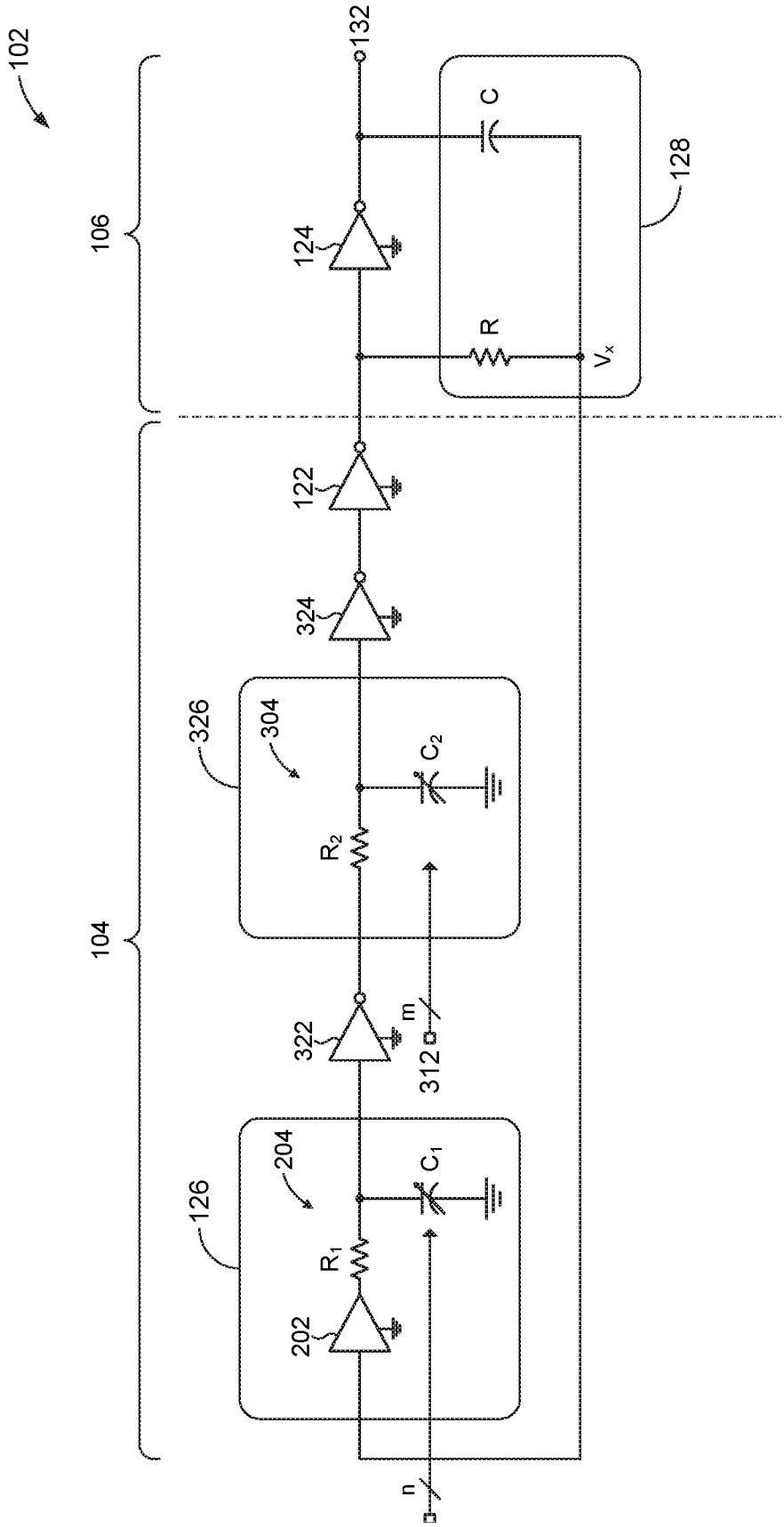
C1
C_x
M_{n-1}
M_2
M_1
M_0
R_1
n signal lines
112

Fig. 2A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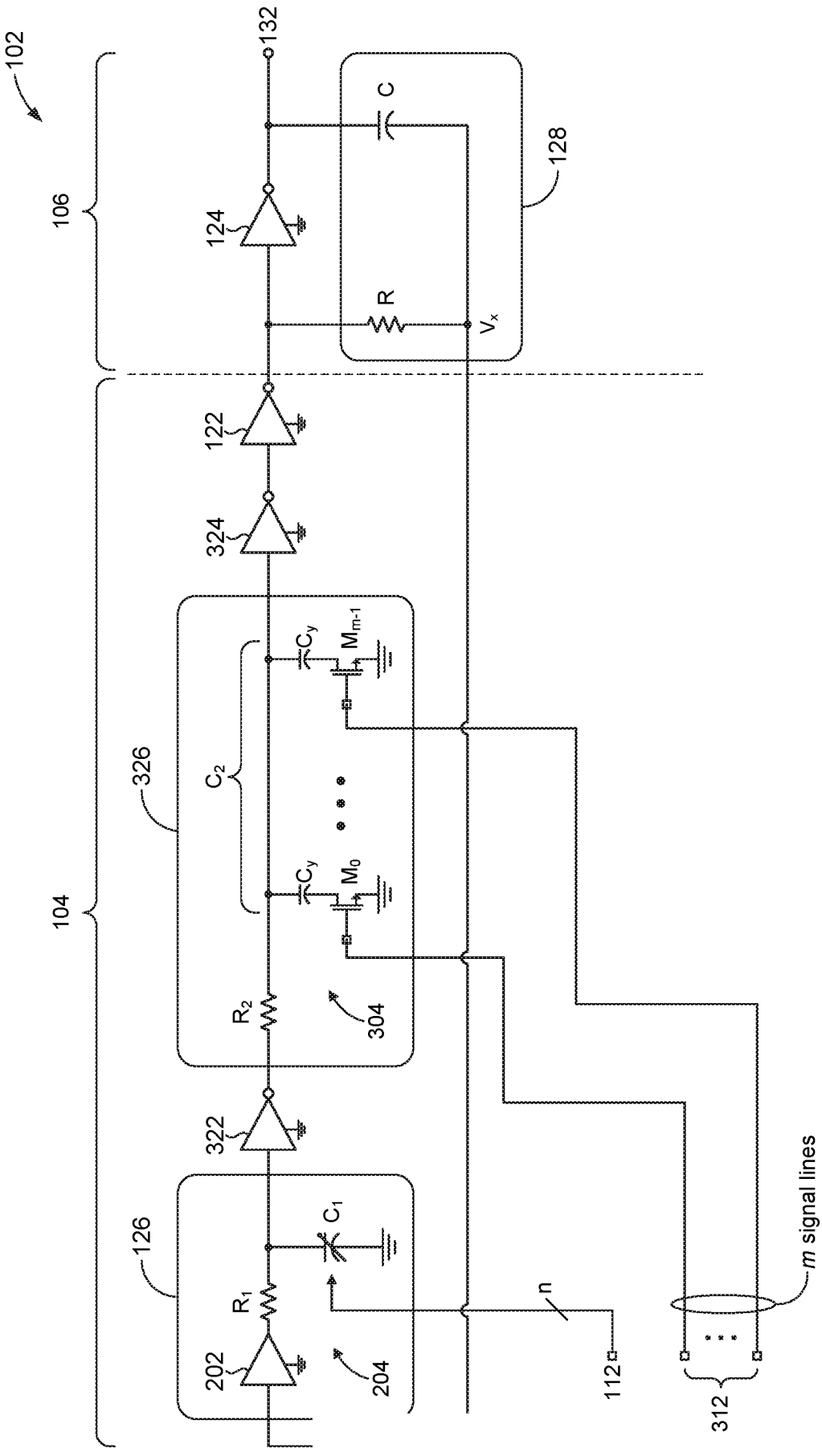
106
104
132
C
128
124
R
V_x
122
324
326
304
C_2
R_2
322
m
312
126
204
C_1
R_1
202
n

Fig. 3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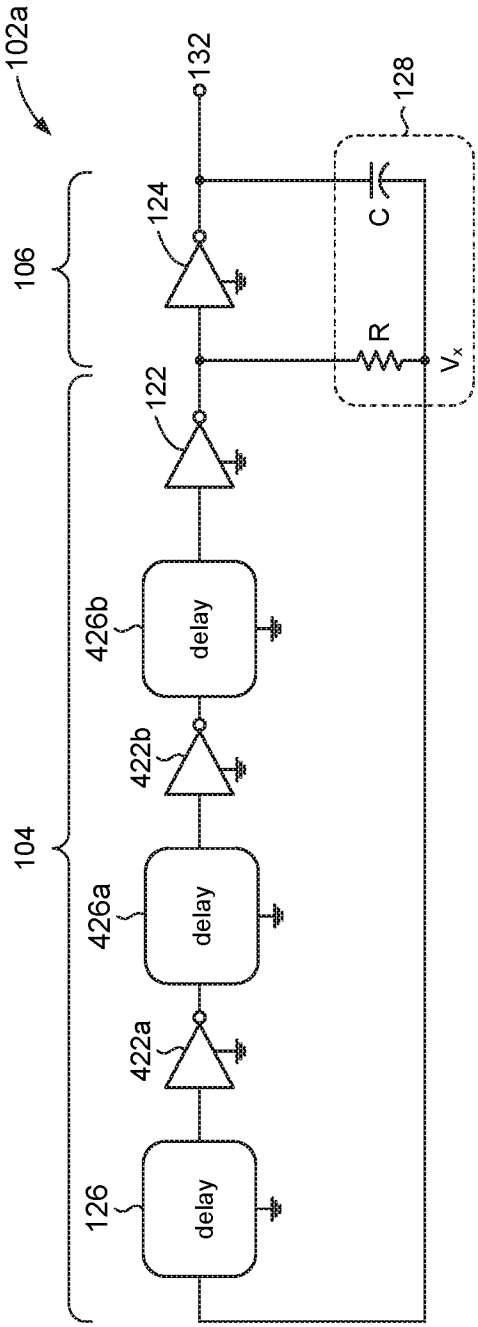
106
104
132
124
122
324
322
126
326
128
C
R
V_x
C_y
M_{m-1}
M_0
C_2
R_2
304
C_1
R_1
202
204
n
112
312
m signal lines

Fig. 3A


102a
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104
132
128
124
122
C
R
V_x
delay
426b
422b
426a
422a
126

Fig. 4A

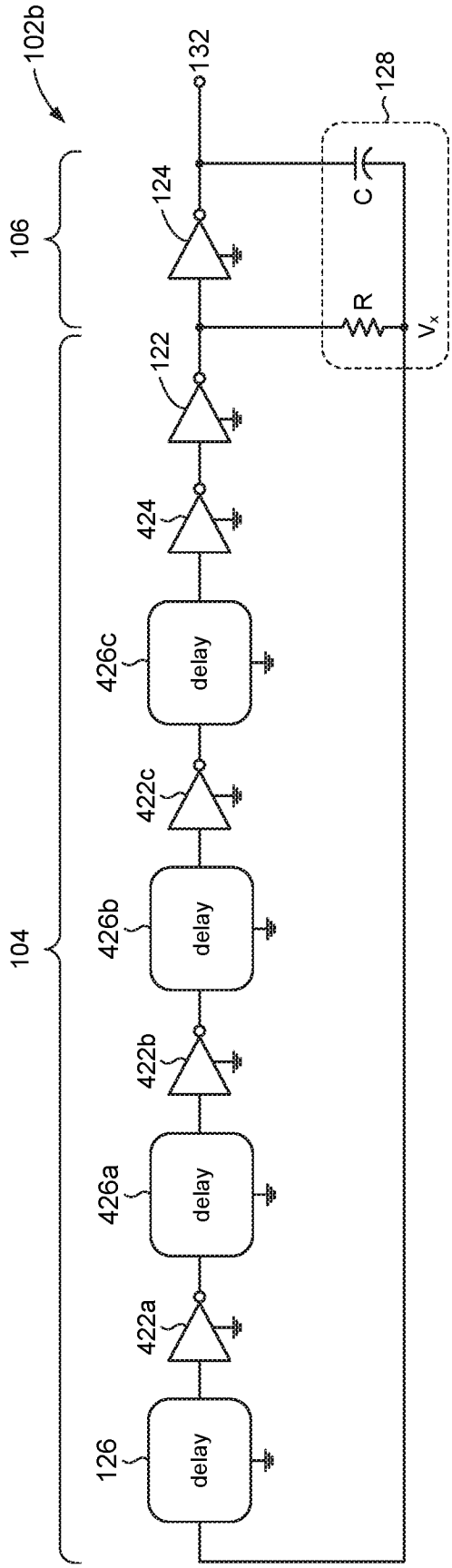
102b
106
104
132
128
124
122
424
C
R
V_x
delay
426c
422c
426b
422b
426a
422a
126

Fig. 4B

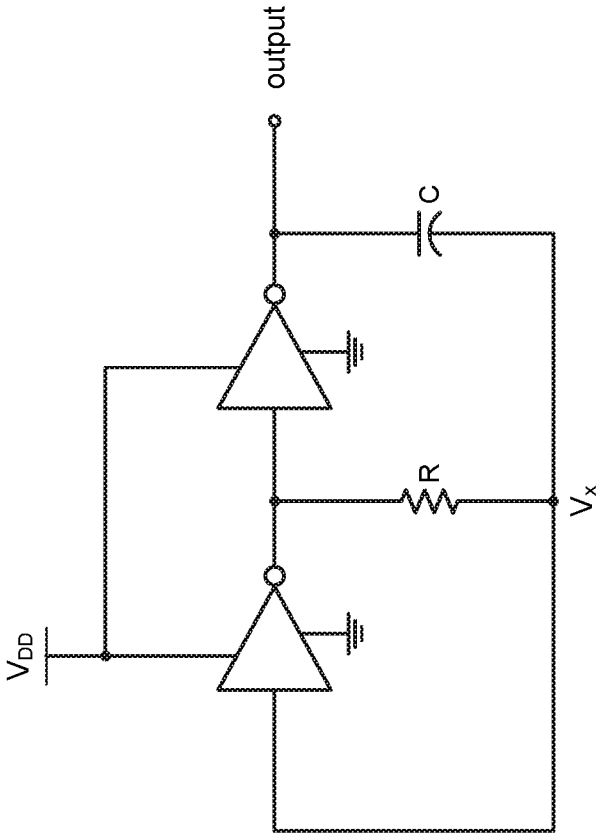

Fig. 5
(prior art)

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2017/017518

A. CLASSIFICATION OF SUBJECT MATTER
INV. H03K3/03 H03B5/20
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H03K H03B H03L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
EPO-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	WO 2013/141837 A1 (SUMESAGLAM TANER [US]) 26 September 2013 (2013-09-26)	1-5,8,9, 12,21,24
A	paragraph [0024] - paragraph [0035]; figures 1-5	10,11, 19,23,27

X	US 2008/136545 A1 (FAYNEH EYAL [IL] ET AL) 12 June 2008 (2008-06-12)	1,6,7, 13-18, 21,22, 25,26
A	paragraph [0009]; figures 1-3 paragraph [0014] - paragraph [0015]	10,11, 19,23,27

A	US 2013/320955 A1 (KRATYUK VOLODYMYR [US] ET AL) 5 December 2013 (2013-12-05) figure 2	1-27

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

* Special categories of cited documents :

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"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
21 April 2017	03/05/2017

Name and mailing address of the ISA/	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Fax: (+31-70) 340-3016	Mesplede, Delphine

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No
PCT/US2017/017518

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
WO 2013141837 A1	26-09-2013	CN 104285375 A	14-01-2015
		US 2013271227 A1	17-10-2013
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US 2013320955 A1	05-12-2013	NONE	