

- [72] Inventors **Pierre M. Lucas**
20 rue Tariel, 92 Issy-Les-Moulineaux;
Charles E. Abraham, 114 Elysees 11, 78-
La Celle, Saint-Cloud; Roger Fabre, 1 rue
Georges Bizet, 78 D'Arcy, France
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[31] **135350**

[54] **DEVICE FOR SELECTIVELY ACTUATING SWITCHING NETWORK ELECTROMAGNETIC RELAYS**
2 Claims, 12 Drawing Figs.

- [52] U.S. Cl. **179/18**
[51] Int. Cl. **H04q 3/54**
[50] Field of Search **179/18**

(SP)

Primary Examiner—Kathleen H. Claffy
Assistant Examiner—Thomas W. Brown
Attorney—Abraham A. Saffitz

ABSTRACT: System for selectively energizing and deenergizing a plurality of signalling and control electromagnetic relays arranged in several groups in the junctors of a switching network under the control of at least two control computers. The relays to be actuated have first and second half-windings interconnected at a common point which is connected to a grounded holding contact of each relay and the terminals of the two half-windings are first connected to a current source pole and second to a selector switch through a crosspoint of an address matrix. This selector switch connects the terminal of the second half-winding to the ground for an activation of the relay and to the current source pole for a release of the relay. An address signal and an order signal are forwarded by one of the control computers respectively to an address register associated with the address matrix and to an order register associated with the selector switch. According to the address signal, a crosspoint of the matrix is actuated and, according to the order signal, the selector switch connects the terminal of the second half-winding of the relay for activation or release. Means are provided for deriving from the establishment or release of the feed current in the relay a check signal and for actuating a fault circuit when the time interval between the order signal and the check signal reaches a predetermined value.

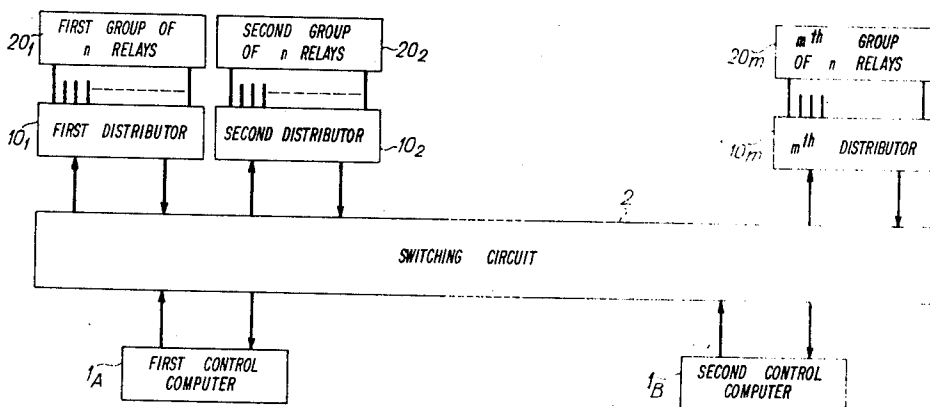
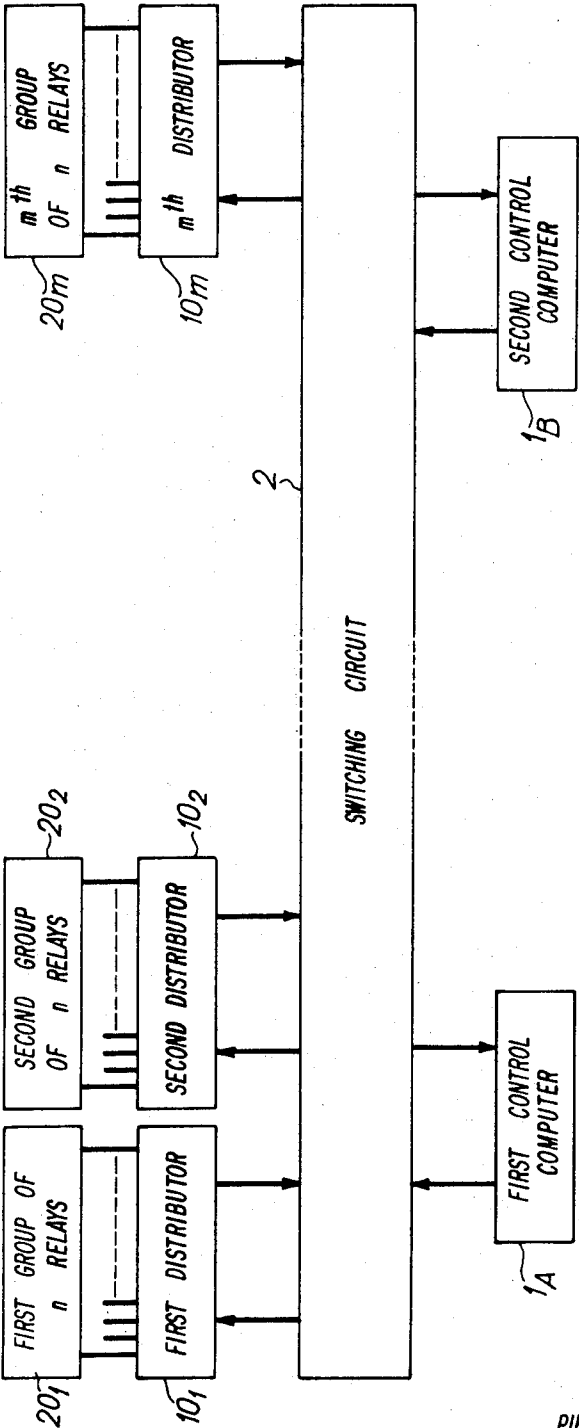


Fig. 1

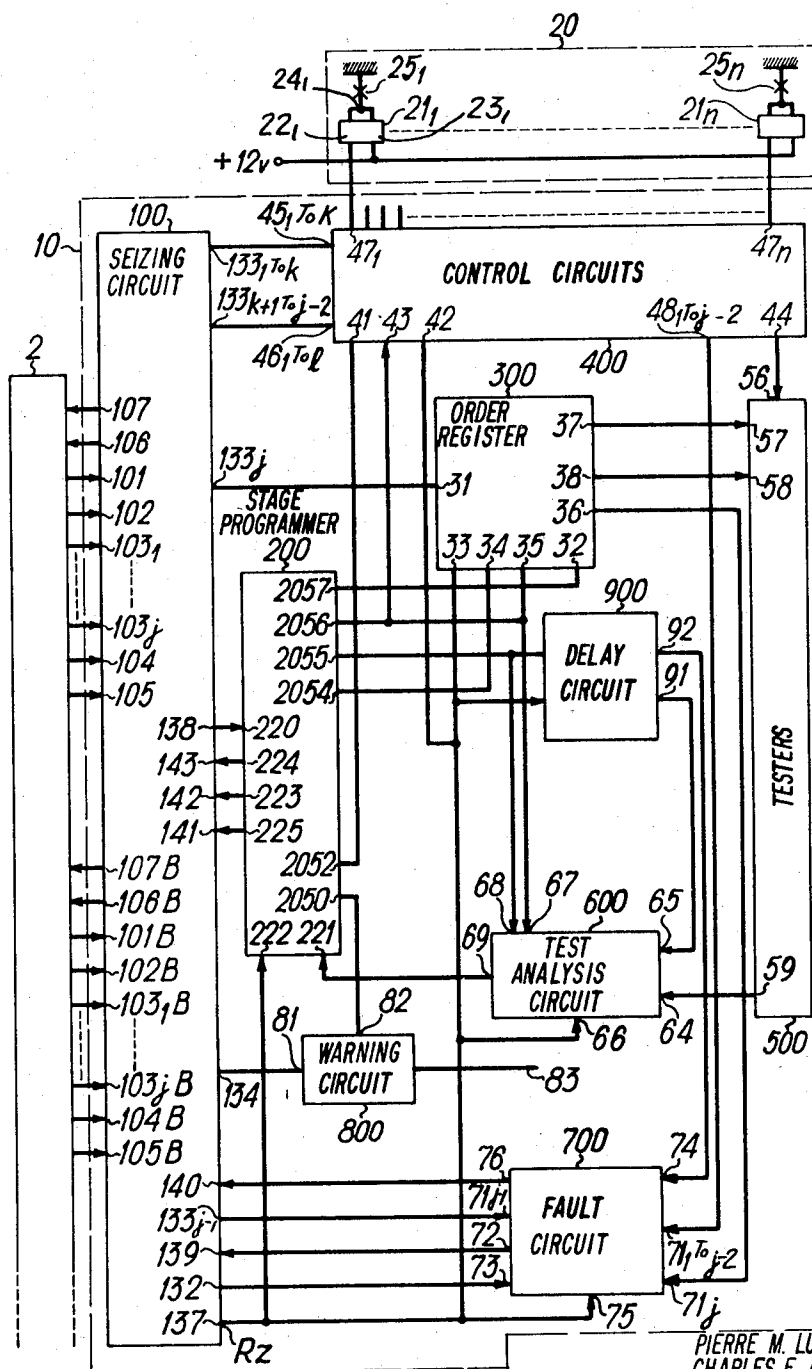


INVENTORS
PIERRE M. LUCAS
CHARLES E. ABRAHAM
ROGER FABRE

BY *Abraham A. Saffitz*

ATTORNEY

Fig. 2



INVENTORS

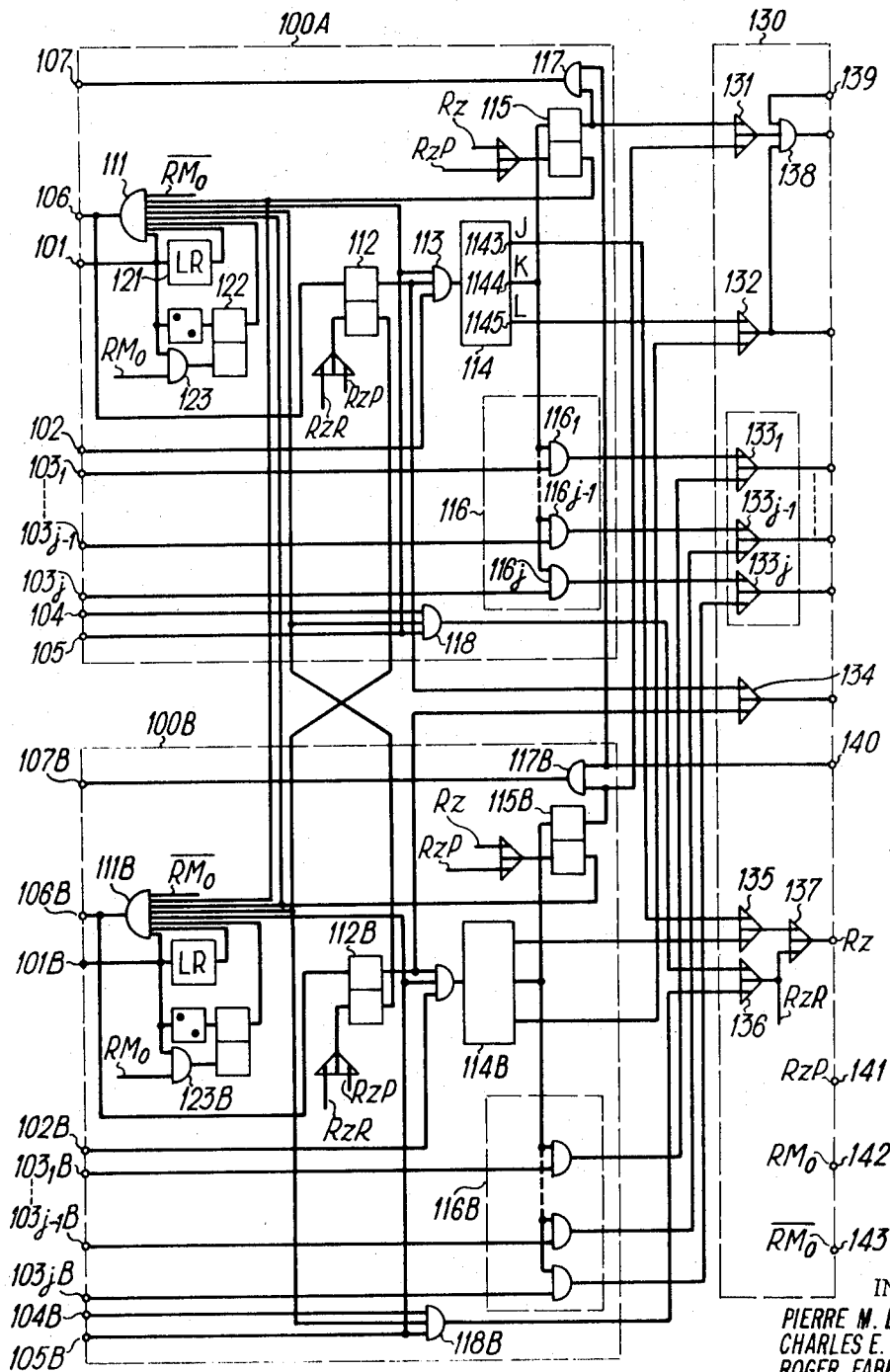
PIERRE M. LUCAS
CHARLES E. ABRAHAM
ROGER FABRE

BY

Abraham A. Saffitz

ATTORNEY

Fig. 3



INVENTORS
 PIERRE M. LUCAS
 CHARLES E. ABRAHAM
 ROGER FABRE

BY *Abraham A. Saffitz*

ATTORNEY

Fig. 4

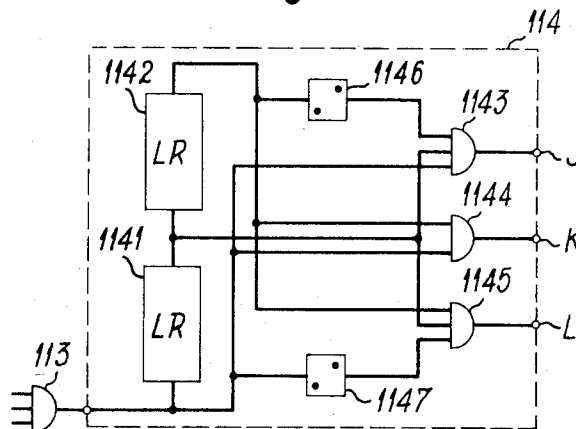
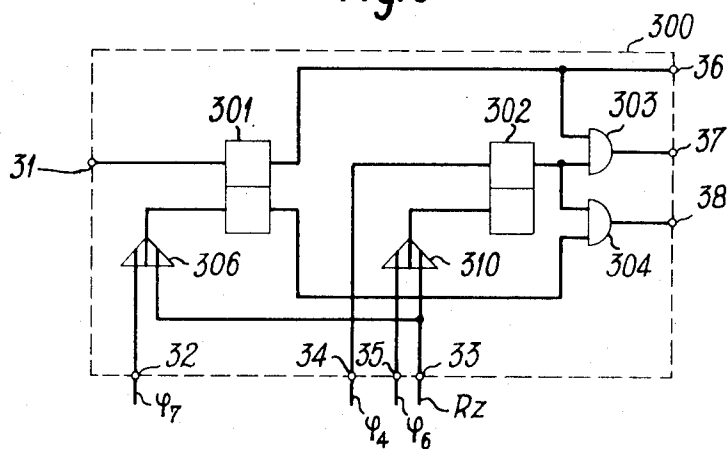


Fig. 6

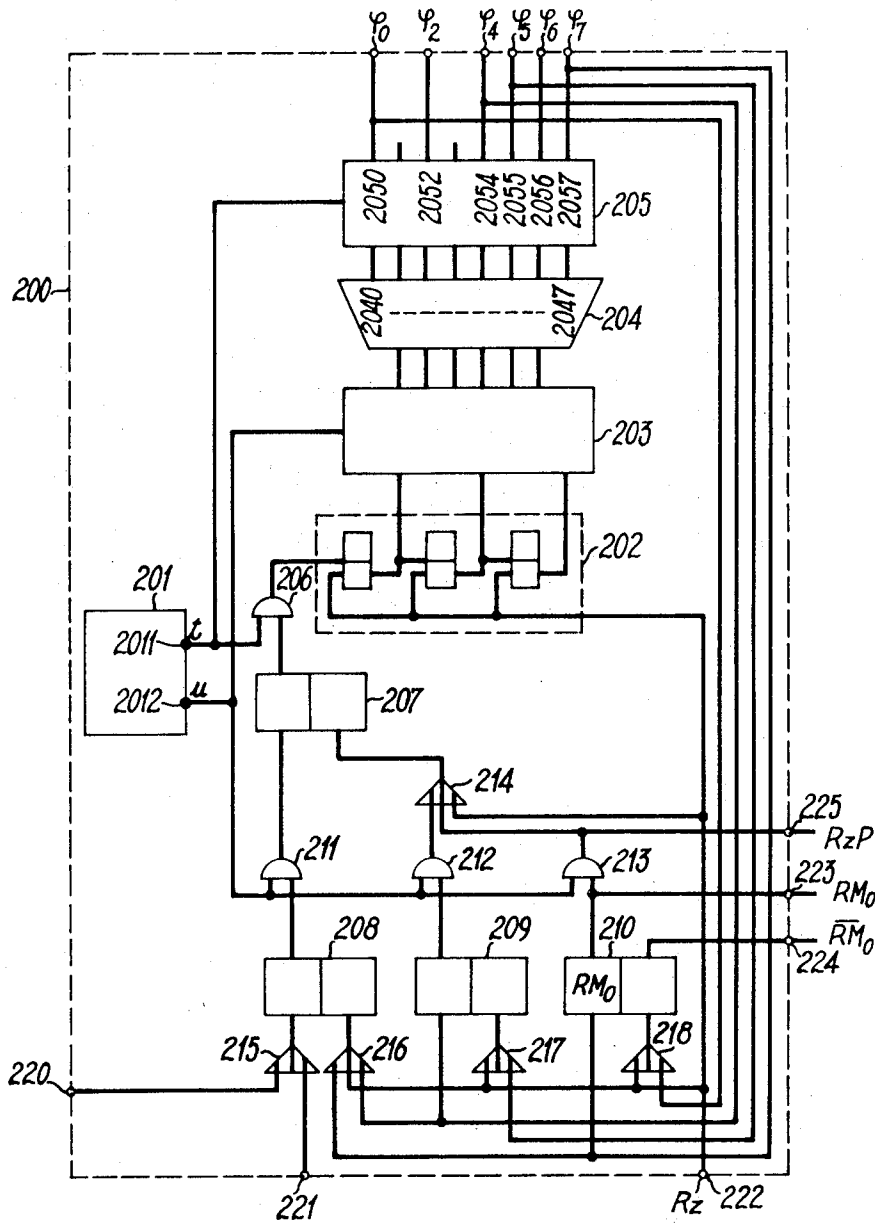


INVENTORS
 PIERRE M. LUCAS
 CHARLES E. ABRAHAM
 ROGER FABRE

BY *Abraham A. Saffitz*

ATTORNEY

Fig. 5

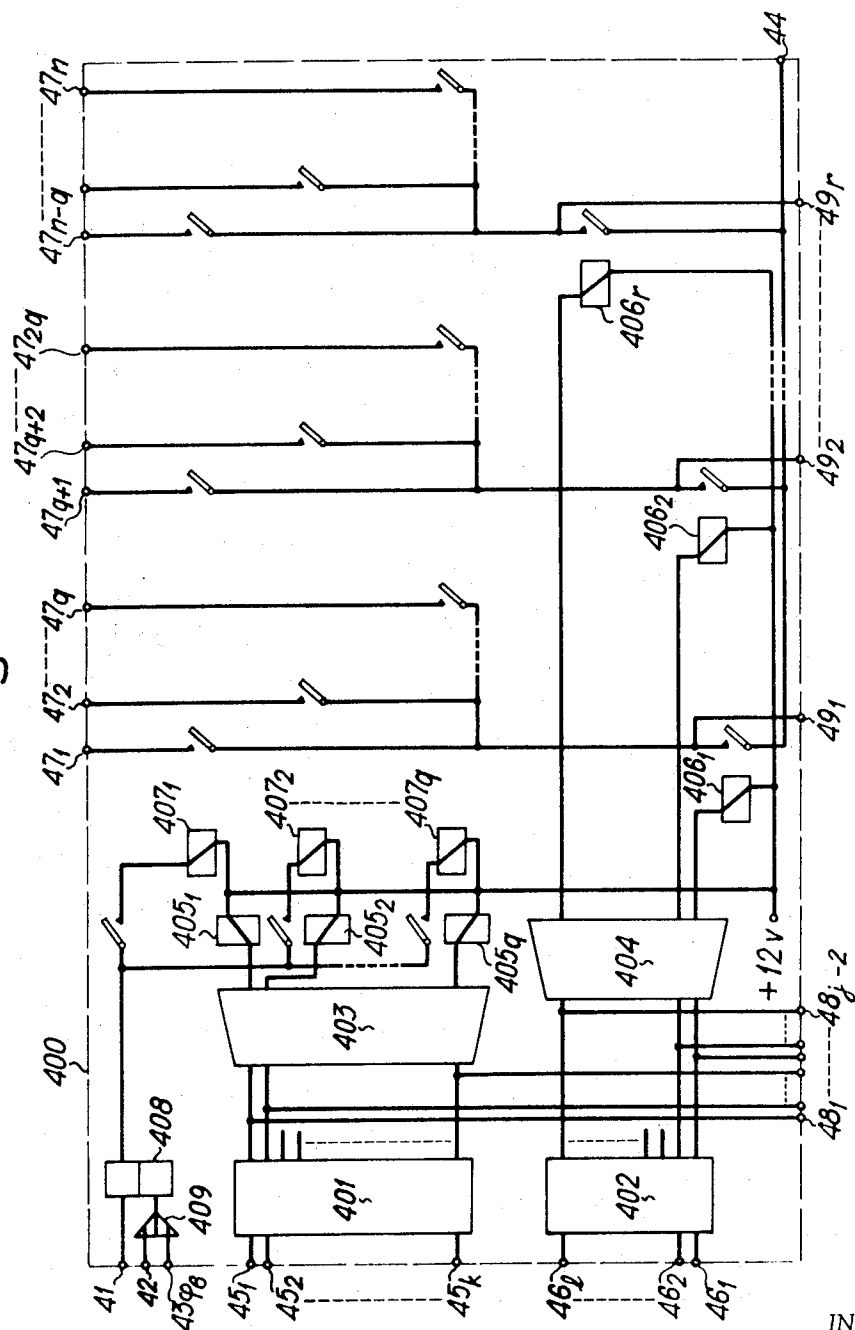


INVENTORS
 PIERRE M. LUCAS
 CHARLES E. ABRAHAM
 ROGER FABRE

BY *Abraham C. Saffitz*

ATTORNEY

Fig. 7



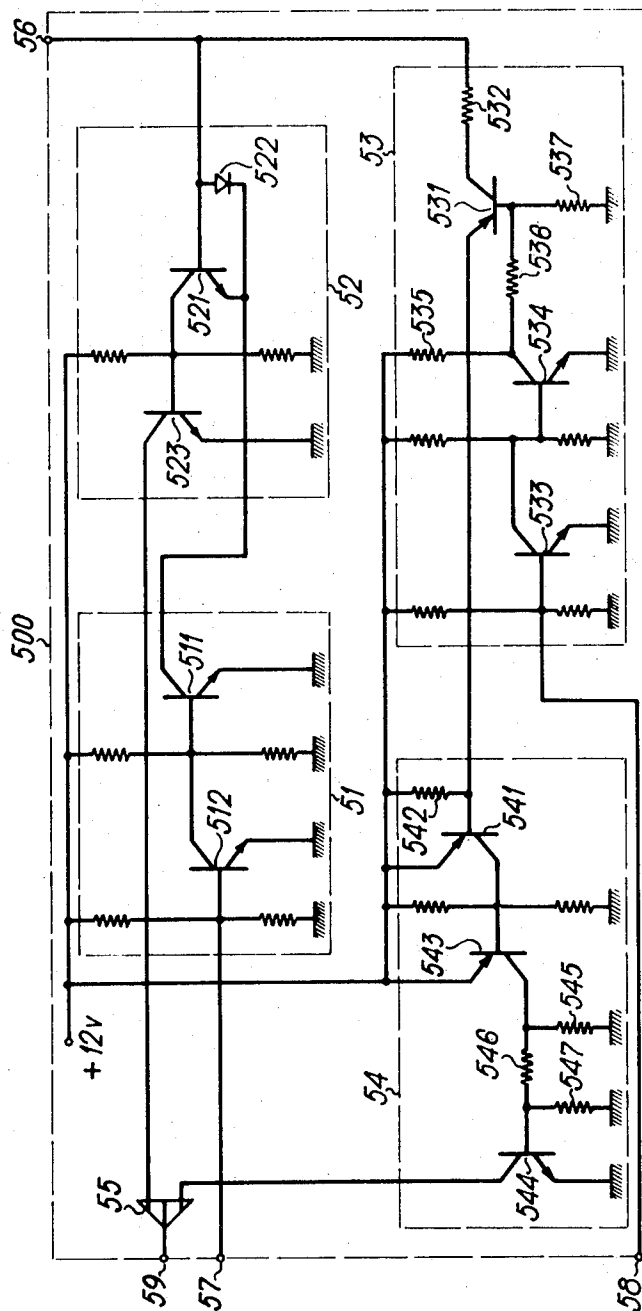
INVENTORS

PIERRE M. LUCAS
CHARLES E. ABRAHAM
ROGER FABRE

BY

Abraham & Saffety
ATTORNEY

Fig. 8



INVENTORS

PIERRE M. LUCAS
CHARLES E. ABRAHAM
ROGER FABRE

BY *Abraham A. Saffitz*

ATTORNEY

Fig. 9

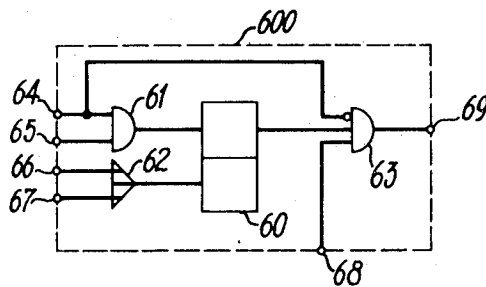


Fig. 10

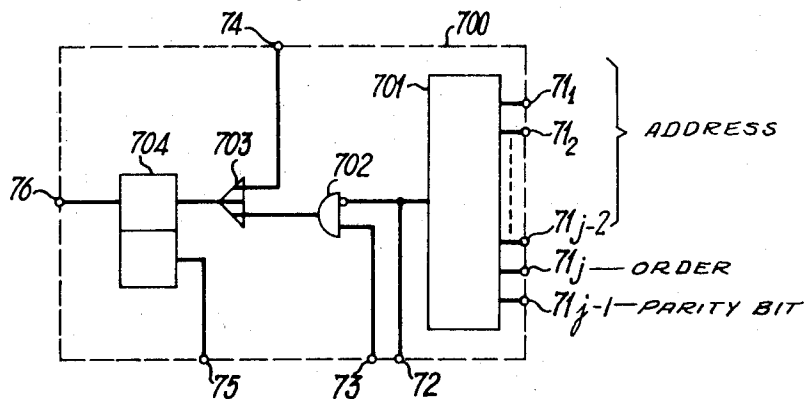
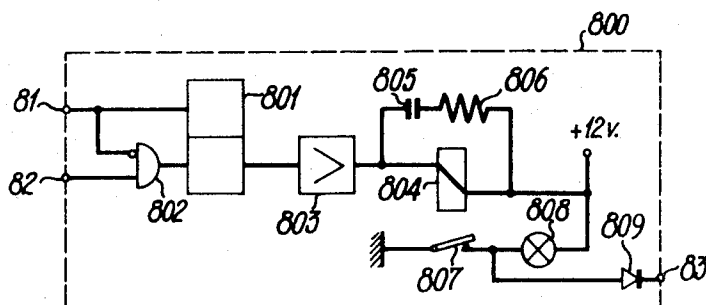


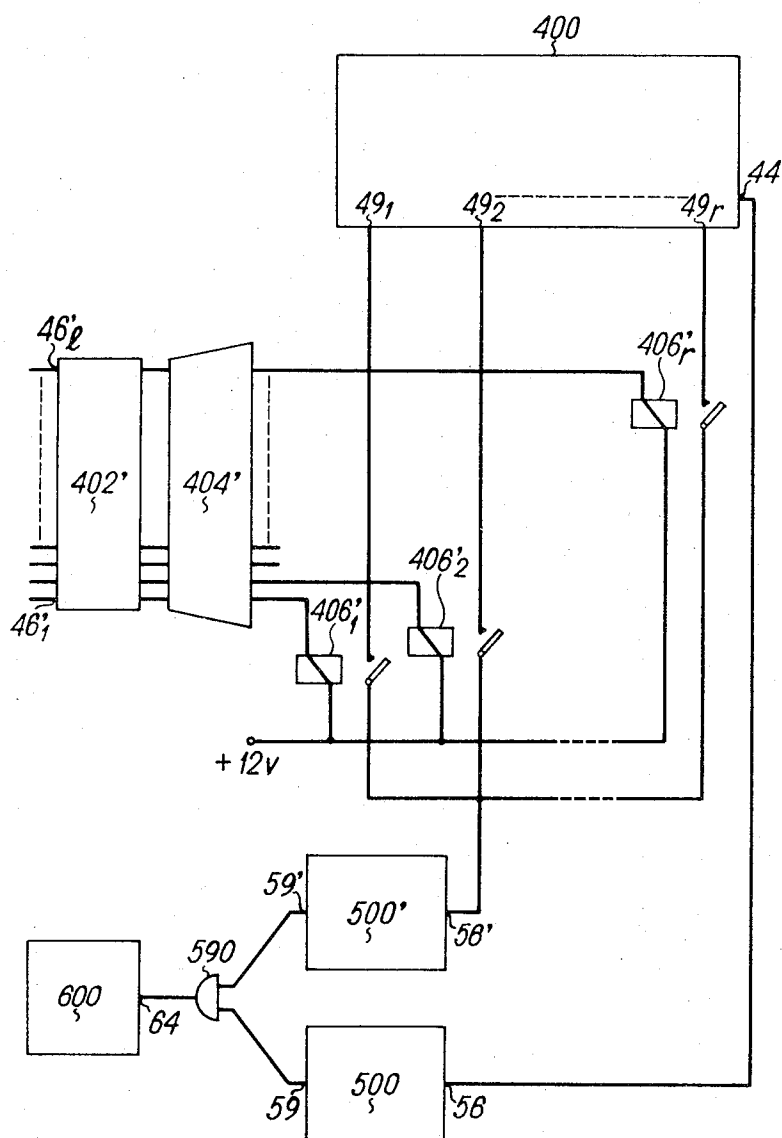
Fig. 11



INVENTORS
PIERRE M. LUCAS
CHARLES E. ABRAHAM
ROGER FABRE

BY *Abraham A. Saffitz*
ATTORNEY

Fig. 12



INVENTORS

PIERRE M. LUCAS
CHARLES E. ABRAHAM
ROGER FABRE

BY *Abraham A. Saffitz*
ATTORNEY

DEVICE FOR SELECTIVELY ACTUATING SWITCHING NETWORK ELECTROMAGNETIC RELAYS

The present invention relates to high speed signalling distributors.

U.S. Pat. No. 3,365,548 issued Jan. 23, 1968 to Pierre Lucas et al. discloses a signal distributor of the autonomous program type, adapted to activate or deactivate a particular electromechanical relay selected in a group of relays according to the instructions received in parallel from a central control unit in the form of an address and an order signal, to check on the fulfillment of the different stages of its program, and to supply the said central control unit with a report indicating a failure to comply with any of the said stages or indicating compliance with the instructions received.

According to the aforesaid patent, each of the electromechanical relays comprises two similar half-windings wound in the same sense, in series, with their common point connected to one terminal of a source of direct current and their extremities connected, respectively, to the other terminal of the said source and to the signal distributor. This distributor comprises electronic means for registering the coded address in a checking code for the relay to be actuated, as well as the activation or deactivation ordered to be performed, electromechanical means for decoding the address and checking the code thereof, a coupling matrix comprising crossbars whereof the crosspoints render it possible to connect the relay to be activated to one terminal or the other of the said source, means for checking on the presence of current flow for actuation of the designated relay, and for checking on the absence of current flow after a definite period, and means for supplying the said central control unit with reports indicating coding errors and operational failures of the designated relays. These checking means comprise a test unit consisting of ferrite rings of the rectangular hysteresis cycle type having as write-in windings the connections between the coupling matrix and the two terminals of the said source.

The practical result of employing electromechanical decoders in this signal distributor is that the number of signal relays it may actuate in a given time is sharply limited, and the result of employing a test unit comprising ferrite rings, which are inherently sensitive to temperature variations, is that the reliability of its operation is adversely affected. Also, this signal distributor can actuate but one relay at a time.

The invention has as an object the provision of a signal distribution system capable of activating all the signalling relays of a high-capacity switching network, and such that two or more signalling relays may be actuated with operational reliability.

The invention accordingly consists of a signal distribution system comprising a multiplicity of signal distributors adapted to be actuated separately or in combination by means of one or more control computers, employing an electronic switching device for selective activation and deactivation of all the signal relays of a high-capacity switching network, in which the said signal distributors comprise electronic means for the decoding of the addresses of the signalling relays to be actuated and for checking on the parity of the address words.

The distributors each comprise a coupling matrix, the contacts of which are established by means of reed relays.

The signal distributors also comprise transistorized set of testers and a test analysis circuit, the said set of testers transmitting signals to the said test analysis circuit indicating satisfactory operation for a connection or disconnection operation, the signals transmitted by the said set of testers being identical, and the absence of these latter signals within a definite period blocking the said distributor in the so-called "occupied" state, against the control computers.

The signal distributors may each be employed for simultaneous actuation of two or more signalling relays by duplication or multiplication of the elements corresponding to one only of the coordinates of their switching matrix, and of the set of testers coordinated with the corresponding connections.

The invention will now be described in detail with reference to the accompanying drawings, in which:

FIG. 1 is a diagram showing the fundamental layout of one form of signal distributor system according to the invention;

FIG. 2 is a block diagram of one of the signal distributors of FIG. 1;

FIG. 3 is a logical diagram of the input or seizing circuit of the signal distributor of FIG. 2;

FIG. 4 is a diagram of a stepped time-delay circuit of the input circuit of FIG. 3;

FIG. 5 is a diagram showing the programmer circuit for programming the stages of the signal distributor of FIG. 2;

FIG. 6 is a diagram of the order register of the same distributor;

FIG. 7 is a diagram of a set of control circuits for actuation of the designated signal relay;

FIG. 8 is a diagram of a set of testers;

FIG. 9 is a diagram of a test analysis circuit;

FIG. 10 is a diagram of a so-called "fault" circuit;

FIG. 11 is a diagram of a warning circuit; and

FIG. 12 is a diagram of a modified embodiment intended for simultaneous actuation of two signalling relays, of a signal distribution system according to the invention.

FIG. 1 shows the block diagram of a set of signalling distributors 10_1 to 10_m , these being identical, and each selectively actuating a group 20_1 to 20_n of n electromagnet relays according to the instructions coming from a first or a second digital control computer, 1A and 1B respectively, these instructions being transmitted to the said relays through a switching circuit 2, in selective manner, as a function of two addresses, a group address and a relay address within its group, either for activation or for deactivation of the said relay.

As an example, but in no restrictive sense, m may be equal to 16 and n may be equal to 768, the total number of relays to be actuated then amounting to $m \times n = 16 \times 768 = 12,288$.

FIG. 2 is a block diagram of one distributor 10 of the m signalling distributors, and of the group 20 of n relays 21_1 to 21_n actuated by the same. The signalling distributor 10 comprises a seizing circuit 100, a stage programmer 200, an order register 300, a set of control or actuating circuits 400, a set of test units 500, a test analysis circuit 600, a fault circuit 700, a warning circuit 800 and a delay circuit 900.

The relays 21_1 to 21_n actuated preferably correspond to those specified in U.S. Pat. referred to above. Each of these relays comprises two half-windings in series, 22_1 and 23_1 for relay 21_1 , and wound in the same sense, their common point, 24_1 for relay 21_1 , being connected to ground through one of its operating contacts, 25_1 for relay 21_1 , and one of their extremities being connected to a source of current, for example of +12 volts, and the other to an output terminal 47_1 to 47_n of the control circuits 400.

FIG. 3 illustrates the seizing circuit 100. The latter comprises two parts 100_A and 100_B , the former being coordinated with the first control computer 1_A and the latter with the second control computer 1_B , and a set of gates 130 for connection of the two parts 100_A and 100_B in parallel with the other circuits of the signal distributor 10.

The two parts 100_A and 100_B being identical, the former only will be described, the elements of the parts 100_B being marked, where appropriate, by the same reference numerals as the identical elements of the part A, but with addition of the index letter B. The part 100_A is connected to the switching circuit 2 by means of input terminals $101, 102, 103, \dots, 103_B, 104, 105$ and of two output terminals $106, 107$. This part essentially comprises an "availability" gate 111, a "reservation" flip-flop or the like 112 actuating a gate 113 for access to a stepped time-delay circuit 114, a seizing flip-flop 115, a set 116 of gates 116_1 to 116_6 for transfer in parallel of the bits of an address and order word, a "fault" gate 117, and a blocking gate 118.

The gate 111 has eight input terminals. The first in connected to the input terminal 101 of the signalling distributor 10 for reservation of the signalling distributor 10 by the first

control computer 1_A. The second is connected to the same terminal 101 through a delay line 121 introducing a delay τ shorter than the duration of the reservation signal, for example of 300 to 500 nanoseconds if the duration of the latter is 2 microseconds. The third input terminal is connected to the one output terminal of a bistable flip-flop 122 whereof the activating input terminal is connected to the same terminal 101 through an inverter circuit and whereof the deactivating input terminal is connected to the output terminal of an AND gate 123 having an input terminal connected to the same terminal 101 and a second input terminal connected by a connection which is not illustrated, to an output terminal 223 of the stage programmer 200 and supplied by this terminal 223 with an opening pulse at the end of a cycle. The fourth input terminal of the gate 111 is connected to the input terminal 105 which receives a pulse from the switching circuit 2 when the first control computer 1_A selects the signalling distributor 10. The fifth input terminal is connected to the zero output terminal of the input flip-flop 115 and the sixth to the zero output terminal of the analogous input flip-flop 115_B. The seventh input terminal of the gate 111 is connected to the zero output terminal of the reservation flip-flop 112_B and the eighth input terminal is connected by a connection which is not illustrated, to an output terminal 224 of the stage programmer 200 through which it receives a signal $\overline{RM}_0$ complementary to that supplied by the terminal 223, that is to say a signal of permanent nature interrupted temporarily at the end of a cycle of the stage programmer 200. Due to delay line LR, gate 111 is controlled for opening by reservation pulses which are cut down by a time interval τ . It is plain that in these circumstances, the flip-flop 122 has the function of closing the gate 111 against the reservation pulses thus curtailed when the signal $\overline{RM}_0$ begins during the duration of these reservation pulses. The gate 111 will be open only by the curtailed reservation pulses which fall entirely within the duration of the signal $\overline{RM}_0$ and not by the reservation pulses which fall only partially within said duration.

The output terminal of the availability gate 111 is connected to the activating input terminal of the flip-flop 112 and to the output terminal 106 through which, when the distributor 10 is available, an availability report signal is fed to the switching circuit 2 as a response delayed by 300 to 500 nanoseconds to a reservation signal fed to the terminal 101 accompanied by a designation signal fed to the terminal 105. The reset input terminal of the flip-flop 112 is actuated by an OR gate possessing two input terminals correspondingly connected by connections which are not shown, to an output terminal 225 of the stage programmer 200 (connected to terminal 141 of the seizing circuit 100), and to an output terminal RzR of the set of gates 130. The zero output terminal of the flip-flop 112 is connected to the seventh input terminal of the gate 111_B.

The one output terminal of the flip-flop 112 is connected to the input terminal of the stepped delay circuit 114 through the AND gate 113 which has two other input terminals connected respectively to the designation terminal 105 and to the seizing terminal 102 to which the first control computer 1_A feeds a seizing pulse through the switching circuit 2 in response to the appearance of an availability signal at the terminal 106.

FIG. 4 is a diagram of the circuit 114. This latter comprises two delay lines 1141, 1142 generating delays equal to about one third of the duration of a seizing pulse, for example each amounting to 600 nanoseconds, connected in series with the output terminal of the gate 113, and three AND gates 1143, 1144, 1145. The gate 1143 has three input terminals connected, respectively, the first to the output terminal of the gate 113, the second to the output terminal of the delay line 1141 and the third through an inverter circuit 1146, to the output terminal of the delay line 1142. The gate 1144 has two input terminals connected, respectively, to the output terminal of the gate 113 and to the output terminal of the delay line 1142. The gate 1145 has three input terminals connected, respectively, to the output terminal of the gate 113 through an in-

verter circuit 1147, to the output terminal of the delay line 1141 and to the output terminal of the delay line 1142. It is apparent that the gates 1143, 1144, 1145 supply pulses of 600 nanoseconds staggered respectively by 600, 1200 and 1800 nanoseconds on the leading front of the seizing pulse.

The output terminal of the gate 1144 is connected in parallel to the one input terminal of the input flip-flop 115 and to the opening input terminals of the gates 116, to 116, whereof the second input terminals are connected, respectively, to the address and order terminals 103, to 103, of the signalling distributor. These terminals are supplied in parallel by the switching circuit 2 simultaneously with the dispatch of the seizing signal through the terminal 102, with the bits of the address of the relay 21, to 21_n, to be actuated and with the bit for the actuation order which is equal to 1 for a connecting action and to zero for a disconnecting action, and an additional parity bit.

To simplify matters, the bits fed to the terminals 103, to 103_{n-1} will be considered as representing the address of the relay to be actuated and the parity bit, and the binary digit fed to the terminal 103_n as the order for activation or for deactivation.

The blocking gate 118 has three input terminals connected, respectively, to the designation terminal 105, to the zero output terminal of the flip-flop 112_B and to the terminal 104 supplied with a signal by the switching circuit 2 when the control computer 1_A decides to free the distributor 10 after reservation or blocking.

The set of gates 130 comprises OR gates 131, 132, 133, to 133_n, 134, 135, 136, 137, and AND gate 138 and five input terminals 139 to 143. The gate 131 connects the one output terminals of the flip-flops 115 and 115_B to an input terminal of the gate 138 which has three input terminals. The gate 132 connects the output terminals of the gates 1145 in the circuits 114 and 114_B to an input terminal 73 of the fault circuit 700 and to the second input terminal of the gate 138. The third input terminal of the gate 138 is connected to the terminal 139 which receives a signal from the terminal 72 of the fault circuit 700 if there is no parity error in the transmission of the address of the relay to be actuated. The output terminal of the gate 138 is connected to the input terminal 220 for triggering the stage programmer 200.

The gates 133₁ to 133_{n-2} transmit the bits of the address of the relay to be actuated coming from the output terminals of the gates 116, to 116_{n-2} and of the analogous gates of the set of gates 116_B to two sets of input terminals 45, to 45_n and 46, to 46_n of the control circuits 400, and the parity bit, to an input terminal 71_{n-1} of the fault circuit 700. The gate 133_n allocated to the bit giving the actuation order 1 or the deactivation order 0, connects the output terminals of the gate 116, and of the analogous gate of the set 116_B to an input terminal 31 of the order register 300. The gate 134 connects the one output terminals of the reservation flip-flops 112 and 112_B to an input terminal 81 of the warning circuit 800. The gate 135 connects the output terminal of the gate 1143 of the circuit 114 and the homologous output terminal of the circuit 114_B to an input terminal of the gate 137. The gate 136 connects the output terminals of the gates 118, 118_B to the second input terminal of the gate 137 on the one hand, and on the other hand through connections which are not shown, to one input terminal of each of the OR gates which operate the reset of the flip-flops 112 and 112_B. The output terminal of the gate 137 is connected to the input terminal 222 of the stage programmer 200, to the input terminal 33 of the order register 300, to the input terminal 66 of the test analysis circuit 600, to the input terminal 75 of the fault circuit 700, to the reset terminal of the delay circuit 900, and through connections which are not shown, to one input terminal of each of the OR gates which operate the reset of the flip-flops 115 and 115_B. The second input terminals of the OR gates operating the reset of the flip-flops 112, 112_B and 115, 115_B are connected by connections which are not shown, to the input terminal 141 which is connected to the output terminal 225 of the stage programmer 200.

The input terminal 140 connects the output terminal 76 of the fault circuit 700, to one input terminal of each of the fault gates 117, 117_B. The output terminals 107, 107_B of these gates are connected to input terminals of the switching circuit 2. The terminal 142 is connected to the output terminal 223 of the stage programmer 200 which it connects through connections which are not shown, to the second input terminals of the gates 123, 123_B. The terminal 143 is connected to the output terminal 224 of the stage programmer 200 which it analogously connects to the eighth input terminals of the gates 111, 111_B.

FIG. 5 is a diagram of the stage programmer 200. The latter comprises a time base circuit 201, a three-stage counter 202 connected by a set of gates 203 to a decoder 204 also possessing a set of output gates 205, and AND gate 206 actuating the progression input terminal of the counter 202 under the control of a flip-flop 207, and three flip-flops 208, 209, 210 which determine the state of the flip-flop 207 through three AND gates 211, 212, 213 and through an OR gate 214.

Through two output terminals 2011 and 2012, the time base 201 delivers "return to zero" alternate pulses t and u , which may for example have a period of 75 milliseconds and a duration of 30 milliseconds. The pulses t are fed to the opening input terminal of the set of gates 205 and through the gate 206 to the progression input terminal of the counter 202. The pulses u are fed to an input terminal of each of the gates 211, 212, 213 and to the opening input terminal of the set of gates 203 which controls the input to the decoder 204. This latter comprises eight output terminals 2040 to 2047, six of these latter corresponding to six output terminals 2050, 2052, and 2054 to 2057 of the set of gates 205. The zero reset input terminal 222 of the counter 202 is connected to the output terminal 137 of the seizing circuit 100.

The one input terminal of the flip-flop 208 is connected through an OR gate 215 to an input terminal 220 connected to the output terminal of the gate 138 of the seizing circuit 100 and to a terminal 221 connected to the output terminal 69 of the test analysis circuit 600. Its zero input terminal is connected by an OR gate 216 to the terminal 222 and to the output terminals 2054 and 2057 of the set of gates 205. The one output terminal of the flip-flop 208 is connected to the one input terminal of the flip-flop 207 by means of the gate 211.

The one input terminal of the flip-flop 209 is connected to the output terminal 2054 of the set of gates 205 and its zero input terminal is connected through an OR gate 217 to the terminal 222 and to the output terminal 2055 of the set of gates 205. The one output terminal of the flip-flop 209 is connected through the gates 212 and 214 in series to the zero input terminal of the flip-flop 207.

The one input terminal of the flip-flop 210 is connected to the output terminal 2057 of the set of gates 205 and its zero input terminal is connected through an OR gate 218 to the terminal 222 and to the output terminal 2050 of the set of gates 205. The one output terminal RM₀ of the flip-flop 210 is connected through the gates 213, 214 in series to the zero input terminal of the flip-flop 207, and to an output terminal 223 connected to the input terminal 142 of the set of gates 130. The zero output terminal $\overline{RM}_0$ of the flip-flop 210 is connected by an output terminal 224 to the input terminal 143 of the set of gates 130. The output terminal of the gate 213 is connected to an output terminal 225 connected to the input terminal 141 of the set of gates 130. The gate 214 has a third input terminal which is connected to the terminal 222. The output terminal 2050 of the set of gates 205 is connected to an input terminal 82 of the warning circuit 800. The output terminal 2052 is connected to an input terminal 41 of the control circuits 400. The output terminal 2054 is connected to an input terminal 34 of the order register 300. The output terminal 2055 is connected to the input terminal of the delay circuit 900 and to an input terminal 68 of the test analysis circuit 600. The output terminal 2056 is connected to the input terminal 35 of the order register 300, to the input terminal 43 of the control circuits 400 and to the input terminal 67 of the test analysis circuit 600. The output terminal 2057 is connected to an input terminal 32 of the order register 300.

FIG. 6 is a diagram of the order register 300. This latter comprises two bistable flip-flops 301, 302, and two AND gates 303, 304. The one input terminal of the flip-flop 301 is connected through the input terminal 31 to the output gate 133, of the seizing circuit 100 and its zero input terminal is connected through an OR gate 306 to the input terminal 32 connected to the terminal 2057 of the stage programmer 200 and to an input terminal 33 connected to the output terminal 137 of the seizing circuit 100. The one and zero output terminals of the flip-flop 301 are connected, respectively, to an input terminal of the gates 303, 304. The one output terminal of the flip-flop 301 is connected moreover to an output terminal 36 which is connected to an input terminal 71, of the fault circuit 700. The one input terminal of the flip-flop 302 is connected to the terminal 34 and its zero input terminal is connected through an OR gate 310 to the terminals 33 and 35. The one output terminal of the flip-flop 302 is connected to the second input terminals of the gates 303 and 304. The output terminals 37 and 38 of the latter are connected, respectively, to input terminals 57 and 58 of the set of testers 500.

FIG. 7 is a diagram of the set of control circuits 400 which comprises a line address register 401 and a column address register 402 associated respectively with decoders 403 and 404. The decoder 403 has q output terminals, each being connected to one extremity of the energizing coil of reed relay 405₁ to 405_q, which has a single line-designation contact, this relay having its other extremity connected to a positive +12 volt source, for example. The decoder 404 has r output terminals, each being connected to one extremity of the energizing coil of a reed relay 406₁ to 406_r, which has a single column-designation contact, this relay having its other extremity connected to the positive +12 volt source. The sole contact of each of the reed relays 406₁ to 406_r connects a set of control connections 47₁ to 47_q, 47_{q+1} to 47_{2q}, ..., 47_{n-q} to 47_n, of the relays 21₁ to 21_q, 21_{q+1} to 21_{2q}, ..., 21_{n-q} to 21_n, to an output terminal 44 connected to an input terminal 56 of the set of testers 500. The sole contactor of each of the reed relays 405₁ to 405_q connects the one output terminal of a flip-flop 408 to the energizing coils of a set of reed relays such as 407₁ to 407_q, each possessing multiple contacts and supplied by the positive +12 volt source. The contacts of the set of relays 407₁ (only one relay 407₁ has been represented but there are four such relays) are inserted in the first connection 47₁, 47_{q+1}, ... of each set of actuating connections of the relays 21₁ to 21_n. The set of relays 407₂ analogously controls the second connection 47₂, 47_{q+2}, ... of each set of actuating connections and the set of relays 407_q controls the final connection 47_q, 47_{2q}, ..., 47_n of each set of actuating connections.

For example, if the signalling distributor 10 actuates $n=768$ relays 21₁ to 21₇₆₈, these may be divided into $r=16$ sets of $q=48$ relays, wherefrom it results that $k=6$ and $l=4$. Each relay 407₁ to 407₄₈ has to actuate 16 contacts which is too much for a single relay. Accordingly 407₁, for example, does not designate a relay with 16 contacts but four relays with 4 contacts each.

The one input terminal of the flip-flop 408 is connected through a terminal 41 to the output terminal 2052 of the stage programmer 200. The zero input terminal of the flip-flop 408 is connected, by means of an OR gate 409 having two input terminals 42, 43, to the output terminal 137 of the seizing circuit 100, and to the output terminal 2056 of the stage programmer 200. The register 401 is controlled in parallel through k input terminals 45₁ to 45_k connected, respectively, to the first k of the output gates 133₁ to 133_k of the seizing circuit 100 and the L input terminals 46₁ to 46_L of the register 402 are connected, respectively, to the L following gates 133 which complete the address of the relay to be actuated. The output terminals of the registers 401 and 402 are connected separately by output terminals 48₁ to 48_k to input terminals 71₁ to 71_k of the fault circuit 700. There are the following relationships between the numbers k, l, r, q and j :

$$2^k = q \quad 2^l = r \quad k + l = j - 2$$

FIG. 8 is a diagram of the set of testers 500. This set comprises a connection amplifier 51 which is associated with a

connection test unit 52 and a disconnection amplifier 53 associated with a disconnection test unit 54.

The connection amplifier 51 comprises a NPN transistor 511 having its emitter grounded and its collector connected through the test unit 52 and the input terminal 56 to the output terminal 44 of the set 400, and a NPN transistor 512 for control of the transistor 511. The bases of the transistors 511 and 512 are biased through potential dividers grounding the positive terminal of a +12 volt source. The emitter of the transistor 512 is grounded, its collector is connected to the base of the transistor 511 and its base is connected through an input terminal 57 to the output terminal 37 of the order register 300. The test unit 52 comprises an input NPN transistor 521 whereof the base is connected to the terminal 56 and connected through a diode 522 to its own emitter and to the collector of the transistor 511. The collector of the transistor 521 is connected to the base of a NPN transistor 523 positively biased by a potential divider between the +12 volt source and ground and having its emitter grounded. The collector of the transistor 523 is connected to an input terminal of an OR gate 55 whose output terminal 59 is connected to the input terminal 64 of the test analysis circuit 600.

The amplifier 53 comprises a NPN transistor 531 whose collector is connected to the terminal 56 through a resistor 532, and the emitter is connected to the +12 volt source through the test unit 54. It also comprises two NPN transistors 533, 534 whereof the bases are positively biased by potential dividers between the +12 volt source and ground and whereof the emitters are grounded. The base of the transistor 533 is connected through an input terminal 58 to the output terminal 38 of the order register 300. Its collector is connected to the base of the transistor 534. The collector of the latter is connected through a resistor 535 to the +12 volt source and through a resistor 536 to the base of the transistor 531, itself connected to ground through a resistor 537. The test unit 54 comprises a NPN transistor 531 and connected to the +12 volt source through a resistor 542. The emitter of the transistor 543 is connected to the +12 volt source and its collector is connected to ground through a resistor 545 on the one hand, and on the other hand through a resistor 546 to the base of PNP transistor 544 itself connected to ground through a resistor 547. The emitter of the transistor 544 is grounded and its collector is connected to the second input terminal of the gate 55.

FIG. 9 is a diagram of the test analysis circuit 600. This circuit comprises a flip-flop 60 having its one input terminal connected to the output terminal of an AND gate 61 having two input terminals 64, 65 connected, respectively, to the output terminal 59 of the set of testers 500 and to an output terminal 91 of the delay circuit 900, its zero input terminal being connected to the output terminal of an OR gate 62 having two input terminals 66, 67 connected, respectively, to the output terminal 137 of the seizing circuit 100 and to the output terminal 2056 of the stage programmer 200, its one output terminal being connected to an input terminal of a gate 63 having three input terminals whereof another normal input terminal is connected to the output terminal 2055 of the stage programmer 200 and blocking input terminal being connected to its input terminal 64.

FIG. 10 is a diagram of the fault circuit 700. This circuit comprises a checking circuit 701 for verification of the parity of the totality of the bits fed to its input terminals, these bits being the address bits of the relay to be actuated which are fed through the output terminals 48₁ to 48_{1,2} of the registers 401 and 402 to its input terminals 71₁ to 71_{1,2}, the order bit applied through the output terminal 36 of the register 300 to its input terminal 71, when the order to be obeyed represents a connection, and the additional parity bit applied to its input terminal 71_{1,1} through gate 133_{1,1}. The output terminal of the circuit 701 provides a signal for as long as there is no error in parity. It is connected on the one hand to the blocking input terminal of a gate 702, and on the other hand through an output terminal 72 to the input terminal 139 of the seizing circuit

100. The second input terminal of the blocking gate 702 is connected through the terminal 73 to the output terminal of the gate 132 of the seizing circuit 100. The output terminal of the gate 702 is connected through an OR gate 703 to the one input terminal of a fault flip-flop 704. The second input terminal of the gate 703 is connected to the output terminal 92 of the delay circuit 900 through an input terminal 74. The zero input terminal of the flip-flop 704 is connected through an input terminal 75 to the output terminal of gate 137 of the seizing circuit 100.

FIG. 11 is a diagram of the warning circuit 800. The latter comprises a flip-flop 801 whose zero input terminal 81 is connected to the output terminal of a gate 134 of the seizing circuit 100 and the zero input terminal is connected to the output terminal of a blocking gate 802 whereof the first input terminal 82 is connected to the output terminal 2050 of the stage programmer, and the blocking input terminal is connected to the input terminal 81. The zero output terminal of the flip-flop 801 is connected through an amplifier 803 to one extremity of the energizing coil of a relay 804 whose other extremity is connected to a +12 volt source and which is shunted by means of a capacitor 805 and a resistor 806 in series delaying its deactivation, for example by 30 milliseconds. The relay 804 has an contactor 807 grounded the circuit of a warning light 808 connected on the other hand to the +12 volt source, and is connected through a diode 809 to an output terminal 83.

The delay circuit 900 is a counter progressing by one unit for each pulse received from the output terminal 2055 of the stage programmer and supplying a signal through its output terminal 91 to the input terminal 65 of the test analysis circuit 600 at the fourth progression pulse and through its output terminal 92 to the input terminal 74 of the fault circuit 700 at the twenty-fourth progression pulse.

When one of the control computers computers, say 1_a, for example, has decided to activate or deactivate one of the relays 21₁ to 21_n referred to hereinafter as 21, coordinated with the signalling distributor 10, the control computer supplies the latter through the switching circuit 2 with a reservation signal to its terminal 101 and with a designation signal through its terminal 105. If the conditions of availability of the distributor 10 are fulfilled, the part of the reservation signal which is not suppressed by the delay line 121 passes the gate 111 and on the one hand activates the reservation flip-flop 112 thereby activating the flip-flop 801 of the warning circuit 800 via gate 134 and terminal 81, on the other hand is transmitted through the terminal 106 and the switching circuit 2, in the guise of a report of availability, to the control computer 1_a. The latter then feeds a seizing signal to the terminal 102, and in parallel to the terminals 103, to 103, the totality of the bits forming the address of the relay to be actuated, the order for connection or disconnection, and the additional parity bit. The flip-flop 112 being activated and the designation signal equally being present at the input terminal of the gate 113, the latter transmits the seizing signal to the stepped delay circuit 114, the latter dividing this signal into three pulses J, K, L appearing consecutively at its terminals 1143, 1144, 1145. The first is fed to the gate 135 and through the latter to the gate 137 which delivers a general zero reset signal Rz to the exclusion of the reservation flip-flops 112, 112_b. The pulse K activates the flip-flop 115 and opens the set of gates 116 so that the bits forming the address of the relay 21 to be actuated are fed by the gates 133₁ to 133_k to the input terminals 45₁ to 45_k of the set of control circuits 400 for the line address which is thus registered in the register 401, and by the gates 133_{k+1} to 133_{1,2} to the input terminals 46₁ to 46_{1,2} for the column address which is registered in the register 402, and from the registers 401, 402 through the terminals 48₁ to 48_{1,2} to the input terminals 71₁ to 71_{1,2} of the fault circuit 700. The order bit is fed through the gate 131, to the activating input terminal 31 of the flip-flop 301 of the order register 300 which thus comes into operation for a connecting order and remains idle for a disconnecting order, and from the operating output terminal 36 of this flip-flop to the input terminal 71, of the fault circuit

which is fed moreover from the gate 133₁ of the seizing circuit 100 with the parity bit. If the word formed by these bits has an odd number of bits, the output terminal 72 of the circuit 701 feeds, via terminal 139, an opening signal to the gate 138 which feeds the pulse L to the input terminal 220 of the stage programmer 200 as soon as it is received from the output terminal 1145 of the circuit 114. This same pulse L transmitted by the gate 132 to the terminal 73 of the fault circuit cannot pass the gate 702 which is inhibited by the output signal of the circuit 701. In case of lack of parity, the gate 138 remains closed so that the stage programmer 200 remains inoperative and the pulse L activates the flip-flop 704 of the fault circuit 700 whereof the output terminal 76 supplies the input terminal 140 of the seizing circuit 100 with a fault signal which is transmitted by the output terminal 107 to the switching circuit 2 and to the control computer 1_A.

When the pulse L is fed to the input terminal 220 of the stage programmer 200, the flip-flop 208 is activated so that the first pulse u of the time base 201 operating permanently causes the activation of the flip-flop 207 to open the gate 206, as well as the set of gates 203. The pulse t then causes the progression of the counter 202 initially set to zero, whilst simultaneously opening the set of gates 205, thus determining stages Φ_0 , Φ_2 , Φ_4 to Φ_7 , characterized, respectively, by the presence of a signal at the output terminals 2050, 2052 and 2054 to 2057 of the set of gates 205. The first pulse t determining the stage Φ_0 , resets the flip-flop 801 of the warning circuit 800 to zero and thus reestablished a supply to the relay 804 which has been interrupted on the occasion of the activation of the reservation flip-flop 212. The delay of 30 milliseconds caused by the capacitor 805 and the resistor 806 which shunt the coil of the relay 804 ensures that the latter does not release and does not trigger a warning through its idle contactor unless the distributor 10 is blocked.

At the same time, the line and column addresses of the relay to be actuated, which are registered in the registers 401 and 402, are decoded by the decoders 403 and 404 and cause the energization of one of the line relays 405₁ to 405₅, and of one of the column relays 406₁ to 406₅. The next pulse t establishes a stage Φ_1 , waiting for the closing of these reed-type relays. The output terminal 2052 of the stage programmer 200 being connected to the activating terminal 41 of the flip-flop 408, the stage Φ_1 causes the grounding of the energizing circuit of the sets 407₁ to 407₅, each comprising four reed-type relays having each four contactors, which is actuated by the line relays 405₁ to 405₅ in operation. The next pulse t establishes a stage Φ_2 , waiting for the closing of the sixteen contactors thus actuated. Thereafter, the energizing coil of the relay 21 to be actuated is connected by the terminal 44 of the control circuits 400 to the terminal 56 of the set of the testers 500, and by the latter, in parallel, to the base of the transistor 521 of the connection test unit 52, and through the resistor 532 to the collector of the transistor 531 of the disconnection amplifier 53.

In the stage Φ_4 , signal is fed by the terminal 2054 to the input terminal 34 for activation of the flip-flop 302 of the order register 300. If the order digit fed to the input terminal 103, of the seizing circuit is equal to 1, the flip-flop 301 is operative and a signal on terminals 37 and 57 brings the base of the transistor 512 to ground potential and blocks the same so that transistor 511 becomes conducting and connects to ground, through the diode 522, the two half-windings in series of the relay 21 actuated, supplied by the +12 volt source. The voltage thus appearing at the terminals of the diode 522 saturates the transistor 521 which blocks the transistor 523. The resulting signal is fed by the latter to the terminal 59 of the set of testers 500 and 64 of the test analysis circuit 600, inhibiting the output gate 63 of the latter. The actuated relay 21 coming into operation, its holding contactor grounds the point common to its two semiwindings and the diode 522 no longer being traversed by any current, the transistor 521 is blocked and saturates the transistor 523 which restores ground potential at the input terminal 64 of the test analysis circuit 600.

The terminal 2054 being connected to the zero input terminal of the flip-flop 208 and to the one input terminal of the flip-flop 209, the first pulse u following passage to stage Φ_4 , deactivates the flip-flop 207, thus stopping the counter 202 in the position Φ_5 and opens the set of gates 203 so that each pulse t fed to the opening input terminal of the set of gates 205 causes a stage pulse Φ_5 to appear at the terminal 2055. The first of these pulses Φ_5 resets the flip-flop 209 and consequently closes the gate 212. The terminal 2055 is connected moreover to the counting input terminal of the time-lagging circuit 900 and to the input terminal 68 of the output gate 63 of the test analysis circuit 600. The fourth pulse Φ_5 causes the application through the output terminal 91 of the time-lagging circuit 900 of a pulse to the input terminal 65 of the gate 61 which causes the activation of the flip-flop 60 of the circuit 600. The holding contactor of the actuated relay 21 lacking time to close, the energizing current passing through the diode 522 keeps the gate 61 open and the flip-flop 60 is activated, but it is only after the closing of the holding contactor 25 and the disappearance of the energizing current at the input terminal of the test unit 52 that the pulse Φ_5 can pass through the gate 63 and reactivate the flip-flop 208 to restart the progression of the counter 202. If the twenty-fourth pulse Φ_5 occurs in the meantime, a pulse is fed through the output terminal 92 of the time-lagging circuit 900 to the terminal 74 of the circuit 700 and the fault flip-flop 704 feeds a fault signal from its output terminal 76 to the input terminal 140 of the distributor 10 which is transmitted by the gate 117 and the terminal 107 to the switching circuit 2 for the control computer 1_A. When the latter has located the distributor 10 which thus remains blocked, it frees the same by feeding it through the terminal 104, the gate 118 and the gates 136, 137, a general reset signal $Rz + RzR$ which is transmitted by the gate 136 to the reservation flip-flops 112, 112_B as well as, through the gate 137, to the other flip-flops and circuits specified in the foregoing.

If the order bit fed to the input terminal 103, of the seizing circuit is zero and thus to the input terminal 31 of circuit 300, when the flip-flop 302 of the order register 300 is activated in the stage Φ_4 , the flip-flop 301 is deactivated and the signal at the output terminal 38 of the gate 304 which is open brings the base of the transistor 533 to ground potential and blocks the same, so that the transistors 534 and 531 are saturated. The latter establishes the connection to the +12 volt supply, through the resistor 542, of the semiwinding 22 of the actuated relay 21, grounded at its other extremity through its holding contactor 25. The voltage drop across resistor 542 blocks the transistor 541. This unblocks the transistor 543 which saturates the transistor 544 whose collector feeds a signal at ground potential to the terminal 59 of circuit 500 and 64 of circuit 600. The two semiwindings 22 and 23 of the relay 21 actuated being in magnetic flux opposition however, this relay is deactivated, the current ceases to flow in the resistor 542 of the test unit 54 and the transistor 544 is blocked. The test analysis circuit 600 thus operates in the same manner as for a connecting order. To summarize, a satisfactory operation of the actuated relay is characterized by the appearance followed by the disappearance within specific periods, of a current on the common return connection which traverses the set of testers 500.

When the counter 202 is placed in operation again following a positive test, a pulse Φ_5 is transmitted through the terminal 2056 of the stage programmer 200 to the terminal 35 of the order register 300 resetting the flip-flop 302, to the terminal 43 of the control circuits 400 resetting the flip-flop 408, and to the terminal 67 of the test analysis circuit 600 resetting the flip-flop 60. The pulse Φ_7 which then appears at the terminal 2057 resets the flip-flop 208 and activates the flip-flop 210 blocking the availability gates 111, 111_B, and unblocking the gates 123, 123_B. It equally resets the flip-flop 301 of the order register 300. The next pulse u passes through gate 213, is transmitted by the terminal 225 to the terminal 141 as a pulse RzP for zero reset of the flip-flops 112, 115, and resets the flip-flop 207. The counter 202 is stopped at its zero posi-

tion. The corresponding signal is decoded by the decoder 204 and appears at the next pulse t on the terminal 2050 where it forms the pulse Φ_0 for deactivation of the flip-flop 210.

The invention has been described in detail in the foregoing in respect of an embodiment in which the distributor 10 actuates no more than one relay during each connecting operation. Reverting to FIG. 7, it is apparent that terminals 49₁, 49₂, ..., 49_n, which have not been referred to until now, are connected respectively to the common points of the connections 47₁ to 47_n, 47_{q+1} to 47_{2q}, ..., 47_{n-q} to 47_n. FIG. 12 demonstrates how such additional output terminals of the control circuits render it possible to actuate several relays at the same time thanks to the addition of as many column address registers 402', coordinated decoders 404', column relays 406', to 406'_n, and sets of testers 500', as it is intended to actuate additional relays of the set of relays 21₁ to 21_n. The signalling relays 21 and 21' to be actuated mandatorily appertain to two different sets, that is to say are connected to different terminals 49₁ to 49_n, and are situated on the same line. The selection of the first relay 21 occurs as in the preceding case by means of the control circuits 400 whereof the output terminal 44 is connected to the input terminal 56 of the set of testers 500. The sole difference is that the output terminal 59 of the set 500 is not connected direct to the input terminal 64 of the test analysis circuit 600 but is connected to the same through an "AND" gate 590. The column address of the second relay 21' is applied in analogous manner to the input terminals 46'₁ to 46'_n of the register 402', decoded by the decoder 404' which activates the appropriate relay 406'₁ to 406'_n, thus connecting the corresponding terminal 49₁ to 49_n to the input terminal 56' of the set of testers 500' which is identical to 500. The output terminal 59' of the set of testers 500' is connected to the second input terminal of the gate 590 so that the analysis of the connection or disconnection tests of the relays 21 and 21' is performed in a single operation by the circuit 600.

We claim:

1. A system for selectively energizing and deenergizing a plurality of signalling and control electromagnetic relays divided into several groups each arranged in a junctor of a switching network under the control of at least two control computers, each of said relays having first and second half-windings and a holding contact, said half-windings being interconnected at a common point, said common point being connected to the grounded holding contact of the relay, the terminal of the first half-winding being connected to a voltage source and the terminal of the second half-winding being the connection and disconnection control terminal of the relays, said system comprising a plurality of seizing circuits each associated with a group of relays, means for allowing each of said seizing circuits to be selectively seized by one of the control computers and to be thereby marked engaged, an address register, an address crosspoint matrix controlled by said address register, each crosspoint of the matrix being associated with a relay having its connection and disconnection control terminal connected thereto, a connection and disconnection control terminal connected thereto, a connection and disconnection

nection order register, means for transmitting, through one seizing circuit, from one control computer a relay address signal to said address register and a selective connection and disconnection order signal to said order register, means for actuating the crosspoint of said matrix corresponding to the transmitted relay address signal and for preparing a continuous path for the relay feed current, means for selectively closing the path thus prepared to ground and to the voltage source according to the connection order signal and disconnection order signal received by the order register, means for deriving from the feed current in said path a connection and disconnection check signal and means for sending to the control computer a fault signal when the time-interval between said order signal and said connection and disconnection check signal reaches a predetermined value.

2. A system for selectively energizing and deenergizing a plurality of signalling and control electromagnetic relays divided into several groups each arranged in a junctor of a switching network under the control of at least two control computers, each of said relays having first and second half-windings and a holding contact, said half-windings being interconnected at a common point, said common point being connected to the grounded holding contact of the relay, the terminal of the first half-winding being connected to a voltage source and the terminal of the second half-winding being the connection and disconnection control terminal of the relay, said system comprising a plurality of seizing circuits each associated with a group of relays, means for allowing each of said seizing circuits to be selectively seized by one of the said seizing circuits to be selectively seized by one of the control computers and to be thereby marked engaged, an address register, an address crosspoint matrix controlled by said address register, each crosspoint of the matrix being associated with a relay having its connection and disconnection control terminal connected thereto, a connection and disconnection order register, a code checking circuit, means for transmitting, through one seizing circuit, from one control computer a relay address binary digit signal to said address register, a selective connection and disconnection order binary digit signal to said order register and a parity binary digit signal to said code checking circuit, the sum of the binary digits of the address signal and the order signal being an even number, means for actuating the crosspoint of said matrix corresponding to the transmitted relay address signal and for preparing a continuous path for the relay feed current, means for selectively closing the path thus prepared to ground and to the voltage source according to the connection order signal and disconnection order signal received by the order register, means for deriving from the feed current in said path a connection and disconnection check signal and means controlled by both said code checking circuit and said deriving means for sending to the actuating unit a fault signal when the sum of the binary digits of the address signal and the order signal is not an even number and when the time-interval between said order signal and said connection and disconnection check signal reaches a predetermined value.