A power-up signal generator for a semiconductor memory device that uses the deep power down power-up signal for a semiconductor element, which should be in a standby state in the deep power down entry, and the power-up signal for an initialization of another semiconductor elements in a DRAM device that operates after an internal power supply voltage is generated is disclosed. The generator also uses the power-up signal, which is disabled in the deep power down entry and enabled in a deep power down exit by the internal power supply voltage. The generator may include a power-up detector for generating a power-up detection signal by means of an external power supply voltage, a deep power down power-up signal generator for generating a deep power down power-up signal in response to the power-up detection signal, a power-up signal generator for generating a power-up signal in response to the power-up detection signal and power-up controller for determining whether or not enable the power-up signal in the deep power down entry.
Fig. 1
(Prior Art)
Fig. 2
(Prior Art)
Fig. 7A
Fig. 7C
Fig. 8
Fig. 9
Fig. 10
POWER-UP SIGNAL GENERATOR FOR SEMICONDUCTOR MEMORY DEVICES

CROSS-REFERENCE TO RELATED APPLICATION

[0001] This is a divisional of application Ser. No. 10/255,999, filed on Sep. 26, 2002, now U.S. Pat. No. ______, which is incorporated herein by reference.

BACKGROUND

[0002] The present invention relates to power-up signal generators for semiconductor memory devices and, more particularly, to a power-up signal generator for generating a power-up signal that is disabled during a deep power down entry and enabled by an internal power supply voltage during a deep power down exit.

[0003] A deep power down entry designates a state in which all internal power supply voltages used inside a dynamic random access memory (DRAM) device are turned off to reduce a standby current drain when the DRAM device is not used for a period time. A power-up signal is a signal indicating that a DRAM device is able to operate normally. When the power-up signal is enabled at a high level, the DRAM device operates normally.

[0004] FIGS. 1 and 2 are circuit diagrams of power-up signal generators known in the prior art. The power-up signal generator includes a voltage divider 11 for dividing an external power supply voltage Vext, a pull-up unit 12 for pulling-up a divided voltage A, a driving unit 16 for receiving the divided voltage A to generate a power-up detection signal DET for determining the time that a power-up signal PWRUP is enabled, and a driving unit 15 for receiving the power-up detection signal DET to generate the power-up signal PWRUP. The driving unit 16 includes a pull-up unit 14 for pulling-up the power-up detection signal DET and a pull-down unit 13 for pulling-down the power-up detection signal DET.

[0005] The voltage divider 11 includes resistors R1 and R2 connected in series between the external power supply voltage Vext and a ground voltage Vss. The pull-up unit 12 includes a NMOS transistor N1 that is connected between the external power supply voltage Vext and a node SN1 and the divided voltage A is applied to its gate. The pull-down unit 13 includes an NMOS transistor N2 connected between an output node SN2 and the ground voltage Vss. The divided voltage A is applied to a gate of the NMOS transistor N2. The pull-up unit 14 includes a resistor R3 connected between the external power supply voltage Vext and the output node SN2. The driving unit 15 includes an inverter INV1 connected between the external power supply voltage Vext and the ground voltage Vss. The inverter INV1 inverts the power-up detection signal DET to output the power-up signal PWRUP.

[0006] The construction of the power-up signal generator of FIG. 2 is the same as that of the power-up signal generator of FIG. 1, except that a PMOS transistor P1 is used in the pull-up unit 14 instead of the resistor R3. Accordingly, a detailed description of FIG. 2 is omitted.

[0007] In the prior power-up signal generator, the power-up signal PWRUP is disabled at a low level until an internal power supply voltage, which is generated from the external power supply voltage Vext, reaches a stable level. The power-up signal PWRUP is enabled at a high level when the current flowing through the resistor R3 (FIG. 3) or the PMOS transistor P1 (FIG. 2) is larger than the current flowing through the NMOS transistor N2.

[0008] The power-up signal PWRUP is always enabled in a deep power down entry, as well as in a deep power down exit. The power-up signal PWRUP is always enabled because some semiconductor elements such as a clock buffer, or a mode register set, etc., should be in an operation state during the deep power down exit.

[0009] However, if the power-up signal PWRUP is enabled at a high level in a deep power down entry, the DRAM device operates in the state in which the internal power supply voltage is not generated. Accordingly, the semiconductor elements that operate by the internal power supply voltage will malfunction because the internal power supply voltage Vint is not provided thereto.

SUMMARY

[0010] It is an object of the present invention to prevent a malfunction in the deep power down entry by using a deep power down power-up signal which is always enabled for semiconductor elements which maintain at a stand by mode in the deep power down entry and using a power up signal which is disabled in the deep power down entry and enabled in a deep power down exit for semiconductor elements which operates after an internal power supply voltage is generated.

[0011] The disclosed apparatus may include a power-up detector for generating a power-up detection signal by means of an external power supply voltage; deep power down power-up signal generator for generating a deep power down power-up signal in response to the power-up detection signal, a power-up signal generator for generating a power-up signal in response to the power-up detection signal and a power-up controller for determining whether or not enable the power-up signal in a deep power down entry.

[0012] In another aspect, the disclosed apparatus may include a power-up detector for generating a power-up detection signal by means of an external power supply voltage, a deep power down power-up signal generator for receiving the power-up detection signal to generate a deep power down power-up signal and a power-up controller for receiving the power-up detection signal and a deep power down mode signal to generate a power-up control signal. The disclosed apparatus may also include a power-up signal generator for generating a power-up signal that is enabled or disabled in response to the power-up control signal.

[0013] In another aspect, the disclosed apparatus may include a deep power down power-up signal generator for generating a deep power down power-up signal by means of an external power supply voltage, power-up signal generator for generating a power-up signal by the means of an internal power supply voltage and power-up controller for determining whether or not enable the power-up signal in a deep power down entry.

BRIEF DESCRIPTION OF THE DRAWINGS

[0014] FIGS. 1 and 2 are circuit diagrams of power-up signal generators according to the prior art;
[0015] FIGS. 3 and 4 are circuit diagrams of a first type of power-up signal generators;

[0016] FIGS. 5 and 6 are circuit diagrams of a second type of power-up signal generators;

[0017] FIGS. 7A to 7C are detailed circuit diagrams of power-up controllers of FIGS. 5 and 6;

[0018] FIGS. 8 and 9 are circuit diagrams of a third type of power-up signal generators; and

[0019] FIG. 10 is a timing diagram of the power-up signal generator.

DETAILED DESCRIPTION

[0020] Turning now to FIGS. 3 and 4, the first type of power-up signal generators include a power-up detector 110, a deep power down power-up signal generator 120, a power-up signal generator 130 and a power-up controller 140.

[0021] The power-up detector 110 includes a voltage divider 111 for dividing an external power supply voltage Vext and a pull-up unit 112 for pulling-up a divided voltage A and a driving unit 115 for receiving the divided voltage A to generate a power-up detection signal DET for determining an enable time of a deep power down power-up signal DPD-PWRUP and a power-up signal PWRUP. The driving unit 115 includes a pull-up unit 114 for pulling-up the power-up detection signal DET and a pull-down unit 113 for pulling-down the power-up detection signal DET.

[0022] The voltage divider 111 includes resistors R11 and R12 connected in series between the external power supply voltage Vext and a ground voltage Vss. The pull-up unit 112 includes an NMOS transistor N11 connected between the external power supply voltage Vext and a node SN12 and has the divided voltage A applied to its gate. The pull-down unit 113 includes a NMOS transistor N12 connected between an output node SN12 and the ground voltage Vss. The divided voltage A is applied to the gate of N12. The pull-up unit 114 includes a resistor R13 connected between the external power supply voltage Vext and the output node SN12.

[0023] The power-up detector 110 outputs the power-up detection signal DET according to a current ratio of the resistor R13 and the NMOS transistor N12. The power-up detection signal DET determines the time that the deep power down power-up signal DPD-PWRUP and the power-up signal PWRUP are enabled. That is, when the current flowing through the resistor R13 (the PMOS transistor P12 of FIG. 4) is larger than the current flowing through the NMOS transistor N12, the power-up detector 110 outputs the power-up detection signal DET of a low level to enable the deep power down power-up signal DPD-PWRUP and the power-up signal PWRUP at a high level.

[0024] The inverter IV11 inverts the power-up detection signal DET. The deep power down power-up signal generator 120 includes inverters IV12 and IV13 connected between the external power supply voltage Vext and the ground voltage Vss. The inverters IV12 and IV13 invert an output signal of an inverter IV11 to generate the deep power down power-up signal DPD-PWRUP.

[0025] The deep power down power-up signal generator 120 generates the deep power down power-up signal DPD-PWRUP, which is always enabled in the deep power down entry as well as the deep power down exit.

[0026] The power-up signal generator 130 includes inverters IV14 and IV15 connected between the internal power supply voltage Vint and the ground voltage Vss. The inverters IV14 and IV15 invert the output signal of the inverter IV11 to generate the power-up signal PWRUP. The power-up signal generator 130 generates the power-up signal PWRUP, which is disabled at a low level in deep power down entry and enabled at a high level by the internal power supply voltage Vint in the deep power down exit.

[0027] The power-up controller 140 includes a PMOS transistor P11 with its source connected to the external power supply voltage Vext. A deep power down mode signal DPD is applied to its gate. In the deep power down entry, the deep power down mode signal DPD is at a high level and, therefore, the power-up controller 140 is not enabled and does not provide the external power supply voltage Vext to the power-up signal generator 130. In the deep power down exit, the deep power down mode signal DPD is at a low level and, therefore, the power-up controller 140 is enabled to provide the internal power supply voltage Vint from the external power supply voltage Vext. The internal power supply voltage Vint is, in turn, supplied to the power-up signal generator 130.

[0028] The construction of the power-up signal generator of FIG. 4 is substantially the same as that of the power-up signal generator in FIG. 3 except that a PMOS transistor P12 is used in the power-up detector 110 rather than the resistor R13 of FIG. 3. Accordingly, a detailed description of FIG. 4 is omitted.

[0029] Hereinafter, operation of the power-up signal generator of FIGS. 3 and 4 is described in brief. First, the deep power down power-up signal DPD-PWRUP is used as a clock enable buffer, or a mode register set, etc., which should be in a standby state in the deep power down entry. The power-up signal PWRUP is used for an initialization of other semiconductor elements in a DRAM device by means of the internal power supply voltage.

[0030] When the current flowing through the resistor R13 (FIG. 3) or the PMOS transistor P12 (FIG. 4) is larger than the current flowing through the NMOS transistor N12, the power-up detection signal DET transitions to a low level. When the power-up detection signal DET transitions to a low state, the deep power down power-up signal DPD-PWRUP and a power-up signal PWRUP become enabled at high levels.

[0031] At this time, the deep power down power-up signal DPD-PWRUP is always enabled at a high level in the deep power down entry and the deep power down exit. On the other hand, the power-up signal PWRUP is disabled at a low level in the deep power down entry and is enabled at a high state by the internal power supply voltage Vint from the PMOS transistor P11 in the deep power down exit.

[0032] In more detail, the deep power down mode signal DPD is at a high level in the deep power down power-up entry and, therefore, the PMOS transistor P11 turns off. Because the external power supply voltage Vext is not provided to the inverters IV14 and IV15, the power-up signal PWRUP is disabled at a low level. In the deep power down power-up exit, the deep power down mode signal
DPD is at a low level and therefore the PMOS transistor P11 turns on and the internal power supply voltage Vint is supplied from the external power supply voltage Vext. Because the internal power supply voltage is provided to the power-up signal generator 130, the power-up signal PWRUP is enabled at a high level by the internal power supply voltage Vint.

[0033] According to the apparatus shown in FIGS. 3 and 4, the deep power down power-up signal DPD-PWRUP is enabled at a high level in the deep power down entry and the deep power down exit. Apparatus shown in FIGS. 3 and 4 disable the power-up signal PWRUP at a low level in the deep power down entry and enable the power-up signal PWRUP at a high level in the deep power down exit. Therefore, the malfunction of the semiconductor chip device can be prevented in the deep power down entry.

[0034] FIG. 5 and FIG. 6 are circuit diagrams of a second type of power-up signal generators. The power-up signal generators include a power-up detector 210, a deep power down power-up signal generator 220, a power-up controller 230, and a power-up signal generator 240.

[0035] The power-up detector 210 includes a voltage divider 211 for dividing an external power supply voltage Vext, a pull-up unit 212 for pulling-up a divided voltage A, and a driving unit 215 for receiving the divided voltage A to generate a power-up detection signal DET for determining an enable time of a deep power down power-up signal DPD-PWRUP and a power-up signal PWRUP. The driving unit 215 includes a pull-down unit 213 for pulling-down the power-up detection signal DET and a pull-up unit 214 for pulling-up the power-up detection signal DET.

[0036] The voltage divider 211 includes resistors R21 and R22 connected in series between the external power supply voltage Vext and a ground voltage Vss. The pull-up unit 212 includes a PMOS transistor N21 with its source and its drain connected to the external power supply voltage Vext and a node SN21, respectively. The divided voltage A is applied to the gate of the NMOS transistor N21. The pull-down unit 213 includes a NMOS transistor N22 with its drain and its source are connected to an output node SN22 and the ground voltage Vss respectively. The divided voltage A is applied to the gate of the NMOS transistor N22. The pull-up unit 214 includes a resistor R23 connected between the external power supply voltage Vext and the output node SN22.

[0037] The power-up detector 210 outputs the power-up detection signal DET according to a current ratio of the resistor R23 and the NMOS transistor N22 and determines when the deep power down power-up signal DPD-PWRUP and the power-up signal PWRUP are enabled by the power-up detection signal DET. That is, when the current flowing through the resistor R23 (FIG. 5) or the PMOS transistor P21 (FIG. 6) is larger than the current flowing through the NMOS transistor N22, the power-up detector 210 outputs the power-up detection signal DET of a low level to enable the deep power down power-up signal DPD-PWRUP and the power-up signal PWRUP at high levels.

[0038] The deep power down power-up signal generator 220 includes inverters IV21, IV22 and IV23 connected between the external power supply voltage Vext and the ground voltage Vss. The inverters IV21-IV23 invert the power-up detection signal DET to generate the deep power down power-up signal DPD-PWRUP.

[0039] The deep power down power-up signal generator 220 generates the deep power down power-up signal DPD-PWRUP, which is always enabled in the deep power down entry and the deep power down exit.

[0040] The power-up controller 230 receives the power-up detection signal DET and the deep power down mode signal DPD and generates a power-up control signal PWRUPZ for controlling whether to enable the power-up signal PWRUP.

[0041] The power-up controller 230 may have the construction as shown in any of FIG. 7A through FIG. 7C.

[0042] The power-up controller 230, as shown in FIG. 7A, includes an inverter IV27 connected between the external power supply voltage Vext and the ground voltage Vss. The inverter IV27 inverts the power-up detection signal DET. An inverter IV28 is also connected between the external power supply voltage Vext and the ground voltage Vss and inverts the deep power down mode signal DPD. A NAND gate ND1 is connected between the external power supply voltage Vext and the ground voltage Vss and carries out NAND logic on the output signals of the inverters IV27 and IV28 to generate the power-up control signal PWRUPZ.

[0043] The power-up controller 230, as shown in FIG. 7B, includes a NOR gate NR1, connected between the external power supply voltage Vext and the ground voltage Vss, which carries out NOR logic on the power-up detection signal DET and the deep power down mode signal DPD. An inverter IV29, which is connected between the external power supply voltage Vext and the ground voltage Vss, inverts an output signal of the NOR gate NR1 to generate the power-up control signal PWRUPZ.

[0044] The power-up controller 230, as shown in FIG. 7C, includes an inverter IV30 that is connected between the external power supply voltage Vext and the ground voltage Vss and inverts the deep power down mode signal DPD. A PMOS transistor P22 has its source and its drain connected to the external power supply voltage Vext and an output stage, respectively. An output signal of the inverter IV30 is applied to the gate of the PMOS transistor P22. A transfer gate T1 receives the power-up detection signal DET to generate the power-up control signal PWRUPZ under the control of the deep power down mode signal DPD and the output signal of the inverter IV30.

[0045] Returning to FIG. 6, the power-up signal generator 240 includes inverters IV24, IV25 and IV26, each of which is connected between the external power supply voltage Vext and the ground voltage Vss. The inverters IV24-IV26 invert the power-up control signal PWRUPZ to generate the power-up signal PWRUP. The power-up signal generator 240 generates the power-up signal PWRUP, which is disabled at a low level in the deep power down entry and is enabled at a high level in the deep power down exit.

[0046] The construction of the power-up signal generator of FIG. 6 is the substantially same as that of the power-up signal generator of FIG. 5, except that a PMOS transistor P21 is used in the power-up detector 210 instead of the resistor R23. Accordingly, a detailed description of FIG. 6 is omitted.

[0047] Hereinafter, an operation of the second type of power-up signal generators is described in brief.
[0048] The deep power down power-up signal DPD-PWRUP is always enabled at a high level in the deep power down entry and the deep power down exit. On the other hand, the power-up signal PWRUP is disabled at a low level in the deep power down entry and is enabled at a high state in the deep power down exit.

[0049] In more detail, the deep power down mode signal DPD is at a high level in the deep power down entry and therefore the power-up control signal PWRUPZ transitions to a high level and the power-up signal PWRUP becomes disabled at a low level. In the deep power down exit, the deep power down mode signal DPD is at a low level and the power-up control signal PWRUPZ transitions to a low level and the power-up signal PWRUP becomes enabled at a high level.

[0050] The second type of power-up signal generators enable the deep power down power-up signal DPD-PWRUP at a high level in the deep power down entry and the deep power down exit. According to the power-up control signal PWRUPZ, the power-up signal PWRUP is disabled at a low level in the deep power down entry power-up signal PWRUP is enabled at a high level in the deep power down exit. Therefore, the malfunction of the semiconductor chip device can be prevented in the deep power down entry.

[0051] Next, power-up signal generators of a third type are described in more detail with reference to the accompanying FIGS. 8 and 9.

[0052] FIGS. 8 and 9 are circuit diagrams of the power-up signal generators of the third type. The power-up signal generators include a deep power down power-up signal generator 310, a power-up signal generator 320, and a power-up controller 330.

[0053] The deep power down power-up signal generator 310 includes a voltage divider 311 for dividing an external power supply voltage Vext, a pull-up unit 312 for pulling-up a divided voltage A, and a driving unit 315 for receiving the divided voltage A to generate a power-up detection signal DET and a driving unit 316 for receiving the power-up signal detection signal DET to generate a deep power down power-up signal DPD-PWRUP. The driving unit 315 includes a pull-up unit 314 for pulling-up the power-up detection signal DET and a pull-down unit 313 for pulling-down the power-up detection signal DET.

[0054] The voltage divider 311 includes resistors R31 and R32 connected in series between the external power supply voltage Vext and a ground voltage Vss. The pull-up unit 312 includes a NMOS transistor N31 with its source and its drain connected to the external power supply voltage Vext and a node SN31, respectively. The divided voltage A is applied to the gate of the NMOS transistor N31. The pull-down unit 313 includes a NMOS transistor N32 with its drain and its source connected to an output node VN32 and the ground voltage Vss, respectively. The divided voltage A is applied to the gate of the NMOS transistor N32. The pull-up unit 314 includes a resistor R33 connected between the external power supply voltage Vext and the output node SN32. The driving unit 316 includes inverters IV31, IV32 and IV33 connected between the external power supply voltage Vext and the ground voltage. The inverters IV31-IV33 invert the power-up detection signal DET to generate the deep power down power-up signal DPD-PWRUP.

[0055] The deep power down power-up signal generator 310 generates the deep power down power-up signal DPD-PWRUP, which is always enabled at the high power down entry and the deep power down exit.

[0056] The power-up signal generator 320 includes a voltage divider 331 for dividing an internal power supply voltage Vint, a pull-up unit 332 for pulling-up a divided voltage A, a driving unit 335 for receiving the divided voltage A to generate a power-up detection signal DET, and a driving unit 336 for receiving the power-up detection signal DET to generate a power-up signal PWRUP. The driving unit 335 includes a pull-up unit 334 for pulling-up the power-up detection signal DET and a pull-down unit 333 for pulling-down the power-up detection signal DET.

[0057] The voltage divider 331 includes resistors R34 and R35 connected in series between the internal voltage Vint and the ground voltage Vss. The pull-up unit 332 includes a NMOS transistor N33 connected between the internal power supply voltage Vint and a node SN33. The divided voltage A is applied to the gate of the NMOS transistor N33. The pull-down unit 333 includes a NMOS transistor N34 with its drain and its source connected to an output node SN34 and the ground voltage Vss, respectively. The divided voltage A is applied to the gate of the NMOS transistor N34. The pull-up unit 334 includes a resistor R36 connected between the internal power supply voltage Vint and the output node SN34. The driving unit 336 includes inverters IV34, IV35 and IV36 connected between the internal power supply voltage Vint and the ground voltage Vss. The inverters IV34-IV36 invert the power-up detection signal DET to generate the power-up signal PWRUP.

[0058] The power-up signal generator 320 generates the power-up signal PWRUP, which is disabled at a low level in the deep power down entry and enabled at a high level in the deep power down exit.

[0059] The power-up controller 330 includes a PMOS transistor P31 with its source connected to the external power supply voltage. The deep power down mode signal DPD is applied to the gate of the PMOS transistor P31.

[0060] In the deep power down entry, the deep power down mode signal DPD is at a high level, and the power-up controller 330 having the above construction turns off the PMOS transistor P31 and, therefore, does not provide the external power supply voltage Vext. In the deep power down exit, the deep power down mode signal DPD is at a low level, which enables the PMOS transistor P31 and generates the internal power supply voltage Vint from the external power supply voltage Vext and provides the internal power supply voltage Vint to the power-up signal generator 320.

[0061] The construction of the power-up signal generator of FIG. 9 is substantially the same as that of the power-up signal generator of FIG. 8 except that PMOS transistors P32 and P33 are used in the deep power down power-up signal generator 310 and the power-up signal generator 320 instead of the resistors R33 and R36. Accordingly, a detailed description of FIG. 9 is omitted.

[0062] Hereinafter, operation of the third type of power-up signal generators is described in brief.

[0063] The deep power down power-up signal DPD-PWRUP is always enabled at a high level in the deep power
down entry and the deep power down exit. On the other hand, the power-up signal PWRUP is disabled at a low level in the deep power down entry and is enabled at a high level in the deep power down exit.

In more detail, the deep power down mode signal DPD is at a high level in the deep power down entry and, therefore, the PMOS transistor P31 turns off. The external power supply voltage Vext is not provided and the power-up signal PWRUP becomes disabled at a low level. In the deep power down exit, the deep power down mode signal DPD is at a low level and the PMOS transistor P31 turns on. The internal power supply voltage Vint, which is made from the external power supply voltage Vext, is provided to the power-up signal generator 320 and the power-up signal PWRUP is enabled at a high level by the internal power supply voltage Vint.

The third type of power-up signal generators enable the deep power down power-up signal DPD-PWRUP at a high level in the deep power down entry as well as the deep power down exit. The third type of power-up signal generators disables the power-up signal PWRUP at a low level in the deep power down entry and enables the power-up signal PWRUP at a high level in the deep power down exit. Therefore, the malfunction of the semiconductor chip device can be prevented in the deep power down entry.

FIG. 10 is an operation waveform of the deep power down power-up signal DPD-PWRUP and the power-up signal PWRUP according to the deep power down mode signal DPD. Referring to FIG. 10, the deep power down power-up signal DPD-PWRUP is continuously enabled at a high level. The power-up signal PWRUP is disabled at a low level in the deep power down entry and, therefore, the internal power supply voltage is not provided.

The disclosed apparatus uses a deep power down power-up signal that is always enabled for semiconductor elements that maintain at a standby mode in the deep power down entry. The disclosed apparatus also uses a power-up signal that is disabled in the deep power down entry and enabled in a deep power down exit for semiconductor elements that operate after an internal power supply voltage is generated, thereby preventing malfunction of the semiconductor elements during the deep power down entry.

The disclosed apparatus generates the deep power down power-up signal that is always enabled at a high level in the deep power down entry and the deep power down exit. The power-up signal is disabled at a low level in the deep power down entry and is enabled at a high level in the deep power down exit to drive a DRAM device. Accordingly, a malfunction of a semiconductor chip device in the deep power down entry is prevented. Therefore, the chip has stable operation, thereby improving the reliability of the chip.

Although certain apparatus constructed in accordance with the teachings of the invention have been described herein, the scope of coverage of this patent is not limited thereto. On the contrary, this patent covers all embodiments of the teachings of the invention fairly falling within the scope of the appended claims either literally or under the doctrine of equivalents.

What is claimed is:

1. A power-up signal generator for a semiconductor memory device, comprising:
   deep power down power-up signal generator for generating a deep power down power-up signal by means of an external power supply voltage;
   power-up signal generator for generating a power-up signal by the means of an internal power supply voltage; and
   power-up controller for determining whether or not enable the power-up signal in a deep power down entry.

2. The power-up signal generator as claimed in claim 1, wherein the deep power down power-up signal generator generates the deep power down power-up signal that is always enabled in the deep power down entry and in a deep power down exit by the external power supply voltage.

3. The power-up signal generator as claimed in claim 1, wherein the deep power down power-up signal generator includes:
   a divider for dividing the external power supply voltage;
   a pull-up device for pulling-up a divided voltage;
   a first driver for generating the power-up detection signal by the divided voltage; and
   a second driver for generating the deep power down power-up signal in response to the power-up detection signal.

4. The power-up signal generator as claimed in claim 1, wherein the power-up signal generator generates the power-up signal that is disabled in the deep power down entry and enabled by the internal power supply voltage in a deep power down exit.

5. The power-up signal generator as claimed in claim 1, wherein the power-up signal generator includes:
   a divider for dividing the internal power supply voltage;
   a pull-up device for pulling-up a divided voltage;
   a first driver for generating the power-up detection signal by the divided voltage; and
   a second driver for generating the power-up signal in response to the power-up detection signal.

6. The power-up signal generator as claimed in claim 1, wherein the power-up controller blocks the external power supply voltage in the deep power down entry and makes the internal power supply voltage from the external power supply voltage and provides it to the power-up signal generator in a deep power down exit.

7. The power-up signal generator as claimed in claim 1, wherein the power-up controller includes a PMOS transistor with the external power supply voltage connected to a source thereof and with a deep power down mode signal applied to a gate thereof.

* * *