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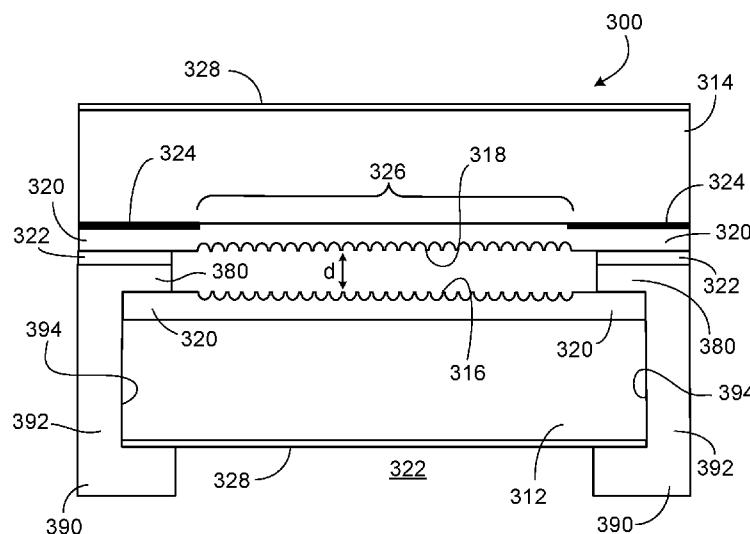


FIG. 3

(57) Abstract: The present disclosure describes optical element stack assemblies that include multiple substrates stacked one over another. At least one of the substrates includes an optical element, such as a DOE, on its surface. The stack assemblies can be fabricated, for example, in wafer-level processes.

OPTICAL ELEMENT STACK ASSEMBLIES

CROSS-REFERENCE TO RELATED APPLICATION(S)

[0001] The present application claims the benefit of priority of U.S. Provisional Patent Application No. 62/063,532, filed on October 14, 2014. The disclosure of the earlier application is incorporated herein by reference in its entirety.

FIELD OF THE DISCLOSURE

[0002] The present disclosure relates to optical element stack assemblies.

BACKGROUND

[0003] Various optoelectronics modules are used, for example, for imaging applications, such as three-dimensional (3D) imaging, or distance measurement applications, such as proximity sensing. In some applications, an optical emitter assembly is operable to emit a structured optical pattern, which can be useful for imaging as well as distance sensing applications. The structured light can result in a pattern of discrete features (i.e., texture) being projected onto an object. Light reflected by the object can be directed back toward an image sensor, where it is sensed. The sensed signals can be used for distance calculations. In some cases, structured light provides additional texture for matching pixels in stereo imaging applications.

[0004] In some modules, an optical element, such as a diffractive optical element (DOE), is introduced into the path of light emitted by a light source such as a vertical cavity semiconductor emitting laser (VCSEL) or VCSEL array. The DOE can be useful in creating the structured light pattern. It also can facilitate multiplying a structured light pattern generated by the VCSEL or other light source.

SUMMARY

[0005] The present disclosure describes optical element stack assemblies that can be fabricated, for example, by wafer-level methods.

[0006] For example, in one aspect, a wafer-level method of fabricating stack assemblies includes attaching a first wafer to a second wafer to form a wafer sub-stack. At least one of the first wafer or the second wafer has optical elements on its surface. The first and second wafers are attached such that each optical element is disposed between the first and second wafers. The method further includes attaching a spacer wafer to the wafer sub-stack to form a wafer stack, and separating the wafer stack into stack assemblies, each of which includes at least one of the optical elements.

[0007] In another aspect, a wafer-level method of fabricating stack assemblies includes providing first and second wafers, wherein at least one of the first wafer or the second wafer has optical elements on its surface. The method includes using a single vacuum injection technique to form upper and lower spacers on opposite surfaces of the second wafer. The method further includes attaching the first wafer to the second wafer to form a wafer stack. The first and second wafers can be attached such that each optical element is disposed between the first and second wafers. The wafer stack then can be separated onto stack assemblies, each of which includes at least one of the optical elements.

[0008] In yet another aspect, a wafer-level method of fabricating stack assemblies includes providing first and second wafers, wherein at least one of the first wafer or the second wafer has optical elements on its surface. The method includes attaching the second wafer to a tape and separating the second wafer into singulated substrates. The singulated substrates are placed into a vacuum injection tool to form upper and lower spacers on opposite surfaces of the singulated substrates. The first wafer is attached to the singulated substrates to form a stack such that each optical element is disposed between the first wafer and one of the singulated substrates. The stack then is separated into stack assemblies, each of which includes at least one of the optical elements.

[0009] The disclosure also describes a stack assembly including a first substrate, a second substrate attached to the first substrate, and an optical element on at least the first substrate or the second substrate, wherein the at least one optical element is disposed between the first and second substrates. The stack assembly includes a first spacer attached to an outer side of the first or second substrate. In some implementations, the stack assembly further includes a second spacer between the first and second substrates, wherein the first and second spacers are part of the same vacuum injection molded piece. Also, in some cases, the vacuum injection molded piece laterally surrounds side edges of the second substrate. Further, the first and second substrates can be attached to one another by adhesive on a lateral side portion of one or more of the optical elements.

[0010] Various implementations include one or more of the following features. For example, each of the first and second wafers can have a respective optical element on its surface, the optical elements facing one another. In some instances, the optical elements are diffractive optical elements. In some implementations, the optical elements are replicated optical elements.

[0011] The wafer-level methods allow multiple assemblies to be fabricated in parallel at the same time. Further, the techniques can be used advantageously to provide for smaller or larger distances between the first and second wafers, depending on the application. Various examples are described in greater detail below. Other aspects, features and advantages will be readily apparent from the following detailed description, the accompanying drawings and the claims.

BRIEF DESCRIPTION OF THE DRAWINGS

[0012] FIG. 1 illustrates a first example of an optical element stack assembly.

[0013] FIGS. 2A – 2F illustrate examples of steps in the fabrication of the optical element stack assembly of FIG. 1.

[0014] FIG. 3 illustrates a second example of an optical element stack assembly.

[0015] FIGS. 4A – 4F illustrate examples of steps in the fabrication of the optical element stack assembly of FIG. 3.

DETAILED DESCRIPTION

[0016] The present disclosure describes optical element stack assemblies that include multiple substrates stacked one over another. At least one of the substrates includes an optical element, such as a DOE, on its surface. In some cases, both substrates have an optical element on their respective surfaces. The substrates, and optical elements, are aligned such that an optical signal passing through the stack passes through the substrates and the optical element(s).

[0017] As shown in FIG. 1, a stack assembly 10 includes first and second substrates 12, 14 stacked one over the other. Each substrate 12, 14 can be composed, for example of a glass, polymer or other material that is transparent to a specified wavelength or range of wavelengths (e.g., in the visible, infra-red (IR) and/or near-IR parts of the spectrum). In the example of FIG. 1, the substrates 12, 14 have passive optical elements 16, 18 formed on their opposing surfaces. In the illustrated example, the optical elements 16, 18 are DOEs. Other types of passive optical elements (e.g., refractive or diffractive lenses, or arrays of optical elements, such as micro-lens arrays) can be provided in some implementations. Further, in some cases, one substrate 12 may have a type of optical element that differs from the type of optical element on the other substrate 14. In some instances, only one of the substrates 12, 14 may have an optical element on its surface.

[0018] The lateral side portions 20 of the material forming the optical elements 16, 18 can serve as spacers to provide a well-defined separation ‘d’ between the opposing optical elements 16, 18. A typical thickness ‘t’ of the lateral side portions 20 is 50 μm or less (e.g., 25-50 μm). In the illustrated example, the optical elements 16, 18 are composed of an epoxy material that is transparent to the specified wavelength or range of wavelengths. The substrates 12, 14 are connected together by a thin layer of glue or other

adhesive 22 disposed on the later side portions 20. A typical thickness of the adhesive 22 is less than 10 μm (e.g., 7 μm). The dimensions mentioned above may differ in some implementations.

[0019] A thin non-transparent coating 24 on the optical-element side of the top substrate 14 defines an optical stop 26, which serves to define a transparent window through which light of the specified wavelength or in the specified range of wavelengths can pass. An outer surface of each substrate 12, 14 can be coated with a thin anti-reflective coating (ARC) 28. The ARC-side of the bottom substrate 12 includes a spacer 30 to provide a well-defined distance between the optical elements 16, 18 and a surface on which the assembly 10 is mounted. The spacer 30, which can be fixed to the ARC-side of the bottom substrate 12 by adhesive, has an opening 32 below the stop 26.

[0020] FIGS. 2A – 2F illustrate steps of a wafer-level method for manufacturing optical element stack assemblies such as the assembly 10 of FIG. 1. Wafer-level processes allow multiple assemblies 10 to be fabricated at the same time. Generally, a wafer refers to a substantially disk- or plate-like shaped item, its extension in one direction (z-direction or vertical direction) is small with respect to its extension in the other two directions (x- and y- or lateral directions). In some implementations, the diameter of the wafer is between 5 cm and 40 cm, and can be, for example, between 10 cm and 31 cm. The wafer may be cylindrical with a diameter, for example, of 2, 4, 6, 8, or 12 inches, one inch being about 2.54 cm. In some implementations of a wafer-level process, there can be provisions for at least ten modules in each lateral direction, and in some cases at least thirty or even fifty or more modules in each lateral direction. To facilitate understanding, in FIGS. 2A – 2F only a portion of each wafer corresponding to a single assembly 10 is illustrated.

[0021] As shown in FIG. 2A, a first transparent wafer 114 is provided and has an ARC 128 on a first surface and a non-transparent layer (e.g., photoresist) 123 on its opposite second surface. The wafer 114 can be composed, for example of a glass, polymer or other material that is transparent to the specified wavelength or range of wavelengths. As shown in FIG. 2B, the layer 123 is patterned (e.g., using standard photolithography

techniques) to form regions 124 of non-transparent material that define the non-transparent coating 24 for each assembly 10.

[0022] Next, as shown in FIG. 2C, optical elements 118 (e.g., DOEs) are formed on the second surface of the substrate 114. The optical elements 118, one of which is shown in FIG. 1C, can be formed, for example, by wafer-level replication. In general, replication refers to a technique by means of which a given tool (the tool including e.g., a negative of the optical elements) structure or a negative positive thereof is used to reproduced via, e.g., etching, embossing or molding a structured surface (e.g., a positive of the optical elements). In a particular example of a replication process, a structured surface (e.g., defining an optical element or a plurality of optical elements) is pressed into a liquid, viscous or plastically deformable material by using a tool, then the material is hardened, e.g., by curing using ultraviolet radiation and/or heating, and then the structured surface tool is removed. Thus, a replica of the structured surface is obtained. Suitable materials for replication are, for example, hardenable (e.g., curable) polymer materials or other replication materials, i.e. materials which are transformable in a hardening or solidification step (e.g., a curing step) from a liquid, viscous or plastically deformable state into a solid state. The thickness of the yard portions 120 of the replicated material typically is 50 μm or less (e.g., 25-50 μm). The processing in FIGS. 2A – 2C results in a first wafer subassembly 140 that provides the top substrate 14 for each assembly 10.

[0023] As part of the fabrication process, a second transparent wafer 112 is provided and has an ARC 128 on its first surface. Optical elements 116 (e.g., DOEs), one of which is shown in FIG. 2D, are formed on the second surface of the wafer 112. The optical elements 116 also can be formed, for example, by wafer-level replication as described above. The processing in FIG. 2D results in a second wafer subassembly 150 that provides the bottom substrate 12 for each assembly 10.

[0024] Next, as shown in FIG. 2E, the first and second wafer subassemblies 140, 150 are attached to one another to form a wafer sub-stack 160. The subassemblies 140, 150 can be attached to one another, for example, by glue or other adhesive (e.g., by glue setting or

screen printing). The subassemblies 140, 150 can be attached to one another such that the optical elements 116, 118 face one another. Further, as shown in FIG. 2F, a spacer wafer 130 is attached to the ARC-side of the second wafer assembly 140 to complete the wafer stack 170. The spacer wafer 130 can be attached, for example, by glue or other adhesive. Once the wafer-level stack 170 is completed, it can be separated (e.g., by dicing) to form multiple individual assemblies 10.

[0025] In the example process of FIGS. 2A – 2F, both wafers 112, 114 have optical elements 116, 118 replicated on their respective surfaces. In some implementations, however, only one of the wafers (either the first wafer 114 or the second wafer 112) has optical elements on its surface. Further, although the optical elements 116, 118 are shown as DOEs, other types of optical elements can be used in some instances.

[0026] FIG. 3 illustrates a second example of an optical element stack assembly 300. The stack assembly 300 includes first and second substrates 312, 314 stacked one over the other. Each substrate 312, 314 can be composed, for example of a glass, polymer or other material that is transparent to a specified wavelength or range of wavelengths (e.g., in the visible, infra-red (IR) and/or near-IR parts of the spectrum).

[0027] In the example of FIG. 3, the substrates 312, 314 have passive optical elements 316, 318 formed on their opposing surfaces. In the illustrated example, the optical elements 316, 318 are DOEs. Other types of passive optical elements (e.g., refractive or diffractive lenses) can be provided in some implementations. Further, in some cases, one substrate 312 may have a type of optical element that differs from the type of optical element on the other substrate 314. In some instances, only one of the substrates 312, 314 may have an optical element on its surface.

[0028] A thin non-transparent coating 324 on the optical-element side of the top substrate 314 defines an optical stop 326, which serves as a transparent window through which light of the specified wavelength or in the specified range of wavelengths can pass.

An outer surface of each substrate 312, 314 can be coated with a thin anti-reflective coating (ARC) 328.

[0029] To increase the separation ‘d’ between the opposing optical elements 16, 18, a vacuum injection molded spacer 380 separates the lateral side portions 320 of the material forming the optical elements 316, 318. The spacer 380 can be fixed directly (without adhesive) to the lateral side portion 320 of the optical element 316 on the bottom substrate 312. The spacer 380 can be attached to the lateral side portion 320 of the optical element 318 on the top substrate 314 by glue or other adhesive 322. The ARC-side of the bottom substrate 312 includes a spacer 390 to provide a well-defined distance between the optical elements 316, 318 and a surface on which the assembly 300 is mounted. The spacer 390 can be a vacuum injection molded spacer, which can be fixed directly to the ARC-side of the bottom substrate 312 (i.e., without adhesive). The spacer 390 has an opening 332 below the stop 326.

[0030] As illustrated in FIG. 3, the spacers 380 and 390 can be formed as a single vacuum injection molded piece, part 392 of which surrounds the lateral side edges 394 of the bottom substrate 312.

[0031] FIGS. 4A – 4F illustrate steps of a wafer-level method for manufacturing optical element stack assemblies such as the assembly 300 of FIG. 3. FIGS. 4A – 4C show a process for forming a first wafer subassembly 440 that provides the top substrate 314 for each assembly 300. This part of the process can be substantially the same as the corresponding steps in FIGS. 2A – 2C. Thus, as shown in FIG. 4A, a first transparent wafer 414 is provided and has an ARC 428 on a first surface and a non-transparent layer (e.g., photoresist) 423 on its opposite second surface. The wafer 414 can be composed, for example of a glass, polymer or other material that is transparent to the specified wavelength or range of wavelengths. As shown in FIG. 4B, the layer 423 is patterned (e.g., using standard photolithography techniques) to form regions 424 of non-transparent material that define the non-transparent coating 324 for each assembly 300.

[0032] Next, as shown in FIG. 4C, optical elements 418 (e.g., DOEs) are formed on the second surface of the substrate 414. The optical elements 418, one of which is shown in FIG. 4C, can be formed, for example, by wafer-level replication, as discussed above. The processing in FIGS. 4A – 4C results in a first wafer subassembly 440 that provides the top substrate 314 for each assembly 300.

[0033] As part of the fabrication process, a second transparent wafer 412 also is provided and has an ARC 428 on its first surface (FIG. 4D). Initial preparation and processing of the second wafer 412 can be similar to that of wafer 112 in FIG. 2D. Thus, optical elements 416 (e.g., DOEs), one of which is shown in FIG. 4D, are formed on the second surface of the wafer 412. The optical elements 416 also can be formed, for example, by wafer-level replication as described above.

[0034] Next, as illustrated in FIG. 4E, second wafer subassembly 450 is subject to formation of through-holes and a vacuum injection molding process that fills the through-holes and forms the top and bottom spacers 380, 390. Thus, the spacers 380, 390 can be formed as a single vacuum injection molded piece, part 392 of which fills though-holes in the second wafer 412. Suitable techniques are described in U.S. Patent No. 9,094,593 and in U.S. Published Patent Application No. 2015-0034975. The techniques include forming through-holes through a wafer, for example, by dicing, micromachining or laser cutting. Vacuum injection then can be used to provide an epoxy or other suitable material to fill the openings in the wafer and form the spacers. In some cases, the epoxy or other material subsequently is cured (e.g., via exposure to heat and/or UV treatments). The disclosures of the aforementioned US patent documents are incorporated herein by reference. The processing in FIG. 4E results in a second wafer subassembly 450 that provides the bottom substrate 412 for each assembly 300.

[0035] Next, as shown in FIG. 4F, the first and second wafer subassemblies 440, 450 are attached to one another to form a wafer stack 470. The subassemblies 440, 450 can be attached to one another, for example, by glue or other adhesive (e.g., by glue jetting or screen printing), and can be attached to one another such that the optical elements 416,

418 face one another. The wafer-level stack 470 then can be separated (e.g., by dicing) to form multiple individual assemblies 300.

[0036] In some instances, in FIG. 4E, the second wafer subassembly 450 can be attached, for example, to UV dicing tape and then diced to form multiple singulated substrates. The singulated substrates then can be provided to a vacuum injection tool to form the upper and lower spacers 380, 390. In that case, the wafer-level method can include attaching the first wafer 414 to the singulated substrates to form a stack such that each optical element is disposed 416, 418 between the first wafer 414 and one of the singulated substrates. The stack then is separated (e.g., by dicing) into a plurality of stack assemblies, each of which includes at least one of the optical elements.

[0037] Using a vacuum injection technique to form the spacers 380, 390 can be advantageous. For example, the addition of the upper spacer 380 allows the distance 'd' between the optical elements 316, 318 to be increased even if the thickness of the lateral side portions 320 of the replicated material for the optical elements 316, 318 is somewhat limited (e.g., limited to 50 μm or less in some cases).

[0038] In the example process of FIGS. 4A – 4F, both wafers 412, 414 have optical elements 416, 418 replicated on their respective surfaces. In some implementations, however, only one of the wafers (either the first wafer 414 or the second wafer 412) has optical elements on its surface. Further, although the optical elements 416, 418 are shown as DOEs, other types of optical elements can be used in some instances.

[0039] The stack assemblies 10 (FIG. 1) and 300 (FIG. 3) can be integrated into, and used with, a wide range of optoelectronic modules. Such modules may include active optoelectronic components such as light emitters (e.g., light emitting diodes (LEDs), infra-red (IR) LEDs, organic LEDs (OLEDs), infra-red (IR) lasers or vertical cavity surface emitting lasers (VCSELs)) and/or light sensors (e.g., CCD or CMOS sensor). Further, such modules can be integrated into various types of consumer electronics and other devices such as mobile phones, smart phones, personal digital assistants (PDAs),

tablets and laptops, as well as bio devices, mobile robots, and digital cameras, among others.

[0040] Various modifications will be readily apparent and are within the spirit of the invention. Thus, other implementations are within the scope of the claims.

What is claimed is:

1. A wafer-level method of fabricating a plurality of stack assemblies, the method comprising:

attaching a first wafer to a second wafer to form a wafer sub-stack, wherein at least one of the first wafer or the second wafer has a plurality of optical elements on its surface, the first and second wafers being attached such that each optical element is disposed between the first and second wafers;

attaching a spacer wafer to the wafer sub-stack to form a wafer stack; and
separating the wafer stack into a plurality of stack assemblies, each of which includes at least one of the optical elements.

2. The method of claim 1 wherein each of the first and second wafers has a plurality of optical elements on their respective surfaces, and wherein each stack assembly includes at least two of the optical elements.

3. The method of claim 2 wherein attaching the first and second wafers includes attaching the first and second wafers to one another through adhesive at lateral side portions of the optical elements.

4. The method of any one of the previous claims wherein the optical elements are diffractive optical elements.

5. The method of any one of the previous claims wherein the optical elements are replicated optical elements.

6. The method of any one of the previous claims wherein each stack assembly includes a spacer formed from the spacer wafer to provide a well-defined distance between the at least one optical element and a surface on which the stack assembly is to be mounted.

7. A wafer-level method of fabricating a plurality of stack assemblies, the method comprising:

providing first and second wafers, wherein at least one of the first wafer or the second wafer has a plurality of optical elements on its surface;

using a single vacuum injection technique to form upper and lower spacers on opposite surfaces of the second wafer;

attaching the first wafer to the second wafer to form a wafer stack, the first and second wafers being attached such that each optical element is disposed between the first and second wafers; and

separating the wafer stack into a plurality of stack assemblies, each of which includes at least one of the optical elements.

8. The method of claim 7 further including forming through-holes in the second substrate, wherein the vacuum injection technique fills the through-holes with a same material that forms the upper and lower spacers.

9. The method of any one of claims 7 and 8, wherein each of the first and second wafers has a plurality of optical elements on their respective surfaces, and wherein each stack assembly includes at least two of the optical elements.

10. The method of any one of claims 7 – 9 wherein attaching the first and second wafers includes attaching the first and second wafers to one another through adhesive disposed between lateral side portions of the optical elements and the upper spacers on the second wafer.

11. The method of any one of claims 7 – 10 wherein the optical elements are diffractive optical elements.

12. The method of any one claims 7 – 11 wherein the optical elements are replicated optical elements.

13. A stack assembly comprising:

a first substrate;

a second substrate attached to the first substrate;
an optical element on at least the first substrate or the second substrate, wherein the at least one optical element is disposed between the first and second substrates; and
a first spacer attached to an outer side of the first or second substrate.

14. The stack assembly of claim 13 further including a second spacer between the first and second substrates, wherein the first and second spacers are part of a same vacuum injection molded piece.
15. The stack assembly of claim 13 wherein the vacuum injection molded piece laterally surrounds side edges of the second substrate.
16. The stack assembly of any one of claim 13 – 15 wherein each of the first and second wafers has a respective optical element on its surface, the optical elements facing one another.
17. The stack assembly of any one of claim 13 – 16 wherein each optical element is a diffractive optical element.
18. The stack assembly of any one of claim 13 – 17 wherein each optical elements is a replicated optical element.
19. The stack assembly of claim 13 wherein the first and second substrates are attached to one another by adhesive on a lateral side portion of the optical element.
20. A wafer-level method of fabricating a plurality of stack assemblies, the method comprising:
 - providing first and second wafers, wherein at least one of the first wafer or the second wafer has a plurality of optical elements on its surface;
 - attaching the second wafer to a tape and separating the second wafer into a plurality of singulated substrates;

placing the singulated substrates into a vacuum injection tool to form upper and lower spacers on opposite surfaces of the singulated substrates;

attaching the first wafer to the singulated substrates to form a stack such that each optical element is disposed between the first wafer and one of the singulated substrates; and

separating the stack into a plurality of stack assemblies, each of which includes at least one of the optical elements.

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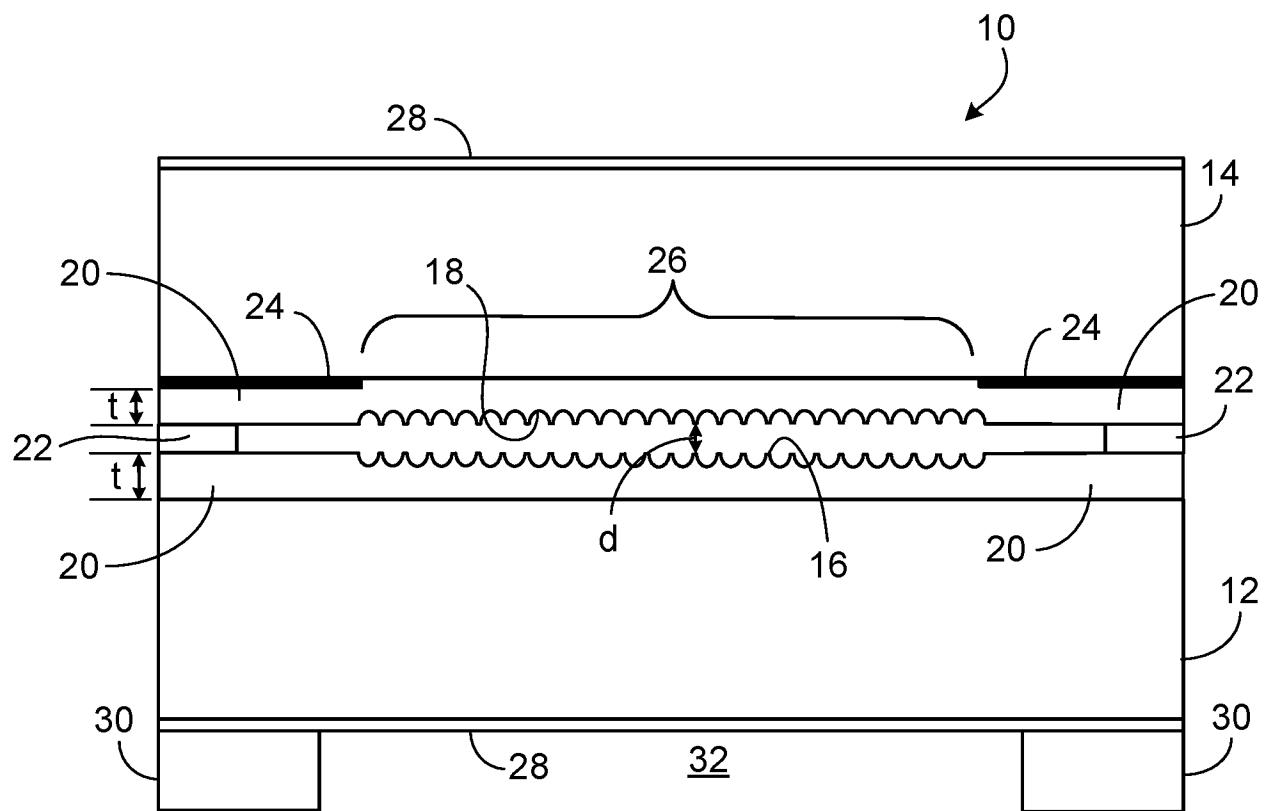


FIG. 1

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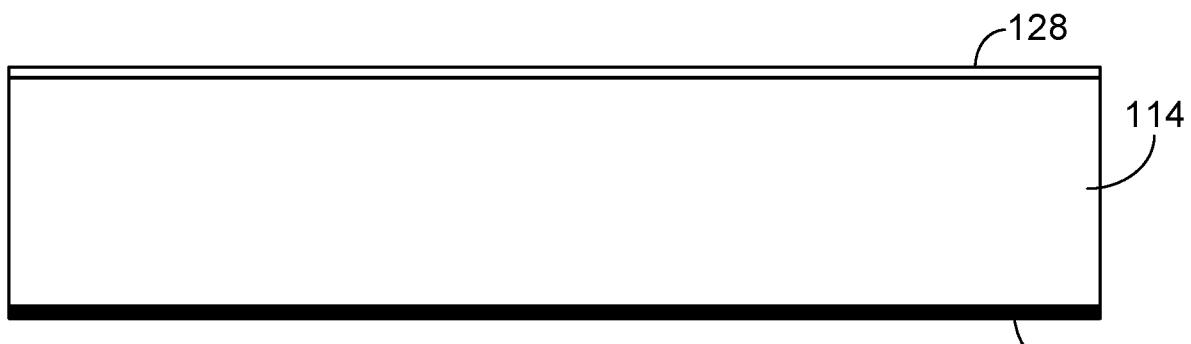


FIG. 2A

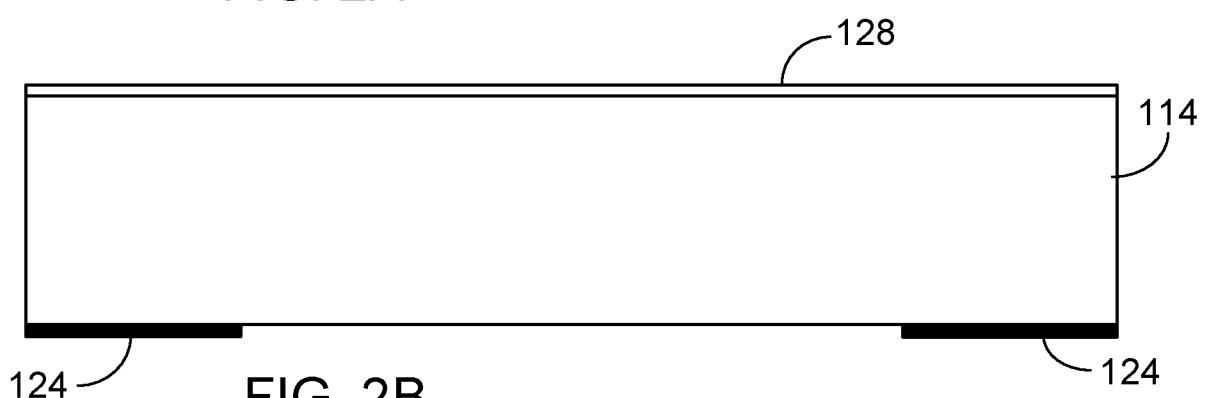


FIG. 2B

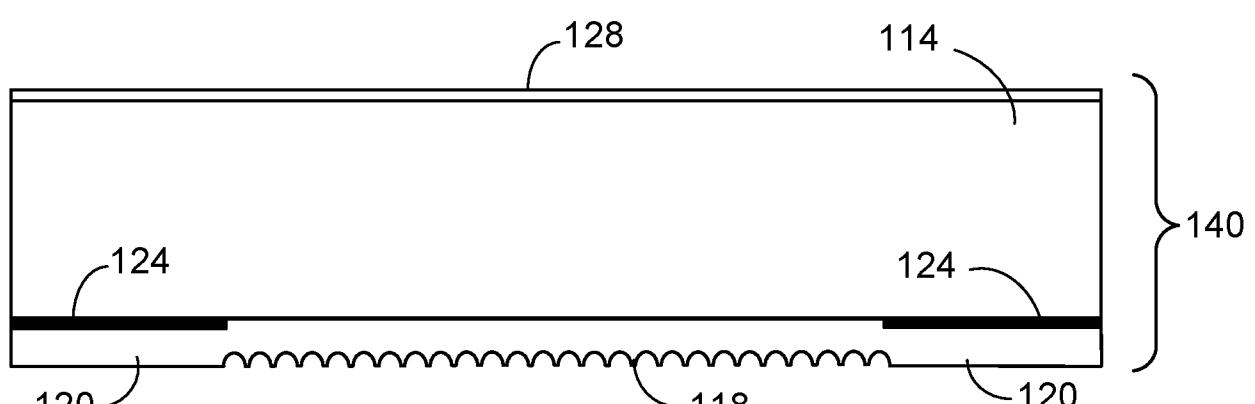


FIG. 2C

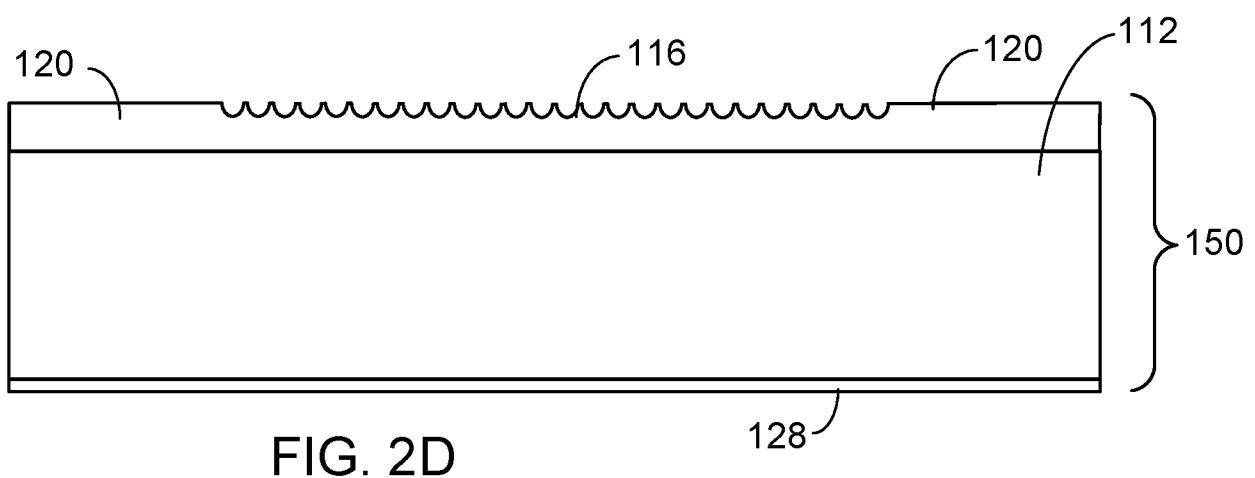


FIG. 2D

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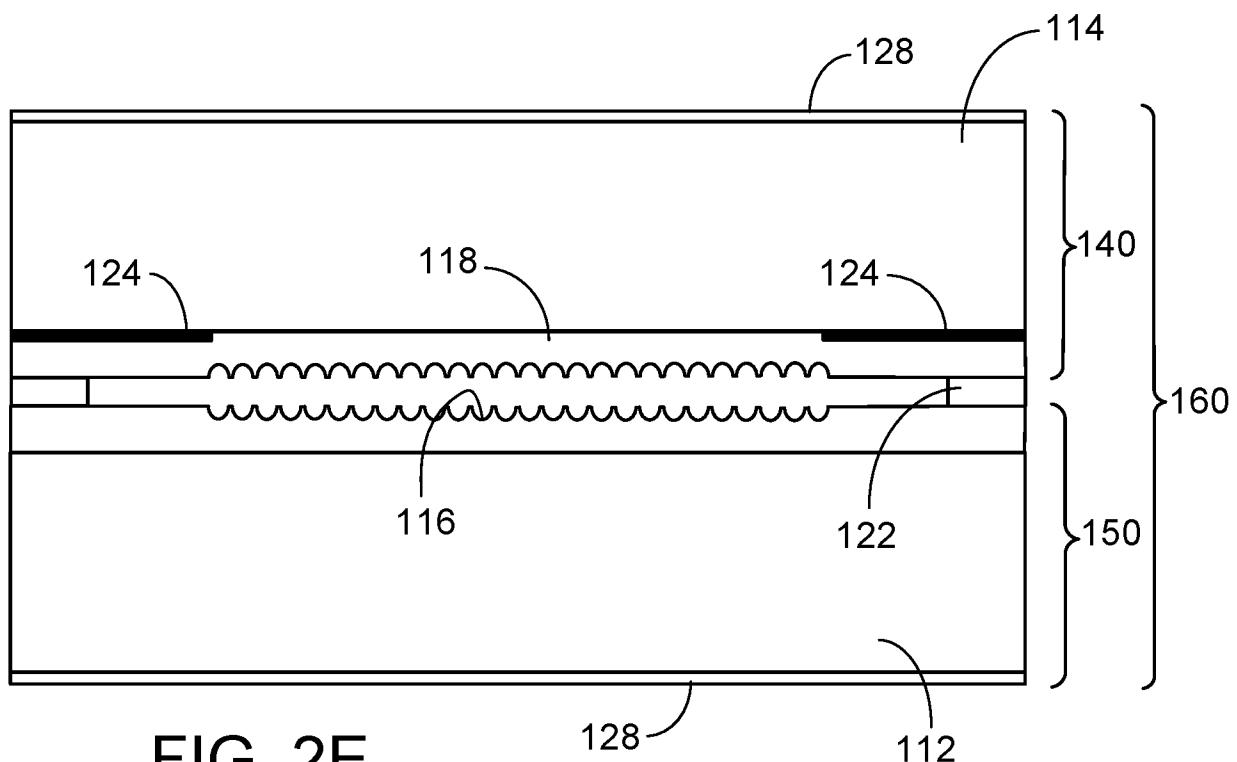


FIG. 2E

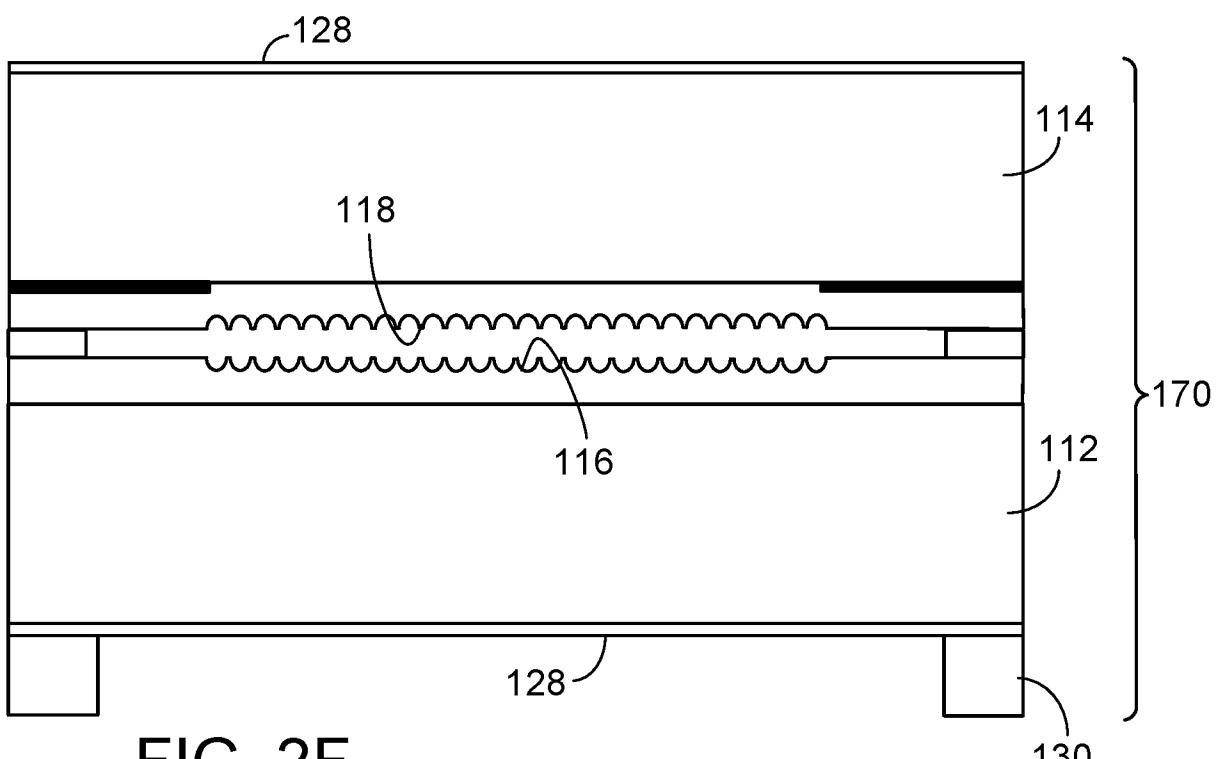


FIG. 2F

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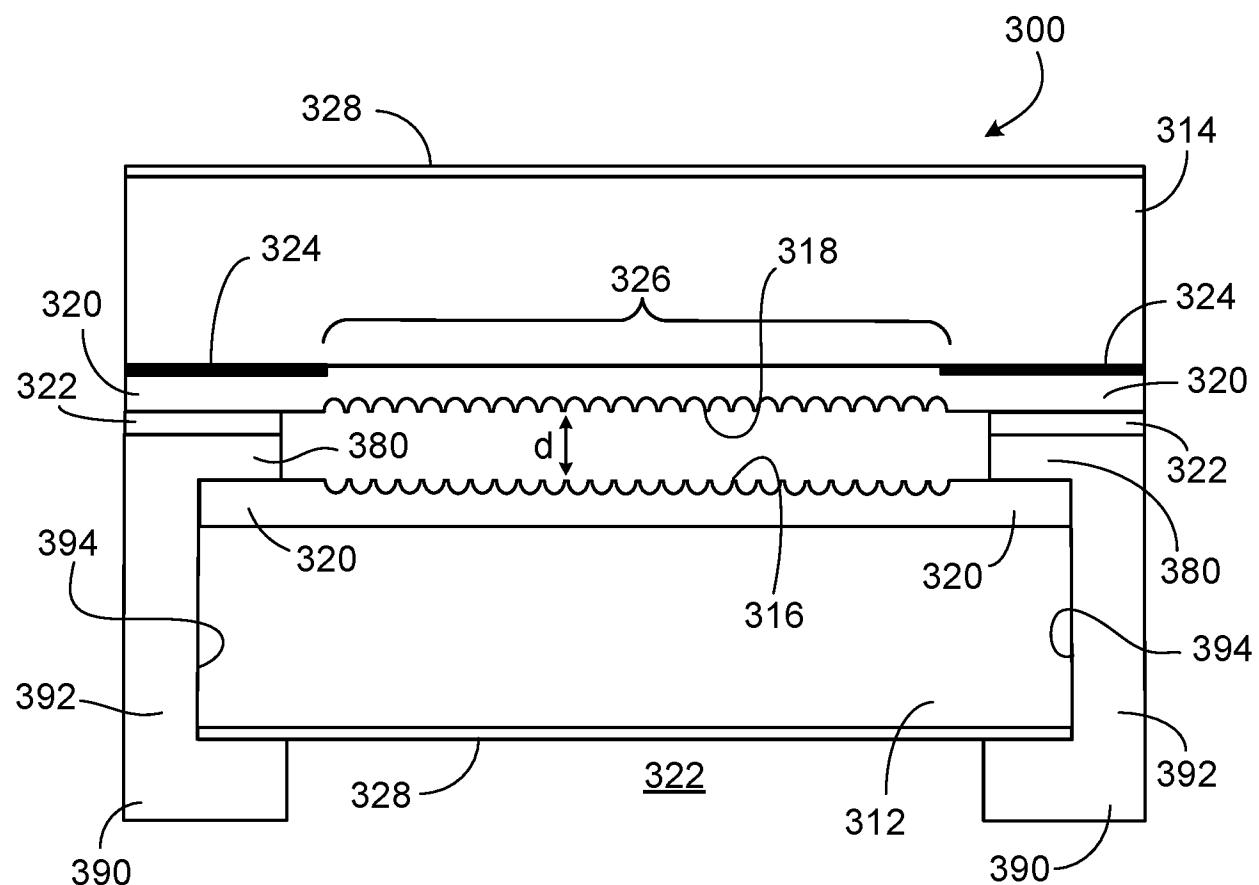
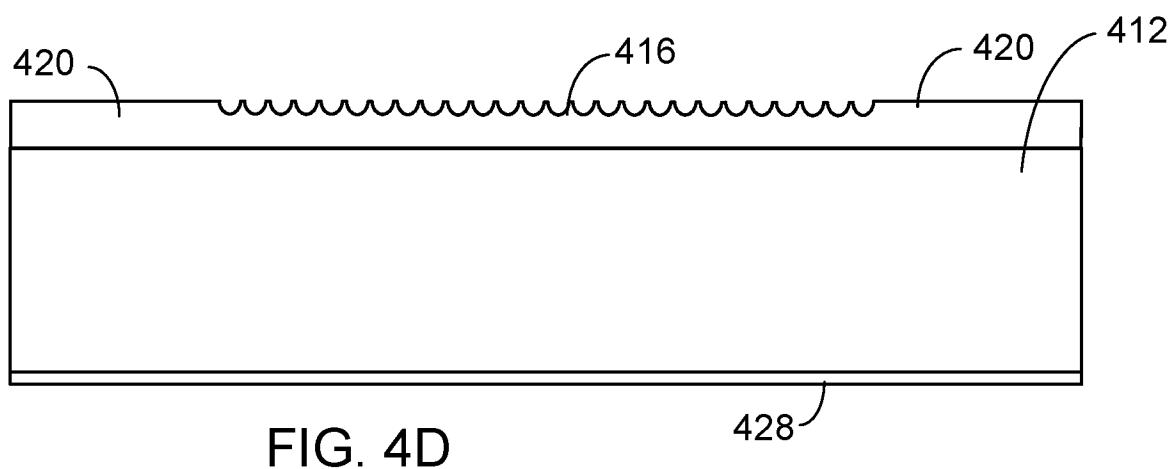
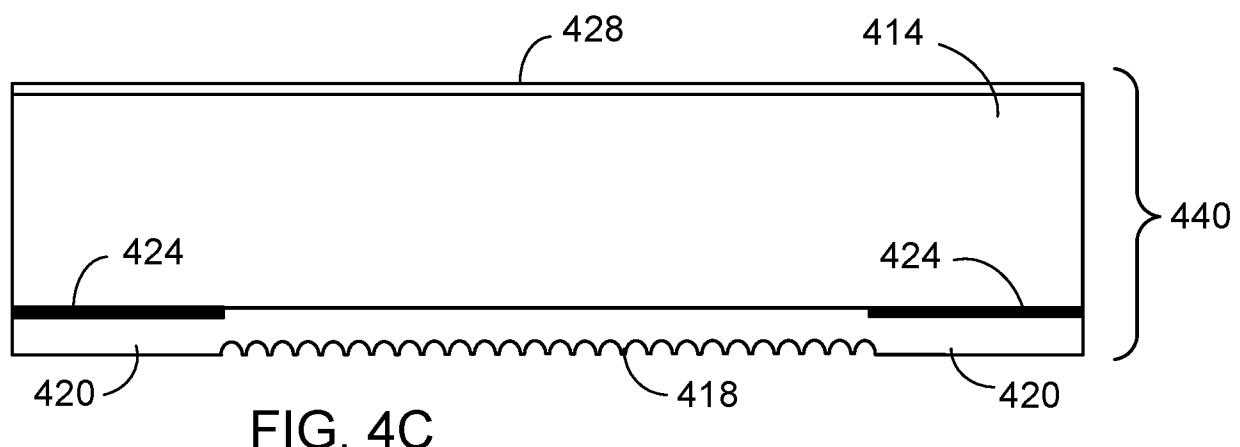
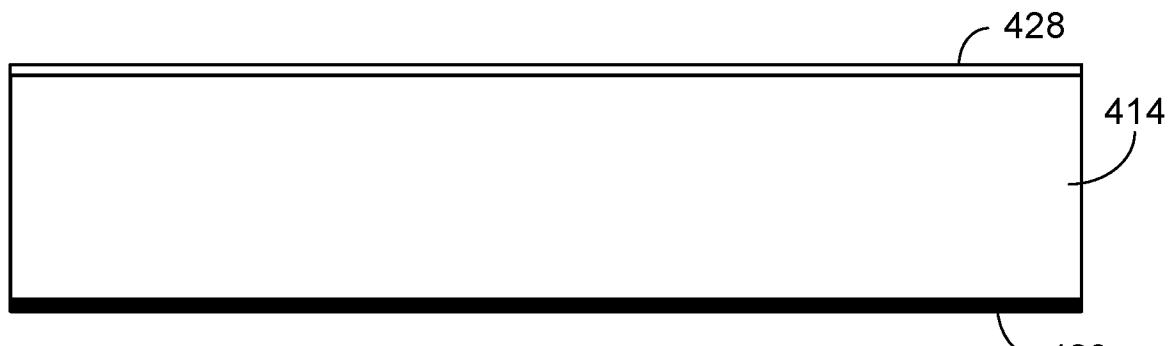


FIG. 3

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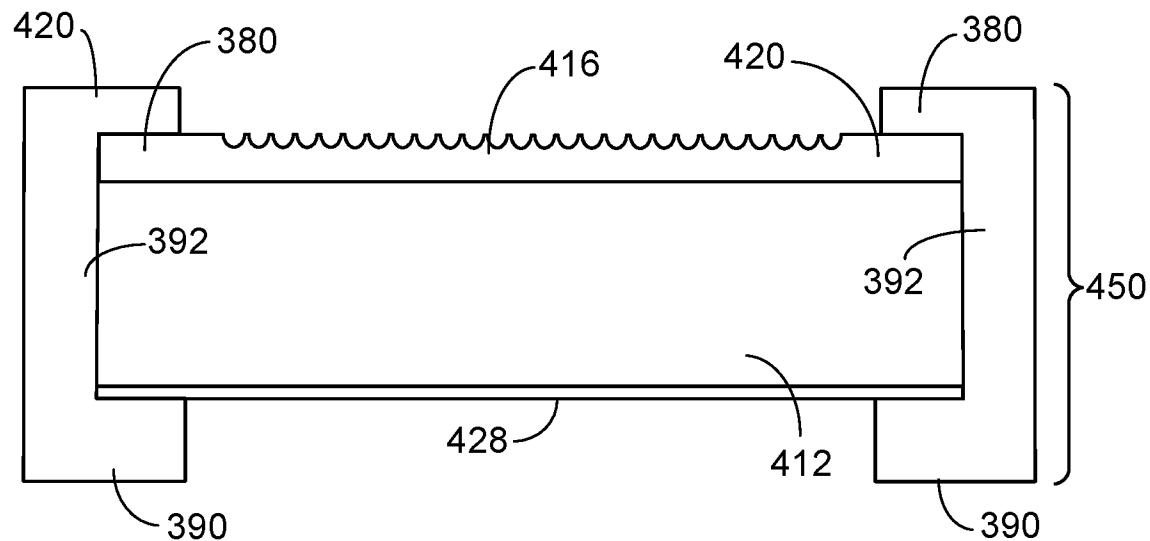


FIG. 4E

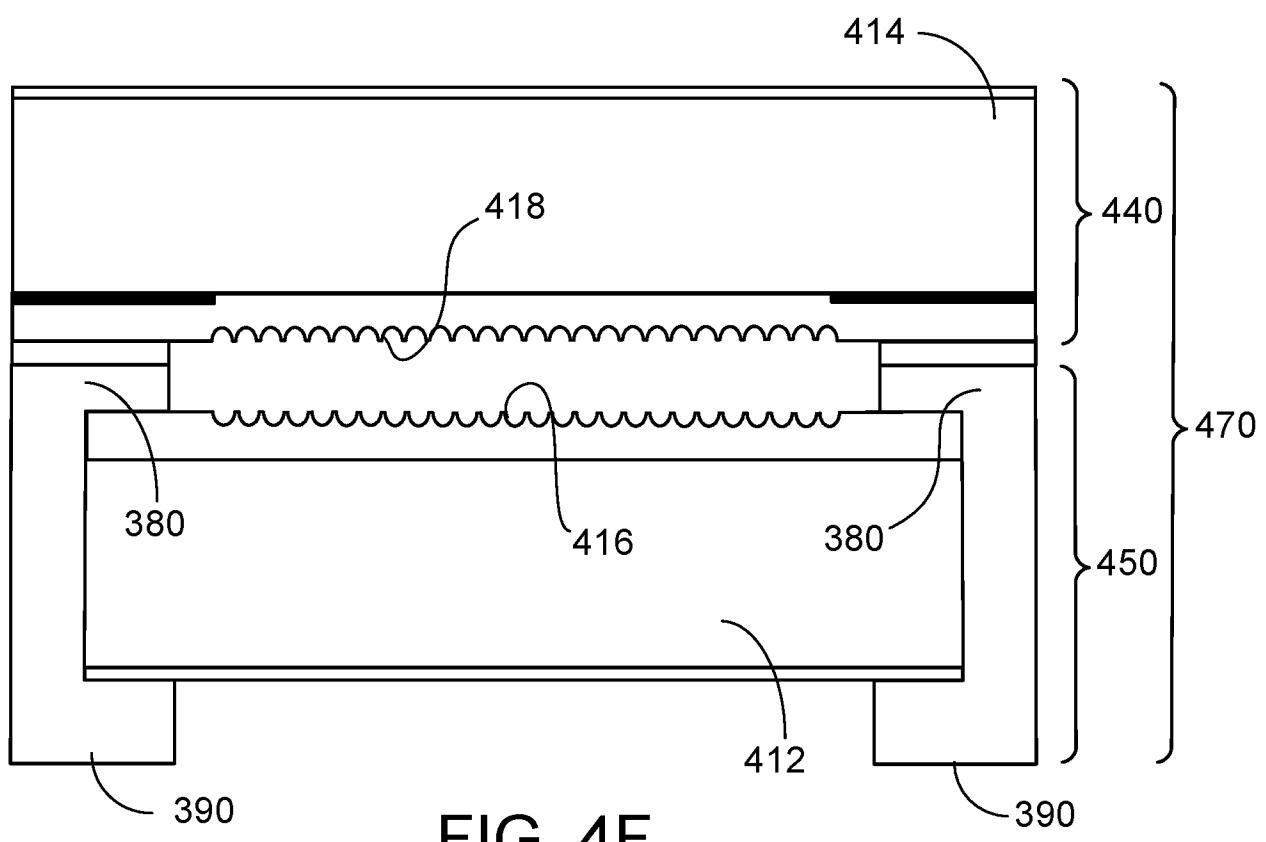


FIG. 4F

INTERNATIONAL SEARCH REPORT

International application No.

PCT/SG2015/050387

A. CLASSIFICATION OF SUBJECT MATTER

G02B 7/00 (2006.01) B32B 37/12 (2006.01) H01L 31/0232 (2014.01)

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

Databases: WPIAP, EPODOC, INSPEC and keywords: Optoelectronic, optics, wafer-level, spacer, separator, isolator, lens, optical element, substrate, wafer, plural, multiple, stack, diffractive, refractive, injection and similar terms.

Applicant(s)/Inventor(s) name search in Espacenet, AusPat, Google Patent, INTESS AND PAMS NOSE:

Applicant name: HEPTAGON*; Inventors name : Heimgartner, Stephan; Bietsch, Alexander; Riel, Peter

keywords: wafer stacking, wafer level, wafer optics, optical elements, optics elements, lens, vacuum injection, injection moulding, injection molding and similar terms.

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
	Documents are listed in the continuation of Box C	

 Further documents are listed in the continuation of Box C See patent family annex

* Special categories of cited documents:		
"A" document defining the general state of the art which is not considered to be of particular relevance	"T"	later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"E" earlier application or patent but published on or after the international filing date	"X"	document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)	"Y"	document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"O" document referring to an oral disclosure, use, exhibition or other means	"&"	document member of the same patent family
"P" document published prior to the international filing date but later than the priority date claimed		

Date of the actual completion of the international search
26 November 2015Date of mailing of the international search report
26 November 2015

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INTERNATIONAL SEARCH REPORT		International application No.
C (Continuation).		PCT/SG2015/050387
Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 8000041 B1 (LIN ET AL.) 16 August 2011 Fig. 11S, column 9, line 61-column 10, line 10; Fig. 11H, column 7, lines 17-35, column 2, lines 39-52, Fig. 11F	1-6, 13-19
X	US 2013/0048208 A1 (LIN ET AL.) 28 February 2013 Figs. 1a-4, paragraphs 0016-0020,	7-12, 20
X	US 2009/0321861 A1 (OLIVER ET AL.) 31 December 2009 Figs. 2A-5B, paragraphs 0015-0028,	7-12, 20
X	US 2010/0208354 A1 (OKAZAKI ET AL.) 19 August 2010 Figs. 8-12c, paragraphs 0065-0076	7-12, 20
X	US 2013/0037054 A1 (SARUYA) 14 February 2013 Fig. 2, paragraphs 0052-0080, Fig. 7	1-6, 13-19

INTERNATIONAL SEARCH REPORT Information on patent family members		International application No. PCT/SG2015/050387	
This Annex lists known patent family members relating to the patent documents cited in the above-mentioned international search report. The Australian Patent Office is in no way liable for these particulars which are merely given for the purpose of information.			
Patent Document/s Cited in Search Report		Patent Family Member/s	
Publication Number	Publication Date	Publication Number	Publication Date
US 8000041 B1	16 August 2011	US 8000041 B1 CN 102411185 A CN 102411185 B TW 201213919 A TW I435134 B	16 Aug 2011 11 Apr 2012 31 Dec 2014 01 Apr 2012 21 Apr 2014
US 2013/0048208 A1	28 February 2013	US 2013048208 A1 US 8388793 B1 CN 102969321 A CN 102969321 B TW 201310106 A TW I460485 B	28 Feb 2013 05 Mar 2013 13 Mar 2013 11 Feb 2015 01 Mar 2013 11 Nov 2014
US 2009/0321861 A1	31 December 2009	US 2009321861 A1 WO 2009158414 A1	31 Dec 2009 30 Dec 2009
US 2010/0208354 A1	19 August 2010	US 2010208354 A1 US 8194323 B2 CN 102016653 A CN 102016653 B CN 103323893 A CN 103323893 B EP 2273289 A1 EP 2273289 B1 JP 4420141 B2 JP 2009301061 A JP 4466789 B2 JP 2010072665 A JP 5310569 B2 US 2012212829 A1 US 8456743 B2 WO 2009133756 A1	19 Aug 2010 05 Jun 2012 13 Apr 2011 10 Jul 2013 25 Sep 2013 29 Jul 2015 12 Jan 2011 21 Jan 2015 24 Feb 2010 24 Dec 2009 26 May 2010 02 Apr 2010 09 Oct 2013 23 Aug 2012 04 Jun 2013 05 Nov 2009
US 2013/0037054 A1	14 February 2013	US 2013037054 A1 WO 2011135979 A1	14 Feb 2013 03 Nov 2011
End of Annex			
<p>Due to data integration issues this family listing may not include 10 digit Australian applications filed since May 2001. Form PCT/ISA/210 (Family Annex)(July 2009)</p>			