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(54) Title: INTEGRATED CIRCUIT HAVING MEMORY ARRAY INCLUDING ECC AND/OR COLUMN REDUNDANCY, AND METHOD OF PROGRAMMING, CONTROLLING AND/OR OPERATING SAME

(57) Abstract: An integrated circuit device (for example, a logic device or a memory device (such as, a discrete memory device)), including a memory cell array having a plurality of memory cells arranged in a matrix of rows and columns, multiplexer circuitry, coupled to the memory cell array, wherein the multiplexer circuitry includes a plurality of data multiplexers, each data multiplexer having a plurality of inputs, including (i) a first input to receive write data which is representative of data to be written into the memory cells of the memory cell array in response to a write operation, and (ii) a second input to receive read data which is representative of data read from memory cells of the memory cell array, and an associated output to responsively output data from one of the plurality of inputs, and syndrome generation circuitry, coupled to the multiplexer circuitry, to generate: (i) a write data syndrome vector using the write data and (ii) a read data syndrome vector using the read data.

# INTERNATIONAL SEARCH REPORT

International application No.

PCT/US07/14679

**A. CLASSIFICATION OF SUBJECT MATTER**  
 IPC: **H03M 13/00**( 2006.01)

USPC: 714/785  
 According to International Patent Classification (IPC) or to both national classification and IPC

**B. FIELDS SEARCHED**

Minimum documentation searched (classification system followed by classification symbols)  
 U.S. : 714/785

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)  
 EAST: USPAT, USPGPUB, IBM\_TDB

**C. DOCUMENTS CONSIDERED TO BE RELEVANT**

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	Applicant Admitted Prior Art, Fig. 1A & Fig. 1B; Page 1-3	1-29
Y	US 5,515,383 (Katoosi) 07 May 1996 (07.05.1996), col. 6, lines 23-53; col. 44-65.	

Further documents are listed in the continuation of Box C.       See patent family annex.

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"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)	"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"O" document referring to an oral disclosure, use, exhibition or other means	"&" document member of the same patent family
"P" document published prior to the international filing date but later than the priority date claimed	

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