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EXTERNAL STORAGE DEVICE

Description

5 **FIELD OF THE INVENTION**

[0001] The invention relates to mobile storage devices and the like.

10 **BACKGROUND**

[0002] Universal serial bus ("USB") sticks consist of a memory data storage device integrated with a USB interface. USB sticks are typically used for similar purposes for which floppy disks or CD-ROMs were previously used. However, USB sticks are smaller,
15 faster, have thousands of times more capacity, and are more durable and reliable. In the case of USB sticks with chip on board ("COB") flash memory, a USB controller and flash memory can be combined into one structure that is embedded into one side of a printed circuit board ("PCB") with the USB connection located on an opposing surface.

20 **[0003]** The USB standard that governs the design of the USB connections has undergone several revisions since its earliest release in 1994. The first widely adopted version, USB 1.1, specified data rates of 1.5 Mbit/s ("Low-Bandwidth") and 12 Mbit/s ("Full-Bandwidth"). USB 1.1 was replaced by USB 2.0 in 2000. USB 2.0 provided a higher maximum data rate of 480 Mbit/s ("Hi-Speed"). In this version, the USB 2.0 cable has four wires: two wires for
25 power (+5 volts and ground) and a twisted pair of wires for carrying data. In the USB 2.0 design, as well as USB 1.1, data is transmitted in one direction at a time (downstream or upstream).

[0004] In 2008, a new USB 3.0 standard was announced. USB 3.0 includes a new "SuperSpeed" bus, which provides a fourth data transfer mode at 5.0 Gbit/s. In order to achieve this increased throughput, the USB 3.0 cable has a total of eight wires: two wires for power (+5 volts and ground), the twisted pair for carrying non-SuperSpeed data (allows backward compatibility with earlier versions of USB devices), and two differential pairs for carrying SuperSpeed data. Full-duplex signaling occurs over the two differential pairs.

[0005] To date, adoption of the USB 3.0 standard has been slow due to the need to redesign motherboard hardware that supports the USB 3.0 standard, and the need to revise operating systems to support the USB 3.0 standard. To ease the transition to the USB 3.0 standard, it is desirable to modify existing USB 2.0 COB sticks to also include USB 3.0 connections.

[0006] Because the USB 2.0 COB stick configuration has a rectilinear design with the components embedded on one side of the PCB and the USB 2.0 connections positioned flush with the opposing side of the PCB, the shape and configuration does not readily allow the addition of a USB 3.0 connection to the existing USB 2.0 COB stick. With USB 3.0 being the coming standard and much faster than USB 2.0, it is desirable to provide a design that incorporates USB 3.0 connections into existing USB 2.0 COB sticks so that the USB COB stick may connect to either version of the USB standard. Publication no. US 2008/0218799 A1 discloses a dual-personality extended USB (EUSB) system that supports both USB and EUSB memory cards using an extended 9-pin EUSB socket.

STATEMENT OF INVENTION

[0007] An external device in accordance with the present invention and features therefore are defined by the appended claims.

SUMMARY

[0008] The above identified problems are solved by an external storage device according to claim 1. Advantageous features are provided in the respective dependent claims.

5 **[0009]** The memory die stack may be mounted to the component surface or a connection surface of the substrate. The external storage device comprises a plurality of memory die stacks. In these features, at least one of the memory die stacks is attached to a connection surface of the substrate, and at least one of the memory die stacks is attached to a component surface of the substrate. The memory die stacks may each comprise a plurality
10 of dies. In some features, at least two of the memory die stacks are stacked in an overlapping arrangement.

BRIEF DESCRIPTION OF THE DRAWINGS

15 **[0010]**

Figure 1 is a front perspective view of an external storage device according to certain features of the present invention.

Figure 2 is a front perspective view of the external storage device of Figure 1 with coupling points.

20 Figure 3 is a perspective view of a contact bar for use with the external storage device of Figure 2.

Figure 4 is a board of the contact bar of Figure 3.

Figure 5 is a cover of the contact bar of Figure 3.

Figure 6 is a bottom view of the contact bar of Figure 3.

25 Figure 7 is a front perspective view of the board of Figure 4 in use with the external storage device of Figure 2.

Figure 8 is a front perspective view of the contact bar of Figure 3 in use with the external storage device of Figure 2.

Figure 9 is a front perspective view of the board of Figure 4 in use with an external
30 storage device according to other features of the present invention.

Figure 10 is a front perspective view of the board of Figure 4 in use with an external storage device according to other features of the present invention.

Figure 11 is a back perspective view of the external storage device of Figure 2.

Figure 12 is a front perspective view of an external storage device according to other features of the present invention.

Figure 13 is a back perspective view of the external storage device of Figure 12.

Figure 14 is a perspective view of a spring of the mounting bar of the external storage device of Figure 12.

Figure 15 is a perspective view of the mounting bar of the external storage device of Figure 12.

Figure 16 is not covered by the subject-matter of the claims and is a side view of the external storage device of Figure 2 with a single memory die stack positioned on a component surface of a substrate, the memory die stack having a single die.

Figure 17 is not covered by the subject-matter of the claims and is a side view of the external storage device of Figure 12 with a single memory die stack positioned on a component surface of a substrate, the memory die stack having a single die

Figure 18 is a side view of the external storage device of Figure 2 with two memory die stacks positioned on two surfaces of a substrate, each memory die stack having a single die.

Figure 19 is a side view of the external storage device of Figure 12 with two memory die stacks positioned on two surfaces of a substrate, each memory die stack having a single die.

Figure 20 is not covered by the subject-matter of the claims and is a side view of the external storage device of Figure 2 with a single memory die stack positioned on a component surface of a substrate, the memory die stack having two dies.

Figure 21 is not covered by the subject-matter of the claims and is a side view of the external storage device of Figure 12 with a single memory die stack positioned on a component surface of a substrate, the memory die stack having two dies.

Figure 22 is a side view of the external storage device of Figure 2 with four memory die stacks positioned on two surfaces of a substrate, each memory die stack having a single die.

Figure 23 is a side view of the external storage device of Figure 12 with four memory die stacks positioned on two surfaces of a substrate, each memory die stack having a single die.

5 Figure 24 is a side view of the external storage device of Figure 2 with two memory die stacks positioned on two surfaces of a substrate, each memory die stack having two dies.

Figure 25 is a side view of the external storage device of Figure 12 with two memory die stacks positioned on two surfaces of a substrate, each memory die stack having two dies.

10 Figure 26 is a side view of the external storage device of Figure 2 with two memory die stacks positioned on a component surface of a substrate, each memory die stack having two dies.

Figure 27 is a side view of the external storage device of Figure 12 with two memory die stacks positioned on a component surface of a substrate, each memory

15 die stack having two dies.

Figure 28 is a side view of the external storage device of Figure 2 with two memory die stacks positioned on a connection surface of a substrate, each memory die stack having two dies.

Figure 29 is a side view of the external storage device of Figure 2 with four memory

20 die stacks positioned on two surfaces of a substrate, each memory die stack having two dies.

Figure 30 is a side view of the external storage device of Figure 12 with four memory die stacks positioned on two surfaces of a substrate, each memory die stack having two dies.

25 Figure 31 is a side view of the external storage device of Figure 2 with two memory die stacks positioned on a component surface of a substrate, each memory die stack having four dies.

Figure 32 is a side view of the external storage device of Figure 12 with two memory die stacks positioned on a component surface of a substrate, each memory

30 die stack having four dies.

Figure 33 is a side view of the memory die stack of the external storage device of Figures 31 or 32, wherein the dies are arranged in a stair step pattern.

Figure 34 is a side view of the memory die stack of the external storage device of Figures 31 or 32, wherein the dies are arranged in an alternating pattern.
Figure 35 is a side perspective view of an external storage device according to other features of the present invention.

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DETAILED DESCRIPTION

[0011] The described features of the invention provide external storage devices for use with multiple interface connection standards. While the designs are discussed for use with
10 external storage devices, they are by no means so limited. Rather, features of these designs may be used for other devices that couple to any type of serial bus connection, parallel bus connection, or otherwise as desired.

[0012] Figures 1-34 illustrate features of an external storage device 10. In the features
15 shown in Figures 8-13, the device 10 comprises a substrate 12, a connector 14, a controller 16, and at least one memory die stack 18.

[0013] As best shown in Figures 11 and 13, the substrate 12 may be a printed circuit board ("PCB"), which is used to mechanically support and electrically connect the other
20 components of the device 10. In some features, the substrate 12 can include a component surface 24 and a connection surface 26. Items such as an oscillator, an LED status light, discrete components, or other suitable devices, may be mounted and electrically coupled to the component surface 24 and/or the connection surface 26.

25 **[0014]** In some features, as illustrated in Figures 1-2, 7-10, and 12, the connector 14 may be positioned proximate an end 46 of the substrate 12 and configured to be inserted within a corresponding connector. In certain features, the connector 14 may be configured to couple to a corresponding USB 2.0 connector, USB 3.0 connector, or any other standard that is forward or backwards compatible with any of the foregoing USB standards, other
30 suitable serial bus connection, parallel bus connection, or otherwise as desired. However, one of ordinary skill in the relevant art will understand that the connection standards may

be any suitable connection standards that achieve the desired performance of the device 10.

[0015] In some features, such as the features illustrated in Figures 8-10, the connector 14 comprises a plurality of connection fingers 20 and may comprise a contact bar 22. In these features, the connection fingers 20 may be mounted to or embedded within the connection surface 26 of the substrate 12 and electrically coupled to the substrate 12. In certain features, such as where the corresponding connector is a USB 2.0 connector or any other standard that is forward or backwards compatible with the USB 2.0 standard, the connection fingers 20 may be configured to electrically couple to the power and ground wires and the twisted pair of wires (for Hi-Speed and lower data transfer) of the corresponding USB 2.0 connector when the connector 14 is inserted within the corresponding USB 2.0 connector. In the features shown in Figures 1-2, 7-10, and 12, the connector 14 may comprise four connection fingers 20. However, one of ordinary skill in the relevant art will understand that any suitable number and configuration of connection fingers 20 may be used in conjunction with the USB 2.0 standard or other suitable standards.

[0016] In some features, such as the features shown in Figures 8-10, the contact bar 22 may be mounted to the connection surface 26 and electrically coupled to the substrate 12 via a plurality of coupling points 28. In these features, as shown in Figure 2, the substrate 12 comprises five coupling points 28. However, one of ordinary skill in the relevant art will understand that any suitable number and configuration of coupling points 28 may be used. In other features, the coupling points 28 are configured to electrically couple to other types of additional components. In these features, the contact bar 22 forms a projection on the otherwise substantially flat connection surface 26.

[0017] In some features, as best illustrated in Figures 3-6, the contact bar 22 comprises a board 30 and a cover 32. In these features, as shown in Figure 4, the board 30 may be a PCB, where an end 34 of the board 30 can include a plurality of connection pads 36. In some features, the board 30 may comprise five connection pads 36, as shown in Figures 4 and 6-7. However, one of ordinary skill in the relevant art will understand that any suitable

number and configuration of connection pads 36 may be used in conjunction with the USB 3.0 standard or other suitable standards.

[0018] The connection pads 36 may be positioned on the board 30 so as to substantially
5 align with the position of the coupling points 28 when the contact bar 22 is mounted to the connection surface 26, as illustrated in Figure 7. The connection pads 36 may be soldered or otherwise electrically coupled to the coupling points 28 in a suitable manner that allows each connection pad 36 to be electrically connected to the corresponding coupling point 28.
10

[0019] In some features, as shown in Figure 2, the coupling points 28 may be mounted to or embedded within the connection surface 26 of the substrate 12 and electrically coupled to the substrate 12. In these features, the coupling points 28 may be positioned adjacent and/or behind the connection fingers 20. In other features, the coupling points 28 may be
15 mounted to or embedded within the component surface 24, while the connection fingers 20 may be mounted to or embedded within the connection surface 26, or vice versa. One of ordinary skill in the relevant art will understand that the coupling points 28 may be positioned in any suitable location on the substrate 12 that allows the contact bar 22 to electrically couple to the substrate 12.
20

[0020] The board 30 can include a plurality of extensions 38, as best shown in Figures 4 and 6-7. In some features, each extension 38 may also be a PCB having some resilient attributes that cause the extension 38, when bent, to exert a force to return to its original position. One of ordinary skill in the relevant art will understand that the extensions 38 may
25 be made of any suitable material and have any suitable design that allows the contact bar 22 to electrically couple to the corresponding connector when the connector 14 is inserted within the corresponding connector.

[0021] In these features, as shown in Figure 4, each extension 38 can include a coupling
30 projection 40 positioned proximate an end 42 of each extension 38. The coupling projection 40 may be soldered or otherwise electrically coupled to the extension 38 in a suitable manner that allows the coupling projection 40 to be electrically coupled to the

corresponding connection pad 36. The coupling projection 40 may have any suitable shape that provides sufficient contact with the corresponding connector when the connector 14 is inserted within the corresponding connector. Examples of suitable shapes include but are not limited to a triangular, L-shape, U-shape, T-shape, solid projection having a circular or rectilinear cross-sectional shape, or other suitable shapes.

[0022] In some features, such as the features illustrated in Figure 3, the cover 32 may be positioned over the board 30. The cover 32 may be formed of materials including but not limited to any high thermal-resistant plastics, polymers, or other suitable materials. As shown in Figures 3 and 5, the cover 32 may also include a plurality of apertures 44 positioned over the plurality of extensions 38 and proximate the end 42 of each extension 38. The apertures 44 are configured to allow the coupling projections 40 to extend through the apertures 44 when the extensions 38 are in an uncompressed position.

[0023] In some features, the connector 14 may be positioned proximate the end 46 of the substrate 12 so that the connection fingers 20 (when inserted within the corresponding USB 2.0 connector or any other standard that is forward or backwards compatible with the USB 2.0 standard) or the connection fingers 20 and coupling projections 40 (when inserted within the corresponding USB 3.0 connector or any other standard that is forward or backwards compatible with the USB 3.0 standard) electrically couple to the corresponding USB connector. When the connector 14 is inserted within the corresponding USB 3.0 connector (not shown), the USB 3.0 connector presses against the coupling projections 40, in turn applying a bending force to the extensions 38. When the extensions 38 are bent by the USB 3.0 connector, the spring-loaded design of each extension 38 then applies a force to the USB 3.0 connector and the coupling projection 40 to ensure that the components are securely and electrically coupled. In some features, as shown in Figure 6, a ball 48 may be positioned on the end 42 of each extension 38 opposite the coupling projection 40. The ball 48 may be formed of materials including but not limited to silicone, normal rubber, latex, or other suitable materials. Moreover, the ball 48 may be a metal spring or a micro spring. One of ordinary skill in the relevant art will understand that the ball 48 may have any suitable construction or form that provides elastic properties to the extension 38. The ball 48 provides additional force to create a firm electrical coupling

between the corresponding USB 3.0 connector and each coupling projection 40 when the connector 14 is inserted within the corresponding USB 3.0 connector because the ball 48 is at least partially compressed when the connector 14 is inserted within the corresponding USB 3.0 connector.

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[0024] In other features, such as the features shown in Figure 12, the connector 14 may comprise the plurality of connection fingers 20 discussed above, along with a mounting bar 50. As best illustrated in Figure 13, the mounting bar 50 is positioned on the component surface 24 so that the connection surface 26 may remain substantially flat if desirable. In

10 these features, as best shown in Figures 13-15, the mounting bar 50 may comprise a plurality of contact springs 52. Each spring 52 may be formed of a resilient material that, when bent or compressed, exerts a force to return to its original shape. One of ordinary skill in the relevant art will understand that the springs 52 may be made of any suitable material and have any suitable design that allows the mounting bar 50 to electrically

15 couple to the corresponding connector when the connector 14 is inserted within the corresponding connector.

[0025] As shown in Figure 15, the mounting bar 50 may also include a plurality of receptacles 54 that are shaped to receive the contact springs 52. As illustrated in Figure

20 14, each spring 52 may include a hook 56 that mounts and electrically couples the spring 52 to an edge 58 of the mounting bar 50, which is best shown in Figure 15. In some features, such as the features shown in Figure 14, the hook 56 may have a U-shape that substantially conforms to the shape of the edge 58. In other features the hook 56 may be substantially straight and configured to be inserted within a corresponding aperture on the

25 edge 58. One of ordinary skill in the relevant art will understand that any suitable coupling arrangement may be used between the hook 56 and the edge 58.

[0026] Each spring 52 also includes a coupling projection 60, as best illustrated in Figures 14-15. In some features, the coupling projection 60 may be integrally formed with the

30 spring 52. In other features, the coupling projection 60 may be soldered or otherwise electrically coupled to the spring 52 in a suitable manner that allows the coupling projection 60 to be electrically coupled to the substrate 12. The coupling projection 60 may

have any suitable shape that provides sufficient contact with the corresponding connector when the connector 14 is inserted within the corresponding connector. Examples of suitable shapes include but are not limited to a triangular, L-shape, U-shape, T-shape, solid projection having a circular or rectilinear cross-sectional shape, or other suitable 5 shapes.

[0027] In these features, the mounting bar 50 may be mounted to and electrically coupled directly to the substrate 12. By incorporating the mounting bar 50 within the internal assembly of the device 10, the mounting bar 50 is electrically coupled directly to the 10 substrate 12 without the need to solder the mounting bar 50 to a plurality of coupling points 28. However, one of ordinary skill in the relevant art will understand that any suitable configuration of the mounting bar 50 and/or springs 52 may be used in conjunction with the USB 3.0 standard or other suitable standards. As illustrated in Figures 17, 19, 21, 23, 25, 27, 30, and 32, one of ordinary skill in the relevant art will understand that the mounting 15 bar 50 may be positioned in any suitable orientation relative to the substrate 12.

[0028] The mounting bar 50 may then electrically couple the substrate 12 to the corresponding connector via the coupling projections 60. In these features, a plurality of apertures 62 are positioned in the component surface 24 adjacent the plurality of 20 connection fingers 20 that are not covered by the subject-matter of the claims. The coupling projections 60 are configured to extend through the apertures 62 when the springs 52 are in an uncompressed position.

[0029] When the connector 14 is inserted within the corresponding USB 3.0 connector (not 25 shown), the USB 3.0 connector presses against the coupling projections 60, in turn applying a compressive force to the springs 52. When the springs 52 are compressed by the USB 3.0 connector, the spring-loaded design of each spring 52 then applies a force to create a firm electrical coupling between the USB 3.0 connector and each coupling projection 60 when the connector 14 is inserted within the corresponding USB 3.0 30 connector.

[0030] In the various features described herein, an outer casing 66 may be applied to

enclose the assembled substrate 12 and components. In some features, a sealant may be applied to the mounting bar 50 to prevent the case material from flowing into the mounting bar 50 and the internal assembly of the device 10 during the assembly process. Specifically, glue or epoxy may be used to ensure a tight connection and avoid having the
5 case material introduced into the space below the contact bar 22.

[0031] In the features where the mounting bar 50 is mounted on the component surface 24, the mounting bar 50 does not form a projection on the otherwise substantially flat connection surface 26. In some features, the thickness of the mounting bar 50 may not
10 exceed the thicknesses of the other components positioned on the component surface 24, thus allowing at least the mounting bar 50 portion of the connector 14 to be incorporated into the existing dimensions of the device 10. Moreover, the retractable design of the contact springs 52 may allow the coupling projections 60 to completely retract within the outer casing 66 when the device 10 is inserted within a corresponding USB 2.0 connector.
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[0032] Furthermore, by incorporating the mounting bar 50 within the outer casing 66, the manufacturing throughput is improved because the device 10 is assembled as one single part, which is easy to handle by pick and place assembly machines.

20 **[0033]** In other features, such as the features shown in Figure 35, the connector 14 may comprise a combination of the contact bar 22 and the springs 52 discussed above. In these features, the connection fingers 20 are embedded within the cover 32 of the contact bar 22 and electrically coupled to the substrate 12. The cover 32 also includes the plurality of apertures 44 positioned behind the connection fingers 20. Each spring 52 may be
25 mounted to the contact bar 22 so that the coupling projection 60 extends through each aperture 44 when the springs 52 are in an uncompressed position. Each spring 52 may also include the connection pad 36, which may be integrally formed with the spring 52, soldered or otherwise electrically coupled to the spring 52 in a suitable matter that allows the coupling projection 60 to electrically couple to the substrate 12.
30

[0034] In these features, such as the features illustrated in Figures 16-32, the memory die stack 18 includes at least one die 64. For example, in Figures 16-19 and 22-23, each

memory die stack 18 can include a single die 64 which is not covered by the subject-matter of the claims. The memory die stacks 18 shown in Figures 20-21 and 24-30 can include two dies 64 in each memory die stack 18. Each memory die stack 18 shown in Figures 31-34 may include four dies 64 within each memory die stack 18. One of ordinary skill in the relevant art will understand that the memory die stack 18 may include 1, 2, 4, or any suitable number of dies 64. Each die 64 may include connectors 68 that connect the die 64 to a memory channel 70, which in turn connects the die 64 to the controller 16. In some features, the design may include a pair of memory channels 70, also known as dual channel processing, wherein each die 64 (in a memory die stack 18 having two dies 64) is connected to each memory channel 70. With a dual channel configuration, the controller 16 may access each die 64 together or separately. As a result, transactions may be executed twice as fast with dual channel processing.

[0035] In the memory die stacks 18 that include more than one die 64, the dies 64 may be arranged within the memory die stack 18 in a variety of stacking patterns. For example, as shown in Figures 33-34, the dies 64 may be arranged in a stair step pattern (Figure 33), an alternating pattern (Figure 34), a straight stack, or other suitable stacking arrangements. Any suitable arrangement of dies 64 may be used that allow the connectors 68 from each die 64 to reach the memory channel 70. In some features, such as the features shown in Figures 20-21, 24-30, and 34, each die 64 may be rotated 180 degrees from each adjacent die 64. By stacking the dies 64 in a rotated orientation, the heat distribution is improved because the heat generating components (such as the connectors 68) are not adjacent one another.

[0036] In some features, such as the features shown in Figures 16-17 and 20-21 that are not covered by the subject-matter of the claims, a single memory die stack 18 may be mounted to and electrically coupled to the substrate 12. In other features, such as the features shown in Figures 18-19, 24-28, and 31-32, the device 10 may comprise two memory die stacks 18. In yet other features, such as the features shown in Figures 22-23 and 29-30, the device 10 may comprise four memory die stacks 18. In some features, the memory die stacks 18 may be arranged opposite one another so that the memory die stacks 18 are equally distributed on the component surface 24 and an opposing

component surface 24A (Figures 18-19, 22-25, 29-30), may be positioned on the component surface 24 only (Figures 16-17, 20-21, 26-27, and 31-32), or may be positioned on the opposing component surface 24A only (Figure 28). However, one of ordinary skill in the relevant art will understand that any suitable location and distribution of memory die stacks 18 on the component surface 24 and the opposing component surface 24A may be utilized to achieve the desired performance of the device 10.

[0037] The inclusion of the additional memory die stacks 18 provides additional data speed for the device 10. In the features shown in Figures 24-28, which include two memory die stacks 18 in a dual channel configuration (with each memory die stack 18 having two dies 64), the use of two memory die stacks 18 increases the design from a two-channel to a four-channel operation, which approximately doubles the data speed. In other features shown in Figures 29-30, which include four memory die stacks 18 in a dual channel configuration (each memory die stack 18 having two dies 64), the design has an eight-channel operation, which approximate quadruples the data speed.

[0038] Alternatively, as shown in Figures 31-32, an eight-channel operation may be achieved through the use of two memory die stacks 18 (with each memory die stack 18 having four dies 64) and a separate memory channel 70 for each die 64. In these features, in order to minimize the height of the connectors 68, the connectors 68 between each die 64 to the memory channel 70 may pass through the other dies 64 located between the die 64 and the memory channel 70.

[0039] In the features where two memory die stacks 18 are positioned adjacent one another (either on the component surface 24 or the opposing component surface 24A), the dies 64 in each memory die stack 18 can be stacked onto each other in an overlapping arrangement to conserve space on the substrate 12.

[0040] One of ordinary skill in the art will understand that any suitable number and configurations of dies 64 and memory die stacks 18 may be used to achieve the desired data speed and compact design of the device 10.

[0041] The foregoing is provided for purposes of illustrating, explaining, and describing features of the present invention. Further modifications and adaptations to these features will be apparent to those skilled in the art and may be made without departing from the
5 scope of the invention.

Patentkrav

1. Ekstern lagerindretning, omfattende:

5 (a) et substrat (12);
(b) en styreindretning (16), som elektrisk er koblet til substratet;
(c) et antal hukommelseschip-stabler (18), der elektrisk er koblet til substratet (12); hvorved mindst én af antallet af hukommelseschip-stabler (18) omfatter et antal chips (64); og
10 (d) en konnektor (14), som elektrisk er koblet til substratet (12);
(e) hvorved den eksterne lagerindretning er konfigureret til at understøtte mindst to USB-standarder med interfaces, som mekanisk er forskellige;
(f) hvorved konnektoren (14) omfatter fjedre (52) samt tilslutningsfingre
15 (20), som elektrisk er koblet til substratet (12);
(g) **hvorved** konnektoren (14) omfatter et dæksel (32) med et antal åbninger (44), der er positioneret bag ved tilslutningsfingrene (20);
(h) hver fjeder (52) omfatter et koblingsfremspring (60), der strækker sig
20 gennem hver åbning (44), når fjedrene (52) er i en ikke-komprimeret position;
(i) **hvorved** tilslutningsfingrene (20) er indlejret i dækslet (32).

2. Ekstern lagerindretning ifølge krav 1, hvorved en konnektor (68) forbinder hver
25 hukommelseschip-stabel (18) til en hukommelseskanal (70).

3. Ekstern lagerindretning ifølge krav 1, hvorved antallet af chips (64) er arrangeret i et trappetrinmønster.

30 **4.** Ekstern lagerindretning ifølge krav 1, hvorved antallet af chips (64) er arrangeret således, at hver chip er roteret 180 grader i forhold til hver tilgrænsende chip.

5. Ekstern lagerindretning ifølge krav 1, hvorved antallet af chips (64) er arrangeret i en retlinjet stabel.

6. Ekstern lagerindretning ifølge krav 1, hvorved antallet af chips (64) er stablet i
5 et overlappende arrangement.

7. Ekstern lagerindretning ifølge et hvilket som helst af kravene 1, 3-6, hvorved mindst to chips (64) grænser op til hinanden.

10 **8.** Ekstern lagerindretning ifølge et hvilket som helst af kravene 1, 3-7, hvorved mindst to chips (64) er roteret i samme retning.

9. Ekstern lagerindretning ifølge et hvilket som helst af kravene 7-8, hvorved en konnektor (68) forbinder de mindst to chips (64) til en hukommelseskanal (70).

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10. Ekstern lagerindretning ifølge krav 9, hvorved konnektoren (68) passerer gennem en af de mindst to chips (64).

11. Ekstern lagerindretning ifølge et hvilket som helst af kravene 1, 3-8. hvorved
20 hver chip omfatter en konnektor (68), der forbinder chippen (64) til en hukommelseskanal (70).

12. Ekstern lagerindretning ifølge krav hvorved konnektoren (68) mellem hver chip (64) og hukommelseskanalen (70) passerer gennem de andre chips (64),
25 som befinder sig mellem chippen (64) og hukommelseskanalen (70).

13. Ekstern lagerindretning ifølge et hvilket som helst af de foregående krav, hvorved mindst én af antallet af hukommelseschip-stabler (18) er monteret på en komponentoverflade (24) eller en forbindelsesoverflade (26) for substratet (12).

30

14. Ekstern lagerindretning ifølge et hvilket som helst af de foregående krav, hvorved mindst én af antallet af hukommelseschip-stabler er monteret på en

forbindelsesoverflade (26) for substratet (12), og mindst én af antallet af hukom-melseschip-stabler er monteret på en komponentoverflade (24) på substratet.

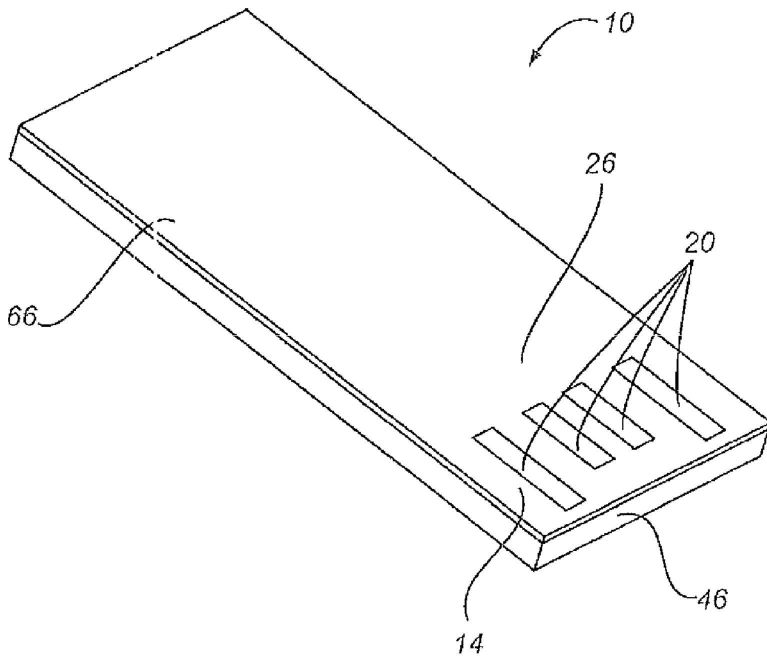


Fig. 1

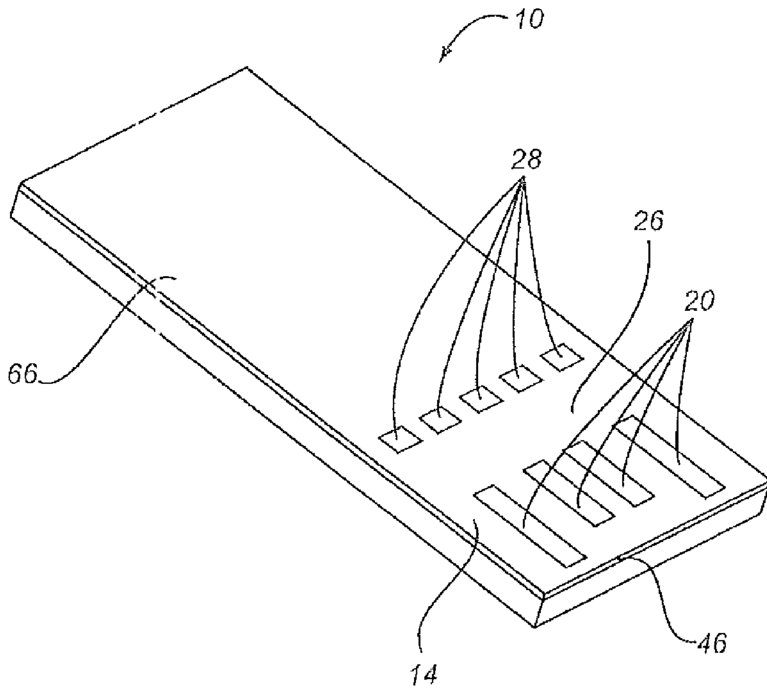


Fig. 2

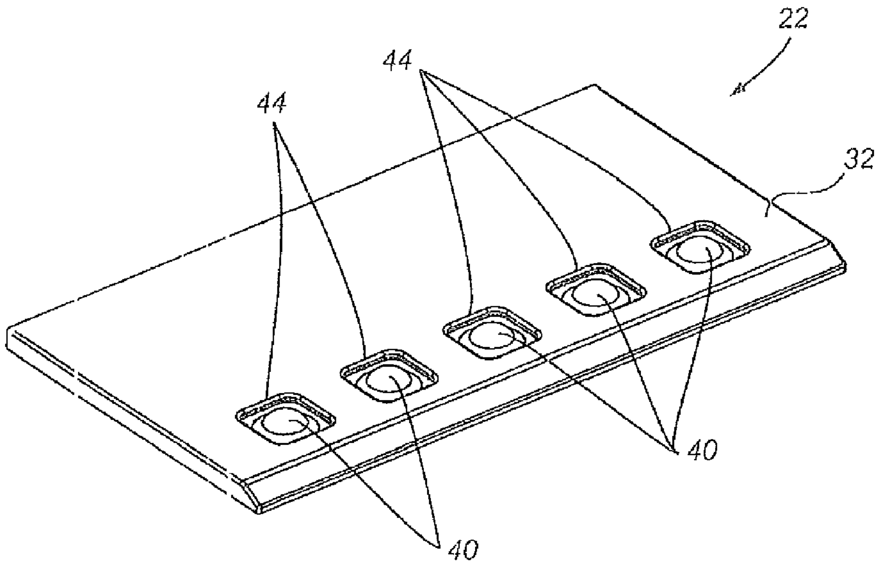
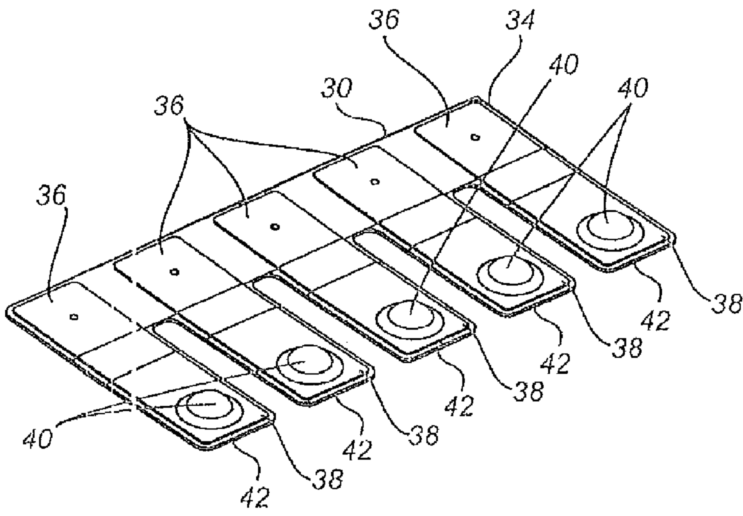


Fig. 3



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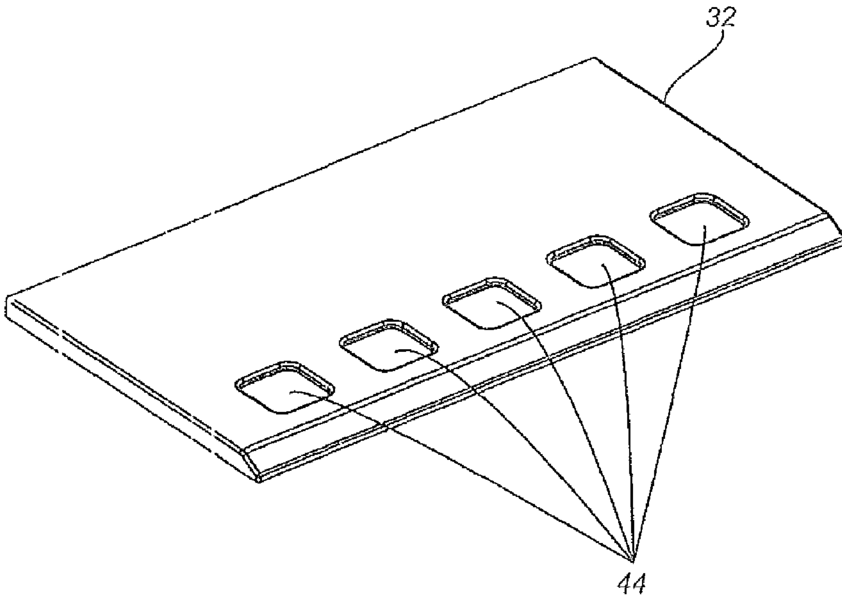


Fig. 5

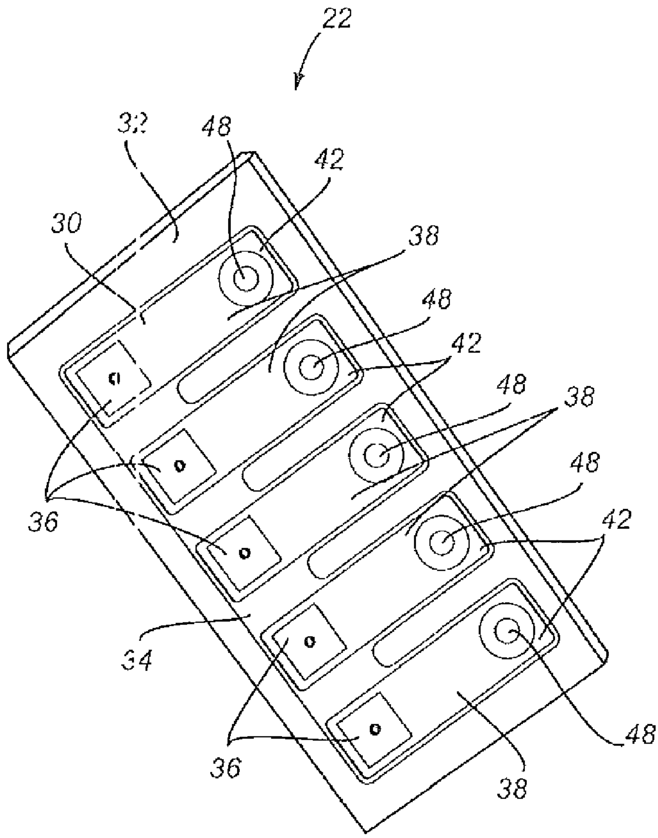
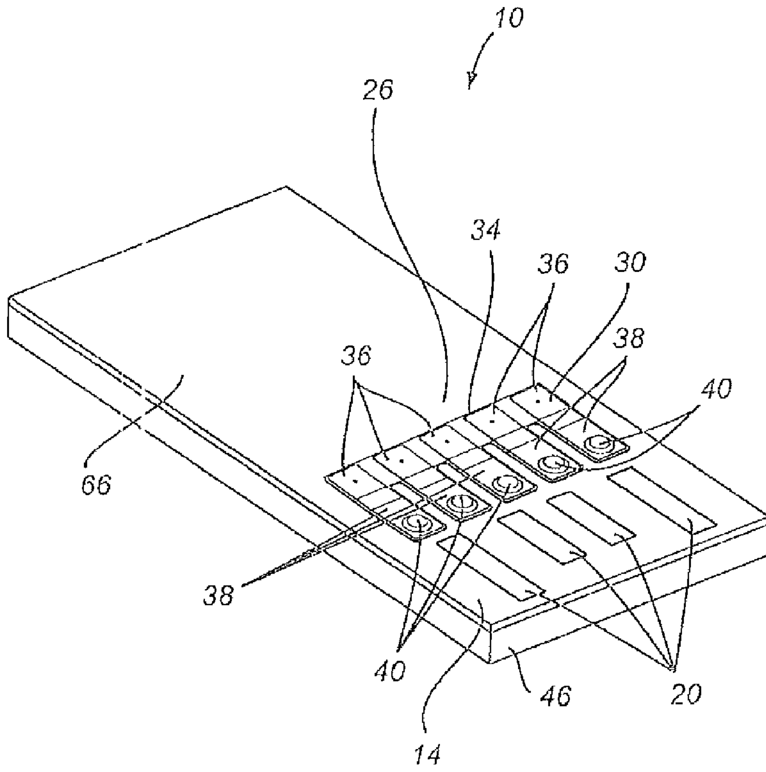


Fig. 6



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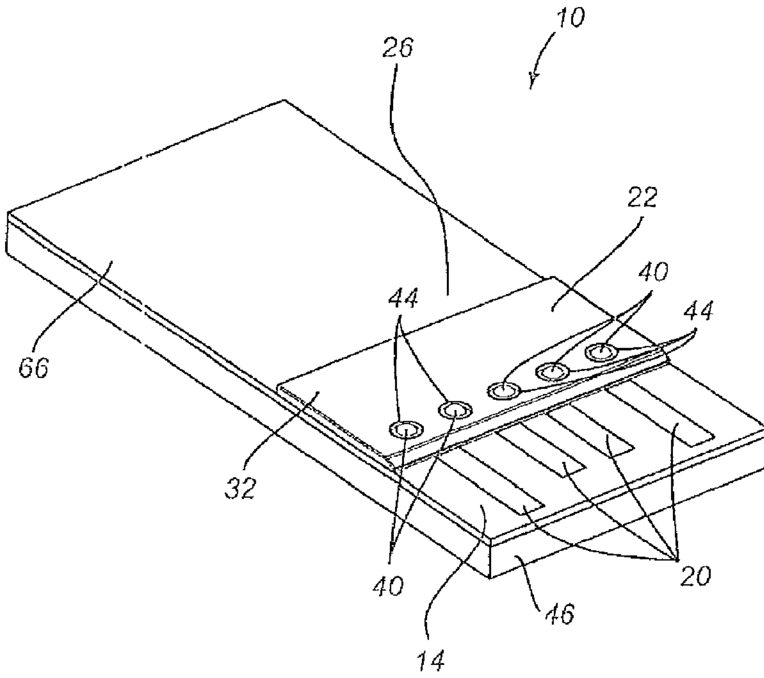


Fig. 8

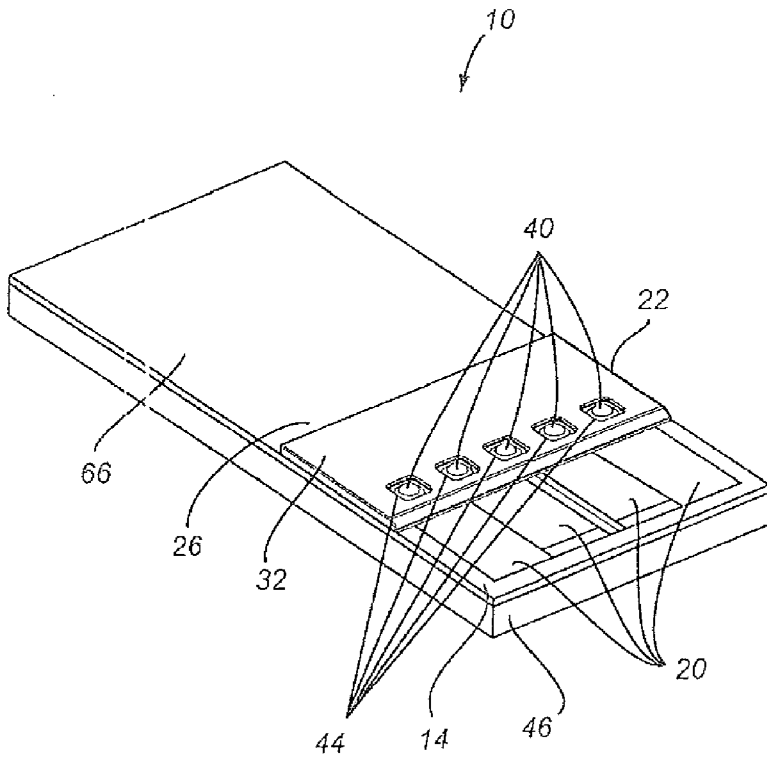


Fig. 9

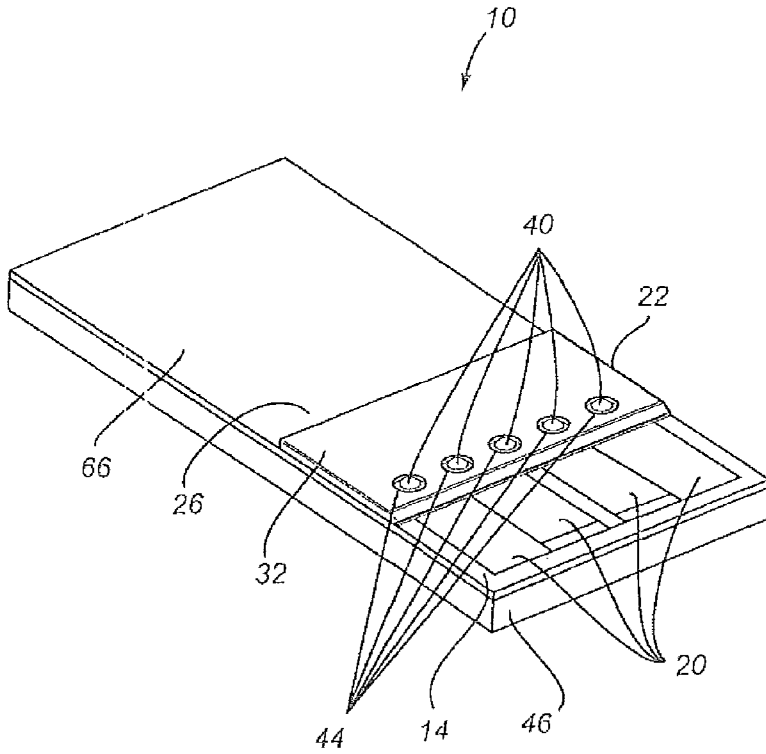


Fig. 10

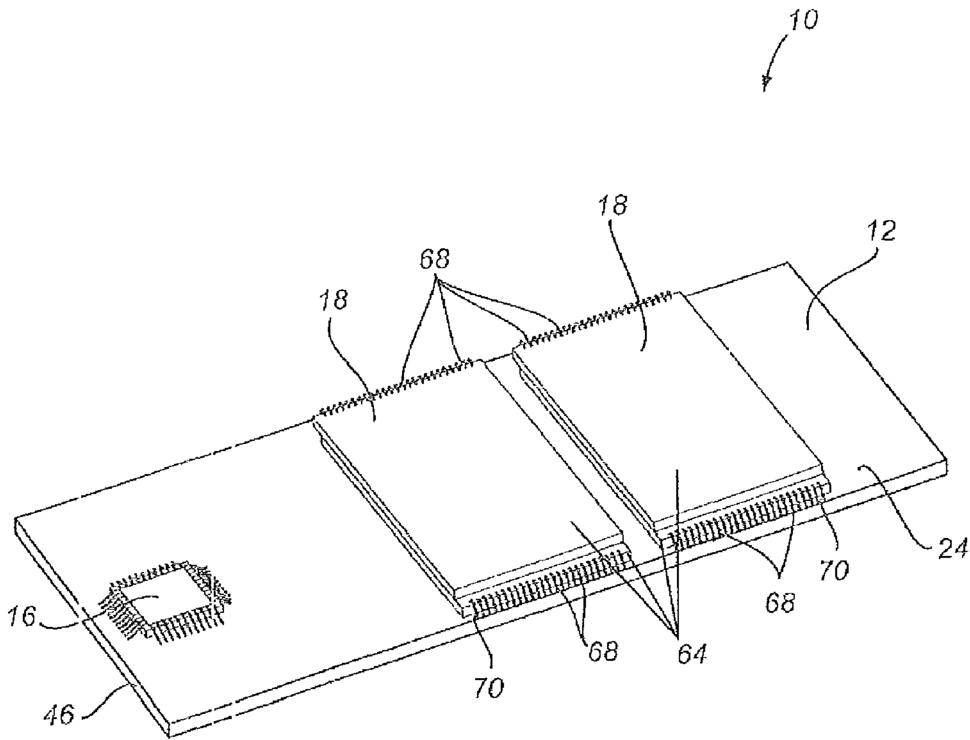


Fig. 11

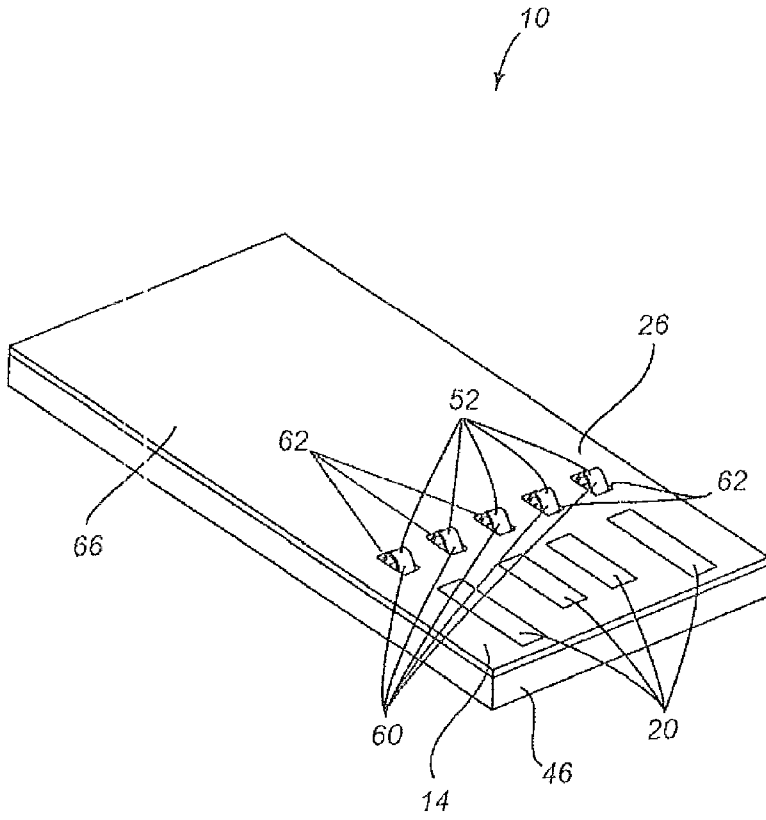


Fig. 12

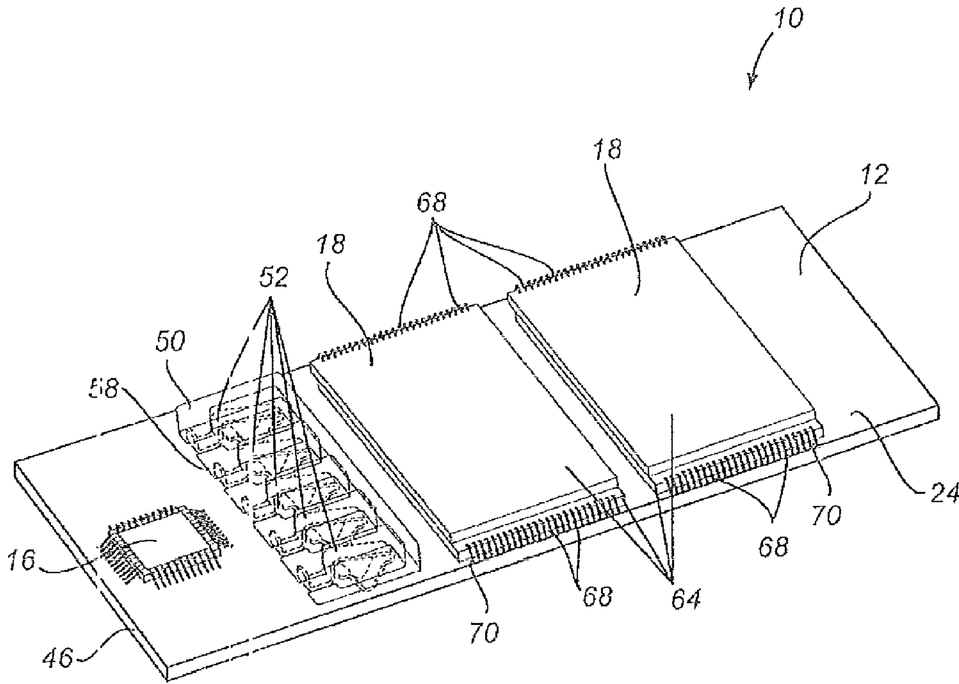


Fig. 13

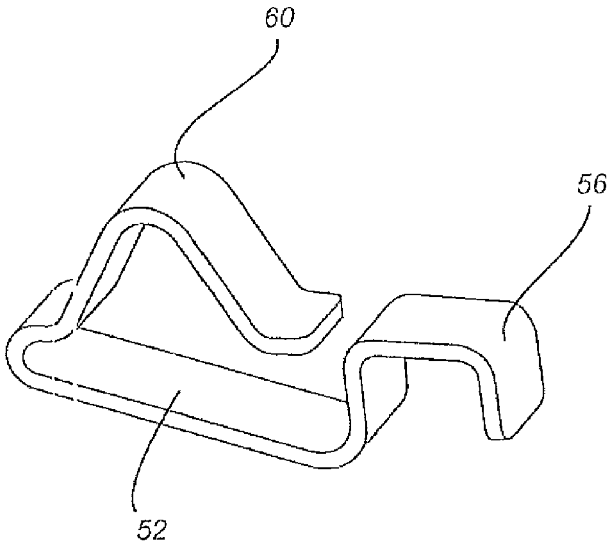


Fig. 14

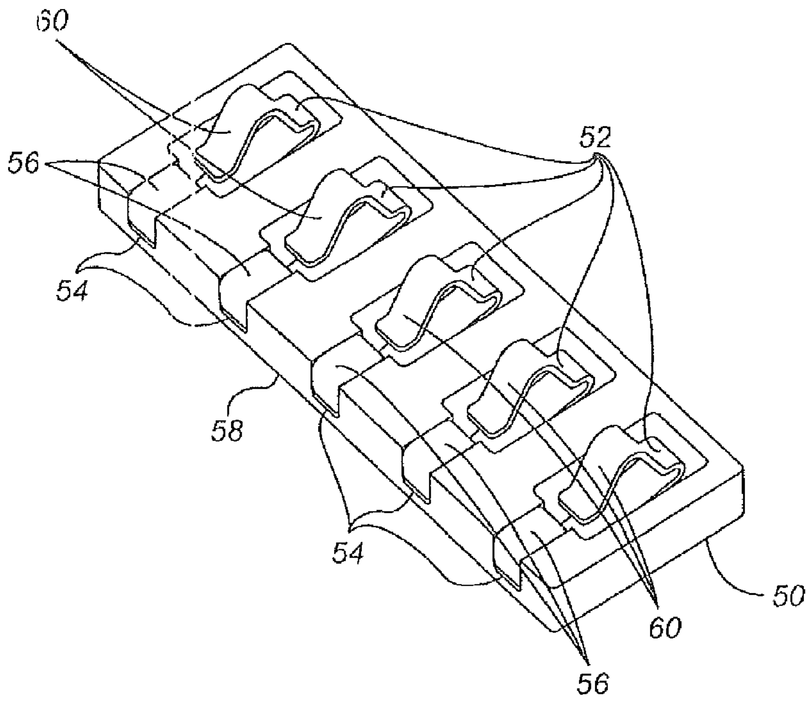


Fig. 15

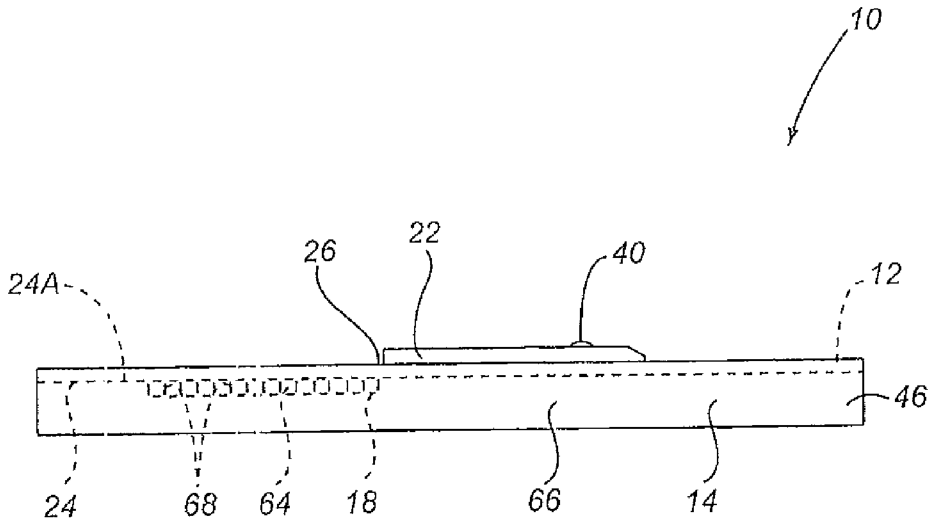


Fig. 16

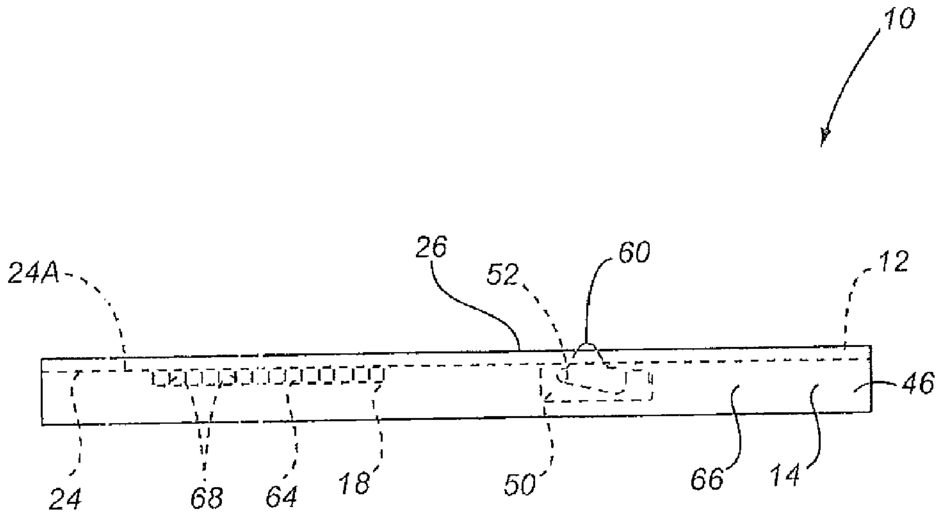
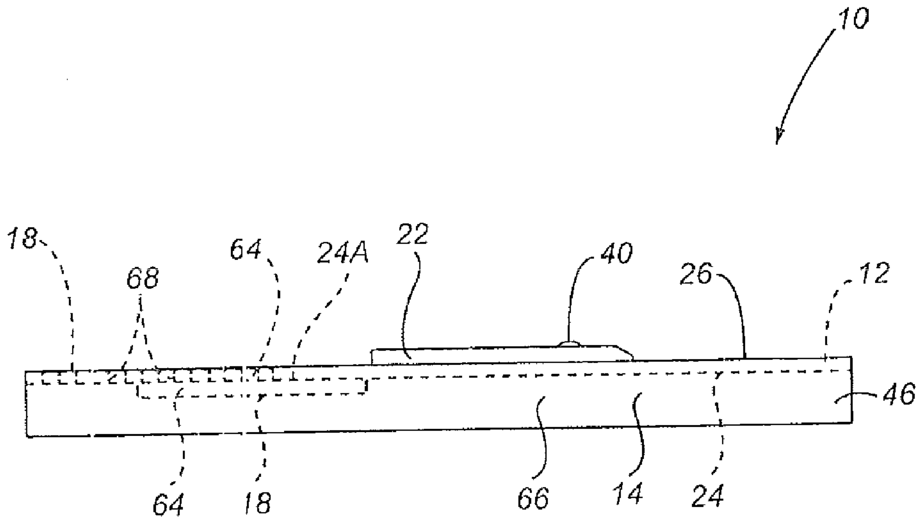


Fig. 17



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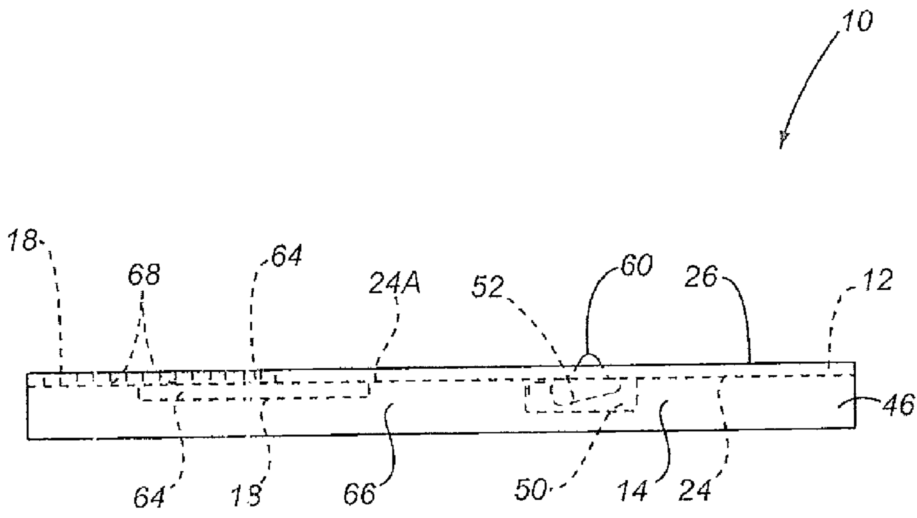

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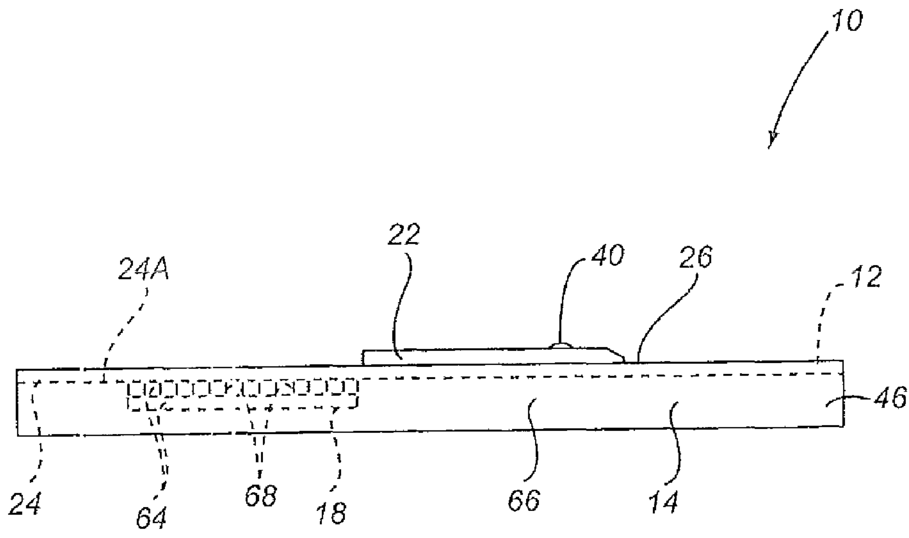


Fig. 20

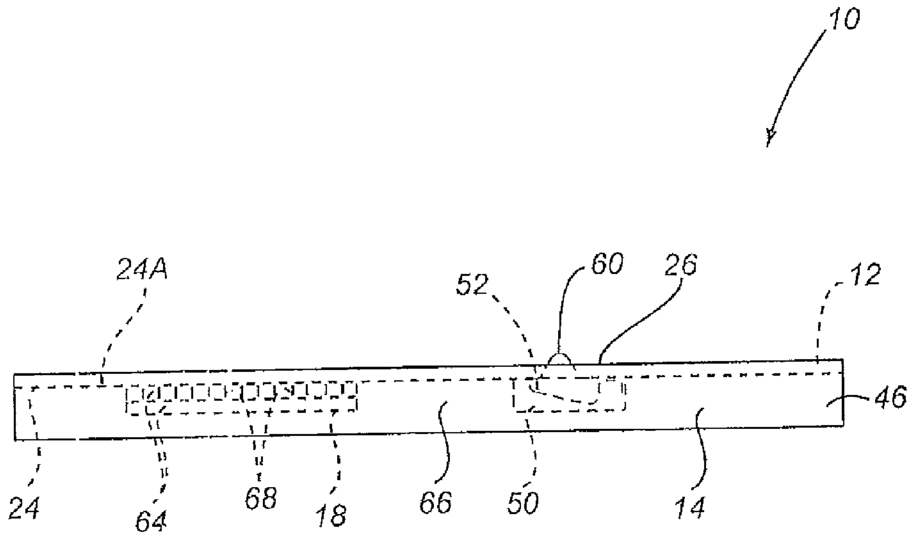


Fig. 21

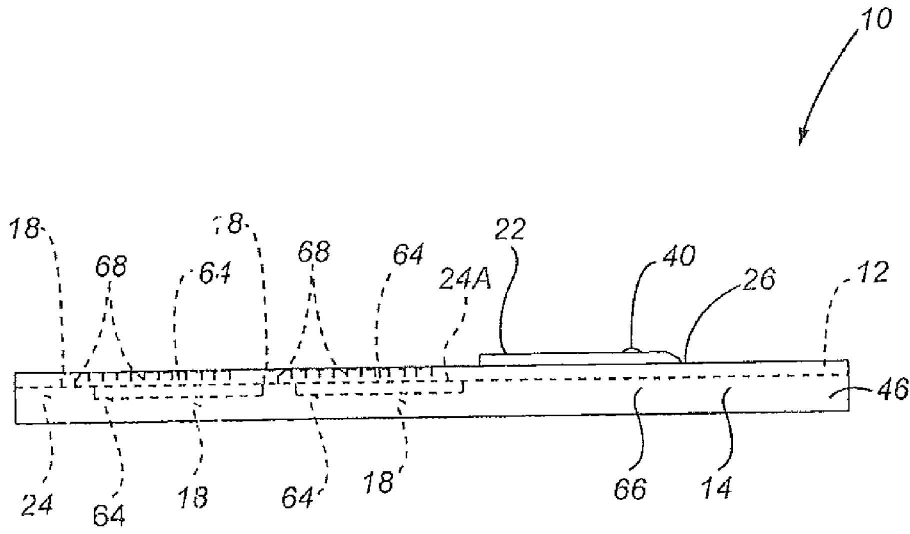


Fig. 22

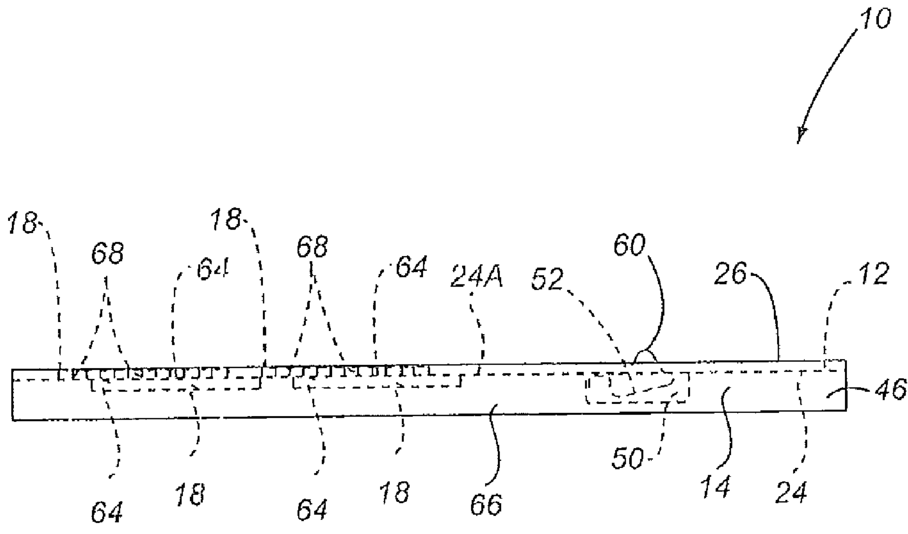


Fig. 23

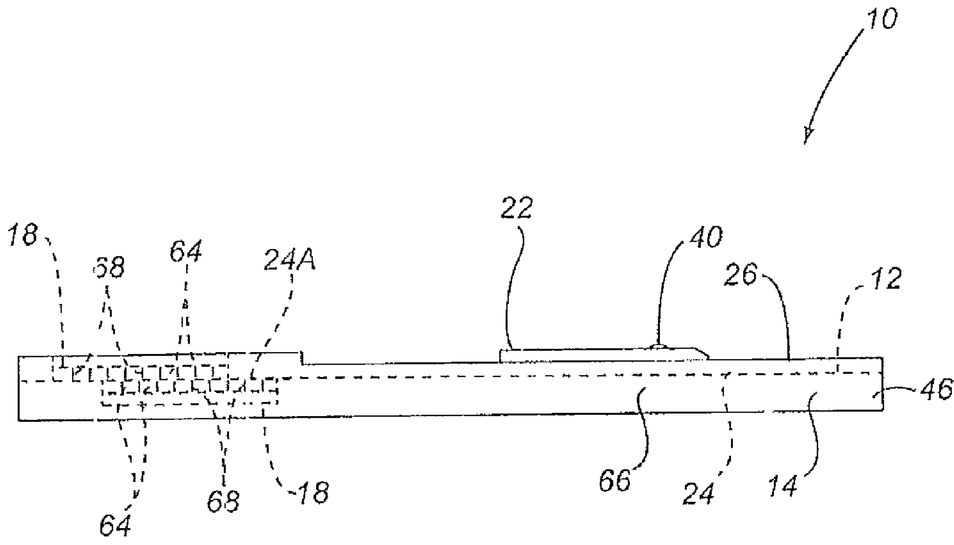


Fig. 24

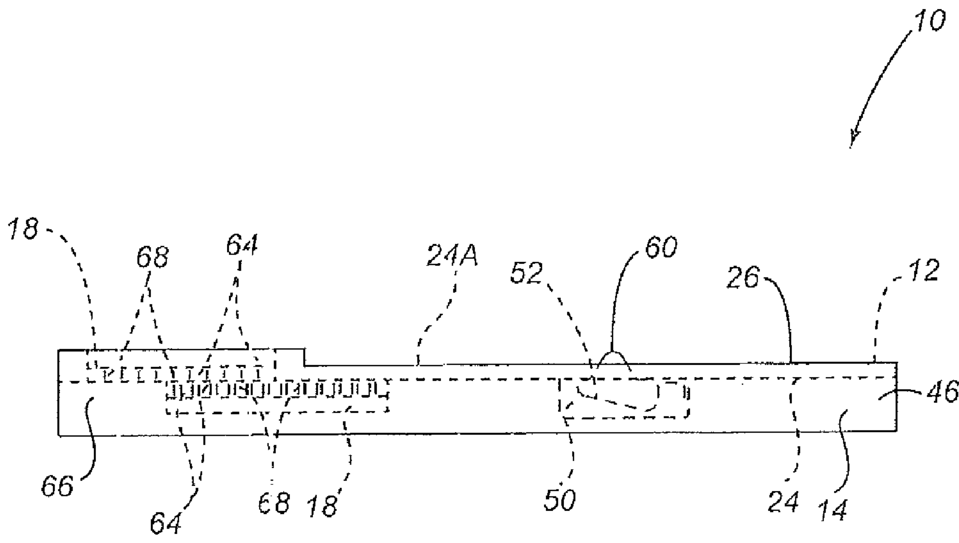


Fig. 25

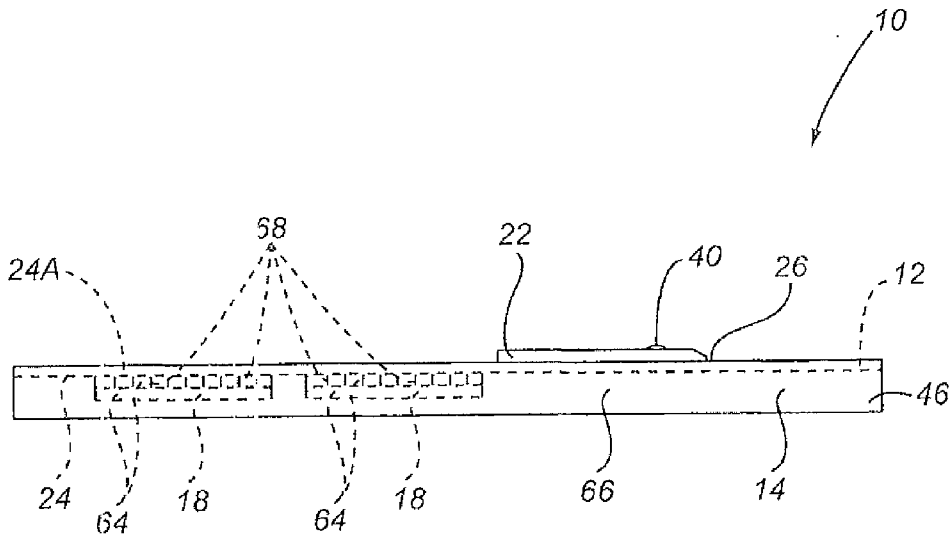


Fig. 26

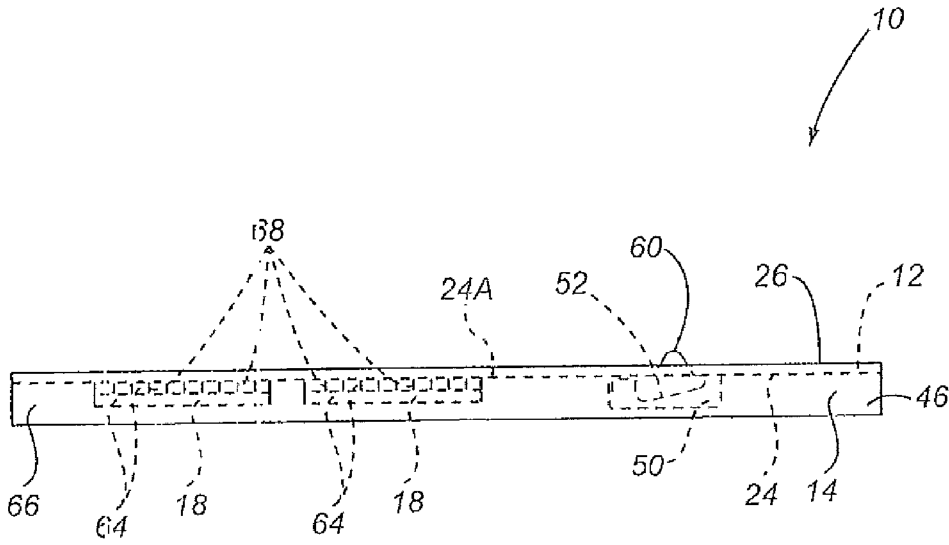


Fig. 27

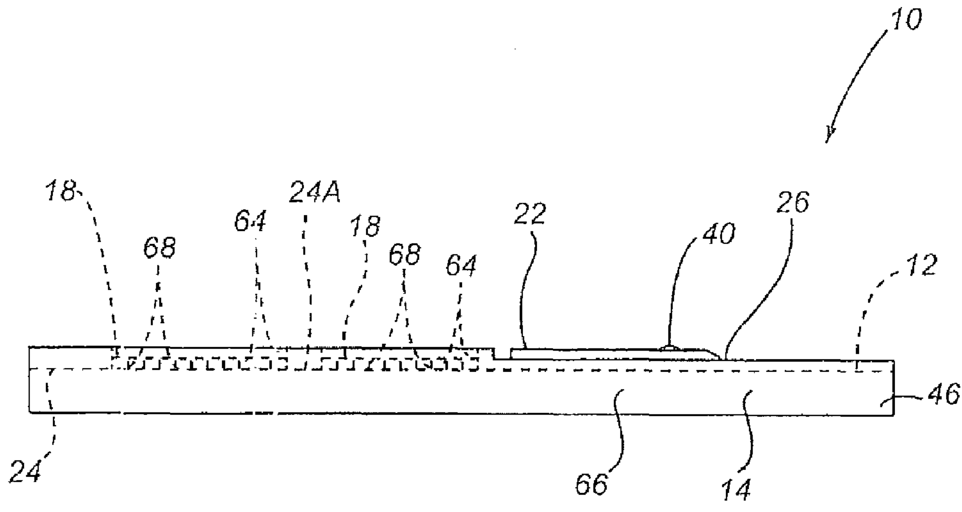


Fig. 28

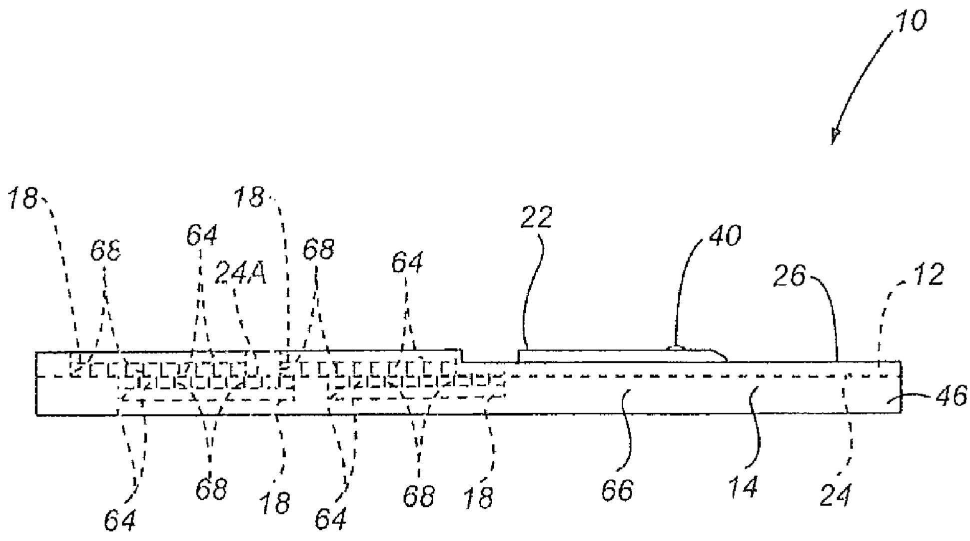


Fig. 29

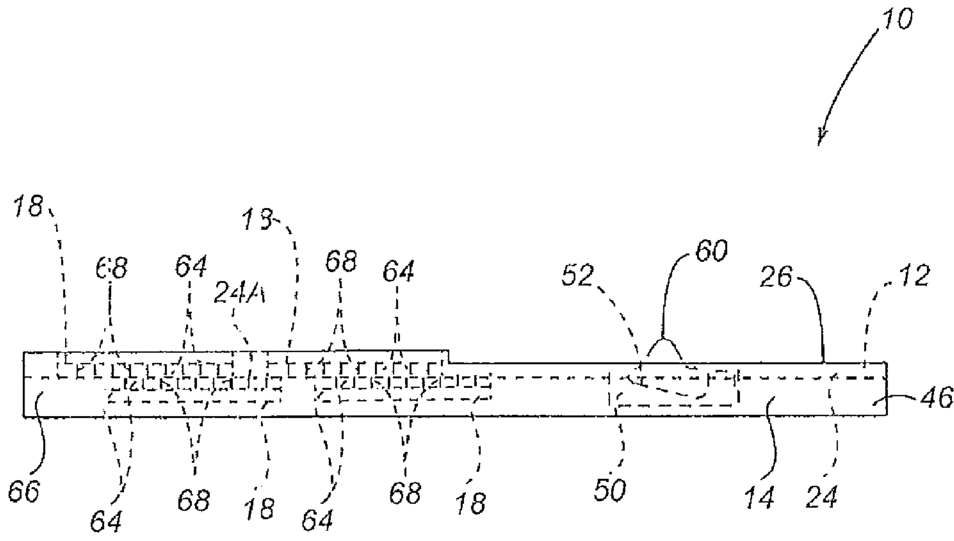
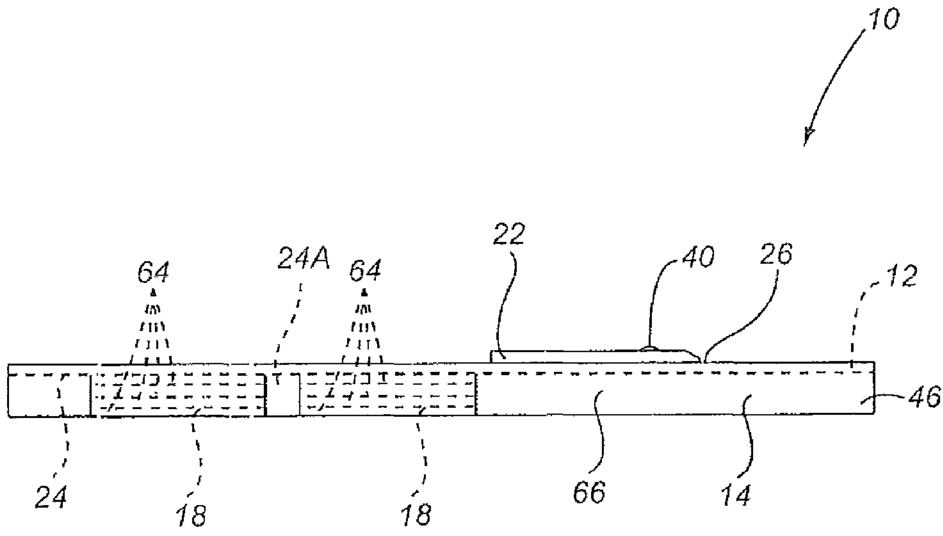


Fig. 30



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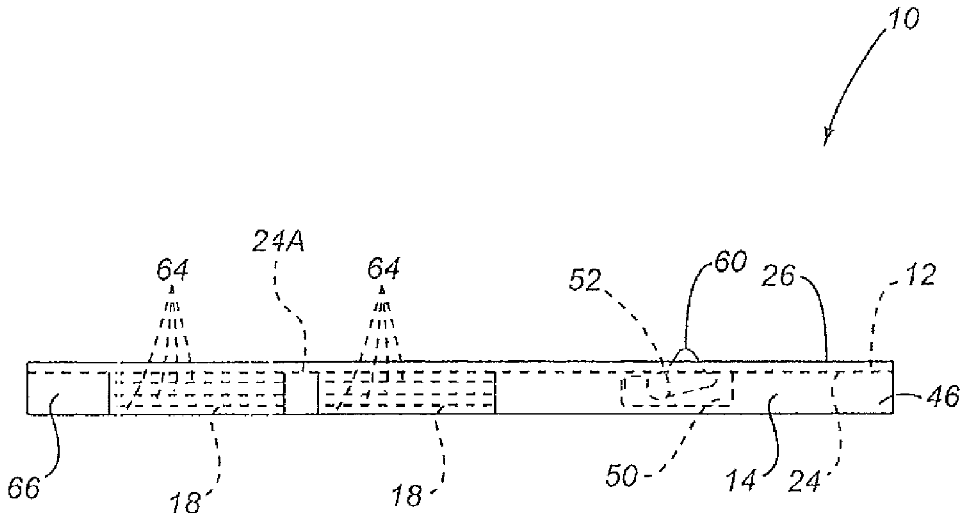

Fig. 32

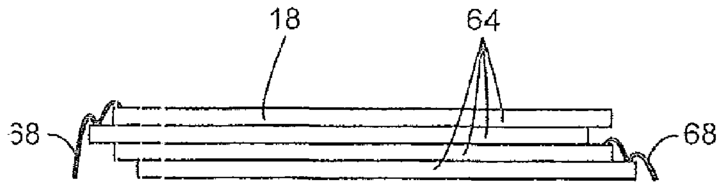

Fig. 33

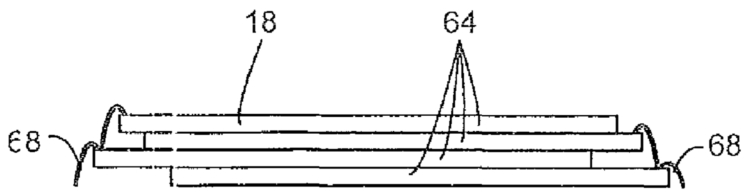

Fig. 34

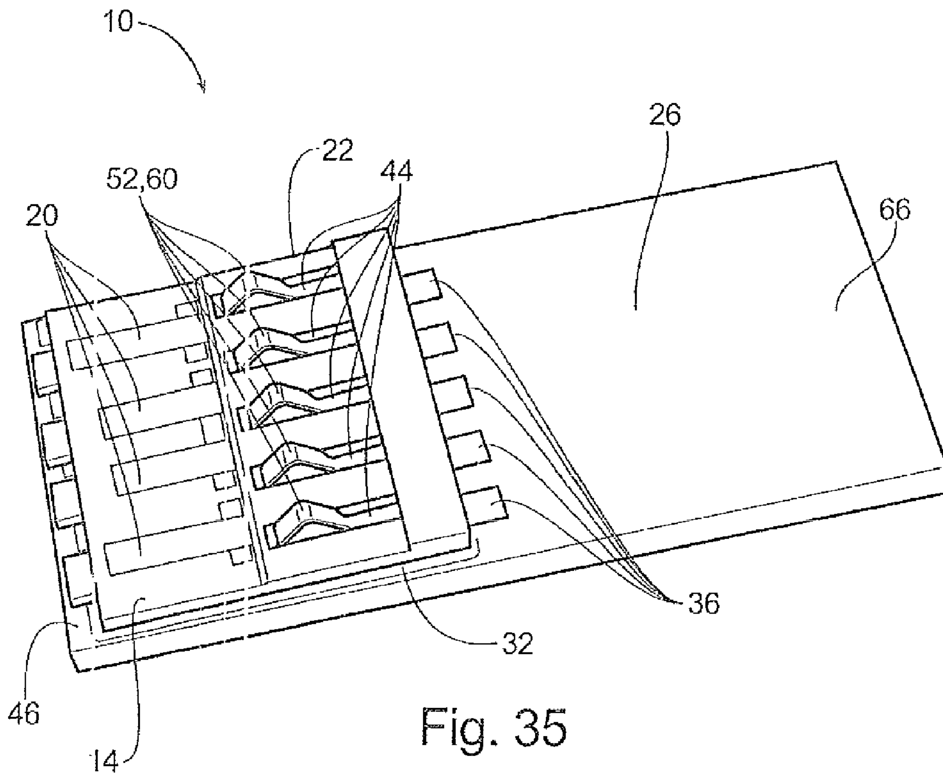

Fig. 35