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(54) **Circuit board of communication product and manufacturing method thereof.**

(57) The present invention provides a circuit board of a communication product and a manufacturing method thereof. The circuit board comprises a main body of a circuit board and an isolation cover. A surface of the main body of the circuit board has a power transistor, an insulating layer, a plurality of first openings disposed at intervals on the insulating layer and around the power transistor, and a plurality of soldering portions exposed from the first openings respectively. The isolation cover comprises a cover body and a plurality of second openings equidistantly opened on a lateral side of the cover body. The isolation cover is disposed on the surface of the main body of the circuit board, and is soldered to the soldering portions through a local spot soldering process.

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Circuit board of communication product and manufacturing method thereof

The present invention relates to a shielding technology capable of eliminating interferences and noises, and more particularly to a circuit board of a communication product and a manufacturing method thereof.

With the development of the broadband network and the trend of the digital technology, the wireless products with wireless transceiving functions are increasingly popular, such as a wireless network access point (AP), a mobile phone, a personal digital assistant (PDA), and a notebook computer. The wireless products not only provide extensive range of functions but also deliver more convenient and effective services. However, the wireless communication products are sensitive to the surrounding electromagnetic waves caused by other wireless communication systems or external noises.

For example, when a wireless product performs the data wireless transmission under a high power state, the high frequency harmonic waves are extremely easily generated by non-linear characteristics of active components, so as to result in an electro-magnetic interference (EMI) emission, which is often the prime contributor to the performance degradation. In order to solve the problem, legal regulations are made in many countries to regulate and restrict illegal input applications and usages of the wireless products. As a result, when the designers and manufactures of the wireless product design a control line of the wireless product, the requirements of the related regulations must be fulfilled and incorporated into the wireless design. Furthermore, the circuit of the wireless product is also affected by the signals of the external

electromagnetic wave, such as, radio frequency (RF) wireless signals, to result performance inconsistencies.

Therefore, it is a critical factor for the designers and developers to know how to effectively eliminate the interference and the noise in order to improve the performance of the wireless products. Several conventional methods are proposed to reduce the impact of EMI and RF emissions on wireless communication products, such as the methods disclosed in, ROC Patent No. 521561, US Patent No. 6, 689,670, and US Patent No. 6,528,866.

Conventionally, an isolation cover is disposed on a circuit board to eliminate emissions related to EMI or RF interference. As shown in FIG. 1, an isolation cover 22 is fully soldered onto a main body 20 of a circuit board 2 by adopting a surface mount technology (SMT), so that the isolation cover 22 can cover part of components on the circuit board 2, such as, the chip(s) located on a surface of the main body 20 of the circuit board 2. A reflow-soldering process is performed on the circuit board 2 through a tin oven (not shown).

However, this conventional method is used a soldering technique called a single-piece fully soldering process to solder the isolation cover 22 entirely onto the main body 20 of the circuit board 2. After the reflow-soldering process, if some of the components underneath the isolation cover 22 fail, a desoldering process must be performed to detach the isolation cover 22 in order to replace the corresponding components. In this manner, the maintenance is costly and time consuming, and the surface of the circuit board main body 20 is easily damaged or deformed, more significantly, the detached isolation cover 22 cannot be reused. As a result, the fabrication cost of the conventional method is extremely high.

Meanwhile, when the isolation cover 22 is disposed onto the circuit board main body 20, the components underneath are entirely covered. The heat generated during the soldering process cannot be effectively dissipated, resulting a temperature differentiation between the components, which leads to a tombstone effect. Thus, the components located in the isolation cover 22 can fail easily.

In order to solve the disadvantage of the single-piece fully soldering technology, a two-pieces fully soldering technology is provided as shown in FIG. 2. A lower frame 24 and an upper cover 26 are used to replace the single piece isolation cover. During assembling process, the lower frame 24 is firstly soldered to the main body 20 of a circuit board 2', and the upper cover 26 is used to cover the main body 20 of the circuit board 2' after the circuit board 2' passing through the tin oven, so that the upper cover 26 can be integrated to the lower frame 24.

However, the requirements of performing the two-pieces fully soldering process are more complicated, and the cost is relatively higher. Furthermore, the lower frame 24 is required to be firstly soldered, and after the circuit board 2' passing through the tin oven, a second processing is performed on the upper cover 26 for the second time. Thus, the assembling process of this method is more costly.

Both the single-piece fully soldering technology and the two-pieces fully soldering technology require the solder to perform the soldering process, and the heat dissipation is the major problem during the soldering process that can severely damage to the components on the circuit board and the circuit board itself.

In EP 1 445 999 A1 a method is disclosed for providing a printed wire board or circuit board with a

shield can or isolation cover. This method involves providing a groove on the surface of the circuit board, which groove has a contour corresponding to a contour of the rim of the shield can. A solder paste is then applied to the circuit board to fill the groove, and the shield can or isolation cover is then placed on the solder paste which its rim aligned with the groove. When the circuit board is then heated, the shield can is solded to the board. In one embodiment the rim of the shield can has protrusions and the groove in the circuit board is made up of a series of shorter, discrete grooves. Although the object of the method of this prior art document is to prevent any gaps between the shield can and the circuit board, the document states that such gaps may occur in the areas between the protrusions. This should however be kept as small as possible. EP 1 445 999 A1 does not disclose any specific dimensions for the gap, and actually proposes adding extra solder paste to fill these gaps.

From the above-mentioned techniques, the conventional methods have serious drawbacks. Therefore, it is an objective of the present invention to provide a true solution to resolve all the drawbacks, and an improved circuit board of a wireless communication product and a fabrication method that can successfully eliminate the interferences.

In view of the disadvantages of the conventional art, the present invention is directed to a circuit board of a communication product and a manufacturing method thereof, so as to simplify a process and a maintaining procedure.

The present invention is further directed to a circuit board of a communication product and a manufacturing method, that increases the productivity and improve the quality of the performance.

In order to achieve the above and other objectives, the present invention provides a circuit board, which is applied to a communication product. The circuit board comprises a main body of the circuit board comprising a power transistor and a predetermined covering region that is used for covering the power transistor; an insulating layer having a plurality of openings disposed at intervals along the circumference of the predetermined covering region; and a plurality of soldering portions, that are respectively exposed from of each opening.

The present invention further provides a circuit board, which is applied to a communication product. The circuit board includes a main body of a circuit board and an isolation cover. The main body of circuit board has a power transistor, an insulating layer, a plurality of first openings disposed at intervals on the insulating layer and around the power transistor, and a plurality of soldering portions exposed respectively from the first openings disposed on a surface thereof. The isolation cover comprises a cover body of a cover soldered to each soldering portion and a plurality of second openings equidistantly opened on a lateral side of the cover body of the cover. A width (a diameter of the heat dissipation portion) of the second opening is between 1λ and 2λ, $\lambda=\nu/f$, in which λ is the wave length, ν is the speed (m/s), f is the frequency (Hz), and a maximum value of f is 26.5 GHz.

In the above-mentioned circuit board, each soldering portion is corresponding to a corner of the cover body. Each soldering portion is used as a soldering pad. Each soldering portion is provided with a solder material respectively. Each insulating layer is a solder mask layer. The circuit board further comprises a plurality of heat dissipation portions equidistantly opened on a top surface

of the cover body in accordance with a preferred embodiment of the present invention. Every second opening is located on a lateral side of the cover body, which is, for example, a rectangular opening.

The present invention further provides a method for manufacturing a circuit board of a communication product. The method of the present invention comprises: providing a main body of a circuit board, in which the main body of the circuit board has a power transistor, an insulating layer, a plurality of first openings disposed at intervals on the insulating layer and around the power transistor, and a plurality of soldering portions exposed from each first opening respectively disposed on a surface thereof; providing an isolation cover, in which the isolation cover comprises a cover body and a plurality of second openings equidistantly opened on a lateral side of the cover body; wherein a width of each second opening is between 1λ and 2λ, $\lambda=v/f$, λ is a wave length, v is a speed (m/s), f is a frequency (Hz), and a maximum value of f is 26.5 GHz; disposing the isolation cover onto the surface of the main body of the circuit board; and soldering the isolation cover to each soldering portion through a method of local spot soldering.

In the above-mentioned manufacturing method, the local spot soldering may be performed through a SMT.

Comparing with the conventional art, the present invention designs a circuit board, in which the local spot soldering technique can be performed, to prevent the non-uniformity of the heat dissipation problem from occurring during the soldering process. As a matter of fact, one of the advantages of the local spot soldering is to allow partial desoldering when the isolation cover is required to be detached, as a result, the time and cost can be

drastically reduced. Therefore, the present invention simplifies the manufacturing process and the maintenance procedure. At the same time, the present invention provides a method in which the reflow-soldering temperature can be modified through the openings or other heat dissipation portions, in such that the internal reflow-soldering temperature becomes uniformly. The productivity will increase and the quality of the performance can be drastically improved.

The present invention will become more fully understood from the detailed description given herein below for illustration only, and thus are not limitative of the present invention, and wherein:

FIG. 1 is a schematic view of a conventional circuit board having a single-piece fully soldered isolation cover;

FIG. 2 is a schematic view of a conventional circuit board having a two-pieces fully soldered isolation cover;

FIGs. 3a to 3e are schematic views of a method for manufacturing a circuit board according to a first embodiment of the present invention;

FIG. 4 is a schematic view of the circuit board according to a second embodiment of the present invention; and

FIGs. 5a and 5b are schematic views of the circuit board according to another embodiment of the present invention, in which FIG. 5a is a schematic partial three-dimensional view, and FIG. 5b is a cross sectional view.

It should be noted that a circuit board of this embodiment and other embodiments is applied to a communication product, various circuit boards used by different communication products can be applicable although

they may slightly be modified. In the present invention, the shielding technology is improved to effectively eliminate the interference and the noise in the circuit board to improve the performance of communication product.

Referring to FIGs. 3a to 3e, schematic views of a first embodiment of the present invention are shown. As shown in FIG. 3a, a substrate 10 is provided and has a power transistor (not shown, described hereafter) and a line layer 101 disposed on a surface thereof. A plurality of soldering portions 113 are formed in the line layer 101. As shown in FIG. 3b, an insulating layer 115 is entirely formed on the surface of the line layer 101. Next, as shown in FIG. 3c, at the position on which an isolation cover (that is, a predetermined covering region, described hereafter) is predetermined to be disposed, a plurality of openings 1151 (first openings) are formed at intervals on the insulating layer 115, and each soldering portion 113 is exposed respectively from every opening 1151. FIG. 3d, each soldering portion 113 is provided with a solder material 1131 above respectively.

The solder material 1131 is deposited on each soldering portion 113 of the circuit board through a stencil printing technology. For example, a stencil (not shown) having a plurality of grids is disposed, after the solder material 1131 is deposited on the stencil, a roller can be used to roll back and forth on the stencil, or a spraying method can be adopted to spray the solder material 1131 through the grids to form the solder material 1131 on each soldering portion 113.

According to the embodiment, a plurality of openings 1151 (first openings) are formed before the circuit board passes through the tin oven, such that each soldering portion 113 is respectively exposed. However, in other

embodiments, the above-mentioned stencil design is modified, and a required layout is directly printed in the predetermined covering region, wherein the insulating layer 115, the plurality of openings 1151 (first openings) positioned at intervals on the insulating layer 115, and the soldering portions 113 exposed from openings 1151 are all formed simultaneously in one process. As a matter of fact, the stencil design is not restrained to the above-mentioned structures.

As shown in FIG. 3e, in accordance with the preferred embodiment of the present invention, a circuit board 1 is provided. The circuit board 1 comprises a main body 11 of circuit board 1 having a predetermined covering region 111; an insulating layer 115 disposed along the edges (circumference) of the predetermined covering region 111 and has a plurality of openings (first openings) 1151 at intervals; and a plurality of soldering portions 113, respectively exposed from each opening 1151. In this embodiment, the power transistor 110 as shown in FIG. 3e can be firstly disposed, but the power transistor 110 can also be disposed after the soldering portions 113 and the insulating layer 115 are formed. The predetermined covering region 111 is used to at least cover the power transistor 110. As a result, the application of present invention is not restricted to this embodiment. The power transistor 110 can be, for example, a chip, and each opening (first opening) 1151 is located around the power transistor 110.

The main body 11 of the circuit board 1 has the predetermined covering region 111 on a surface, in which the isolation cover is disposed. According to the embodiment, the main body 11 of the circuit board 1 and the predetermined covering region 111 are rectangular-shaped. The shape of the components of the present invention is not

limited.

Each insulating layer 115 is a solder mask layer. Each soldering portion 113 is, for example, a pad, and each soldering portion 113 respectively has a solder material 1131. In this embodiment, each soldering portion 113 is correspondingly disposed on the edges of the predetermined covering region 111, and is located on the corner of the predetermined covering region 111. At the same time, the soldering portions 113 are spaced by the insulating layer 115, such that a local spot soldering process is adopted when the isolation cover is integrated to the circuit board 1.

The predetermined covering region 111 is rectangular-shaped, and each soldering portion 113 is located on the corner and two sides of the predetermined covering region 111. According to the mechanics analysis, the stress will be concentrated at the corner. In other words, the corner is the weakest position than others. Therefore the corresponding soldering portions 113 are disposed on the corners and the two sides of the predetermined covering region 111 to strengthen the position. However, in other embodiments, the shape of the predetermined covering region 111 and the disposing positions of each soldering portion 113 can also be changed. Each soldering portion 113 can also be disposed on the positions having concentrated stress of the predetermined covering regions 111 with different shapes, other than the corner(s) or the sidewalls. In other words, the locations of the soldering portions 113 are not restricted to the shapes or the corners or the sidewalls of the predetermined covering regions 111. Although in this embodiment, eight soldering portions 113 are disposed. But according to other preferred embodiments, two or more soldering portions 113

are disposed and the local spot soldering process is performed.

In this embodiment, the circuit board 1 is a circuit board without an isolation cover. The circuit board 1 may also be a circuit board with the isolation cover assembled onto the main body 11 of the circuit board 1.

Referring to FIGs. 4 to 5b, schematic views of a second embodiment of the present invention are shown. As shown in FIG. 4, a circuit board 1' of this embodiment comprises a main body 11 of circuit board 1 and an isolation cover 13 disposed on the main body 11 of circuit board 1, in which the components that are identical or similar to those of the first embodiment are marked with identical or similar reference numerals.

A surface of the main body 11 has a power transistor 110, an insulating layer 115, a plurality of first openings 1151 (as shown in FIG. 3b of the first embodiment) disposed at intervals on the insulating layer 115 and around the power transistor 110, and a plurality of soldering portions 113 exposed from each first opening 1151 respectively.

The isolation cover 13 comprises a cover body 131 soldered to each soldering portion 113, a plurality of second openings 133 equidistantly opened on the lateral side of the cover body 131, a plurality of heat dissipation portions 135 equidistantly opened on the top surface of the cover body 131.

The cover body 131of the second embodiment is, for example, a rectangular-shaped cover body. The design of the cover body 131 of present invention is not limited to rectangular-shaped structure. The width of each second opening 133 is larger than or equal to a pitch of each first opening 1151. The distance and an opening height between

every two second openings 133 are designed according to a wave length calculated in respect of the frequency (maximally being 26.5 GHz) of the communication product. Generally, after converting to a wave length formula, when the value of the opening width is smaller than 1.2 mm, it indicates that most of the EMI high frequency noise can be eliminated.

For example, an aperture ratio of each second opening 133 disposed on the side of the cover main body 131 must satisfy the formula as follows:

$$\lambda = \nu / f \qquad \text{(Formula 1)}$$

λ is a wave length, ν is a speed (m/s), and f is a frequency (Hz). An EMI maximum value of f is 26.5 GHz, when ν is $3*10^8$ m, λ is 1.2 mm, which is the value meets the requirements of the EMI Safety rule of different countries.

At the same time, for the RF communication technology, when a wireless local area network (WLAN) or an ultra wide band (UWB) communication protocol is applied to the communication, the value of f in the WLAN is usually from 2.4 GHz to 5 GHz, and the value of f in the UWB system is usually from 3 GHz to 10 GHz. Therefore, as long as the value of f is more than double frequency of the low power UWB (that is, approximately 1.2 mm), the requirement of shielding the external noise is achieved. In addition, disregard whether there is linear or the non-linear effect, when the value of f is wireless fidelity (WIFI) 2.4 GHZ, and the width of each second opening is 10 times λ (5 times λ for the WIFI 5 GHz), it is enough to shield the external noise.

It may be known that the width of each second opening 133 is between 1λ and 2λ.

Each heat dissipation portion 135 can be used for heat dissipation, although in this embodiment, twelve heat dissipation portions 135 are respectively disposed on the top surface of the cover body 131 corresponding to each second opening 133, it should be noted that the disposing position, the size, and the number of the heat dissipation portions 135 are not restricted to the embodiments. The heat dissipation portions 135 can be omitted in the design. The aperture ratio of each heat dissipation portion 135 may be calculated by using the Formula 1, and its value is between 1λ and 2λ.

When it intends to assemble the isolation cover 13 to the main body 11 of the circuit board 1, as shown in FIG. 4, the main body 11 and the isolation cover 13 are provided. The main body 11 has an insulating layer 115, a plurality of first openings 1151 disposed at intervals on the insulating layer 115, and a plurality of soldering portions 113 respectively exposed from each first opening 1151 disposed on a surface thereof. The isolation cover 13 comprises a cover body 131 and a plurality of second openings 133 equidistantly opened on the lateral side of the cover body 131.

Then, the isolation cover 13 is disposed on the surface of the main body 11 of the circuit board 1. In this embodiment, the surface of the main body 11 has the predetermined covering region 111, such that the isolation cover 13 is disposed after being aligned to predetermined covering region 111. The shape of the predetermined covering region 111 is not limited to particular shapes. Therefore it can be changed in accordance with the shape of the isolation cover 13.

Finally, the isolation cover 13 is soldered to the soldering portions 113 through the local spot soldering

process. In this process, the local spot soldering is performed on each soldering portion 113 through the SMT technique in order to integrate the isolation cover 13 fixedly onto the main body 11 of the circuit board 1.

As shown in FIGs. 5a and 5b, the isolation cover 13 of the circuit board 1' has the second openings 133 equidistantly disposed on the lateral side to prevent the RF noise interference, and the height and the width of each second opening 133 are optimally adjusted in accordance with the wave length of the communication product. Meanwhile, the second openings 133 and the heat dissipation portions 135 on the lateral side of the isolation cover 13 can be used for heat dissipation in order to unify the internal reflow-soldering temperature, and to increase the productivity. In addition, in the main body 11 of the circuit board 1, the soldering portions 113 are spaced by the insulating layer 115 without using the entire soldering. As a result, the time consuming on soldering process is reduced, heat dissipation is effectively dissipated, and the maintenance cost is decreased.

Further, when it is necessary to disassemble the isolation cover 13, only partial desoldering is required to be performed on the circuit board 1, such as the soldering points between the isolation cover 13 and the soldering portions 113. Thus, implementation of the local spot soldering technology of the present invention is to effectively reduce time consuming during the soldering process and to simply the manufacturing process, such as less time is required to partially desoldering the soldering points between the isolation cover and the soldering portions.

The invention being thus described, it will be obvious that the same may be varied in many ways. Such

variations are not to be regarded as a departure from the spirit and scope of the invention, and all such modifications as would be obvious to one skilled in the art are intended to be included within the scope of the following claims.

Conclusies

1. Printplaat zoals toegepast in een communicatieproduct, omvattende:

een hoofdgedeelte van de printplaat waarin op een oppervlak een vermogenstransistor is geplaatst, een isolatielaag, meerdere primaire openingen die steeds op enige afstand van elkaar rondom de vermogenstransistor in de isolatielaag zijn aangebracht en meerdere soldeerplaatsen die elk, respectievelijk, toegankelijk zijn via één van de primaire openingen; en

een isolatiedeksel, dat het hoofdgedeelte van de printplaat afdekt, waarbij het afsluitende gedeelte van het isolatiedeksel is gesoldeerd aan elk van de soldeergedeelten en waarbij er zich meerdere secundaire openingen, op onderling gelijke afstanden, bevinden langs de zijkanten van het afsluitende gedeelte,

waarbij de breedte van elke opening ligt tussen 1λ en 2λ, waarbij $\lambda=\nu/f$, en λ een golflengte is, ν een snelheid is (m/s), f een frequentie is (Hz) en een maximale waarde van f 26,5 GHz bedraagt.

2. Printplaat volgens conclusie 1, waarin elke isolerende laag een laag is met een soldeermasker.

3. Printplaat volgens conclusie 1 of 2, waarin elk soldeergedeelte overeenkomt met een hoek van het afsluitende gedeelte.

4. Printplaat volgens één der voorgaande conclusies, waarin elk soldeergedeelte als het ware een onderlegger vormt.

5. Printplaat volgens één der voorgaande conclusies, waarin elk soldeergedeelte is voorzien van een soldeermateriaal.

6. Printplaat volgens één der voorgaande conclusies, waarin elke secundaire opening een rechthoekige opening is.

7. Printplaat volgens één der voorgaande conclusies, die verder meerdere voorzieningen heeft voor warmteafvoer in de vorm van openingen die op onderling gelijke afstanden zijn aangebracht in het bovenvlak van het afsluitende gedeelte.

8. Printplaat volgens conclusie 7, waarin elke voorziening voor warmteafvoer een cirkelvormige opening is.

9. Printplaat volgens conclusie 7 of 8, waarin de onderlinge afstand tussen voorzieningen voor warmteafvoer ligt tussen 1λ en 2λ, $\lambda=v/f$, waarbij λ een golflengte is, waarin v een snelheid (m/s) is, f een frequentie (Hz) is en een maximale waarde van f 26,5 GHz bedraagt.

10. Fabricagemethode voor een printplaat van een communicatieproduct, omvattende:

het aanvoeren van een hoofdgedeelte van een printplaat waarbij het hoofdgedeelte is voorzien van een vermogenstransistor, van een isolerende laag, van meerdere primaire openingen die steeds op enige afstand van elkaar rondom de vermogenstransistor zijn aangebracht in de isolerende laag en van meerdere soldeergedeelten die elk via een primaire opening toegankelijk zijn;

het aanvoeren van een isolatiedeksel waarbij het isolatiedeksel een afsluitend gedeelte omvat en er zich meerdere secundaire openingen, op onderling gelijke afstanden, bevinden langs de zijkanten van het afsluitende gedeelte waarbij de breedte van elke opening ligt tussen 1λ en 2λ, waarbij $\lambda=v/f$, en λ een golflengte is, v een snelheid is (m/s), f een frequentie is (Hz) en een maximale waarde van f 26,5 GHz bedraagt;

het plaatsen van het isolatiedeksel op het hoofdgedeelte van de printplaat; en

het solderen van het isolatiedeksel aan elke soldeerplaats door middel van een punt-soldeermethode.

11. Fabricagemethode volgens conclusie 10, waarbij elke isolerende laag en elke soldeerplaats op het oppervlak van het hoofdgedeelte van de printplaat worden aangebracht door middel van een stencil-druktechniek.

12. Fabricagemethode volgens conclusie 10 of 11, waarbij er eerst alle soldeerplaatsen op het oppervlak van het hoofdgedeelte van de printplaat worden aangebracht, vervolgens de isolerende laag en er tenslotte in de isolerende laag primaire openingen worden gemaakt waardoor elke soldeerplaats toegankelijk wordt.

13. Fabricagemethode volgens één der conclusies 10-12, waarbij het puntsolderen wordt uitgevoerd door middel van een oppervlakte-montagetechniek.

14. Printplaat zoals gebruikt in een communicatie product, omvattende:

een hoofdgedeelte van een printplaat met daarop een vermogenstransistor en een vooraf bepaald af dekken gebied voor het afdekken van de vermogenstransistor;

een isolerende laag die op het hoofdgedeelte van de printplaat is aangebracht en is voorzien van meerdere openingen die zich, steeds op enige afstand van elkaar rondom het vooraf bepaalde af te dekken gebied bevinden; en

meerdere soldeerplaatsen die elk via één van deze openingen toegankelijk zijn.

15. Printplaat volgens conclusie 14, waarin elke isolerende laag een soldeermasker is.

16. Printplaat volgens conclusie 14 of 15, waarin elke soldeerplaats als het ware een onderlegger vormt.

17. Printplaat volgens één der conclusies 14-16, waarin elke soldeerplaats is voorzien van een soldeermateriaal.

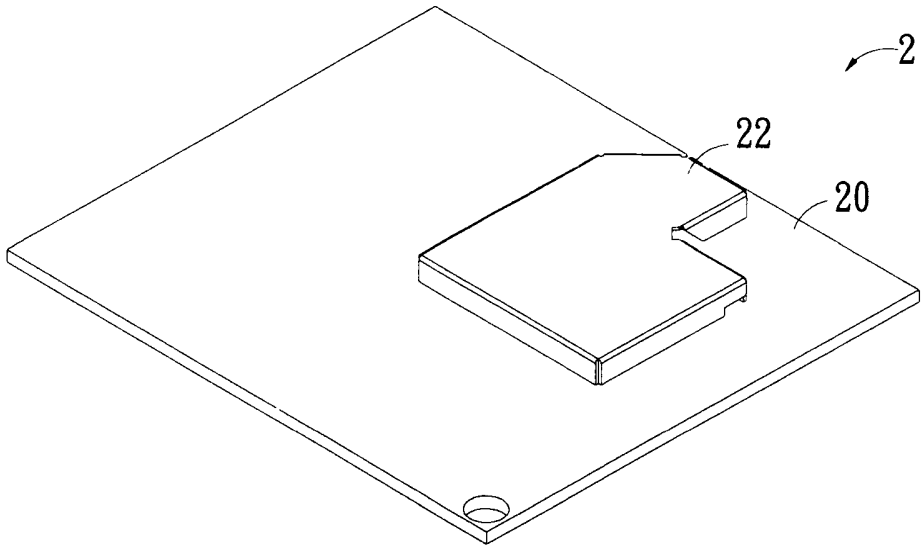

Fig. 1

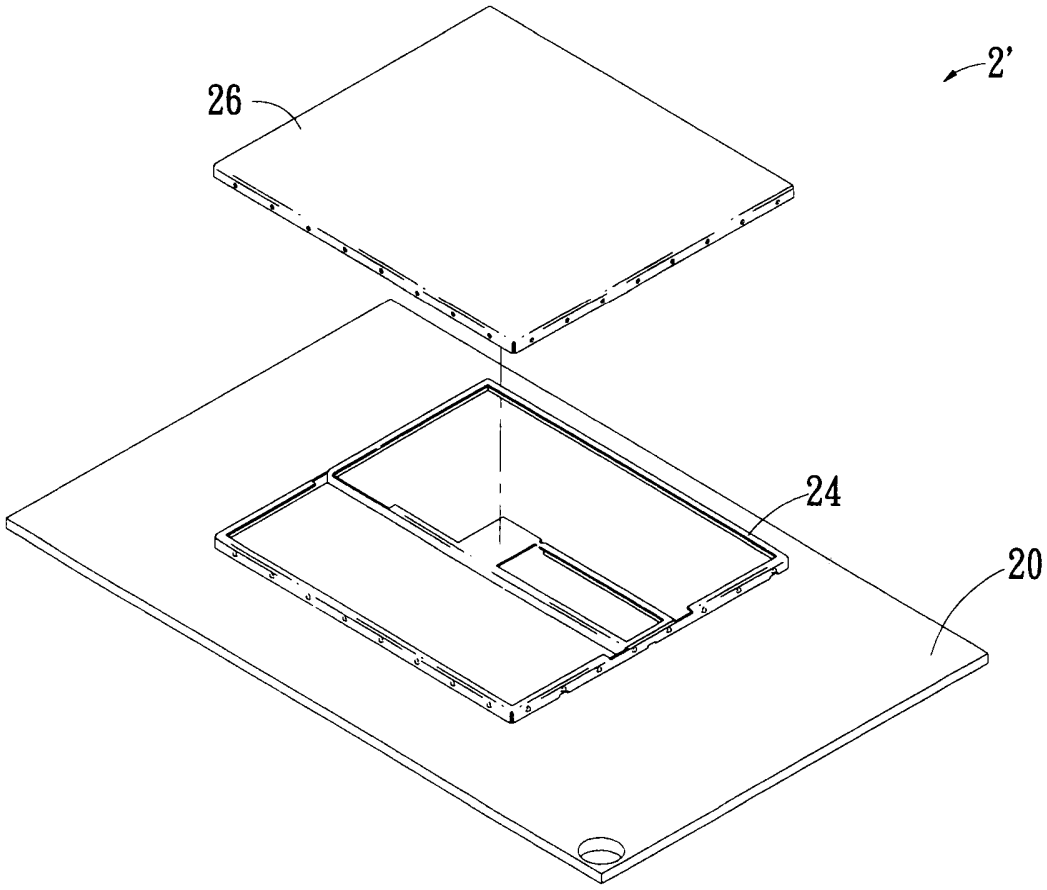

Fig. 2

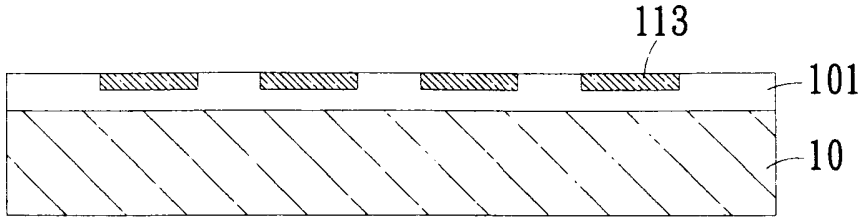

Fig. 3a

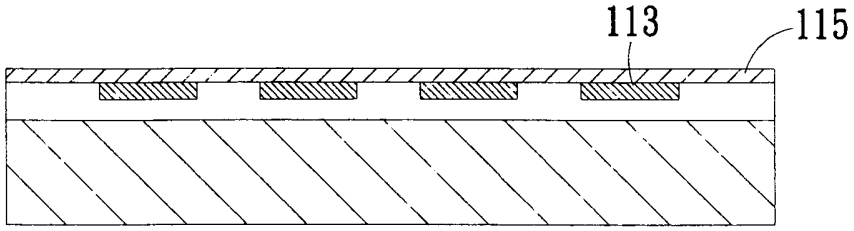

Fig. 3b

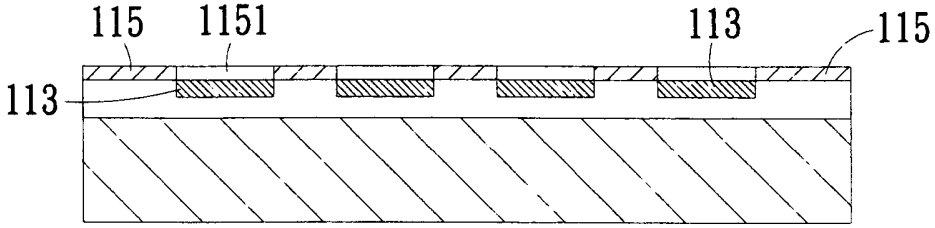

Fig. 3c

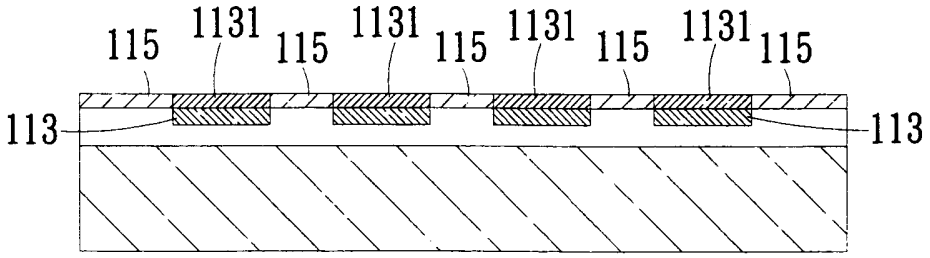

Fig. 3d

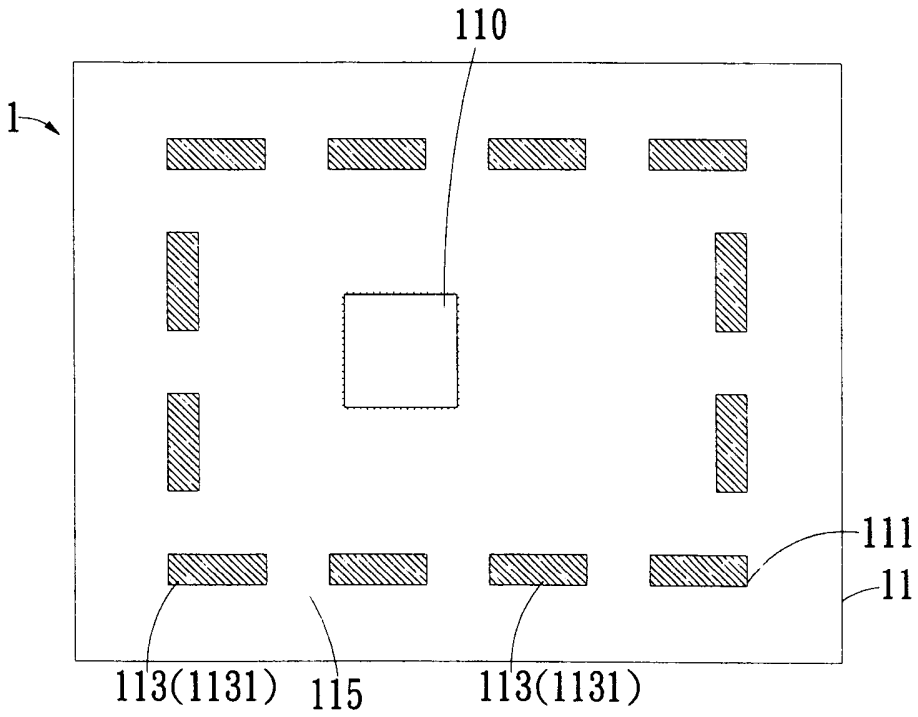

Fig. 3e

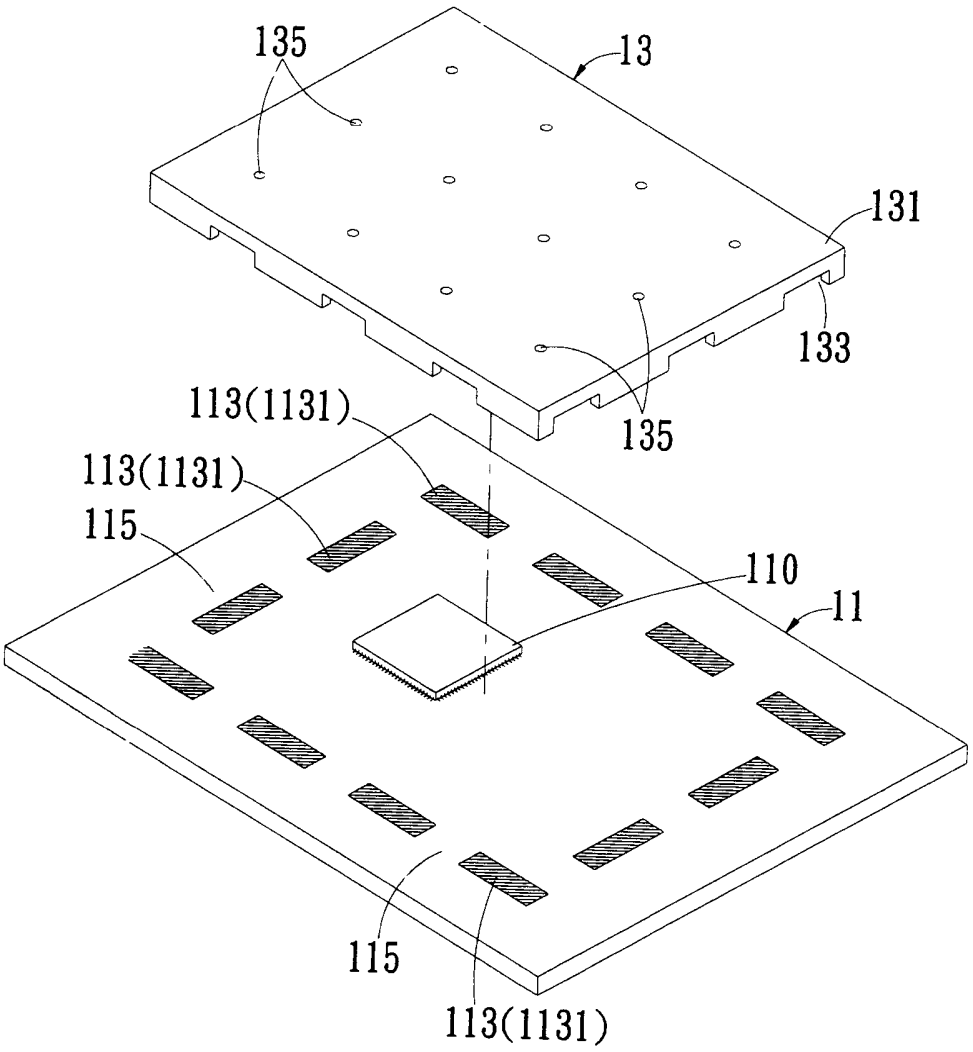

Fig. 4

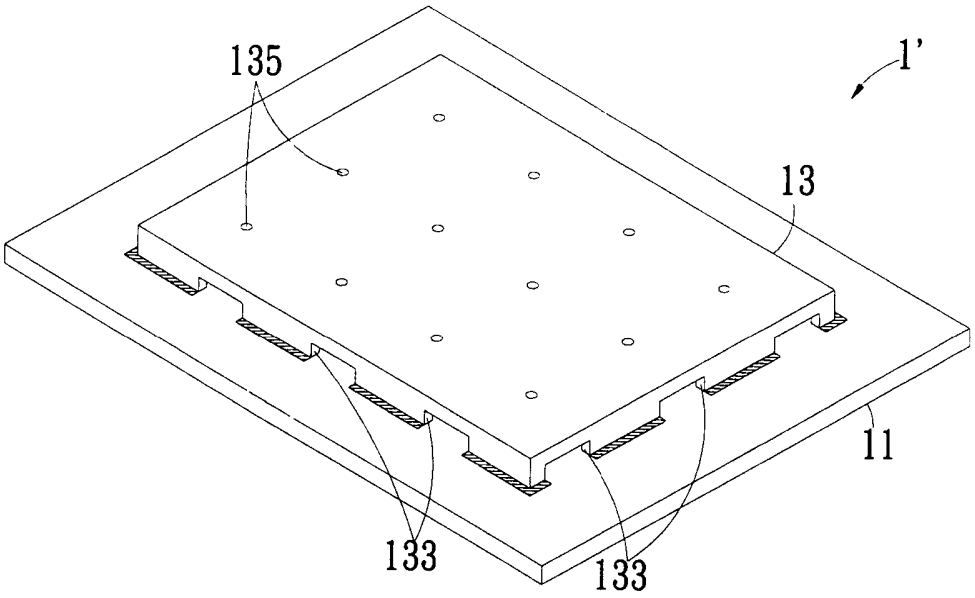
135
1'
13
11
133
133

Fig. 5a

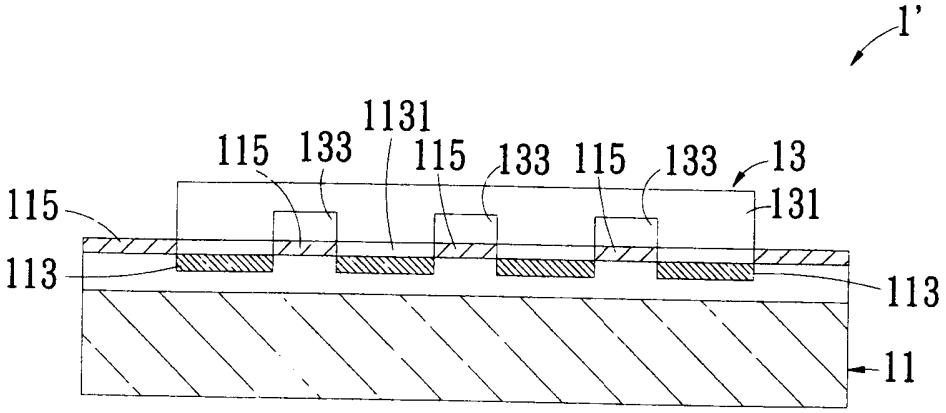
1'
1131
115
133
115
133
115
133
13
115
131
113
113
11

Fig. 5b

OCTROOICENTRUM NEDERLAND

OCTROOIAANVRAAG NR.:
NO 136581
NL 1036863

ONDERZOEKSRAPPORT

BETREFFENDE HET RESULTAAT VAN HET ONDERZOEK NAAR DE STAND VAN DE TECHNIEK

RELEVANTE LITERATUUR

Categorie[1]	Literatuur met, voor zover nodig, aanduiding van speciaal van belang zijnde tekstgedeelten of figuren.	Van belang voor conclusie(s) nr:	Classificatie (IPC)
X A	EP 1 445 999 A1 (SONY ERICSSON MOBILE COMM AB [SE]) 11 augustus 2004 (2004-08-11) * alineas [0001], [0028], [0029], [0034] - [0037]; figuren 8,9 * -----	1-14 15	INV. H05K9/00
A	EP 1 139 712 A2 (LUCENT TECHNOLOGIES INC [US]) 4 oktober 2001 (2001-10-04) * alineas [0014], [0015], [0022]; figuren 1E,4D * -----	1,11,15	
A	US 2002/096344 A1 (OKADA MASAAKI [JP] ET AL) 25 juli 2002 (2002-07-25) * alineas [0035], [0036], [0039] - [0045]; figuren 1-4 * -----	1,11,15	

Onderzochte gebieden van de techniek

H05K

Indien gewijzigde conclusies zijn ingediend, heeft dit rapport betrekking op de conclusies ingediend op:

Plaats van onderzoek:	Datum waarop het onderzoek werd voltooid:	Bevoegd ambtenaar:
's-Gravenhage	13 oktober 2011	Schneider, Florian

[1] CATEGORIE VAN DE VERMELDE LITERATUUR

X: de conclusie wordt als niet nieuw of niet inventief beschouwd ten opzichte van deze literatuur
Y: de conclusie wordt als niet inventief beschouwd ten opzichte van de combinatie van deze literatuur met andere geciteerde literatuur van dezelfde categorie, waarbij de combinatie voor de vakman voor de hand liggend wordt geacht
A: niet tot de categorie X of Y behorende literatuur die de stand van de techniek beschrijft
O: niet-schriftelijke stand van de techniek
P: tussen de voorrangsdatum en de indieningsdatum gepubliceerde literatuur
T: na de indieningsdatum of de voorrangsdatum gepubliceerde literatuur die niet bezwarend is voor de octrooiaanvrage, maar wordt vermeld ter verheldering van de theorie of het principe dat ten grondslag ligt aan de uitvinding
E: eerdere octrooi(aanvrage), gepubliceerd op of na de indieningsdatum, waarin dezelfde uitvinding wordt beschreven
D: in de octrooiaanvrage vermeld
L: om andere redenen vermelde literatuur
&: lid van dezelfde octrooifamilie of overeenkomstige octrooipublicatie

EOB FORM 02.83 (P0414B)

AANHANGSEL BEHORENDE BIJ HET RAPPORT BETREFFENDE HET ONDERZOEK NAAR DE STAND VAN DE TECHNIEK, UITGEVOERD IN DE OCTROOIAANVRAGE NR.

NO 136581
NL 1036863

Het aanhangsel bevat een opgave van elders gepubliceerde octrooiaanvragen of octrooien (zogenaamde leden van dezelfde octrooifamilie), die overeenkomen met octrooischriften genoemd in het rapport.
De opgave is samengesteld aan de hand van gegevens uit het computerbestand van het Europees Octrooibureau per
De juistheid en volledigheid van deze opgave wordt noch door het Europees Octrooibureau, noch door het Bureau voor de Industriële eigendom gegarandeerd; de gegevens worden verstrekt voor informatiedoeleinden.

13-10-2011

In het rapport genoemd octrooigeschrift	Datum van publicatie	Overeenkomend(e) geschrift(en)	Datum van publicatie
EP 1445999 A1	11-08-2004	GEEN	
EP 1139712 A2	04-10-2001	JP 2001284871 A	12-10-2001
US 2002096344 A1	25-07-2002	FR 2819979 A1	26-07-2002
		JP 3792518 B2	05-07-2006
		JP 2002217580 A	02-08-2002

Algemene informatie over dit aanhangsel is gepubliceerd in de 'Official Journal' van het Europees Octrooibureau nr 12/82 blz 448 ev

OCTROOICENTRUM NEDERLAND

SCHRIFTELIJKE OPINIE

DOSSIER NUMMER	INDIENINGSDATUM	VOORRANGSDATUM	AANVRAAGNUMMER
NO136581	16.04.2009	13.10.2008	NL1036863

CLASSIFICATIE
INV. H05K9/00

AANVRAGER
Askey Computer Corp. te Taipei, Taiwan (TW)

Deze schriftelijke opinie bevat een toelichting op de volgende onderdelen:

- ☒ Onderdeel I Basis van de schriftelijke opinie
- ☐ Onderdeel II Voorrang
- ☐ Onderdeel III Vaststelling nieuwheid, inventiviteit en industriële toepasbaarheid niet mogelijk
- ☐ Onderdeel IV De aanvraag heeft betrekking op meer dan één uitvinding
- ☒ Onderdeel V Gemotiveerde verklaring ten aanzien van nieuwheid, inventiviteit en industriële toepasbaarheid
- ☐ Onderdeel VI Andere geciteerde documenten
- ☐ Onderdeel VII Overige gebreken
- ☐ Onderdeel VIII Overige opmerkingen

DE BEVOEGDE AMBTENAAR
Schneider, Florian

Aanvraag nr.:

SCHRIFTELIJKE OPINIE

NL1036863

Onderdeel I Basis van de Schriftelijke Opinie

1. Deze schriftelijke opinie is opgesteld op basis van de meest recente conclusies ingediend voor aanvang van het onderzoek.

2. Met betrekking tot **nucleotide en/of aminozuur sequenties** die genoemd worden in de aanvraag en relevant zijn voor de uitvinding zoals beschreven in de conclusies, is dit onderzoek gedaan op basis van:

   a. type materiaal:

   ☐ sequentie opsomming

   ☐ tabel met betrekking tot de sequentie lijst

   b. vorm van het materiaal:

   ☐ op papier

   ☐ in elektronische vorm

   c. moment van indiening/aanlevering:

   ☐ opgenomen in de aanvraag zoals ingediend

   ☐ samen met de aanvraag elektronisch ingediend

   ☐ later aangeleverd voor het onderzoek

3. ☐ In geval er meer dan één versie of kopie van een sequentie opsomming of tabel met betrekking op een sequentie is ingediend of aangeleverd, zijn de benodigde verklaringen ingediend dat de informatie in de latere of additionele kopieën identiek is aan de aanvraag zoals ingediend of niet meer informatie bevatten dan de aanvraag zoals oorspronkelijk werd ingediend.

4. Overige opmerkingen:

Aanvraag nr.:

SCHRIFTELIJKE OPINIE

NL1036863

Onderdeel V Gemotiveerde verklaring ten aanzien van nieuwheid, inventiviteit en industriële toepasbaarheid

1. Verklaring

Nieuwheid	Ja:	Conclusies 2-10, 12-18
	Nee:	Conclusies 1, 11
Inventiviteit	Ja:	Conclusies 15-18
	Nee:	Conclusies 1-14
Industriële toepasbaarheid	Ja:	Conclusies 1-18
	Nee:	Conclusies

2. Citaties en toelichting:

Zie aparte bladzijde

Re Item V

1 Reference is made to the following document.

D1 EP 1 445 999 A1 (SONY ERICSSON MOBILE COMM AB [SE]) 11 augustus 2004 (2004-08-11)

2 The present application does not meet the criteria of patentability, because the subject-matter of claim 1 is not new.

2.1 The document D1 is regarded as being the closest prior art to the subject-matter of claim 1, and discloses (see paragraphs 34-36; figures 8,9) a circuit board (22) for a communication apparatus comprising a main body on which an electronic component is mounted, a plurality of first openings (26) provided at regular intervals in the circuit board which is made of an insulating material and surrounding the electronic component (see figure 8; column 7, lines 47-51), a plurality of soldering portions exposed respectively from the first openings (26) (see column 7, lines 53-56), and an isolation cover (21) soldered to each soldering portion (see column 7, line 56 - column 8, line 2), said isolation cover (21) comprising a plurality of second openings (=openings defined between the protrusions 25a) equidistantly opened on a lateral side of the isolation cover (21) (see figure 8).

Hence, the subject-matter of claim 1 is not new.

3 The arguments given for claim 1 apply similarly to independent method claim 11, which likewise lacks novelty.

4 The subject- matter of dependent claims 2-10,12-14 relates to measures routinely used in the art of mounting a shielding can on a circuit board not involving an inventive step.

5 Applying a perforated insulating layer (115) (see figure 5B of the application) on a circuit board for creating a plurality of first openings on the surface of the circuit board, the soldering portions provided on the circuit board being exposed through said first openings is regarded as a non obvious alternative to the solution disclosed in D1. The problem to be solved could be to simplify the manufacturing process.

This embodiment is defined in claim 15, which is therefore regarded as new and inventive.