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[54] DIGITAL TO ANALOG CONVERTER INCLUDING IMPROVED REFERENCE CURRENT SOURCE

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[58] **Field of Search**.....307/235, 296, 297; 330/30 D, 330/38 M

[56] **References Cited**

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[57] **ABSTRACT**

This disclosure relates to a digital to analog converter including a simplified reference current source whose current output may be determined by a reference resistor and a positive or negative reference voltage source.

11 Claims, 2 Drawing Figures

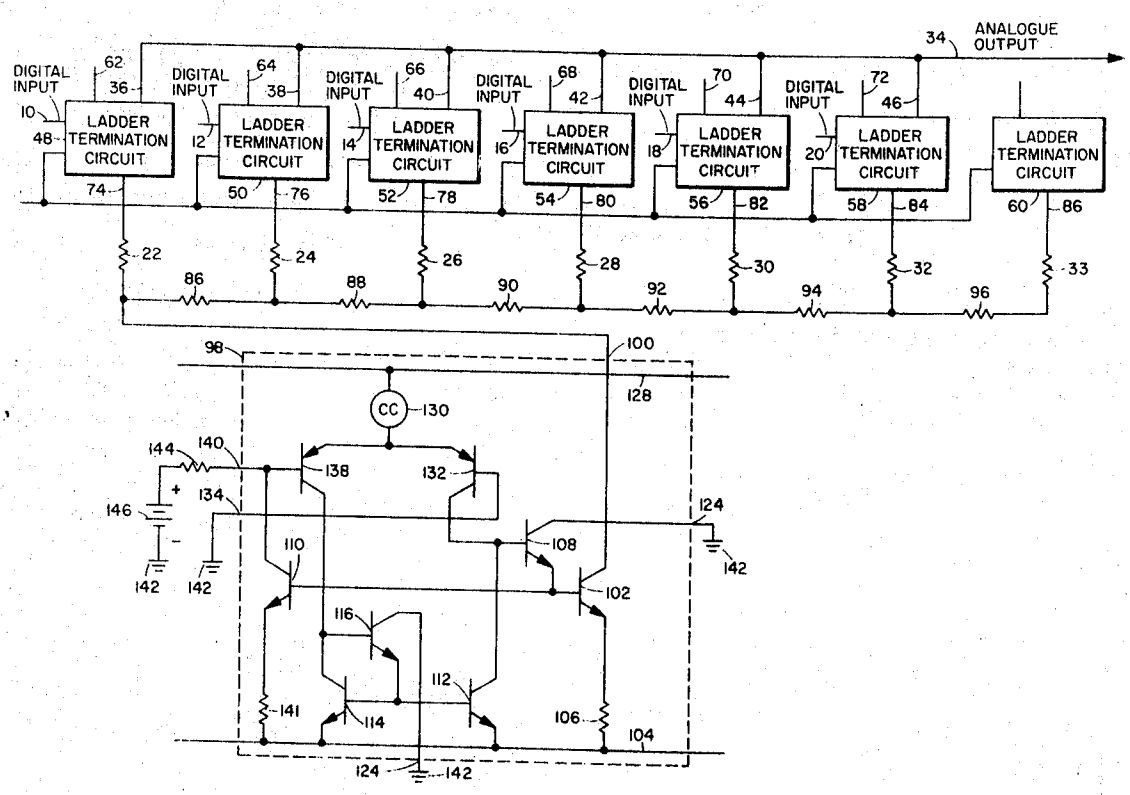

Fig. 1

Fig. 2

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DIGITAL TO ANALOG CONVERTER INCLUDING IMPROVED REFERENCE CURRENT SOURCE

BACKGROUND

It is known how to convert a digital value, indicated by a group of digits to an analog amount of current. This can be done by using an R–2R resistance ladder. The current flowing from each resistance comprising a rung of the ladder to the analog output is binarily related to the current flow from the other rungs of the ladder, and one or more of the rungs supplies current (or no current) to the analog output as determined by the several digits. For proper operation of such a ladder, the current supplied by the supply means which provides current to the ladder and all its rungs, must be very constant and this constancy should be independent of the voltage of the current supply.

It is an object of this invention to provide an improved digital to analog converter.

It is another object of this invention to provide a digital to analog converter including an improved constant current source.

It is still another object of this invention to provide a constant current source whose constant current is determined by ordinarily available standard elements.

SUMMARY

In accordance with this invention, the constant current source for supplying the resistance ladder is adapted to be put on a chip. The chip has a positive and a negative control terminal. The positive control terminal may be connected to ground by way of a control resistor and a standard voltage source which is positive with respect to ground in which case the negative controlled terminal is grounded, or, the positive and the negative terminals may be connected to ground by way of a control resistor and a standard source which is negative with respect to ground, respectively. Means are included in the constant current source to cause the constant current to be determined by the value of the control resistor and the standard voltage. This means includes a pair of transistors which are connected as a differential amplifier, a dual active load featuring double to single ended conversion for transferring the amplified output from an electrode of one of the transistors to the other, a feedback from said electrode of the other transistor to the control electrode of the one transistor of the pair and means to keep the control electrodes of the two transistors equal.

DESCRIPTION

The invention will be better understood upon reading the following description in connection with the accompanying drawing in which

FIG. 1 illustrates a digital to analog conversion circuit including a constant current source in accordance with this invention, and

FIG. 2 is a fragmentary illustration of another connection of the constant current source of this invention, also in accordance with this invention.

Turning first to FIG. 1, the digits of a binary number are applied to the input terminals 10, 12, 14, 16, 18 and 20, respectively of ladder termination circuits 48, 50, 52, 54, 56 and 58, the most significant digit being applied to the terminal 10 and the least significant to the terminal 20. The current provided by the several rungs 22, 24, 26, 28, 30 and 32 of the ladder are supplied to the analog output terminal 34 by way of the respective output connections 36, 38, 40, 42, 44 and 46 of the ladder termination circuits 48, 50, 52, 54, 56 and 58, or is connected to a power supply (not shown) by way of respective terminals 62, 64, 66, 68, 70 or 72, depending on whether the digit applied to the terminals 10 to 20 are ones or zeros.

While the ladder itself is well known, for completeness, it will be described here. One terminal of each of the resistors 22, 24, 26, 28, 30, 32 and 33 is connected to a respective ladder terminal 74, 76, 78, 80, 82, 84 and 86 of a ladder termination circuit 48 to 60 respectively.

The other terminals of the resistors 22 and 24 are connected together by way of a resistor 86. The other terminals of the resistors 24 and 26 are connected by way of a resistor 88. The other terminals of the resistors 26 and 28 are connected by way of a resistor 90. The other terminals of the resistors 28 and 30 are connected by way of resistor 92. The other terminals of the resistors 30 and 32 are connected by way of a resistor 94 and the other terminals of the resistors 32 and 33 are connected by way of a resistor 96. Since the resistors 22, 24, 26, 28, 30 and 32 are each equal to 2R and since the resistors 86, 88, 90, 92, 94, 96 and 33 are equal to R, the current flow from or to the constant current source 98 at the terminals 74, 76, 78, 80, 82, 84 and 86 respectively 32I, 16I, 8I, 4I, 2I, I and I, the total current flow of the constant current source 98 being 64I. It will be noted that the ladder termination circuit 60 differs from the ladder termination circuits 48 to 58 in that there is no digital input to the circuit 60 and in that the output of the circuit 60 is not connected to the analog output terminal 34, whereby, the maximum current flow into the analog output 34 is 63I when the digital number is 000000, and is zero when the digital number is 111111, and is an intermediate value when the digital number has an intermediate value, using positive type logic. The output terminal 100 of the constant current source 98 is connected to the junction of the resistors 22 and 86. Since the accuracy of the digital to analog conversion depends on the constancy of the current of the constant current source 98, the constant current source 98 must be of high quality. The analog to digital converter may be put on a chip in which case the absolute values of the resistors 22 to 33 and 86 to 96 is hard to control, however their ratios may be easily made the required ones as noted above. Therefore, a constant voltage source cannot be used instead of the constant current source 98 since using a constant voltage source the amount of current at the analog output terminal 34 will depend not only on the digital number applied to the converter but also on the absolute values (as distinct from the relative values) of the ladder resistors 22 to 33 and 86 to 96. Using a constant current source, the analog output at 34 is not dependent on the absolute values of the resistors 22 to 33 and 86 to 96 but on their relative values. Also, it is advantageous, for known reasons, to put the constant current source 98 on a chip, the boundaries of the chip being indicated by the reference character 98 which is used in a dual capacity also to indicate the constant current source. However, if desired, the complete

digital to analog converter may be put on the same chip.

The constant current source **98** comprises an NPN transistor **102** whose collector is connected to the terminal **100** of the chip **98**. The emitter of the transistor **102** is connected to a negative potential bus **104** by way of a resistor **106**. The base of the transistor **102** is connected to the emitter of an NPN transistor **108** whose collector is connected to a ground terminal **124** of the chip **98**. The ground terminal **124** is connected to a point of reference potential such as the ground **142**. The base of the transistor **108** is connected to the collector of a PNP transistor **132** and to the collector of an NPN transistor **112**. The emitter of the PNP transistor **132** is directly connected to the emitter of a PNP transistor **138** and by way of a constant current source **130** to the positive bus **128**. The collector of the transistor **138** is connected to the collector of an NPN transistor **114** whose emitter is connected directly to the emitter of the transistor **112** and to the negative bus **104**. The bases of the transistors **112** and **114** are connected together and to the emitter of an NPN transistor **116**. The collector of the transistor **116** is connected to a ground terminal **124** which is connected to ground **142**. The base of the transistor **116** is connected to the collector of the transistor **114**. The bases of the transistors **132** and **138** are connected respectively to the control terminals **134** and **140**. The base of an NPN **110** is connected to the base of the transistor **102**. The collector of the transistor **110** is connected to the base of the transistor **138** and the emitter of the transistor **110** is connected to the bus **104** by way of a resistor **141**.

As shown in FIG. **1**, each ground terminal **124** may be connected to a reference potential such as ground **142** and the control terminal **134** is also connected to ground **142**. The control terminal **140** is connected by way of a standard resistor **144** and the positive to negative terminal of a standard voltage source **146** to ground **142**. As shown in FIG. **2**, in which the details of the chip **98** are not shown but the terminals thereof are shown and are given the same reference characters as the corresponding parts of FIG. **1**, the control terminal **140** may be connected to ground by way of the standard resistor **144** but the voltage source **146** is omitted from FIG. **2** and a standard voltage source **148** which is negative with respect to ground is connected between the control terminal **134** and ground **142**. That is, the circuit of FIG. **1** is versatile in that it can be used as shown in FIG. **1** with the standard source **146** which is positive with respect to ground or as shown in FIG. **2** with the standard source **148** which is negative with respect to ground, the standard resistor **144** being used with either source **146** or **148**.

Although the voltage applied between the positive bus **128** and the negative bus **104** may vary, the constant current source **98** will draw constant current from the terminal **100** under control of the standard resistor **144** and one or the other of the standard voltage sources **146** and **148**. The operation of the constant current source **98** is as follows:

The operation of the constant current means of the chip **98** is explained first with respect to FIG. **1**. The constant current source **130** supplies current for the two PNP transistors **132** and **138**, which are nearly identical as is possible and which act as a differential amplifier. Also the transistors **112** and **114** are as nearly identical as possible. Therefore the transistors **132** and **138** will divide the current from the source **130** in half. However, the transistors **112** and **114** and **116** will act as a double to single ended converter. That is, the difference in voltages across the control terminals **134** and **140** appears as a current difference between the collectors of these transistors. Transistors **116**, **114**, and **112** force all of the difference current thus produced to appear at the collector of transistor **132**. This difference current is obtained from or applied to the base of transistor **108**, which acts as a means to reduce the current drawn from the collectors of transistors **132** and **112**, and the emitter of transistor **108** drives the transistors **110** and **102**.

The operation of the circuit as shown in FIG. **1** is as follows. A negative feedback path exists from the base of transistor **138** to the collector of transistor **132**, down through the transistor **108** to the base of the transistor **110** and finally through the collector of transistor **110**. This negative feedback works in such a way to drive the base of the transistor **138** to be at the same voltage as applied to the base of transistor **132**. The current source **130** is small compared to the current through the standard resistor **144**, and the beta of transistor **138** and **132** are large. Thus, the current entering the base of transistor **138** is very small. Therefore, most of the current entering the terminal **140** will go down through transistor **110** and emitter degeneration resistor **141**. Since transistors **110** and **102** as well as resistors **141** and **106** are made as nearly equal as possible, the current through transistor **110** will be duplicated by transistor **102**, and this second current will then go on to drive the ladder.

It will be noted that the control terminal **134** is grounded and that the control terminal **140** is grounded by way of the standard resistor **144** and the standard voltage source **146**. The negative feedback, as described above, will cause a current to flow in the resistor **141** and therefore in the resistor **144** that is such that the base of the transistor **138** is at the potential of the base of the transistor **132**, which is connected to the control terminal **134** which is grounded. This current is of a constant value, and does not depend, between reasonable operating voltage differences, on the voltages applied to the buses **128** and **104**, but only on the resistor **144** and on the voltage source **146**. Since, as described earlier, the current through transistor **110** is duplicated by transistor **102** and this second current then drives the ladder, this said current therefore is only dependent on the resistor **144** and on the voltage source **146**.

In FIG. **2**, the terminal **134** is at the voltage of the source **148** with respect to ground, whereby the current flowing in the resistor **144** is such as to make the terminal **140** at the same voltage as the terminal **134**. Again, this current which is constant since the voltage source **148** and the resistor **144** are standard, flows through transistor **110** and resistor **141** and is then duplicated by transistor or **102** and resistor **106** which then drives the ladder (these elements not shown in FIG. **2**), whereby the chip **98** operates the same whether the resistor **144** and the sources **146** or **148** are connected as shown in FIG. **1** or as shown in FIG. **2**.

While PNP and NPN transistors have been used, one skilled in the art will know how to use either type of transistor where the other is used as above described.

What is claimed is:

1. A constant current source, the current flow of which is independent over a wide range of supply voltage to be connected to supply terminals thereof and in which the current flow is determined by a connection to control terminals thereof including in combination:

a differential amplifier including first and second transistors each having first and second main electrodes and a control electrode,

control terminals respectively connected to said control electrodes whereby the difference in voltages appearing at the control electrodes appears as a current difference between the first main electrodes of said first and second transistors,

means for transferring the current difference appearing between said first main electrodes of said first and second transistors to the first main electrode of said first transistor,

a third transistor having a pair of main electrodes and a control electrode, one of said main electrodes being connected to the control electrode of said second transistor and having its other main electrode connected by way of a resistor to a supply terminal and

means for coupling said first main electrode of said first transistor with the control electrode of said third transistor.

2. The combination of claim 1 in which said current difference transferring means comprises a fourth, fifth and sixth transistor each having first and second main electrodes and a control electrode, the first main electrodes of said fourth and fifth transistors being connected in series with the first main electrodes respectively of said second and first transistors and the second main electrodes of said fourth and fifth transistors being connected with a supply terminal, the control electrodes of said fourth and fifth transistors being connected together and to the second main electrode of said sixth transistor, the control electrode of said sixth transistor being connected to a junction with the first main electrodes of said second and fourth transistors and the first main electrode of said sixth transistor being connected to a supply reference point.

3. The combination of claim 1 further including a fourth transistor having a pair of main electrodes and a control electrode, said control electrodes of said third and fourth transistors being connected together, one of the main electrodes of said fourth transistor being connected through a resistor to a supply terminal and the other of the main electrodes of said fourth transistor being connected to a load terminal.

4. The combination of claim 2 further including a seventh transistor having a pair of main electrodes and a control electrode, said control electrodes of said third and seventh transistors being connected together, one of the main electrodes of said seventh transistor being connected through a resistor to a supply terminal and the other of the main electrodes of said seventh transistor being connected to a load terminal.

5. The combination of claim 1 wherein said differential amplifier includes a constant current source having a terminal connected to the second main electrodes of said first and second transistors and in which said current difference transferring means comprises a fourth, fifth and sixth transistor each having first and second main electrodes and a control electrode, the first main electrodes of said fourth and fifth transistors being connected in series with the first main electrodes respectively of said second and first transistors and the second main electrodes of said fourth and fifth transistors being connected with a supply terminal, the control electrodes of said fourth and fifth transistors being connected together and to the second main electrode of said sixth transistor, the control electrode of said sixth transistor being connected to a junction with the first main electrodes of said second and fourth transistors and the first main electrode of said sixth transistor being connected to a supply reference point.

6. The combination of claim 5 in which said first and second transistors are of the PNP type and said second main electrodes thereof are the emitters.

7. The combination of claim 6 in which said fourth and fifth transistors are of the NPN type and the second main electrodes of the fourth and fifth transistors are emitters.

8. A constant current source including in combination

a positive and a negative terminal,

a constant current source,

a first and a second PNP transistor,

a first, a second and a third NPN transistor,

a connection by way of said constant current source from said positive terminal to the emitters of said PNP transistors,

a respective connection from the collectors of the first and second PNP transistors to the collectors of the first and second NPN transistors,

a connection from each of the emitters of the first and second NPN transistors to said negative terminal,

a connection between the bases of the first and second NPN transistors to the emitter of the third NPN transistor,

a connection from the base of the third NPN transistor to the collector of the first NPN transistor,

means for holding the collector of the third NPN transistor at constant voltage,

feedback means coupled between the collector of one of said PNP transistors and the base of the other of said PNP transistors, and

control terminals connected to the bases of said PNP transistors.

9. The combination of claim 8 further including a standard voltage source and a standard resistor connected between said bases of said PNP transistors.

10. The combination of claim 8 further including a fourth NPN transistor, the collector of said fourth transistor being connected to the base of said second PNP transistor and the emitter of said fourth transistor being connected to said negative terminal by way of a resistor and said feedback means is coupled from the collector of said first PNP transistor to the base of said fourth NPN transistor.

11. The combination of claim 10 further including a load terminal and a fifth NPN transistor with the bases of said fourth and fifth transistors being connected

together and the emitter of said fifth transistor connected to said negative terminal by way of a resistor and said load terminal is connected to the collector of said fifth transistor and wherein said feedback means is a sixth NPN transistor, the base of which is connected to the collector of said first PNP transistor, the emitter of which is connected to the bases of said fourth and fifth transistors and the collector of which is coupled with a constant voltage.

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