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(71) Applicant: **POLYERA CORPORATION** [US/US]; 8045 Lamon Avenue, Suite 140, Skokie, IL 60077 (US).

(72) Inventors: **HSIEH, Hsin-Hung**; Rm. 9-11, 4F, No. 38, Taiyuan St., Zhubei City, 302 (TW). **HSIAO, Chung-Chin**; Rm 9-11, 4F, No. 38, Taiyuan St., Zhubei City, 302 (TW). **FACCHETTI, Antonio**; 5412 N. Glenwood Ave., Chicago, IL 60640 (US).

(74) Agent: **CHAN, Karen, K.**; Polyera Corporation, 8045 Lamon Avenue, Suite 140, Skokie, IL 60077 (US).

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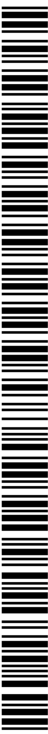

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(54) **Title**: SELF-ALIGNED METAL OXIDE TRANSISTORS AND METHODS OF FABRICATING SAME

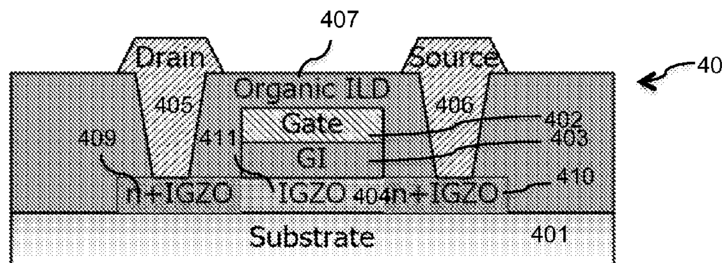


FIG. 7

(57) **Abstract**: A self-aligned metal oxide transistor can be fabricated by contacting the source and drain regions of the metal oxide active layer with a reductive polymer, thereby doping the source and drain regions with valence electrons from the reductive polymer and reducing the electrical resistance in the source and drain regions. The reductive polymer can be an electrically insulating polymer that has, in its backbone and/or its pendant group(s), one or more nitrogen atoms with a lone pair of electrons. The reductive polymer can be deposited over the oxide semiconductor layer as the organic interlayer dielectric.

SELF-ALIGNED METAL OXIDE TRANSISTORS AND METHODS OF FABRICATING SAME

Cross-Reference to Related applications

[0001] This is a Patent Cooperation Treaty (PCT) application that claims priority to and the benefit of the filing date of U.S. Provisional Patent Application Serial No. 62/009,144, filed on June 6, 2014, the entire disclosure of which is incorporated by reference herein for all purposes.

Background

[0002] Flat-panel displays such as liquid crystal displays, organic light-emitting displays, and electrophoretic displays have been adopted as the current mainstream display technologies. These displays are much lighter and thinner than traditional cathode ray tube displays, allowing their applications beyond television sets and video displays, such as in laptops, mobile phones, digital cameras, camcorders, and other smaller portable devices.

[0003] A flat-panel display having a thin-film transistor backplane is referred to as an active matrix flat-panel display. The thin-film transistors in the backplane are used to switch or drive pixels in the display front plane, so that each pixel can be turned on and off individually. Thus, the thin-film transistors are one of the key factors of the display performance.

[0004] One of the development trends for flat-panel displays is to achieve higher resolution, which means smaller pixel size, and in turn, smaller thin-film transistors. Different approaches have been proposed for shrinking the size of thin-film transistors.

[0005] In recent years, a new thin-film transistor technology based upon semiconducting metal oxides has drawn great attention. These transistors are fabricated with a semiconducting metal oxide (such as ZnO, In_2O_3, IGZO, etc.) as the channel layer. Metal oxide thin-film transistors (or oxide TFTs) can confer many advantages including high mobility, uniformity, and operational stability; as such, they have become a strong candidate to compete with traditional thin-film transistor technology based upon amorphous silicon or polycrystalline silicon.

[0006] The most commonly used structure of oxide TFTs is a bottom-gate structure which can have either an etch stop configuration or a back-channel-etch (BCE) configuration. Both configurations have their respective benefits and drawbacks. For example, the etch stop

configuration typically is more stable than the back-channel-etch type because the back channel is protected by the etch stop layer, while the back channel of a BCE oxide TFT often is damaged during the etching process of the source and drain electrodes. However, the device size of etch stop oxide TFTs is larger than BCE oxide TFTs because of the additional etch stop layer.

[0007] With respect to device size, a critical feature is the channel length of the TFT. Referring to Fig. 1, which illustrates an oxide TFT 10 having a BCE type structure, the channel length is defined by the spacing of the source and drain electrodes 105, 106. Accordingly, the minimum channel length is determined by the minimum spacing between the source and drain electrodes that can be achieved.

[0008] By comparison, an oxide TFT 20 having an etch stop type structure is illustrated in Fig. 2. As shown in Fig. 2, there is an etch stop layer (or etching stopper) 208 between the oxide semiconductor 204 and the source/drain electrodes 205, 206. In this architecture, the channel length of the TFT is actually defined by the width of the etch stop layer. Accordingly, the minimum channel length of an etch stop type TFT is determined by not only the minimum spacing of the source and drain electrodes that can be achieved, but also by the length of the channel that overlaps with the source and drain electrodes on each side. Therefore, the minimum channel length of the etch stop type structure is inherently larger than that of the back channel etch type structure, which means BCE transistors are more suitable than etch stop type TFTs to realize high-resolution displays because of smaller device size. However, as mentioned above, when fabricating BCE structures, the back channel often is damaged during source and drain etching, which leads to poor bias stress stability and other device performance issues.

[0009] More recently, several studies in the literature have proposed a new self-aligned top gate (SA-TG) structure for oxide TFTs. As shown in Figs. 3-6, in a self-aligned oxide TFT 30, a metal oxide semiconductor (e.g. IGZO) island 304 is formed on the substrate 301, followed by the gate dielectric (or gate insulator, GI) 303 and the gate electrode 302 on top of the metal oxide semiconductor layer. The gate electrode and gate dielectric are etched with the same pattern to expose side regions 309, 310 of the metal oxide semiconductor layer. Then, these exposed side regions are treated to give them lower electrical resistance compared to the untreated portion beneath the gate electrode, i.e., the channel region 311. An inter-layer dielectric (ILD) material 307 is deposited over the exposed side portions 309, 310 of the metal oxide island 304, the gate dielectric 303, and the gate electrode 302. The ILD

307 is then patterned to open via holes for the deposition of the source and drain electrodes 305, 306, which are in contact with the source and drain regions 309, 310 of the metal oxide semiconductor layer 304. The minimum channel length of this type of structure is defined by the minimum width one can achieve with the gate electrode (in other words, the channel length is self-aligned with the width of the gate), which is similar to the minimum channel length one can achieve with the BCE type structure because no additional etch stop layer is required. Meanwhile, because the source and drain electrodes are not etched on top of the channel region, self-aligned TFTs also tend to give more stable device performance. Therefore, self-aligned TFTs have the potential to provide the advantages of both BCE type TFTs and etch stop type TFTs and can be a good option to enable future high resolution flat-panel display applications.

[0010] Nonetheless, one of the difficulties to realize SA-TG oxide TFTs is how to lower the electrical resistance of the source and drain regions of the metal oxide layer. Three different methods have been reported in the literature. The first method uses plasma treatment, the process flow of which is shown in Fig. 4. Specifically, after the metal oxide island (e.g., IGZO) 304 has been formed, and the gate dielectric 303 and the gate electrode 302 sequentially deposited then patterned together, one can apply a plasma treatment 312 such as Ar plasma or NH_3 plasma to the exposed metal oxide regions 309, 310 as shown in Fig. 4(c). The electrical resistance of the exposed metal oxide regions 309, 310 is lowered after the treatment, because the plasma treatment creates oxygen vacancies in the exposed metal oxide regions (e.g., IGZO $\longrightarrow$ n^+ IGZO), thus increasing the number of charge carriers therein and making these exposed regions 309, 310 more conductive than the channel region 311 of the metal oxide island 304 which is protected by the gate dielectric 303 and the gate electrode 302. However, the oxygen vacancies created are not stable and the resistance in the exposed metal oxide regions can easily increase again over time after the plasma treatment process. *See e.g.*, Park et al., Applied Phys. Letts, 93: 053501 (2008); and Kim et al., IEEE Electron Device Letts., 30(4): 374-376 (2009).

[0011] The second method is referred to as the hydrogen diffusion method, the process flow of which is illustrated in Fig. 5. As shown in Fig. 5(c), the hydrogen diffusion method involves depositing a hydrogen-rich film 313 (often SiN_x:H, which could also serve as the interlayer dielectric) on top of the gate electrode 302 and the exposed metal oxide regions 309, 310. As hydrogen from the hydrogen-rich film 313 diffuses into the exposed metal oxide regions 309, 310, charge carriers are generated in those regions, thereby reducing their

electrical resistance. Unfortunately, like the plasma treatment method, the low-resistance metal oxide regions created by the hydrogen diffusion method are not stable because some hydrogen will also diffuse into the channel region, especially upon thermal annealing, which makes the channel region over conductive. *See e.g.*, Wu et al., J. Display Technology, 5(12): 515-519 (2009).

[0012] The third method is known as the metal reaction method, the process flow of which is illustrated in Fig. 6. This method involves depositing a very thin reactive metal layer 314 such as an aluminum foil on top of the gate electrode 302 and the exposed metal oxide regions 309, 310 as shown in Fig. 6(c). Then, an oxidation step (e.g., by annealing) is performed to oxidize the aluminum foil into Al_2O_3. In the oxidation reaction of the metal film 314, some of the oxygen in the exposed metal oxide regions 309, 310 is used. This creates oxygen vacancies and generates carriers in the exposed metal oxide regions, reducing the electrical resistance in the regions 309, 310 compared to the channel region 311. However, a problem associated with this method is that it is not easy to control either the film thickness uniformity or the oxidation process of the thin reactive metal. *See e.g.*, U.S. Patent Application Publication No. 2012/0001167.

[0013] Accordingly, there is a desire in the art to develop a new method for lowering the resistance in the source/drain regions of a self-aligned oxide TFT.

Summary

[0014] In light of the foregoing, the present teachings provide a self-aligned oxide TFT, in which the source/drain regions of the oxide semiconductor layer is created by contacting it with a reductive polymer, thereby doping the source/drain regions with valence electrons from the reductive polymer and reducing the electrical resistance in the source/drain regions. The reductive polymer can be an electrically insulating polymer that has, in its backbone and/or its pendant group(s), one or more nitrogen atoms with a lone pair of electrons. The reductive polymer can be deposited over the oxide semiconductor layer as the organic interlayer dielectric. The present self-aligned oxide TFT can be fabricated as follows. A metal oxide (e.g. IGZO) layer is formed on a substrate, followed by a gate dielectric (or gate insulator, GI) and a gate electrode on top of the metal oxide layer. The gate electrode and gate dielectric are etched with the same pattern to expose side portions of the metal oxide layer. Unlike prior art methods that require a separate step (whether by plasma treatment, hydrogen diffusion, or metal reaction) to lower the electrical resistance in the source/drain region (i.e., the exposed metal oxide regions on top of which the source and drain electrodes

are formed), the present method uses a reductive polymer as the inter-layer dielectric (ILD). After the ILD is deposited onto the source/drain regions of the metal oxide active layer, valence electrons from the reductive polymer diffuse into the source/drain regions (but not the channel region which is masked by the gate dielectric/gate electrode), increasing the number of charge carriers in the source/drain regions and consequently, reducing the electrical resistance in the source/drain regions. The ILD is then patterned to open via holes for the deposition of the source and drain electrodes.

[0015] The foregoing as well as other features and advantages of the present teachings will be more fully understood from the following figures, description, examples, and claims.

Brief Description of Drawings

[0016] It should be understood that the drawings described below are for illustration purposes only. The drawings are not necessarily to scale, with emphasis generally being placed upon illustrating the principles of the present teachings. The drawings are not intended to limit the scope of the present teachings in any way.

[0017] **Fig. 1** illustrates the structure of a bottom-gate back-channel-etch (BCE) oxide thin film transistor 10, which includes a substrate 101, a gate electrode 102, a gate insulator 103, an oxide semiconductor active layer 104, source and drain electrodes 105, 106, and a passivation layer 107.

[0018] **Fig. 2** illustrates the structure of a bottom-gate etch stop oxide thin film transistor 20, which includes a substrate 201, a gate electrode 202, a gate insulator 203, an oxide semiconductor active layer 204, source and drain electrodes 205, 206, a passivation layer 207, and an etch stop layer 208.

[0019] **Fig. 3** illustrates the structure of a self-aligned top-gate (SA-TG) oxide thin film transistor 30, which includes a substrate 301, a gate electrode 302, a gate insulator 303, an oxide semiconductor active layer 304, source and drain electrodes 305, 306, and an interlayer dielectric 307. The oxide semiconductor layer 304 includes source and drain regions 309, 310, which have lower electrical resistance compared to the channel region 311.

[0020] **Fig. 4** illustrates the process flow of how to fabricate an SA-TG oxide thin film transistor, where the low-resistance source/drain regions are formed by doping the oxide semiconductor layer partially using a prior art plasma treatment method.

[0021] **Fig. 5** illustrates the process flow of how to fabricate an SA-TG oxide thin film transistor, where the low-resistance source/drain regions are formed by doping the oxide semiconductor layer partially using a prior art hydrogen diffusion method.

[0022] **Fig. 6** illustrates the process flow of how to fabricate an SA-TG oxide thin film transistor, where the low-resistance source/drain regions are formed by doping the oxide semiconductor layer partially using a prior art metal reaction method.

[0023] **Fig. 7** illustrates the structure of a self-aligned top-gate (SA-TG) oxide thin film transistor 40 according to the present teachings, which incorporates an organic interlayer dielectric (ILD) 407 composed of a reductive polymer. The transistor 40 includes a substrate 401, a gate electrode 402, a gate insulator 403, an oxide semiconductor active layer 404, source and drain electrodes 405, 406, and the interlayer dielectric 407 composed of a reductive polymer. The oxide semiconductor layer 404 includes source and drain regions 409, 410, which have lower electrical resistance compared to the channel region 411.

[0024] **Fig. 8** illustrates the process flow of how to fabricate an SA-TG oxide thin film transistor according to the present teachings, where the low-resistance source/drain regions are formed by contacting the source/drain regions with an organic interlayer dielectric (ILD) composed of a reductive polymer.

[0025] **Fig. 9** illustrates the process flow of how to fabricate a self-aligned bottom-gate oxide thin film transistor 50 according to the present teachings, where the low-resistance source/drain regions are formed by contacting the source/drain regions with an organic interlayer dielectric (ILD) 507 composed of a reductive polymer.

[0026] **Fig. 10** illustrates (a) the device structure 60 used by the inventors to measure the doping effect of depositing a reductive ILD 607 according to the present teachings directly onto an exposed surface of a metal oxide semiconductor layer 604, and (b) a comparison device structure 70 where the metal oxide semiconductor layer 704 is untreated. The device structure 60 includes a substrate 601, a metal oxide semiconductor layer 604, patterned source and drain electrodes 605, 606 that define a channel region 609, and a reductive ILD 607 deposited over and in direct contact with the channel region 609 and the source and drain electrodes 605, 606. The comparison device structure 70 includes a substrate 701, a metal oxide semiconductor layer 704, and patterned source and drain electrodes 705, 706 that define a channel region 709 which is left exposed.

[0027] **Fig. 11** compares the sheet resistance of the metal oxide semiconductor layer (IGZO) as measured in the channel region 709 in the comparative device structure 70 (without an organic ILD overlayer) versus in the channel region 609 in the device structure 60 having a reductive organic ILD overlayer according to the present teachings. Specifically, poly(2-vinylpyridine), poly(4-vinylpyridine), branched polyethylenimine, and polyvinylpyrrolidone are used as exemplary reductive organic ILD.

Detailed Description

[0028] Throughout the application, where compositions are described as having, including, or comprising specific components, or where processes are described as having, including, or comprising specific process steps, it is contemplated that compositions of the present teachings also consist essentially of, or consist of, the recited components, and that the processes of the present teachings also consist essentially of, or consist of, the recited process steps.

[0029] In the application, where an element or component is said to be included in and/or selected from a list of recited elements or components, it should be understood that the element or component can be any one of the recited elements or components, or the element or component can be selected from a group consisting of two or more of the recited elements or components. Further, it should be understood that elements and/or features of a composition, an apparatus, or a method described herein can be combined in a variety of ways without departing from the spirit and scope of the present teachings, whether explicit or implicit herein.

[0030] The use of the terms “include,” “includes”, “including,” “have,” “has,” or “having” should be generally understood as open-ended and non-limiting unless specifically stated otherwise.

[0031] The use of the singular herein includes the plural (and vice versa) unless specifically stated otherwise. In addition, where the use of the term “about” is before a quantitative value, the present teachings also include the specific quantitative value itself, unless specifically stated otherwise. As used herein, the term “about” refers to a ±10% variation from the nominal value unless otherwise indicated or inferred.

[0032] It should be understood that the order of steps or order for performing certain actions is immaterial so long as the present teachings remain operable. Moreover, two or more steps or actions may be conducted simultaneously.

[0033] Throughout the specification, chemical structures may or may not be presented with chemical names. Where any question arises as to nomenclature, the structure prevails.

[0034] To address the limitations presented by prior art methods for doping the source/drain regions in a self-aligned metal oxide thin film transistor, the present teachings provide a new method to create doped source/drain regions in a metal oxide semiconductor layer by contacting those regions with an overlying organic layer that is capable of varying the electrical conductivity of the metal oxide semiconductor layer upon direct contact. More specifically, this organic layer can comprise a reductive polymer, which upon contact with the metal oxide semiconductor layer can dope the source/drain regions with valence electrons, thereby reducing the sheet resistance in the source/drain regions. In some embodiments, this organic layer can be a sacrificial layer that can be removed after the doping effect has been achieved. In other embodiments, this organic layer can be an additional layer onto which a much thicker organic interlayer dielectric (ILD) can be deposited to complete the device. However, in preferred embodiments, to simply the fabrication process and to reduce the number of photolithography steps, the organic layer comprising the reductive polymer is electrically insulating and therefore can be incorporated as the ILD. This organic layer also can be formulated as a photopatternable material such that it can be directly photopatterned (e.g., allowing the opening of via holes) without the use of a photoresist.

[0035] A self-aligned top-gate oxide semiconductor according to the present teachings is illustrated in Fig. 7. Referring to Fig. 7, the present self-aligned top-gate metal oxide thin film transistor 40 includes in sequence, from bottom to top, a substrate 401, a metal oxide semiconductor layer 404, a gate dielectric 403, a gate electrode 402, an organic interlayer dielectric 407 that includes a reductive polymer as described in more detail below, and the source and drain electrodes 405, 406. The gate dielectric 402 and the gate electrode 403 atop the metal oxide semiconductor layer 404 are etched with the same pattern, such that the metal oxide semiconductor layer includes a masked region 411 (underneath the gate dielectric and the gate electrode) and two unmasked (exposed) side regions 409, 410. The masked region 411 defines the channel region in the metal oxide semiconductor layer 404 and is aligned with the gate electrode 402. The channel length therefore corresponds to the width of the gate electrode. As shown in Fig. 7, the two unmasked side regions 409, 410 are in direct contact with the organic ILD 407, while the masked channel region 411 are protected by the gate dielectric 403 and gate electrode 402. As valence electrons diffuse from the organic ILD

into the unmasked side regions, the electrical conductivity increases in the unmasked side regions compared to the masked channel region in the metal oxide semiconductor layer, low-resistance source/drain regions are created. Source and drains 405, 406 deposited on the organic ILD extend through via holes in the organic ILD to make electrical contact with the low-resistance source/drain regions 409, 410 in the metal oxide semiconductor layer.

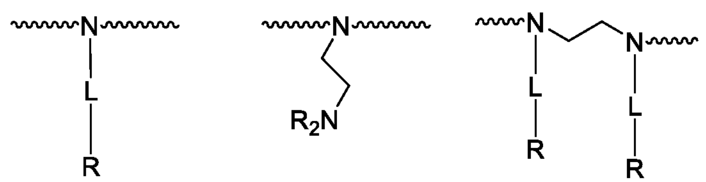
[0036] Fig. 8 illustrates the process flow of how to fabricate an SA-TG oxide thin film transistor according to the present teachings. The substrate 401 used in the present oxide TFT can be any of the substrate materials known in the art including, without limitation, doped silicon, an indium tin oxide (ITO), ITO-coated glass, ITO-coated polyimide or other plastics, copper, molybdenum, chromium, aluminum or other metals alone or coated on a polymer or other substrate. In preferred embodiments, the substrate can be a transparent substrate such as glass or a high-temperature plastic, examples of which include polycarbonate (PC), polyethersulfone (PES), polyacrylate (PA), polynorbornene (PNB), polyethylene terephthalate (PET), polyetheretherketone (PEEK), polyethylene naphthalate (PEN) or polyetherimide (PEI).

[0037] A metal oxide semiconductor island 404 can then be deposited on the substrate using processes known in the art (Fig. 8(a)). Suitable metal oxide semiconductors include, without limitation, indium oxide (In_2O_3), indium zinc oxide (IZO), zinc tin oxide (ZTO), indium gallium oxide (IGO), indium-gallium-zinc oxide (IGZO), indium-gallium-oxide (IGO), indium-yttrium-oxide (IYO), indium tin zinc oxide (ITZO), tin oxide (SnO_2), zinc oxide (ZnO), zirconium indium zinc oxide (ZrInZnO), and zirconium zinc tin oxide (ZrZnSnO). In preferred embodiments, the metal oxide semiconductor layer in the present TFT comprises IGZO. In conventional processes, the metal oxide semiconductor layer is vapor-phase processed (e.g., by DC sputtering from a target). However, solution-phase processes have been described, for example, in U.S. Patent No. 8,017,458. An annealing step (between about 250-400°C, preferably below about 300°C) can be performed to improve the semiconducting properties of the metal oxide layer. To pattern the metal oxide layer, a photoresist can be used, followed by etching of the metal oxide semiconductor according to the developed pattern of the photoresist. A wet etchant such as oxalic acid can be used, or a dry etching step can be performed.

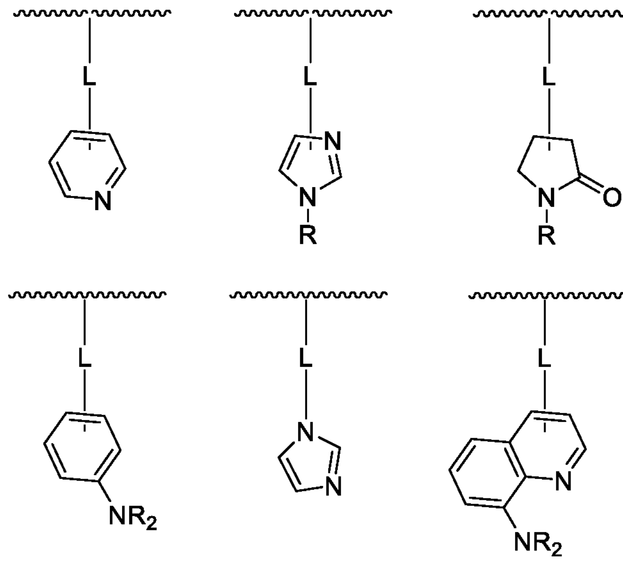
[0038] Subsequently, the gate dielectric 403 and gate electrode 402 can be deposited and patterned by conventional photolithography steps. The gate dielectric 403 can be composed of inorganic (e.g., oxides such as SiO_x, Al_2O_3, or HfO_2; nitrides such as Si_xN_y; and

oxynitrides such as silicon oxynitride SiO_xN_y), organic (e.g., polymers such as polymethylmethacrylate, polyester, polystyrene, polyhaloethylene, and other organic dielectric polymers known in the art), or hybrid organic/inorganic materials. If an inorganic dielectric such as silicon oxide or silicon nitride is used, a vapor-phase deposition method such as plasma-enhanced chemical vapor deposition (PECVD) can be used. Solution-phase processes such as printing, spin-coating, slot-coating, or spray-coating are usually used with organic dielectrics. The gate electrode 402 can be formed by sputtering a thin layer of metal (e.g., Mo or Ag) on top of the gate dielectric. The gate electrode is then patterned by photolithography and etching as described above with the patterning of the metal oxide semiconductor layer. Using the patterned gate electrode as a hard mask, the gate dielectric can be patterned by dry or wet etching to give the same pattern as the gate electrode (Fig. 8(b)). As shown in Fig. 8(b) and Fig. 8(c), a center region 411 of the metal oxide semiconductor layer 404 is masked by the gate dielectric 403 and the gate electrode 402, whereas the two side regions 409, 410 are exposed (unmasked). The center masked region 411 defines the channel region, and the unmasked regions 409, 410 on the two sides of the center masked region will be doped in the next step to increase their electrical conductivity compared to the masked channel region comprising the intrinsic metal oxide.

[0039] An organic interlayer dielectric 407 including a reductive polymer is then deposited over the partial stack, directly contacting the unmasked side regions 409, 410 in the metal oxide semiconductor layer 404 (Fig. 8(c)). The reductive polymer generally is an electrically insulating polymer that includes in its backbone and/or pendant group(s) one or more nitrogen atoms having a lone pair of electrons. For example, the reductive polymer can be an electrically insulating polymer that includes in its backbone and/or pendant group(s) an amine moiety, an imine moiety, an amide moiety, an imide moiety, an azine moiety, an azole moiety, or combinations thereof. In some embodiments, the backbone of the reductive polymer can include one of the following moieties:



wherein L is a covalent bond or a divalent organic group; and each R, independently, is H or a C_{1-20} alkyl group. In some embodiments, the reductive polymer can include one of the following pendant groups:



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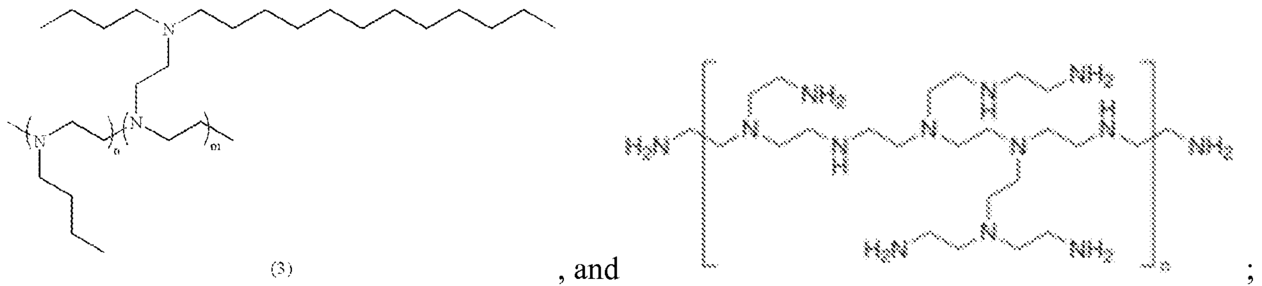
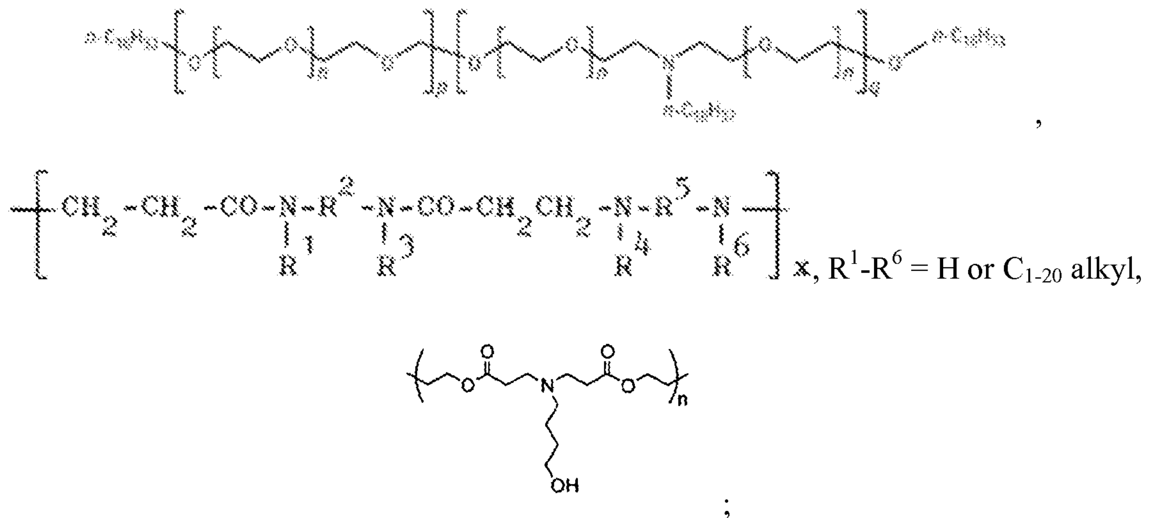
wherein L is a covalent bond or a divalent organic group; and each R, independently, is H or a C_{1-20} alkyl group. Exemplary reductive polymers that can be used as the organic ILD in the self-aligned oxide TFT according to the present teachings include:

i) polyimines such as:



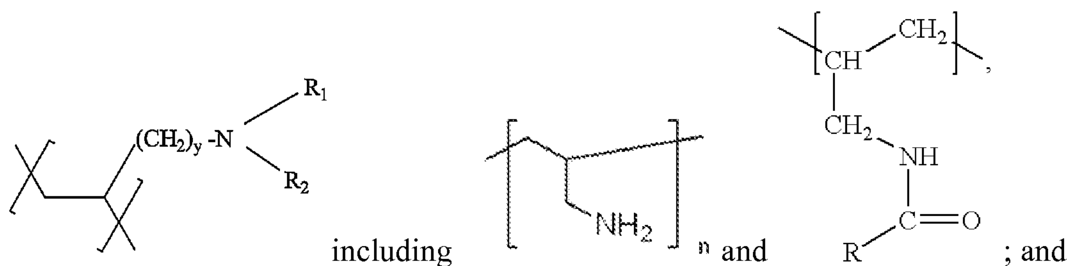
, and ;

ii) imine copolymers such as:

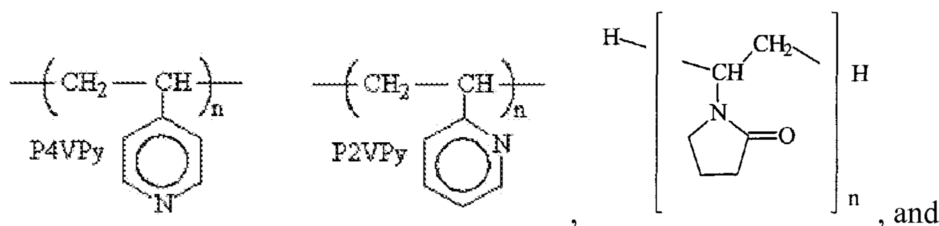


, x, R^1-R^6 = H or C_{1-20} alkyl, ;

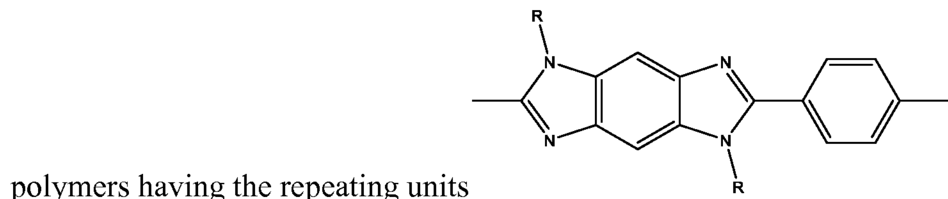
iii) polyallylamines such as:

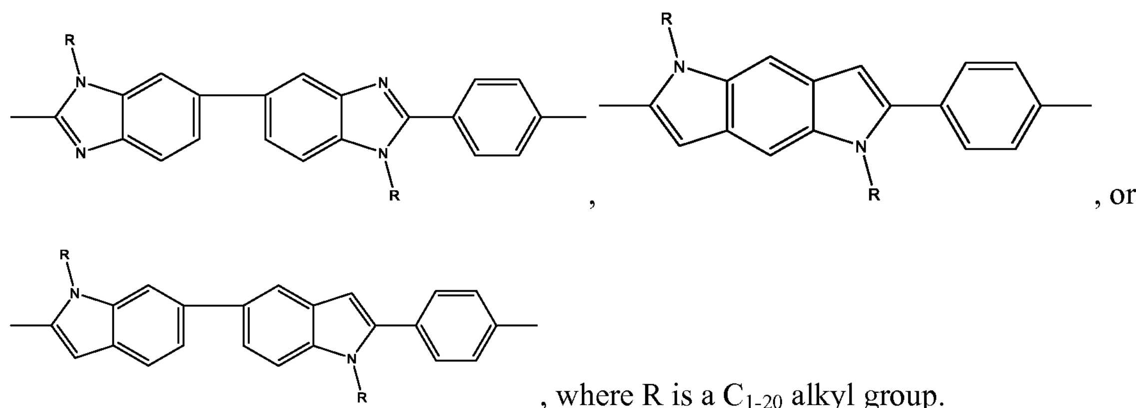


polymers including a nitrogen-containing cyclic (e.g., pyridine, pyrrole, pyrrolidone, imidazole, benzimidazole) moiety such as:



polymers having the repeating units





, where R is a C_{1-20} alkyl group.

[0040] The organic interlayer dielectric can be deposited from a composition comprising the reductive polymer in a solvent via various solution-phase processes (e.g., printing, spin-coating, slot-coating, spray-coating, and the like). The reductive polymer can be formulated with a crosslinking agent, to improve the mechanical and thermal stability of the resulting organic ILD. Various crosslinking agents are known in the art, examples of which include various epoxides, acrylates, maleimides, dienes, and cinnamates. In preferred embodiments, the reductive polymer composition is formulated as a photopatternable composition, such that the organic ILD can be photocrosslinked and patterned without the use of a photoresist.

Embodiments of such composition can include one or more photocrosslinking agents and/or photosensitizers. Examples of useful photosensitizers include fluorenones, indenes, nitrones, and phenantrolines. To improve adhesion between the organic ILD and the underlying layer, the reductive polymer composition also can include an adhesion promoter such as a silicate, a silane, a phosphonate, or a carboxylate.

[0041] Experimental data confirmed that the electrical resistance of a metal oxide thin film semiconductor can be lowered by at least 10 times (one order of magnitude) upon direct contact with a reductive polymer according to the present teachings. In some embodiments, the reduction in resistance has been shown to be 2-3 orders of magnitude (i.e., >100-1000 times). Accordingly, the present method can be used to create doped source/drain regions in a self-aligned oxide TFT.

[0042] Referring to Fig. 8(d), the reductive ILD 407 can be patterned to create via holes that expose part of the unmasked source/drain regions 409, 410. Subsequently, source/drain electrodes 405, 406 are formed by depositing (e.g., sputtering) and patterning metallic (e.g., Mo) thin films on top of the reductive ILD 407 and through the via holes to make electrical contact with the low-resistance source/drain regions 409, 410 in the metal oxide semiconductor layer 404 (Fig. 8(e)). A passivation layer (not shown) can be deposited on top of the stack to complete the device.

[0043] A self-aligned oxide TFT having a bottom-gate structure 50 can be fabricated as shown in Fig. 9. Specifically, an etch stop layer 508 is used to mask the metal oxide channel region 511 instead of the gate dielectric 503/gate electrode 502. As a whole, the bottom-gate structure 50 includes in sequence, from bottom to top, a substrate 501, a gate electrode 502, a gate dielectric 503, a metal oxide semiconductor layer 504, an etch stop layer 508, an reductive organic ILD 507 according to the present teachings, and the source and drain electrodes 505, 506. The channel region 511 is aligned with the gate electrode 502 by patterning the etch stop layer 508 to be aligned with the gate electrode 502. This can be done by using the gate electrode 502 as a photomask and exposing the etch stop layer 508 to irradiation through the transparent substrate 501 (i.e., from the bottom of the device) as described in more details below.

[0044] Referring to Fig. 9(a), the gate electrode can be formed by sputtering a thin metallic film (e.g., Mo) on a transparent substrate, followed by photolithography patterning and etching as described with the top-gate structure. The gate dielectric can be formed by

depositing an organic dielectric (e.g., by spin-coating) or an inorganic dielectric (e.g., SiO_x by PECVD) over the gate electrode. A metal oxide semiconductor island then can be formed on the gate dielectric by, for example, sputtering IGZO followed by patterning, as shown in Fig. 9b. An etch stop (ES) layer such as SiO_x then can be deposited on the metal oxide semiconductor layer, and patterned by photolithography with back side exposure (Fig. 9c). An organic material, preferably, a photopatternable polymeric material, also can be used as the ES layer and similarly patterned with back side exposure. The ES layer accordingly will have the same pattern as the gate electrode, and the masked region of the metal oxide semiconductor layer underneath the ES layer, which defines the channel region, will be aligned with the gate electrode. The subsequent steps are the same as the fabrication of the top-gate structure. Namely, an organic interlayer dielectric including a reductive polymer according to the present teachings is deposited over the partial stack, directly contacting the unmasked side regions in the metal oxide semiconductor layer (Fig. 9(d)). The organic ILD can be patterned to create via holes that expose part of the unmasked source/drain regions (Fig. 9(e)). Subsequently, source/drain electrodes are formed by depositing (e.g., sputtering) metallic (e.g., Mo) thin films on top of the organic ILD and through the via holes to make electrical contact with the low-resistance source/drain regions in the metal oxide semiconductor layer followed by patterning (Fig. 9(f)). A passivation layer can be deposited on top of the stack to complete the device.

[0045] Various embodiments of the transistors described herein can be arranged in an array and used as switching devices or peripheral drivers in active matrix displays such as active matrix liquid crystal displays (AMLCDs), active matrix organic light-emitting displays, and active matrix electrophoretic displays; and as pixel drivers for active matrix organic light-emitting diodes (AMOLEDs).

[0046] The following examples are provided to illustrate further and to facilitate the understanding of the present teachings and are not in any way intended to limit the invention.

[0047] Example 1: Doping effect of reductive polymers

[0048] To verify the doping effects of contacting a reductive polymer with a metal oxide thin film semiconductor, test devices having the structures shown in Fig. 10 were fabricated. The structure shown in Fig. 10(b) is a control device without a reductive polymer coating. The devices were fabricated as follows. IGZO was used as the representative metal oxide, and a thin film (30 nm) of IGZO was sputtered on a glass substrate using a sputtering system

with DC power of 300 W, Ar flow of 100 sccm, and O_2 flow of 10 sccm. The IGZO thin film was patterned by photolithography and wet etching in oxalic acid to form IGZO islands. Molybdenum was then patterned by photolithography and wet etching to form contact pads on both sides of each IGZO island. The width of each IGZO island was about 500 μm, and the channel length (the distance between two molybdenum pads) was about 250 μm. For the control device, the average initial sheet resistance of IGZO in between the two metal pads was measured to be around 2.95×10^{10} ohm.

[0049] For the test devices, one of four different formulations was spin-coated on top of the metal pads and the exposed IGZO channel. The four formulations include, respectively, poly(2-vinylpyridine) (P2VPy), poly(4-vinylpyridine) (P4VPy), a branched polyethylenimine (PEI) (polyethylenimine, ethylenediamine branched from Sigma-Aldrich), and polyvinylpyrrolidone. After spin-coating, the organic ILD was cured at 200°C. The sheet resistance of the IGZO channel region in contact with the organic ILD was measured, and the results are shown in Fig. 11.

[0050] Specifically, poly(2-vinylpyridine)-coated IGZO showed an average resistance of 2.08×10^7 ohm; poly(4-vinylpyridine)-coated IGZO showed an average resistance of 7.99×10^6 ohm, branched PEI-coated IGZO showed an average resistance of 1.31×10^8 ohm, and polyvinylpyrrolidone-coated IGZO showed an average resistance of 2.50×10^8 ohm. Accordingly, each of the organic ILD-coated IGZO exhibited a decrease in resistance at least 2~3 orders of magnitude lower than that of intrinsic IGZO.

[0051] The experimental data therefore confirmed that contacting a reductive polymer with a metal oxide thin film semiconductor could effectively lower the electrical resistance of the metal oxide thin film semiconductor.

[0052] All publications, patent applications, patents, and other references mentioned herein are incorporated by reference in their entirety. In case of conflict, the present specification, including definitions, controls.

[0053] The present teachings can be embodied in other specific forms without departing from the spirit or essential characteristics thereof. The foregoing embodiments are therefore to be considered in all respects illustrative rather than limiting on the present teachings described herein. The scope of the present teachings is thus indicated by the appended claims rather than by the foregoing description, and all changes that come within the meaning and range of equivalency of the claims are intended to be embraced therein.

CLAIMS

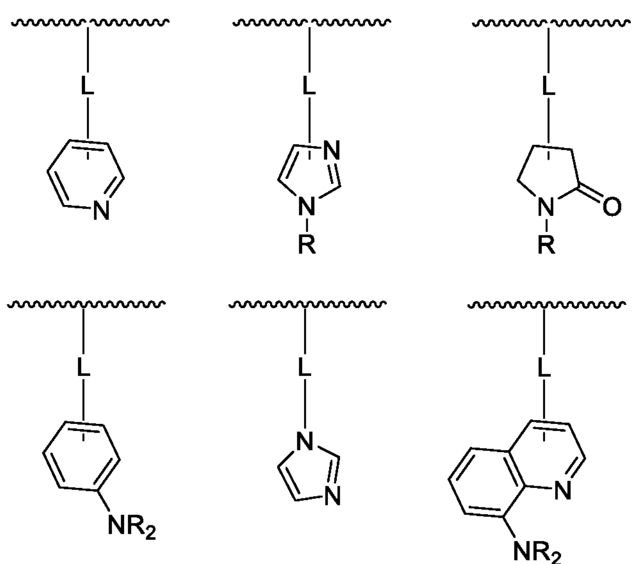
1. A self-aligned metal oxide thin film transistor comprising a substrate, a metal oxide semiconductor layer, a gate dielectric, an organic interlayer dielectric, a gate electrode, and source and drain electrodes, wherein the metal oxide semiconductor layer comprises a masked region aligned with the gate electrode that is not in direct contact with the organic interlayer dielectric and unmasked regions that are in direct contact with the organic interlayer dielectric, and wherein the organic interlayer dielectric comprises a polymeric material capable of increasing the electrical conductivity of the metal oxide semiconductor layer upon direct contact.

2. The transistor of claim 1, wherein the polymeric material comprises a reductive polymer.

3. The transistor of claim 2, wherein the reductive polymer is an electrically insulating polymer comprising in its backbone and/or pendant group(s) one or more nitrogen atoms having a lone pair of electrons.

4. The transistor of claim 2, wherein the reductive polymer is an electrically insulating polymer comprising in its backbone and/or pendant group(s) an amine moiety, an imine moiety, an amide moiety, an imide moiety, an azine moiety, an azole moiety, or combinations thereof.

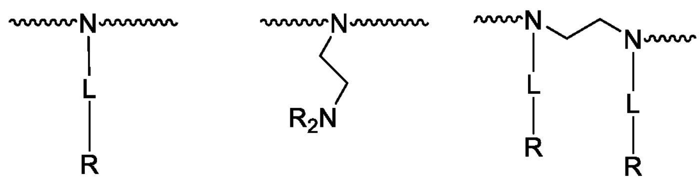
5. The transistor of claim 4, wherein the reductive polymer comprises one of the following pendant groups:



,

wherein L is a covalent bond or a divalent organic group; and each R, independently, is H or a C_{1-20} alkyl group.

6. The transistor of claim 4, wherein the backbone of the reductive polymer comprises one of the following moieties:



wherein L is a covalent bond or a divalent organic group; and each R, independently, is H or a C_{1-20} alkyl group.

7. The transistor of claim 4, wherein the reductive polymer is a polyimine.

8. The transistor of claim 4, wherein the reductive polymer is a polyallyl amine.

9. The transistor of claim 4, wherein the reductive polymer comprises in its backbone and/or pendant group(s) a pyridine moiety, a pyrrole moiety, an imidazole moiety, a benzimidazole moiety, a pyrrolidone moiety, or combinations thereof.

10. The transistor of claim 2, wherein the reductive polymer is selected from the group consisting of poly(vinylpyridine), poly(vinylpyrrolidone), and poly(ethylenimine).

11. The transistor of claim 2, wherein the polymeric material comprises a crosslinked matrix of the reductive polymer.

12. The transistor of claim 1, wherein the metal oxide semiconductor layer comprises IGZO.

13. The transistor of claim 1, wherein the gate dielectric comprises silicon oxide, silicon nitride, or silicon oxynitride.

14. The transistor of claim 1, wherein the gate dielectric comprises an organic material.

15. The transistor of claim 1, wherein the substrate comprises a flexible plastic substrate.

16. The transistor of claim 1, wherein the unmasked regions of the metal oxide semiconductor layer that are in direct contact with the organic interlayer dielectric have a conductivity that is more than 10 times higher than the conductivity of the masked region

of the metal oxide semiconductor layer not in direct contact with the organic interlayer dielectric.

17. The transistor of claim 16, wherein the unmasked regions of the metal oxide semiconductor layer that are in direct contact with the organic interlayer dielectric have a conductivity that is more than 100 times higher than the conductivity of the masked region of the metal oxide semiconductor layer not in direct contact with the organic interlayer dielectric.

18. The transistor of claim 17, wherein the unmasked regions of the metal oxide semiconductor layer that are in direct contact with the organic interlayer dielectric have a conductivity that is more than 1000 times higher than the conductivity of the masked region of the metal oxide semiconductor layer not in direct contact with the organic interlayer dielectric.

19. The transistor of any one of claims 1-18, wherein the transistor has a top gate structure comprising in sequence from bottom to top: the substrate, the metal oxide semiconductor layer, the gate dielectric, the gate electrode, the organic interlayer dielectric, and the source and drain electrodes, wherein the masked region of the metal oxide semiconductor layer is aligned with the gate dielectric and the gate electrode, and the organic interlayer dielectric comprises via holes through which the source and drain electrodes make contact with the unmasked regions of the metal oxide semiconductor layer.

20. The transistor of any one of claims 1-18, wherein the transistor has a bottom gate structure comprising in sequence from bottom to top: the substrate, the gate electrode, the gate dielectric, the metal oxide semiconductor layer, an etch stop layer, the organic interlayer dielectric, and the source and drain electrodes, wherein the masked region of the metal oxide semiconductor layer is aligned with the gate electrode and the etch stop layer, and the organic interlayer dielectric comprises via holes through which the source and drain electrodes make contact with the unmasked regions of the metal oxide semiconductor layer.

21. A method of fabricating a self-aligned metal oxide thin film transistor, the method comprising:

forming a metal oxide semiconductor layer over a substrate;

forming a gate dielectric over the metal oxide semiconductor layer;

forming a gate electrode over the gate dielectric and patterning the gate electrode and the gate dielectric together to provide a masked region of the metal oxide semiconductor layer and unmasked regions of the metal oxide semiconductor layer;

forming an organic interlayer dielectric by depositing over the gate electrode and the unmasked regions of the metal oxide semiconductor layer a composition comprising a reductive polymer;

patterning the organic interlayer dielectric to provide via holes through the organic interlayer dielectric that extend to the unmasked regions of the metal oxide semiconductor layer; and

forming source and drain electrodes in contact with the unmasked regions of the metal oxide semiconductor layer through the via holes.

22. The method of claim 21, wherein the composition comprising the reductive polymer further comprises a crosslinking agent.

23. The method of claim 22, wherein the crosslinking agent is selected from the group consisting of a cinnamate, a diene, a maleimide, an acrylate, and an epoxide.

24. The method of claim 21, wherein the composition comprising the reductive polymer further comprises an adhesion promoter.

25. The method of claim 24, wherein the adhesion promoter is selected from the group consisting of a silicate, a silane, a phosphonate, and a carboxylate.

26. The method of claim 21, wherein the composition comprising the reductive polymer further comprises a photosensitizer.

27. The method of claim 26, wherein the photosensitizer is selected from the group consisting of a fluorenone, an indene, a nitrone, and a phenantroline.

28. The method of claim 21 further comprising forming a passivation layer over the organic interlayer dielectric and the source and drain electrodes.

29. A method of fabricating a self-aligned metal oxide thin film transistor, the method comprising:

forming a gate electrode over a substrate;

forming a gate dielectric over the gate electrode;

forming a metal oxide semiconductor layer over the gate dielectric;

forming an etch stop layer over the metal oxide semiconductor layer;

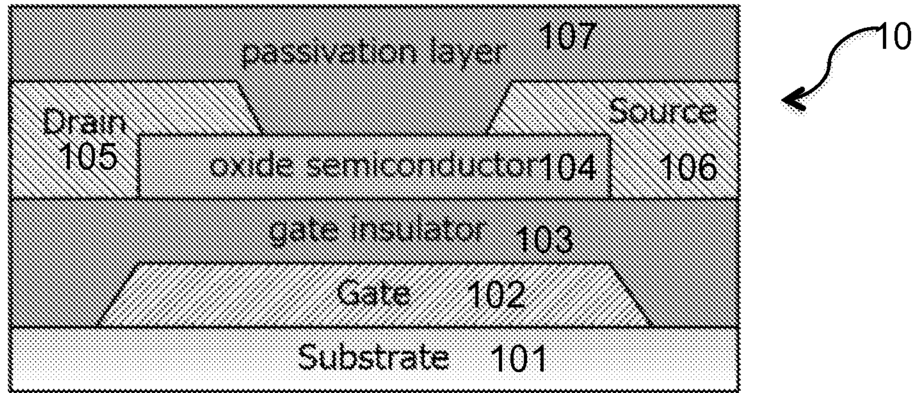
patterning the etch stop layer to be aligned with the gate electrode and to provide a masked region of the metal oxide semiconductor layer and unmasked regions of the metal oxide semiconductor layer;

forming an organic interlayer dielectric by depositing over the etch stop layer and the unmasked regions of the metal oxide semiconductor layer a composition comprising a reductive polymer;

patterning the organic interlayer dielectric to provide via holes through the organic interlayer dielectric that extend to the unmasked regions of the metal oxide semiconductor layer; and

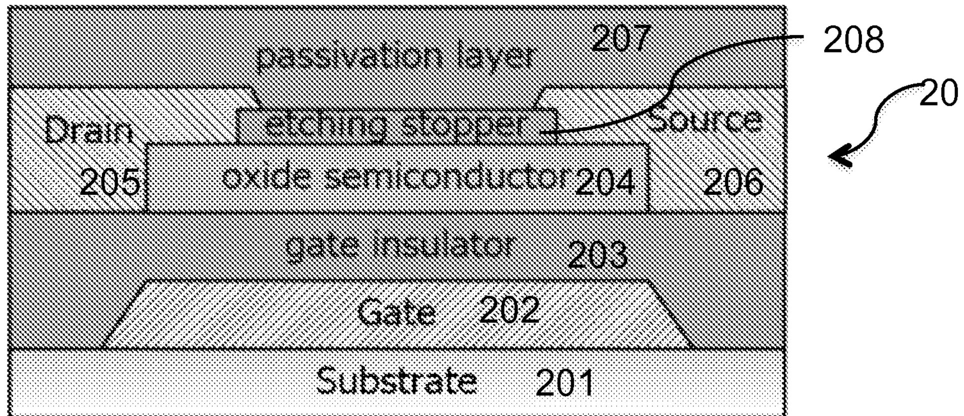
forming source and drain electrodes in contact with the unmasked regions of the metal oxide semiconductor layer through the via holes.

30. The method of claim 29, wherein the composition comprising the reductive polymer further comprises a crosslinking agent, an adhesion promoter, and/or a photosensitizer.



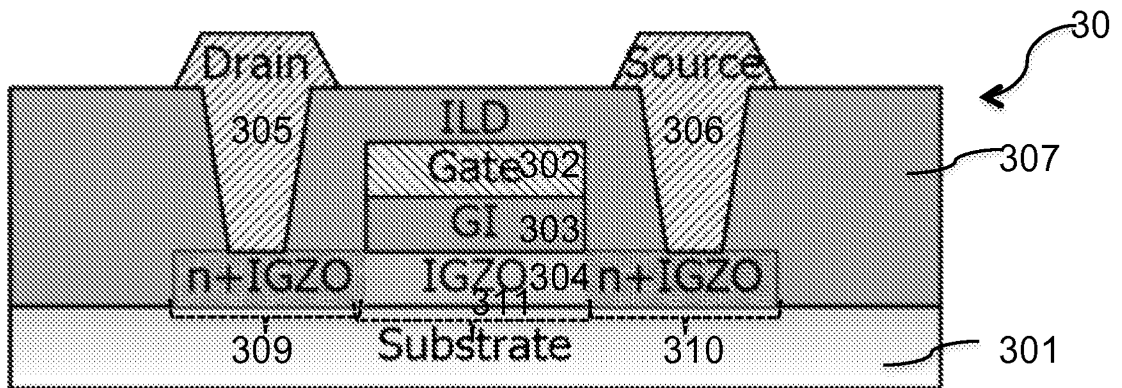
PRIOR ART

FIG. 1



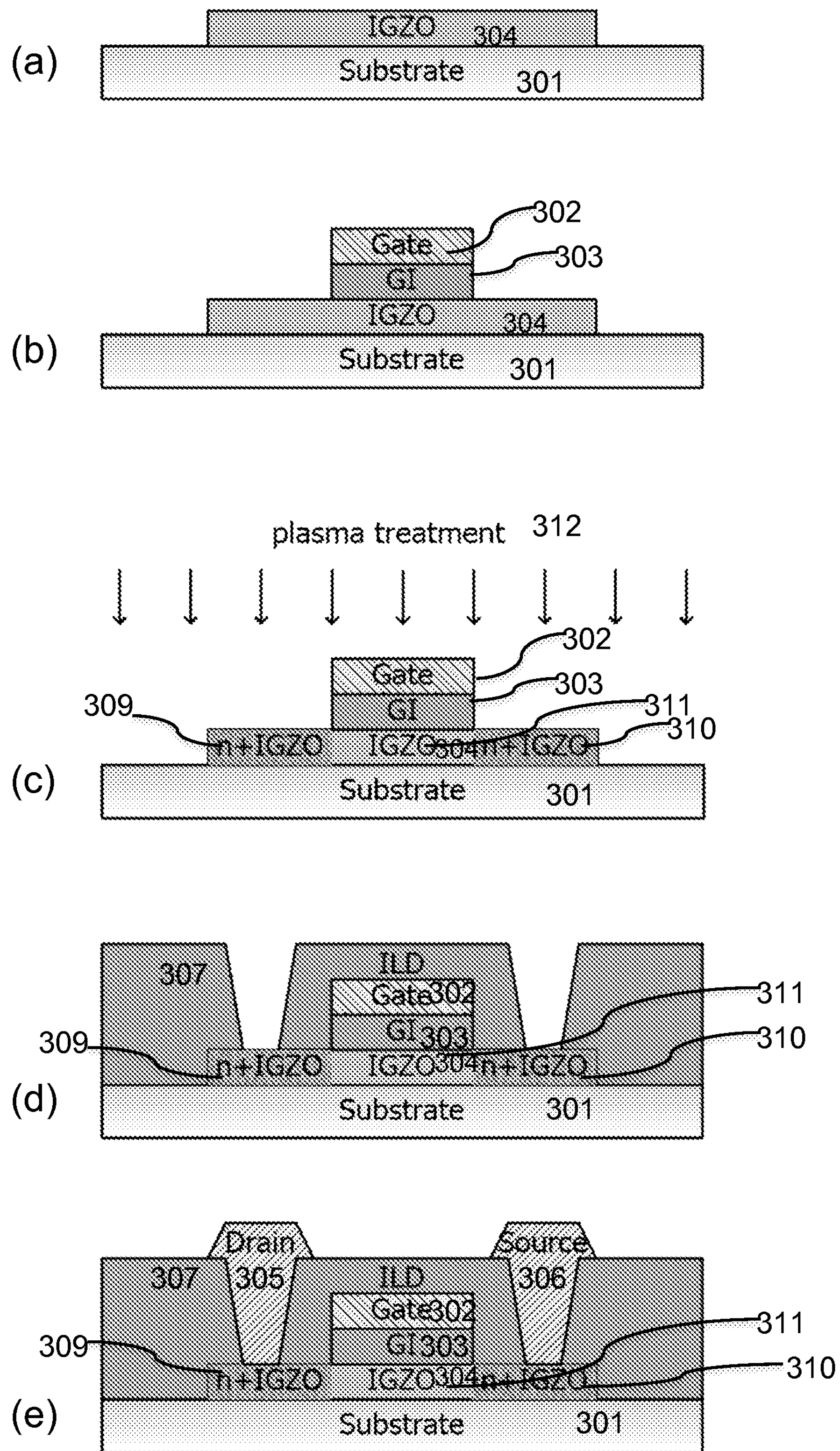
PRIOR ART

FIG. 2



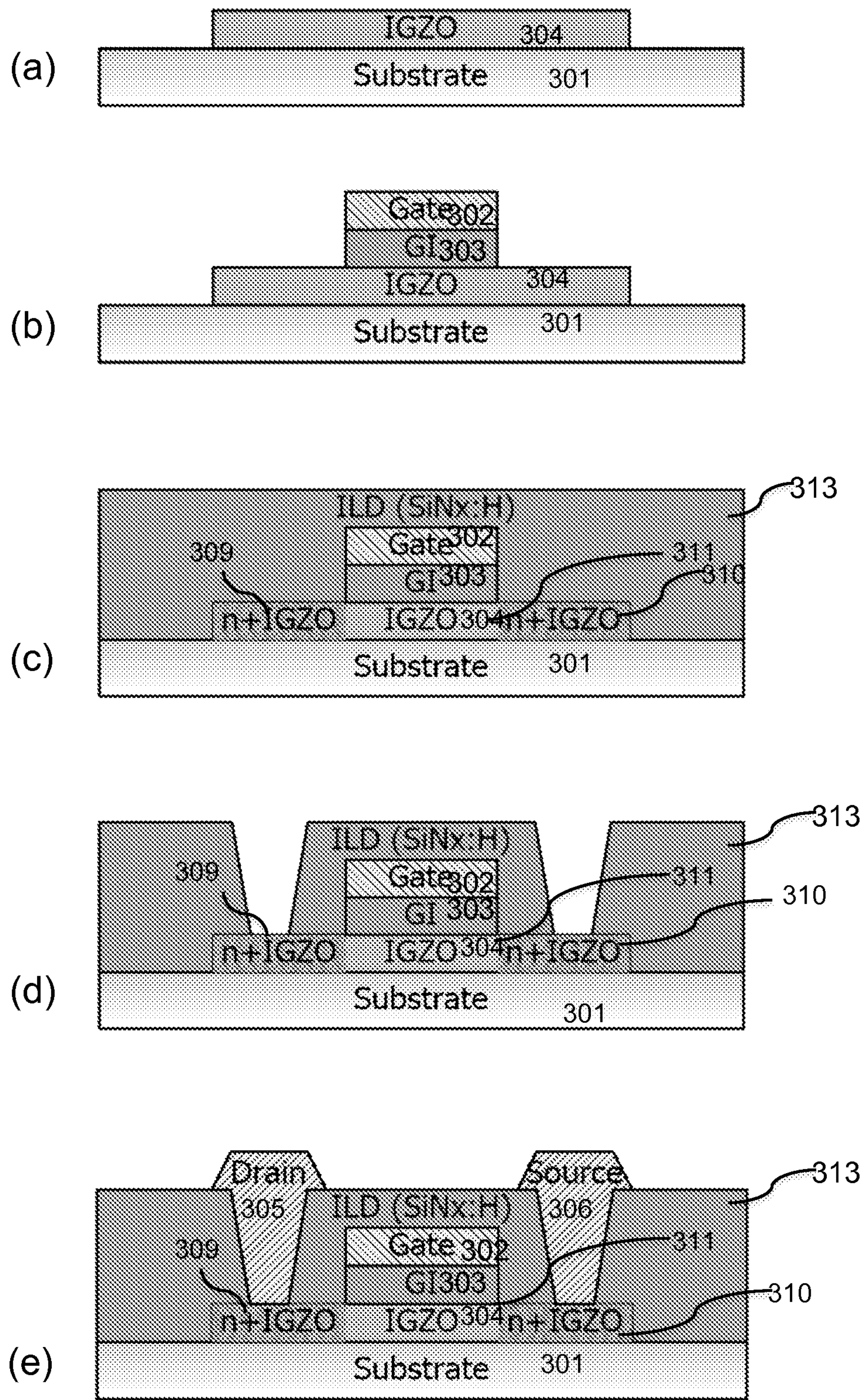
PRIOR ART

FIG. 3



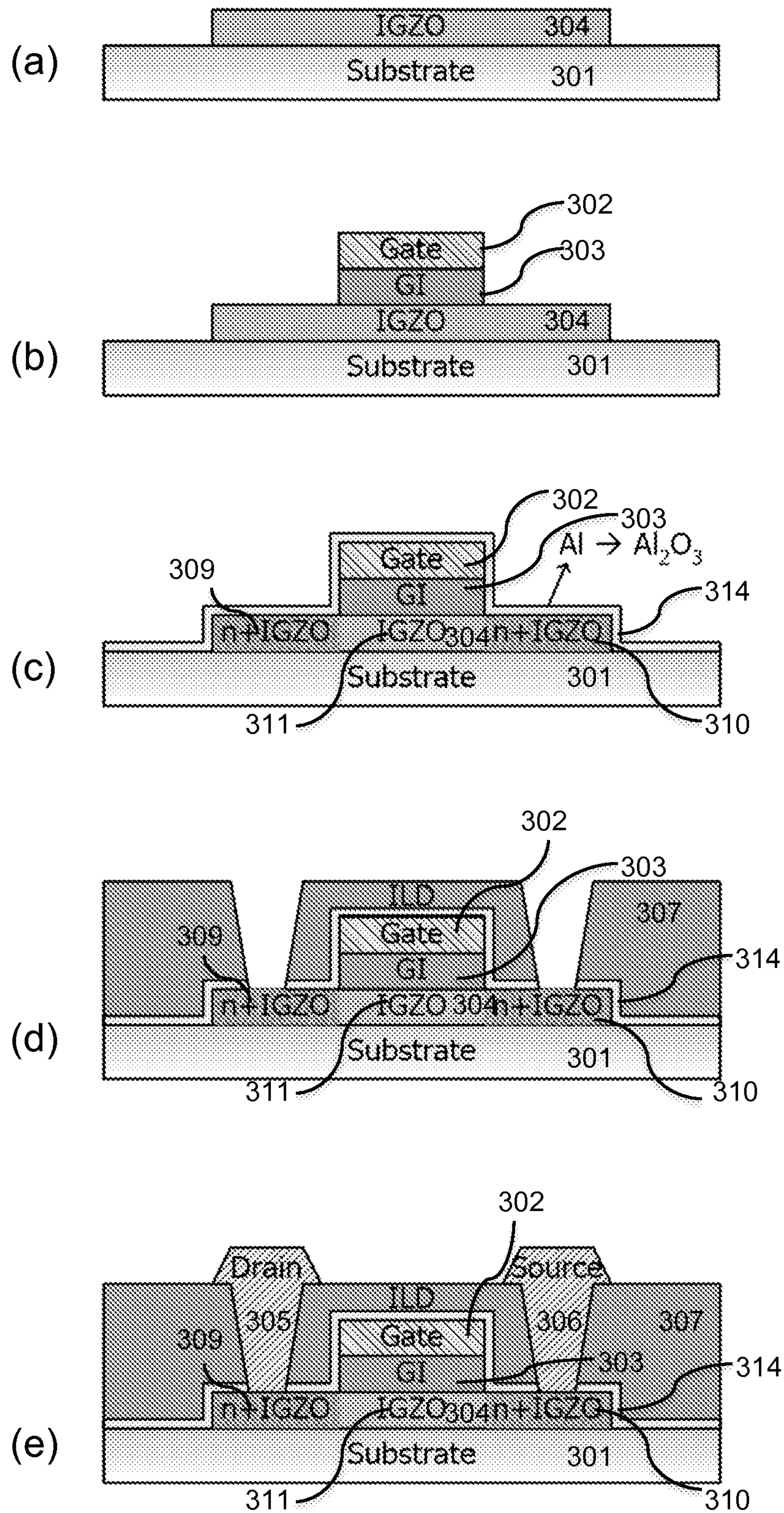
PRIOR ART

FIG. 4



PRIOR ART

FIG. 5



PRIOR ART

FIG. 6

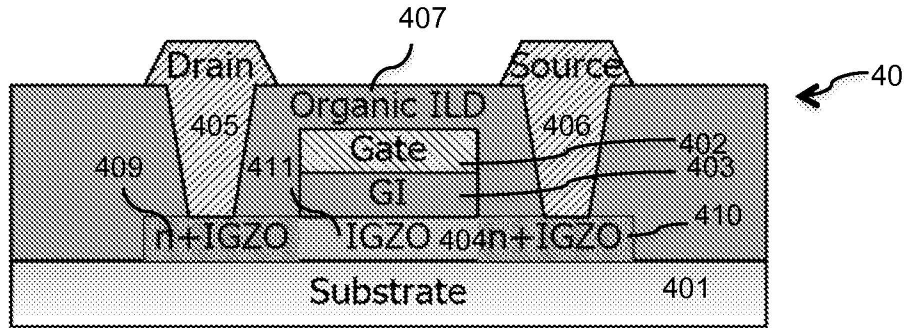


FIG. 7

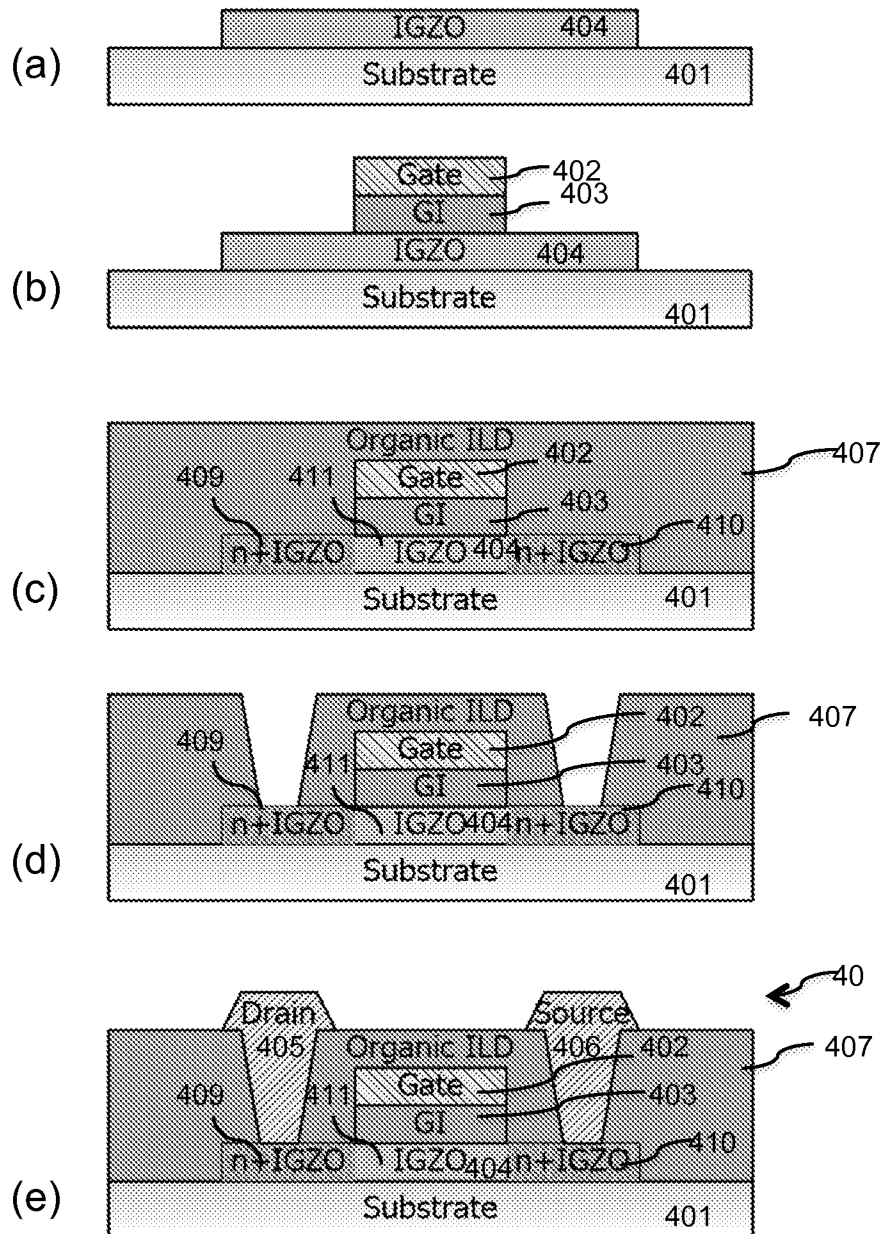


FIG. 8

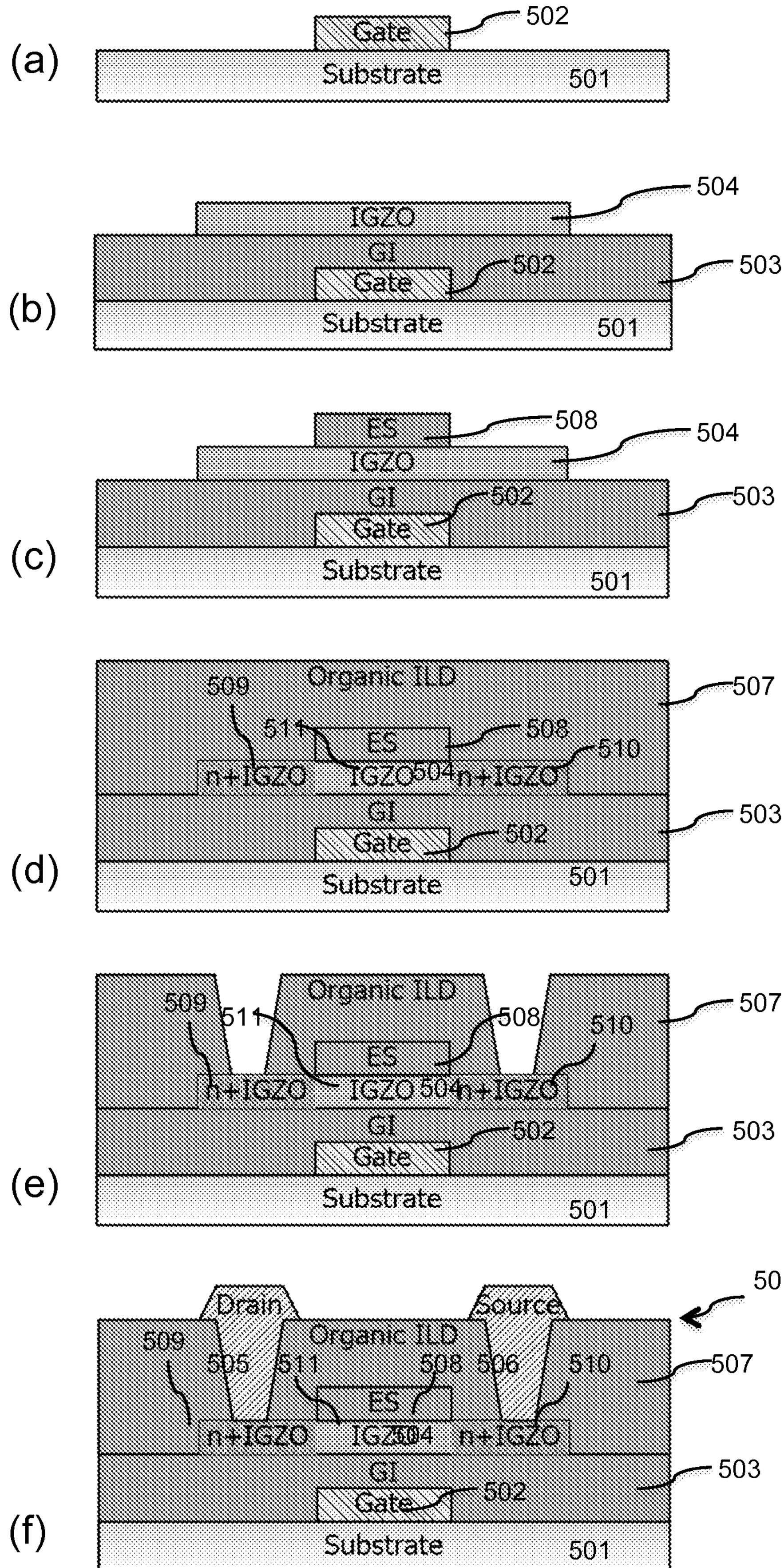


FIG. 9

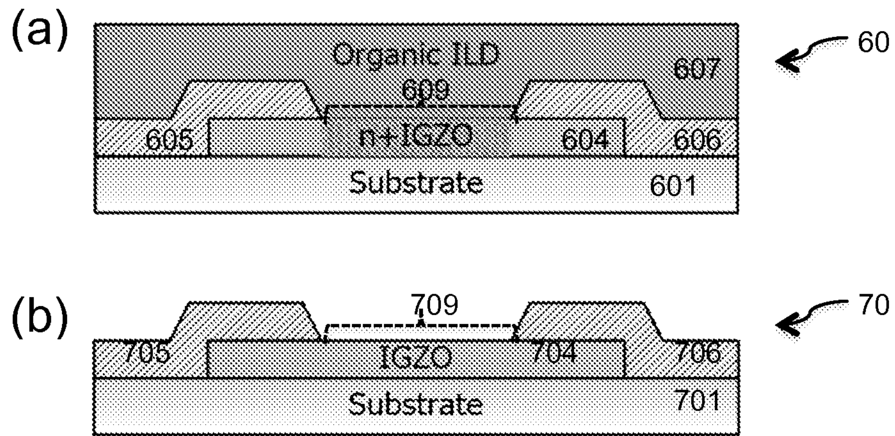


FIG. 10

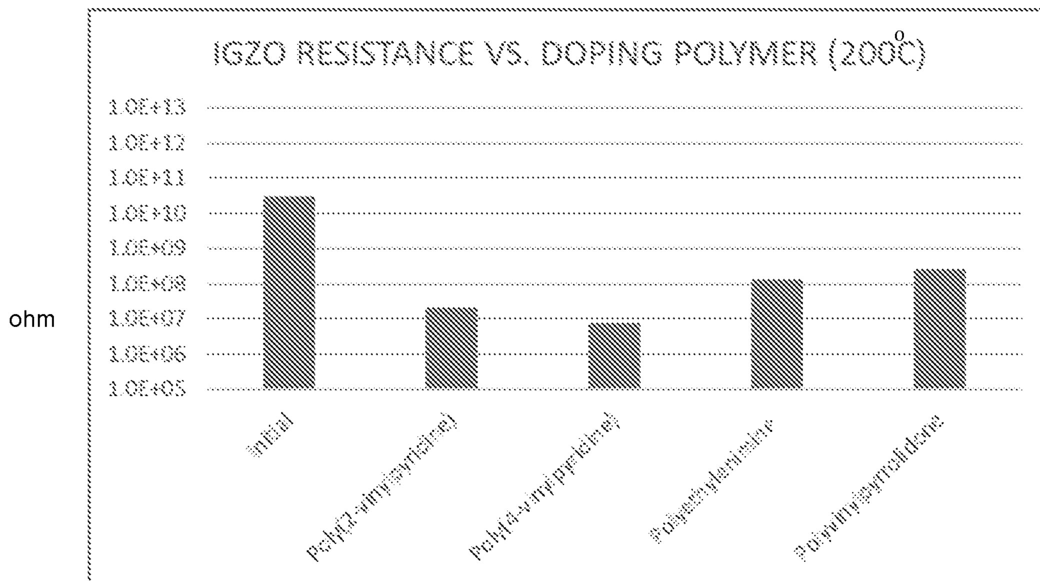


FIG. 11

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2015/034686

A. CLASSIFICATION OF SUBJECT MATTER

H01L 27/32(2006.01)i, H01L 51/56(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L 27/32; H01L 51/05; C08J 3/24; H01L 29/786; G03F 7/004; G02F 1/1368; B32B 9/04; G02F 1/139; G03F 7/039; H01L 51/56

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
Korean utility models and applications for utility models
Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
eKOMPASS(KIPO internal) & Keywords: metal oxide semiconductor, organic interlayer dielectric, thin film transistor, reductive polymer

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X Y	US 2012-0001167 A1 (NARIHIRO MOROSAWA) 05 January 2012 See paragraphs [0047]-[0182] and figures 1-21.	1-2,12-13,15-21,28-29 3-11,14,22-27,30
Y	US 2009-0152537 A1 (SEONG HYUN KIM et al.) 18 June 2009 See paragraphs [0018]-[0025] and claim 1.	3-11,14,22-23
Y	US 2003-0099844 A1 (HIROYUKI HANAHATA et al.) 29 May 2003 See paragraph [0105] and claim 1.	6-7
Y	KR 10-2010-0009801 A (TECHNO SEMICHEM CO., LTD. et al.) 29 January 2010 See paragraphs [0057]-[0067].	24-27,30
A	US 7872722 B2 (HAJIME KIMURA) 18 January 2011 See abstract, claims 1-27 and figures 1-33.	1-30

☐ Further documents are listed in the continuation of Box C. ☒ See patent family annex.

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
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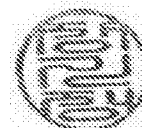
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents,such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
31 August 2015 (31.08.2015)	**31 August 2015 (31.08.2015)**

Name and mailing address of the ISA/KR
International Application Division
Korean Intellectual Property Office
189 Cheongsa-ro, Seo-gu, Daejeon Metropolitan City, 35208, Republic of Korea
Facsimile No. +82-42-472-7140

Authorized officer
Jang, Gijeong
Telephone No. +82-42-481-8364



INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

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