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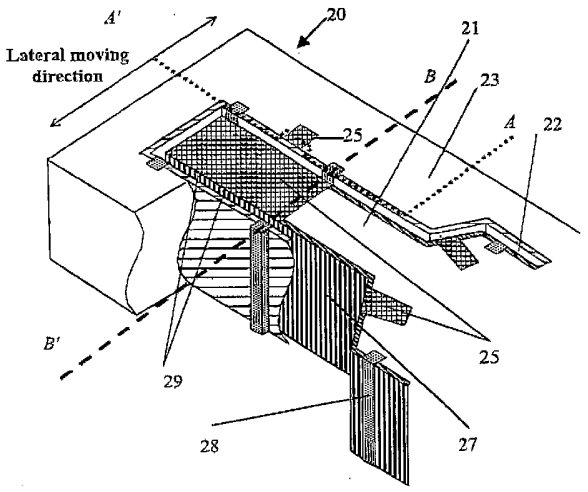
(54) **Title:** A MEMS DEVICE INCLUDING A LATERALLY MOVABLE PORTION WIHT PIEZO-RESISTIVE SENSING ELEMENTS AND ELECTROSTATIC ACTUATING ELEMENTS ON TRENCH SIDE WALLS AND METHODS FOR PRODUCING THE SAME



(57) **Abstract:** P-type doped region(s) 25 are formed in the upper surface of an n-type substrate 20. A trench 22 is formed in the substrate (e.g. by DRIE cutting) intersecting with the doped regions and defining a portion 21 of the substrate which is movable in the plane of the substrate relative to the rest of the substrate. Then diffusion of P-type dopant is effected into the trench side-walls to create piezoelectric elements 27 and electrode elements 29 for electrostatic actuation. Owing to the intersection of two doped regions, there are good electrical paths between the electrical elements 27, 29 on the trench side-walls and the previously doped portions on the wafer surface. The trench 22 intersects with insulating elements 28, so that the insulating elements 28 mutually insulate adjacent ones of the electrical elements 27, 29. P-n junctions between the electrical elements 27, 29 and the substrate 20 insulate the electrical elements 27, 29 from the substrate.

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For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

A MEMS device including a laterally movable portion with piezo-resistive sensing elements and electrostatic actuating elements on trench side walls, and methods for producing the same

Field of the invention

The present invention relates to the fabrication of MEMS devices, in particular MEMS devices including a laterally movable portion having one or more piezoresistive elements and/or electrostatic actuating elements on its sides.

Background of Invention

Since the advent of inductively coupled plasma (ICP) deep reactive etching (DRIE) technology, various MEMS (micro-electromechanical systems) structures have been proposed comprising an element which is movable laterally in-plane, i.e. in the plane of the semiconductor substrate(s) from which the devices are typically produced. The laterally movable portion may take the form of a laterally deflectable cantilever. This kind of MEMS device benefits from advanced bulk-micro-machining fabrication capabilities of DRIE to form high aspect ratio micro-structures. In some applications of the such MEMS devices, the motion of the movable portion is sensed (typically, by capacitive sensing); in other applications, the movable portion is moved by electrostatic actuation.

Unlike surface micro-machining fabrication, DRIE-based fabrication enjoys sticking-free release. In addition, in-plane lateral configuration can be exploited for other advanced features such as elimination of squeeze-film damping effects, comb-drive actuation and over-range self-caging, etc.

The fabrication technologies for in-plane lateral MEMS structures can be classified into two categories. The first category is SOI (silicon-on-insulator)

wafer based technology [1, 2], in which a wafer includes a silicon layer formed over an insulating layer. The other category is based on the use of a single homogenous wafer such as crystalline silicon (such techniques are referred to here as "single-wafer-based"). Compared with SOI-wafer based technology, the single-wafer-based technique has advantages in terms of low-cost, simplification and integration compatibility with circuits, etc.

A single-wafer-based technology called "SCREAM" was developed for one-mask or two-mask processes [3, 4]. In this technology, a trench is formed by DRIE and lateral etching is performed by dry isotropic release at the trench bottom, to form lateral MEMS structures. Following this scheme, enhanced isolation capability was realised by chemical vapor deposition of insulating "bus-bars" at the trench bottom [5].

Instead of dry etching release methods, it is known to perform lateral wet release by anisotropic etching of a (111) silicon wafer for the formation of single-wafer-based in-plane lateral MEMS [6, 7]. These above mentioned technologies have been mainly used for capacitive sensors and electrostatic actuators.

Note that the MEMS devices described above have not made use of piezoresistive devices. Although piezoresistive devices have been widely adopted in MEMS devices having a conventional vertical configuration and which are fabricated using conventional anisotropic wet etching and sandwiched bonding, etc., piezoresistive sensing has seldom been employed for MEMS devices with a laterally movable portion. This is because there is no straightforward processing technology available for integration of both piezoresistive sensors and electrostatic actuators on the trench-sidewalls in MEMS devices with laterally movable portions. It is also a challenging task to form electric lead-out connections from the sidewalls to the wafer surface

sufficiently precisely and ensure that piezoresistive sensing and electrostatic actuating elements on the trench sidewalls are electrically isolated from each other.

For these reasons, those few MEMS devices having laterally movable portions which use of piezoresistive sensors usually locate the piezoresistors on the top surface of laterally movable portion [8]. In this configuration the piezoresistors do not sense the stress at the sidewalls of the movable portion, where stress may be maximal, thereby resulting in low piezoresistive sensitivity.

It is true that an oblique ion implantation method has been proposed for the integration of piezoresistors on the trench-sidewall of lateral MEMS structure [9], but this oblique implantation is not a standard process. It requires that the wafer is inclined at a certain angle in the processing equipment during the implantation. For a cantilever structure, the oblique implantation would have to be processed twice (in order that piezoresistors are formed on both sides of the cantilever). For a square shaped structure, the oblique implementation would have to be performed 4 times. For a circular MEMS structure, uniform sidewall doping cannot be obtained even if the oblique implantation process is performed an unlimited number of times.

One particular difficulty in providing MEMS devices with piezoresistive sensors and electrostatic actuators is the creation of paths for electrical transfer between the wafer surface (where circuitry is located) and the side walls of the movable portion or its surrounding frame, while simultaneously providing adequate electrical isolation between adjacent elements formed on the side walls.

Summary of the Invention

The present invention aims to provide new and useful methods for producing MEMS devices, and in particular novel methods using a single homogenous wafer (i.e. single-wafer-based techniques) to produce MEMS devices comprising a portion which is movable laterally in-plane and having piezoresistive sensing elements and/or electrostatic actuator elements on trench sidewalls.

The invention further aims to provide new and useful MEMS devices produced using such methods.

The invention proposes in general terms that a doped region is formed in the upper surface of a substrate. A trench is formed in the substrate (e.g. by DRIE cutting) intersecting with the doped region and defining a portion of the substrate which is movable relatively to the rest of the substrate. Then diffusion of the dopant is effected into the trench walls, so that the some of the dopant moves onto the walls of the trench to create electrical elements (piezoresistor sensing elements and/or electrode elements for electrostatic actuation).

The electrical elements will still be in good electrical contact with the doped regions previously formed at the wafer surface, and thus there are good electrical paths between the electrical elements on the trench side-walls and respective portions of the surface of the substrate. This can be regarded as a "self-alignment" of the electrical elements and conductive doped regions of the substrate surface. The doped regions may in turn be connected to electrical lead-out paths formed of, say, aluminium.

Prior to the formation of the trench, electrically insulating elements are formed extending through the vertical depth of the laterally movable portion. The

trench intersects with these insulating elements, so that the insulating elements mutually insulate adjacent ones of the electrical elements (i.e. pairs of electrical elements on the same trench side-wall and on respective sides of the insulating elements). Conveniently, the insulating elements may be formed from silicon dioxide SiO_2, e.g. produced by oxidising polysilicon deposited into apertures in the surface of the substrate.

The dopant is of a first conductivity type (e.g. a p-type dopant) and the substrate of a second conductivity type (e.g. an n-type dopant). For example, the dopant may be boron, and the substrate may be arsenic doped. This means that between the electrical elements and the substrates is a p-n junction, which implies that the electrical elements are insulated from the substrate.

Typically, the substrate is a homogenous single wafer, such as n-type silicon. Normally the substrate surface is (100) oriented with the piezoresistivity along <110> orientation. However, if the piezoresistor direction is designed along <100> orientation, n-type dopant may be used for the sidewall diffusion instead of p-type one. Accordingly, a p-type substrate would be used instead of an n-type one in this case. For consistent trench-sidewall doping, the same type dopant is normally used for both the piezoresistors and the electrostatic actuators at the same device.

Thus, the invention makes it possible for the first time to realise the formation of piezoresistive sensors and electrostatic actuators on the trench sidewalls of a MEMS device with a laterally movable portion formed from a homogenous single wafer. It is believed that this possibility will be high valuable, particularly for 3-axis sensing with a self-calibration function, since such MEMS devices can be employed as advanced inertial sensors, resonators, etc.

In the simplest form, the movable portion may be an elongate cantilever which is arranged for motion in a single direction (e.g. in the plane of the wafer and transverse to a length direction of the cantilever). Alternatively, the movable portion may be formed to be capable of vibration in two transverse directions in the plane of the substrate. For example, the movable portion may be L-shaped or T-shaped and supported at one of its ends. In this case, the trench defining the movable portion extends in respective directions in different locations. The method of the invention can be used to form electrical elements in each of these locations. Thus, MEMS devices are fabricated which produce and/or measure motion in each of these two directions.

Furthermore, the principles of the invention can be applied in combination with existing techniques which produce piezoresistors and/or electrostatic actuators on the top surface of the wafer to produce MEMS devices in which the movable portion is movable in a direction transverse to the wafer surface. Optionally, the surface electrical elements can be produced before the electrical elements on the side walls of the trench.

Thus, the present method can be used to produce MEMS devices in which the movable portion is movable in 2- or 3-axes.

Brief Description of The Figures

Preferred features of the invention will now be described, for the sake of illustration only, with reference to the following figures in which:

Fig. 1, which is composed of Figs. 1(a) to 1(d), shows the steps of a technique proposed herein for forming electrical elements on the side walls of a trench in a MEMS;

Fig. 2 is a perspective, partially cut-away view of a MEMS device which is an embodiment of the invention;

Fig. 3, which is composed of Figs. 3(a) to 3(l), shows the process steps to produce the device of Fig. 2;

Fig. 4, which is composed of Figs. 4(a) to 4(d), is four SEM views of actual devices of the kind shown in Fig. 2;

Fig. 5 is an I-V plot of the electrical properties of the piezoresistors of the devices of Fig. 4;

Fig. 6 is an I-V plot illustrating breakthrough properties (including breakthrough voltage) between two mutually isolated actuating electrodes of the devices of Fig. 4;

Fig. 7, which is composed of Figs. 7(a) and 7(b), shows the piezoresistive output of the devices of Fig. 4 as a function of the actuating voltage and of its frequency respectively; and

Fig. 8 is a flow diagram of the main processing steps of the embodiment of Fig. 3.

Detailed Description of the embodiments

Referring to Fig. 1, a process proposed here is described for creating a MEMS device having a trench and including electrical elements in the side walls of the trench. Subsequently, with reference to Figs. 2 and 3 it is described how this technique can be used to produce a MEMS device which is an embodiment of the present invention, simply by producing a trench of a different shape which defines a laterally movable element.

Fig. 1 is composed of rows (a) to (d). In each row of the figure, the right part is a top view of a wafer and includes a dashed line. The left part of the row is a cross-sectional view along the corresponding line. The bottom part of Fig. 1 is a key indicating the meaning of the shading used in the figure.

The starting point of the method is a (100) n-type wafer 1. As shown in Fig. 1(a), short bar-shaped trenches 3 are formed in the wafer 1 using a DRIE process. The trenches 3 should be slightly deeper than the in-plane structure to be formed. The high aspect-ratio trenches 3 are partially refilled with LPCVD (low pressure chemical vapor deposition) polysilicon 5. Then, the poly silicon is thermally oxidized. By volume expansion of the oxidized poly silicon, the trenches are fully refilled and insulated by the SiO_2. This is the stage shown in Fig. 1(a).

Thermal oxidation is performed and then patterning is performed at the backside of the wafer (the bottom as shown in representations on the left of Fig. 1). Then, anisotropic wet etching is performed at backside until the bottom of SiO_2-refilled trench 3 is exposed. Subsequently the wafer is oxidized and patterned at its top side, and p^+ is selectively doped in regions 7 (e.g. by ion implantation or pre-deposition) and then is driven into the top surface (e.g. by a high temperature process which causes an oxidation on the surface). Then contact holes 9 are opened through the oxide generated in the drive-in process, as shown in Fig. 1(b).

Using photo-resist as a mask, structural trenches 11 are DRIE formed in the MEMS structure. The SiO2 layer at the backside provides the etching stop for the trench etching. The trenches 11 cut across the ends of the SiO2-refilled trenches 3 and the p^+ patterns 7. The device is then place in a boron rich atmosphere and, under high temperature conditions, boron diffuses into the sidewalls, to form piezoresistors and capacitive electrodes 13, as shown in Fig. 1(c). Since the trenches 11 cuts the ends of the SiO_2-refilled trenches and the p+ patterns, adjacent piezoresistors and capacitive electrodes 13 on the sidewall are electrically isolated by a combination of the insulated-trenches 5 and the boron-diffusion-formed p-n junctions along the sidewall. Electrical

transfer from the sidewall to wafer surface is achieved via the intersection between the regions 7 and 13.

Subsequently, aluminium interconnects 15 are formed by deposition followed by a lift-off technique, and the SiO_2 layer at the backside is stripped by plasma etching to release the MEMS structure. The completed structure is shown in Fig. 1(d).

We now turn to a use of the method described above for the creation of a MEMS device which is embodiment of the invention. The embodiment is shown in perspective view in Fig. 2, and is an integrated in-plane cantilever with piezoresistive sensing and capacitive actuating elements integrated on trench-sidewalls.

The embodiment is formed from a substrate 20 through which a trench 22 is formed to define a cantilever 21 surrounded by a frame 23. The upper surface of the substrate is thus partitioned into the upper surface of the cantilever 21 and the upper surface of the frame 23. The MEMS device is mirror symmetric about the length direction of the cantilever 21, but in Fig. 2 a nearside portion of the frame 23 is treated as transparent to explain the structure more clearly. The cantilever is free to vibrate in the direction marked in Fig. 2 as the "lateral moving direction", which is within the plane of the upper surface of the cantilever 21.

Some portions 25 of the upper surface of the substrate 20 have been doped with p+ dopant (i.e. boron). During the formation process (as described above) some of the doping atoms diffuse into the lateral surfaces of the cantilever 21 and of the cantilever base, where they produce a piezoresistor layer 27 for differential sensing. Furthermore, diffusion of the dopant into the

trench walls of the frame 23 produces electrostatic actuating plates 29 on the inwardly facing lateral surfaces of the frame for actuation of the cantilever 21.

Before the formation of the trench 22, SiO_2 elements 28 were formed within the substrate extending transverse to the surface (and corresponding to the SiO_2 bodies 5 of Fig. 1). In the completed MEMS device of Fig. 2 the piezoresistor layer 27 intersects with some of these SiO_2 elements 28, and is thus divided into separate piezoresistor sensors 25. Similarly, the electrostatic actuation plates intersect with others of the SiO_2 elements 28 and are divided into individual actuation electrodes 29. Lateral deflection of the cantilever 21 can be electro-statically driven by the electrodes 29 and measured by the piezorestive sensors 27 on the side walls. This kind of structure with both sensing and actuating functions can be used straightforwardly in many MEMS applications such as inertial sensors and resonators, etc.

The process steps to produce the MEMS device of Fig. 2 are described as follows with reference to Fig. 3. Items present in both Figs. 2 and 3 are labelled by the same reference numerals.

(1): The starting material for the fabrication process is a 4-inch (100) wafer with N-type substrate 20 doped at a level in the range 1 to 5Ω·cm. First, deep trenches 30 perpendicular to the substrate are etched by induction coupled plasma (ICP) DRIE (with Alcatel 601E etching system). The etching depth is 50μm-deep and 3.5μm-wide. After DRIE, the by-product polymer compound generated during the DRIE is stripped by cleaning sequence as follows: the wafer is wet cleaned with EKC265 solution at 70°C for 30 minutes. Then an oxygen-plasma etch of 10 minutes is used for dry cleaning. After the wafer 20 is cleaned, a 300nm-thick layer of silicon dioxide 31 is thermally grown on it. Then the trenches 30 are partly refilled with conformal poly-silicon 33 by LPCVD. The deposition is processed under 630°C for the thickness of 850nm.

The structure at this time is shown in Figs. 3(a) and 3(b), which show respectively cross-sections along the lines A-A' and B-B' in Fig. 2.

(2): The trenches 30 are fully refilled and SiO_2-insulated by volume expansion due to oxidization of the poly-silicon 33. To reduce thermal stress, the oxidation temperature is set as 950-1000°C. The insulated trench 30 is fully refilled without void throughout the trench cross-section to create SiO_2 bodies 28. During the poly silicon oxidation, a thick SiO_2 layer is also formed on both sides of the wafer. After patterning at backside, TMAH anisotropical etching from the backside thins down the substrate under the cantilever regions till the bottom of the insulated trenches 30 is reached. For a 400μm-thick wafer, the backside etching is about 350μm in depth. The SiO_2 layer covering the front wafer surface can protect the front side from the backside etching. Then, the frontside SiO_2 is stripped by buffered HF except for the areas of the insulated trenches 30. The structure at this time is shown in Figs. 3(c) and 3(d), which show respectively cross-sections along the lines A-A' and B-B' in Fig. 2.

(3): A 300nm-thick SiO_2 layer is thermally grown on both sides of the wafer. After patterning at front side, a region 25 of the front of the wafter is heavily doped with boron. As described above with reference to Fig. 2, the p^+ regions 25 provide electrical transference from the wafer surface to the sidewalls of the trenches produced later in the fabrication process. Either an implantation or a diffusion process can be used for this p^+ doping. During drive-in, a new layer of SiO_2 grows over the doping regions 25. The heavy doping level is set at a sheet resistance of about 20Ωcm. During the heavy doping, the backside is protected by the existing SiO_2 layer 37. The structure at this time is shown in Figs. 3(e) and 3(f), which show respectively cross-sections along the lines A-A' and B-B' in Fig. 2.

(4): Contact-holes 38 are opened in the SiO_2 layer for the latter aluminum interconnection. Then, 5.5μm-wide trenches 22 are produced using an ICP process with photo-resist 39 as the mask. This produces the <110>-oriented cantilever 21. The trench etching is stopped automatically at the backside SiO_2-layer 37. These structural trenches 22 are cut across the surface p+ areas 25 with the p^+ cross-sections exposed at the sidewall-surface for latter electric transference. The structural trenches 22 also cut cross the previously formed SiO_2-trenches 30. The oxide 28 filled in the insulated trenches 30 should be partially exposed outside of the trench-sidewalls so as to ensure electric isolation on the trench sidewall. The structure at this time is shown in Figs. 3(g) and 3(h), which show respectively cross-sections along the lines A-A' and B-B' in Fig. 2.

(5): The surface cleaning process used in step (1) is used again for stripping the deposited compound residues generated in the ICP process. Boron diffusion for the trench sidewalls is performed by placing the device in a boron-rich atmosphere at a predetermined temperature. The wafer surface and backside are protected from diffusion by the existing SiO_2 layers 35, 37 with the exception of the contact holes 38. The diffusion at the contact holes 38 has little influence as the p^+ areas are already heavily doped. After boron diffusion on the sidewalls, both piezoresistors 27 and self-testing electrodes 29 are formed on the trench-sidewalls and electrically isolated by combination of the SiO_2-insulation elements 28 as well as p-n junctions along the sidewalls formed by the boron-diffusion. The electric transference from trench sidewall to wafer surface is simultaneously completed via the overlaps between the sidewall diffusion regions 27, 29 and the surface p^+ doping regions 25. During the drive-in phase of the sidewall diffusion, nitrogen is first induced and switched to oxygen at the last minutes in order to grow a thin SiO_2 layer on the sidewall for surface passivation and protection of the sidewall

piezoresistors. The structure at this time is shown in Figs. 3(i) and 3(j), which show respectively cross-sections along the lines A-A' and B-B' in Fig. 2.

(6): Reactive ion etching (RIE) is used to remove the thin oxide layer in the contact holes 38 while the relatively thick oxide layer at other areas remains. Then aluminum is sputtered onto the structure and patterned with a photoresist lift-off technique to provide interconnections 40. After aluminum sintering, the cantilever 21 is freed by RIE stripping the SiO_2 layer 37 from the backside of the wafer. The structure at this time is shown in Figs. 3(k) and 3(l), which show respectively cross-sections along the lines A-A' and B-B' in Fig. 2.

Fig. 4 shows SEM images of a devices fabricated as described above. The lower resolution image Fig. 4(c) shows the overall cantilever structure. Fig. (d) shows the cantilever base area, and in particular two SiO_2 isolation bodies 28 near the base of the cantilever. Fig. 4(a) shows the tip of the cantilever, and Fig. 4(b) shows an intermediate region along the cantilever. Both views Fig. 4(a) and 4(b) show further SiO_2 isolation bodies 28.

We now turn to experiments characterising the devices pictured in Fig. 4.

Firstly, the electrical characteristics of the fabricated devices are evaluated. A negative electrical potential is supplied to the aluminium contacts of the piezoelectric elements 27 relative to the substrate. As shown in Fig. 5, the measured linear I-V property of the sidewall piezoresistor elements 27 indicates ohmic contact of the sidewall-to-surface electric transference. The sheet resistivity is about 200Ω.

The electrical isolation provided by the SiO_2-refilled trenches and the sidewall-diffused p-n junction is also evaluated. A potential difference is applied to two

adjacent electrodes 29, and the current between them is measured. The result is plotted on Fig. 5, which shows that the breakdown voltage is higher than 50V. Such an electrical isolation is good enough for most MEMS operations.

Additionally, the electro-mechanical performance of the fabricated cantilever is characterized. Firstly, a static measurement is performed in which a DC voltage is applied to electrostatically actuate the cantilever beam 21 and the piezoresistive response of the piezoresistors 27 is recorded and plotted in Fig. 7(a). As shown in Fig.7 (a), the measured piezoresistive output rises in proportion to the square of the actuating voltage, which agrees well with analytical predictions. Secondly, a dynamic test is performed, in which a differential AC voltage signal of $15\pm10\cos\omega t$ (V) is applied to the electrodes 29, and thus used to drive the cantilever beam. The measured piezoresistive response is plotted in Fig. 7(b), and shows a 3.2mV peak output at a resonant frequency of 96.6kHz. These results also match well with analytical predictions (shown in the dotted line).

The main method steps of the embodiment discussed above in relation to Fig. 3 are summarized in the flow diagram of Fig. 8.

Note that the embodiments described above employ both piezoresistive sensor elements and actuator elements. However, the invention is not limited in this respect, and alternative useful devices may be formed in which only one of these two types of elements is formed. An advantage of using both is that it makes possible a self-calibration in which the sensor elements detect a motion caused by the actuator elements, so that the properties of the device can be measured.

Although only a single embodiment of the invention has been illustrated in detail, many variations of are possible within the scope of the invention, as will be clear to a skilled reader. For example, whereas the cantilever 21 of Fig. 2 is arranged for motion in a single direction, in other embodiments the movable portion of the device may be arranged for motion in 2 directions in the plane of the substrate (e.g. by an appropriate shaping of the trench 22, and provision of the piezoresistors and actuating electrodes at locations along the trench which respectively sense and produce these two motions) and/or for motion also in a direction out of the plane of the substrate (e.g. using motion sensors and/or actuating elements on the surface of the substrate). In this case, the cantilever may be formed with a more complex configuration, e.g. comprising a comb, beam and/or plate.

Devices in which the movable portion can be moved in 2 or 3 directions are useful, for example, for multi-axis sensing applications. The design of movable portions which are capable of such motion are known in the literature, and these designs may readily be combined with the techniques disclosed herein for formation of the sensor elements and actuator elements.

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Claims

1. A process for forming a MEMS device including a portion movable laterally in the plane of the device, the method including the steps of:

forming electrically insulating elements extending through a substrate of a first conductivity type;

doping regions of the surface of the substrate with a dopant of a second conductivity type opposite to the first conductivity type, to form doped regions of the surface of the substrate;

forming at least one trench in the substrate intersecting with the electrically insulating elements and the doping regions and defining the movable portion of the substrate which is arranged for movement in the plane of the surface of the substrate, the electrically insulating elements extending through the thickness of the laterally movable portion; and

effecting diffusion of dopant of the second conductivity type into the side walls of the at least one trench to form one or more piezoelectric sensing elements for detecting motion of the movable portion of the substrate and/or one or more electrostatic actuator elements for moving the movable portion of the substrate, whereby electric contact is achieved between the doped regions on the trench side walls and the doped regions on the surface by intersection of the doped regions on the trench side walls with the doped regions on the surface.

2. A method according to claim 1 in which the at least one trench is formed by DRIE cutting.

3. A method according to claim 1 or claim 2 in which the substrate is a homogenous single wafer.

4. A method according to any preceding claim in which the insulting elements are formed by producing one or more apertures in the substrate and filling the apertures with insulating material.

5. A method according to claim 4 in which, at the time the apertures are formed, the apertures do not extend through the entire thickness of the substrate, and in which, following the formation of the insulating elements, the substrate is reduced in thickness proximate the insulating elements until the insulating elements are exposed at the thin-downed portion of the substrate.

6. A method according to claim 4 or claim 5 in which the apertures in the substrate are filled with insulating material by the steps of depositing polysilicon into the one or more apertures and oxidising the polysilicon.

7. A method according to any of claims 1 to 6 in which, following the formation of the trench, the insulating elements protrude into the trench from the side walls of the trench.

8. A method according to any preceding claim in which the movable portion is a cantilever movable in a single direction in the plane of the substrate.

9. A method according to any of claims 1 to 7 in which the movable portion is moveable in multiple axis directions.

10. A method according to any preceding claim further including forming one or more piezoresistor elements in the surface of the wafer.

11. A MEMS device produced by a method according to any preceding claim.

12. A MEMS device including a substrate of a first conductivity type,

the substrate including at least one trench extending through the substrate, intersecting with the one or more insulating elements, and defining a portion of the substrate which is movable laterally in the plane of the substrate and a frame surrounding the substrate,

one or more insulating elements extending though the whole thickness of the movable portion of the substrate,

the surface of the substrate including one or more regions doped with a dopant to have a second conductivity type opposite to the first conductivity type,

the side-walls of the at least one trench including one or more piezoresistive sensing elements and/or one or more electrostatic actuator elements formed by diffusion of dopant of the second conductivity type into the side walls of the at least one trench, the piezoresistive sensing elements and/or electrostatic actuator elements being mutually electrically isolated by the insulating elements and electrically connected to corresponding ones of the doped regions on the surface of the substrate.

13. A MEMS device according to claim 12 in which the movable portion is an elongate cantilever arranged for motion in a single direction in the plane of the wafer and transverse to the length direction of the cantilever.

14. A MEMS device according to claim 12 in which the movable portion is arranged for in-plane and out-plane motions with respect to the wafer.

15. A MEMS device according to any of claims 12 or14 further including one or more sensing elements on the surface of the wafer.

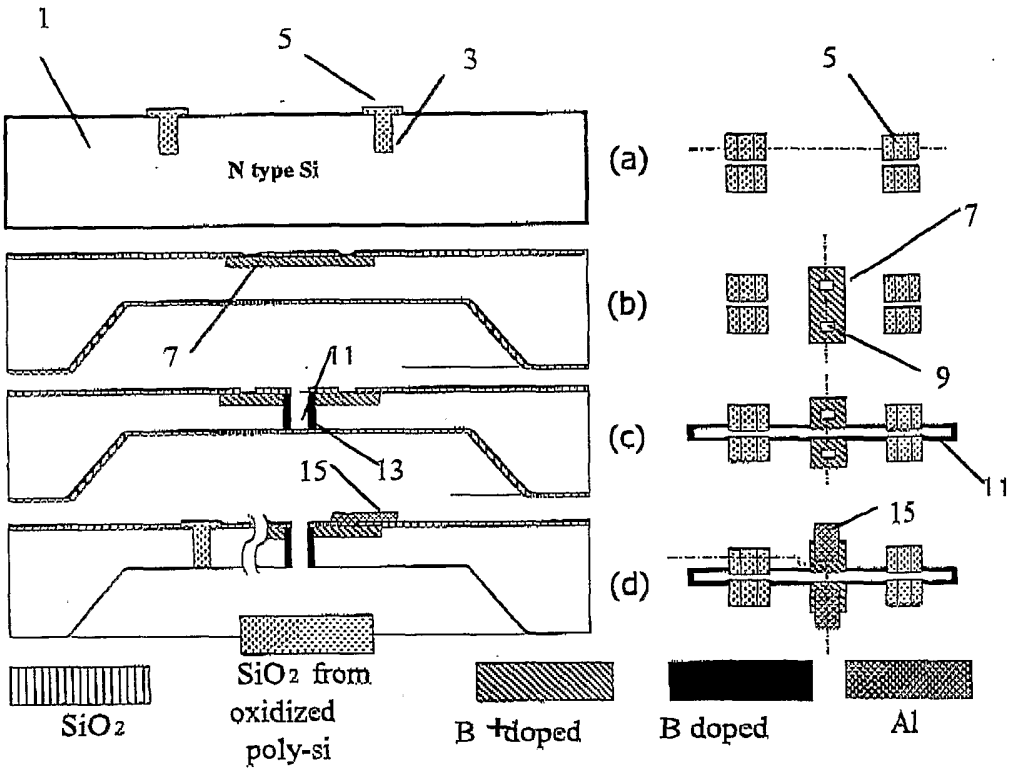
1
5
3
N type Si
(a)
5
7
(b)
7
11
9
(c)
15
13
11
(d)
15
SiO2
SiO2 from oxidized poly-si
B +doped
B doped
Al

Fig. 1

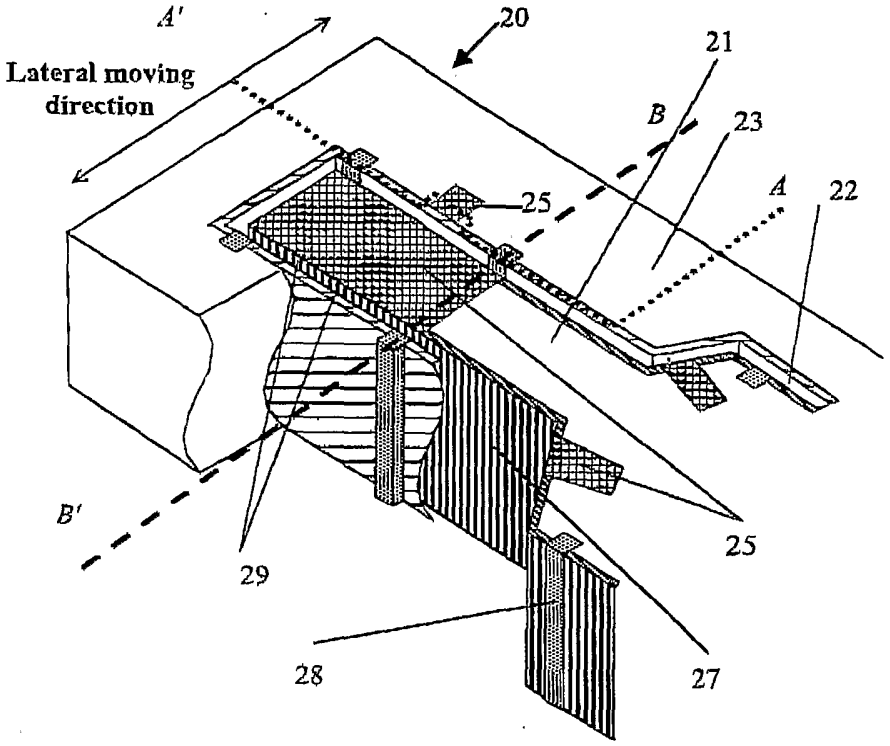

Fig. 2

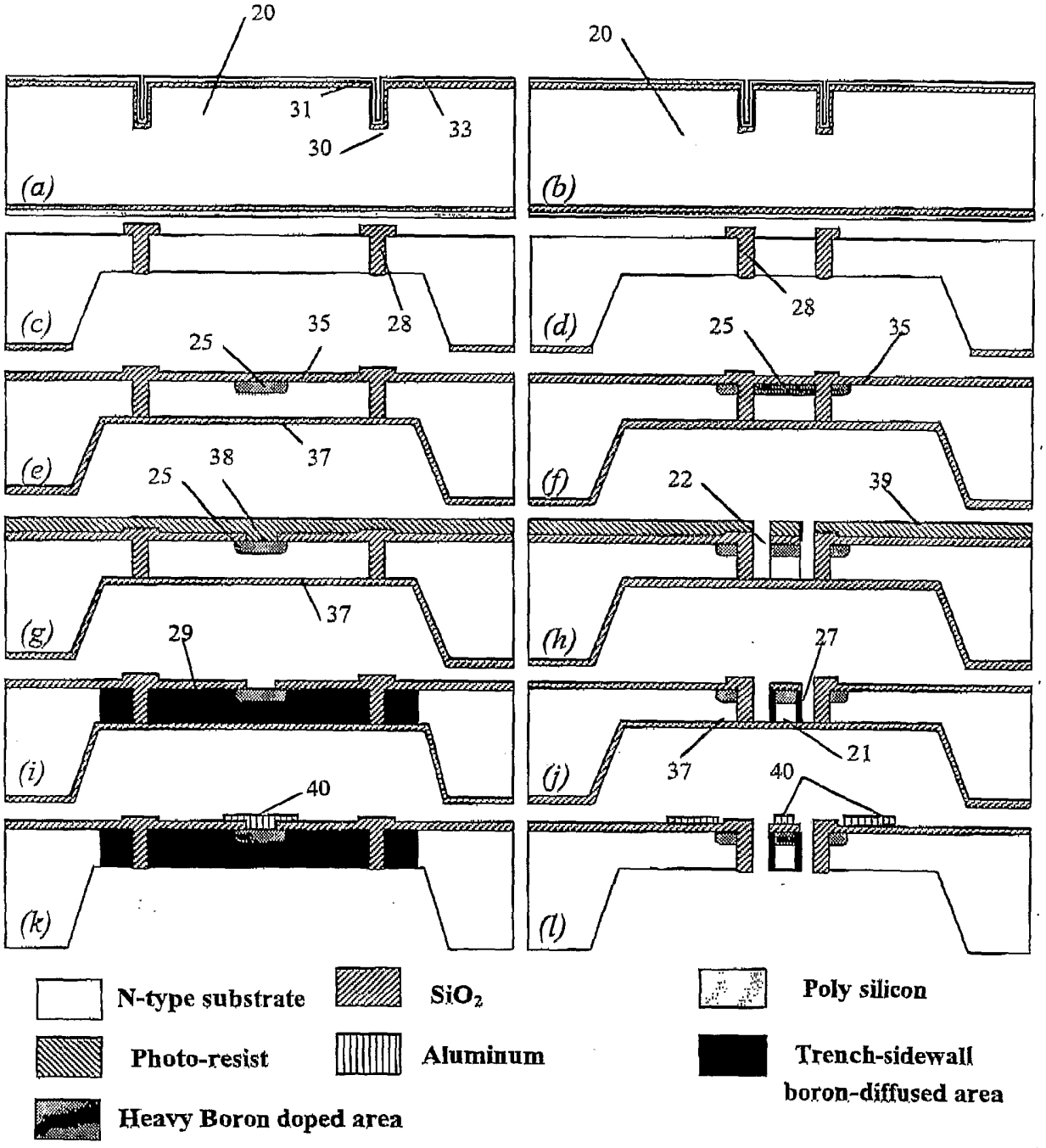
20
31
33
30
(a)
20
(b)
(c)
35
28
25
(d)
28
25
35
(e)
38
37
25
(f)
22
39
(g)
37
29
(h)
27
(i)
40
(j)
37
40
21
(k)
(l)
N-type substrate
SiO2
Poly silicon
Photo-resist
Aluminum
Trench-sidewall boron-diffused area
Heavy Boron doped area

Fig. 3

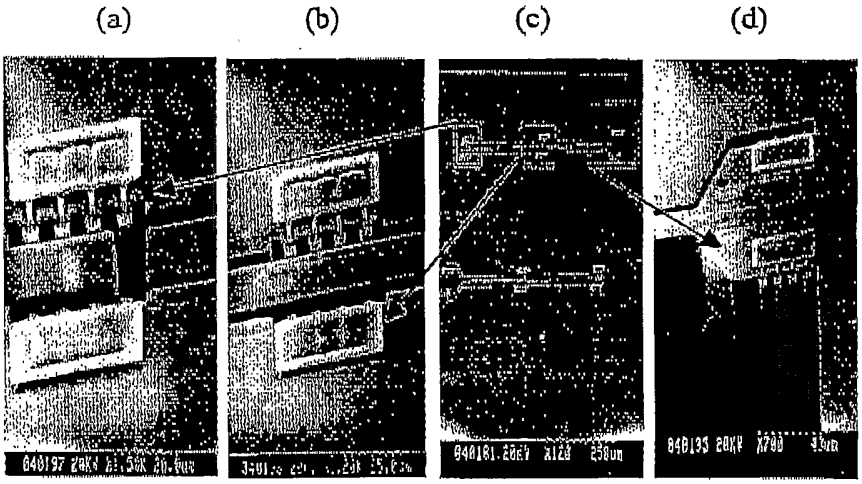

Fig. 4

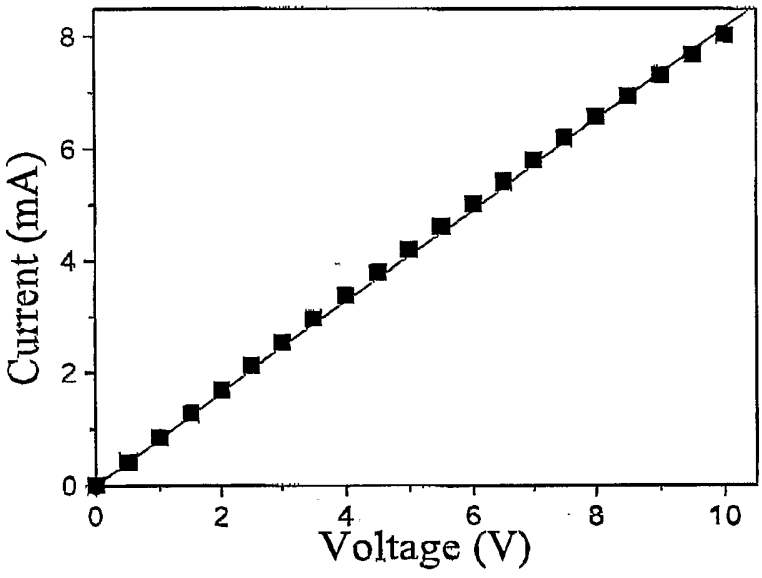

Fig. 5

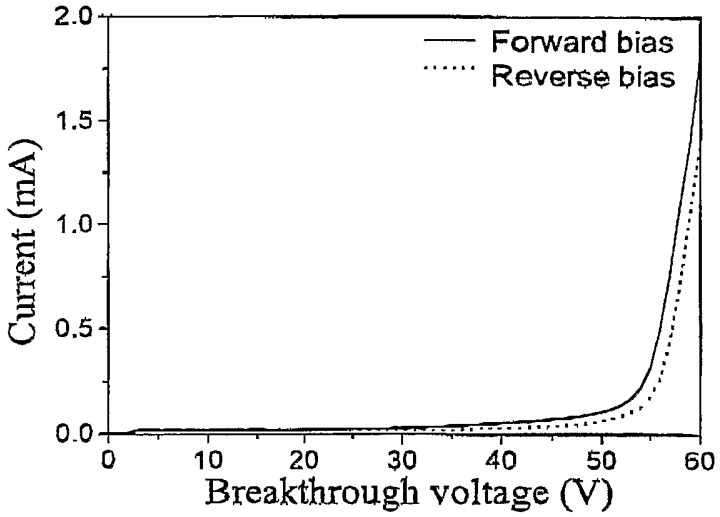
Forward bias
Reverse bias
Current (mA)
Breakthrough voltage (V)
2.0
1.5
1.0
0.5
0.0
0
10
20
30
40
50
60

Fig. 6

(a) (b)

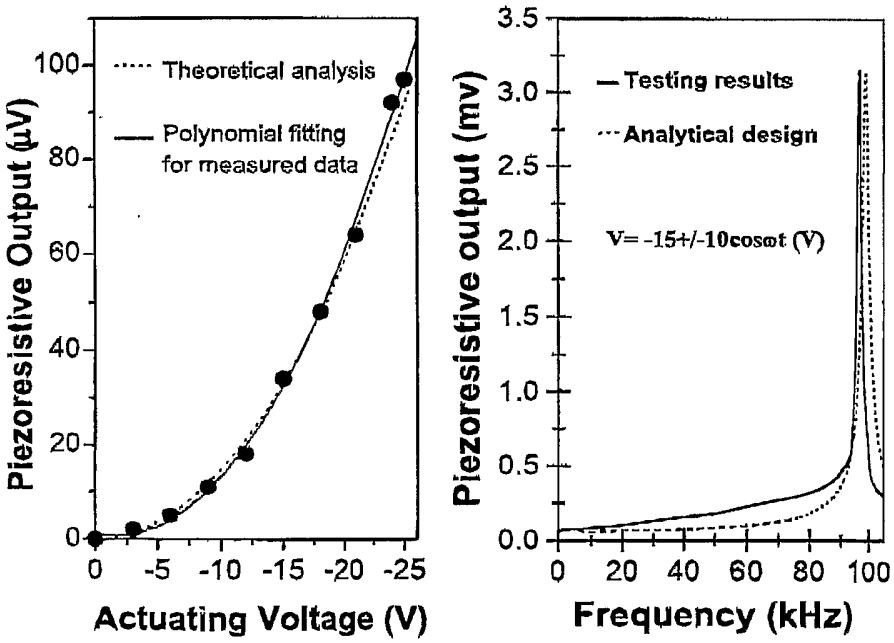
Theoretical analysis
Polynomial fitting for measured data
Piezoresistive Output (μV)
Actuating Voltage (V)
100
80
60
40
20
0
0 -5 -10 -15 -20 -25
Testing results
Analytical design
V= -15+/-10cosωt (V)
Piezoresistive output (mv)
Frequency (kHz)
3.5
3.0
2.5
2.0
1.5
1.0
0.5
0.0
0 20 40 60 80 100

Fig. 7

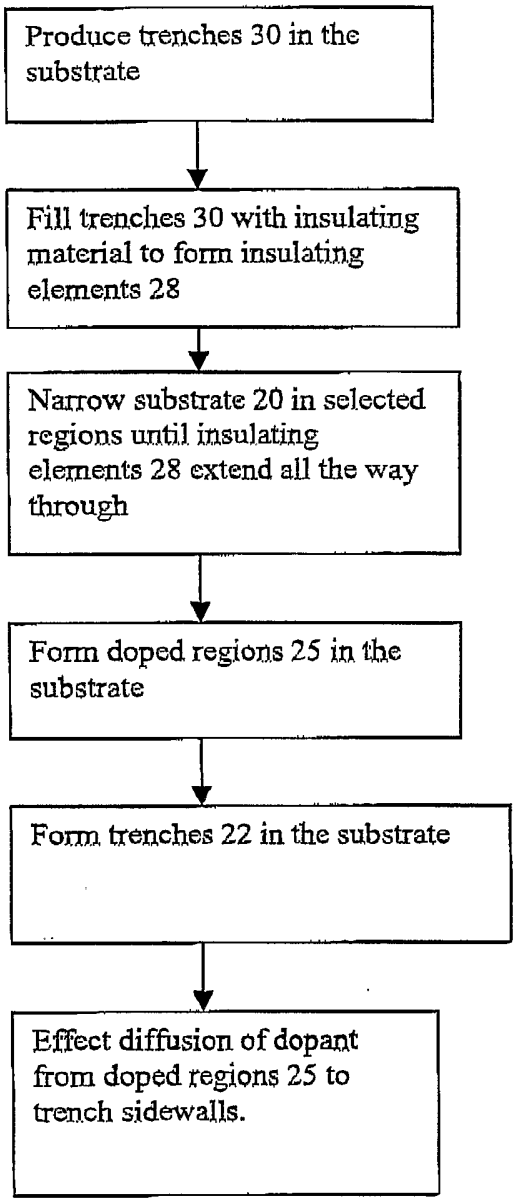
Produce trenches 30 in the substrate
Fill trenches 30 with insulating material to form insulating elements 28
Narrow substrate 20 in selected regions until insulating elements 28 extend all the way through
Form doped regions 25 in the substrate
Form trenches 22 in the substrate
Effect diffusion of dopant from doped regions 25 to trench sidewalls.

Fig. 8

INTERNATIONAL SEARCH REPORT

International application No.
PCT/CN2004/001437

A. CLASSIFICATION OF SUBJECT MATTER

IPC[7] H01L 21/70 H01L 21/00 B81B 7/02 B81C 1/00

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC[7] H01L 21/70 H01L 21/00 B81B 7/02 B81C 1/00

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

China Patent Documentation (From Apr. 1, 1985)

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

WPI EPODOC PAJ:MEMS DRIE trench insulat+ oxid+ polysilicon

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages			Relevant to claim No.
E	CN1570651A	26. Jan. 2005	see entire document	1-15
Y	CN1376925A	30. Oct.2002	see entire document	1-15
Y	CN1516257A	28. Jul. 2004	see entire document	1-15
A	WO 02/084374 A1	24. Oct.2002	see entire document	1-15
A	WO 99/36948 A1	22. Jul.1999	see entire document	1-15
A	US6291875 B1	18. Sep.2001	see entire document	1-15

☐ Further documents are listed in the continuation of Box C. ☒ See patent family annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim (S) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&"document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
01. Aug. 2005(01.08.2005)	22 · SEP 2005 (22 · 09 · 2005)
Name and mailing address of the ISA/CN The State Intellectual Property Office, the P.R.China 6 Xitucheng Rd., Jimen Bridge, Haidian District, Beijing, China 100088 Facsimile No. 86-10-62019451	Authorized officer Nie Shaoyan Telephone No. 86-10-62084856

Form PCT/ISA/210 (second sheet) (April 2005)

INTERNATIONAL SEARCH REPORT
Information on patent family members

International application No.
PCT/CN2004/001437

Patent Documents referred in the Report	Publication Date	Patent Family	Publication Date
CN1570651A	26. Jan. 2005	NONE	
CN1376925A	30. Oct.2002	NONE	
CN1516257A	28. Jul. 2004	NONE	
WO 02/084374 A1	24. Oct.2002	US2002046985 A1	25. Apr. 2002
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		US6819820 B1	16. Nov. 2004
WO 99/36948 A1	22. Jul.1999	US6756247 B1	29. Jun. 2004
		EP1062685 A1	27. Dec. 2000
		JP2002509808 T	02. Apr. 2002
US6291875 B1	18. Sep.2001	NONE	