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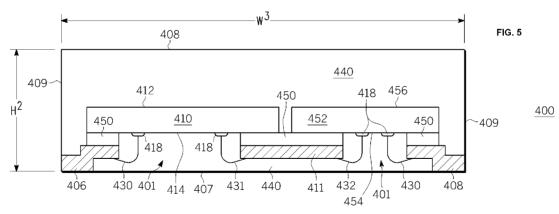
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(57) Abstract: Methods and apparatus are provided for decreasing the size of Quad Flat No-Lead (QFN) packages (300, 400) down to chip-scale packages. Such QFN packages include a first semiconductor chip (310, 410), a plurality of recessed leads (306, 406, 408, 411) having mold lock features, and a mold material 340, 440 substantially encasing all sides of the semiconductor chip. An active surface (314, 414) of the semiconductor chip is oriented toward a mounting side (307, 407) of the QFN package, and a plurality of wire bonds 330, 430 disposed between the active surface and the mounting side couple the active side to the leads. The QFN packages may also include a second semiconductor chip (452) coupled to a plurality of leads (408) and to the first semiconductor chip via wire bonds (431, 432) in a manner similar to the first semiconductor chip.



## INTERNATIONAL SEARCH REPORT

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C. DOC	JMENTS CONSIDERED TO BE RELEVANT		
Category *	Citation of document, with indication, where a		Relevant to claim No.
X	US 6,075,284 A (CHOI et al) 13 June 2000 (13.06.2000), Figure 6a		1-8,17-19
Α	US 6,189,171 A (HUANG et al) 06 March 2001 (06.03.2001), Figure 7		1-23
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Further documents are listed in the continuation of Box C. See patent family annex.			
"A" document	pecial categories of cited documents:  defining the general state of the art which is not considered to be of relevance	"T" later document published after the inte date and not in conflict with the applic principle or theory underlying the inve	ation but cited to understand the
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