(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
9 November 2006 (09.11.2006)

PCT

(10) International Publication Number
WO 2006/118632 A1

(51) International Patent Classification:
H01L 29/778 (2006.01) *H01L 29/20* (2006.01)
H01L 29/812 (2006.01) *H01L 29/205* (2006.01)
H01L 29/10 (2006.01)

(21) International Application Number:
PCT/US2006/006146

(22) International Filing Date:
23 February 2006 (23.02.2006)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
11/118,575 29 April 2005 (29.04.2005) US

(71) Applicant *(for all designated States except US)*: **CREE, INC.** [US/US]; 4600 Silicon Drive, Durham, North Carolina 27703 (US).

(72) Inventor; and
(75) Inventor/Applicant *(for US only)*: **SAXLER, Adam William** [US/US]; 525 Beaver Dam Run, Durham, North Carolina 27703 (US).

(74) Agent: **MYERS BIGEL SIBLEY & SAJOVEC, P.A.**; P.o. Box 37428, Raleigh, North Carolina 27627 (US).

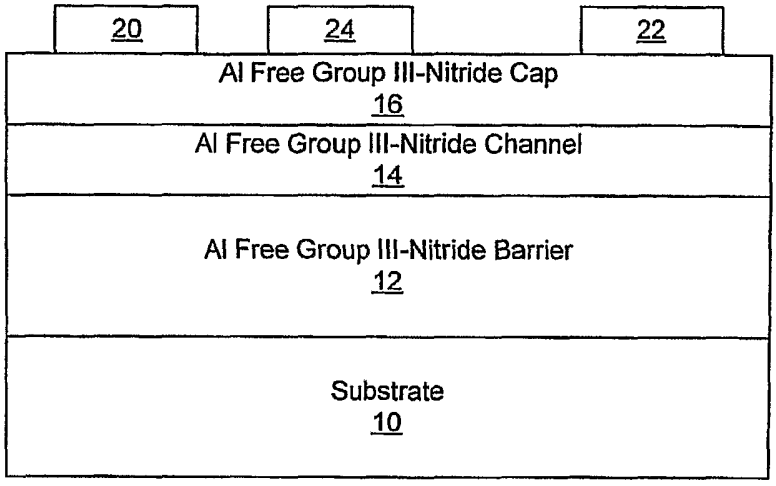
(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BW, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KN, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, LY, MA, MD, MG, MK, MN, MW, MX, MZ, NA, NG, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RU, SC, SD, SE, SG, SK, SL, SM, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, YU, ZA, ZM, ZW.

(84) Designated States *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IS, IT, LT, LU, LV, MC, NL, PL, PT, RO, SE, SI, SK, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Published:
— *with international search report*
— *before the expiration of the time limit for amending the claims and to be republished in the event of receipt of amendments*

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

(54) Title: ALUMINUM FREE GROUP III-NITRIDE BASED HIGH ELECTRON MOBILITY TRANSISTORS AND METHODS OF FABRICATING SAME



(57) Abstract: Aluminum free high electron mobility transistors (HEMTs) and methods of fabricating aluminum free HEMTs are provided. In some embodiments, the aluminum free HEMTs include an aluminum free Group III-nitride barrier layer, an aluminum free Group III-nitride channel layer on the barrier layer and an aluminum free Group III-nitride cap layer on the channel layer.

WO 2006/118632 A1

ALUMINUM FREE GROUP III-NITRIDE BASED HIGH ELECTRON MOBILITY TRANSISTORS AND METHODS OF FABRICATING SAME

FIELD OF THE INVENTION

The present invention relates to semiconductor devices and, more particularly, to transistors that incorporate nitride-based active layers.

BACKGROUND

Materials such as silicon (Si) and gallium arsenide (GaAs) have found wide application in semiconductor devices for lower power and (in the case of Si) lower frequency applications. These, more familiar, semiconductor materials may not be well suited for higher power and/or high frequency applications, however, because of their relatively small bandgaps (*e.g.*, 1.12 eV for Si and 1.42 for GaAs at room temperature) and/or relatively small breakdown voltages.

In light of the difficulties presented by Si and GaAs, interest in high power, high temperature and/or high frequency applications and devices has turned to wide bandgap semiconductor materials such as silicon carbide (2.996 eV for alpha SiC at room temperature) and the Group III nitrides (*e.g.*, 3.36 eV for GaN at room temperature). These materials, typically, have higher electric field breakdown strengths and higher electron saturation velocities as compared to gallium arsenide and silicon.

A device of particular interest for high power and/or high frequency applications is the High Electron Mobility Transistor (HEMT), which, in certain cases, is also known as a modulation doped field effect transistor (MODFET). These devices may offer operational advantages under a number of circumstances because a two-dimensional electron gas (2DEG) is formed at the heterojunction of two semiconductor materials with different bandgap energies, and where the smaller bandgap material has a higher electron affinity. The 2DEG is an accumulation layer in the undoped ("unintentionally doped"), smaller bandgap material and can contain a very high sheet electron concentration in excess of, for example, 10^{13} carriers/cm^2. Additionally, electrons that originate in the wider-bandgap semiconductor transfer to

the 2DEG, allowing a high electron mobility due to reduced ionized impurity scattering.

This combination of high carrier concentration and high carrier mobility can give the HEMT a very large transconductance and may provide a strong performance advantage over metal-semiconductor field effect transistors (MESFETs) for high-frequency applications.

High electron mobility transistors fabricated in the gallium nitride/aluminum gallium nitride (GaN/AlGaN) material system have the potential to generate large amounts of RF power because of the combination of material characteristics that includes the aforementioned high breakdown fields, their wide bandgaps, large conduction band offset, and/or high saturated electron drift velocity. A major portion of the electrons in the 2DEG is attributed to polarization in the AlGaN. HEMTs in the GaN/AlGaN system have already been demonstrated. U.S. Patents 5,192,987 and 5,296,395 describe AlGaN/GaN HEMT structures and methods of manufacture. U.S. Patent No. 6,316,793, to Sheppard et al., which is commonly assigned and is incorporated herein by reference, describes a HEMT device having a semi-insulating silicon carbide substrate, an aluminum nitride buffer layer on the substrate, an insulating gallium nitride layer on the buffer layer, an aluminum gallium nitride barrier layer on the gallium nitride layer, and a passivation layer on the aluminum gallium nitride active structure.

Conventional HEMTs typically have an AlGaN layer on a GaN channel layer. However, the presence of aluminum in the active region of the device may reduce the reliability of the device as a result of oxidation effects, dislocation related pits and/or the presence of DX centers.

SUMMARY OF THE INVENTION

Some embodiments of the present invention provide high electron mobility transistors (HEMTs) and methods of fabricating HEMTs that include an aluminum free Group III-nitride barrier layer, an aluminum free Group III-nitride channel layer on the barrier layer and an aluminum free Group III-nitride cap layer on the channel layer. In some embodiments of the present invention, the barrier layer comprises a doped Group III-nitride region adjacent the aluminum free Group III-nitride channel layer. An undoped Group III-nitride layer may also be provided disposed between the doped Group III-nitride region and the channel layer.

In additional embodiments of the present invention, the cap layer comprises a first doped Group III-nitride region adjacent the aluminum free Group III-nitride channel layer. An undoped Group III-nitride layer may be disposed between the first doped Group III-nitride region and the channel layer.

In some embodiments of the present invention, the barrier layer comprises a GaN layer, the channel layer comprises an InGaN layer and the cap layer comprises a GaN layer. The barrier layer may have a thickness of from about 0.1 μm to about 1000 μm, the channel layer may have a thickness of from about 1 nm to about 20 nm and the cap layer may have a thickness of from about 5 nm to about 100 nm. The InGaN layer may have a percentage of indium of from about 1 to about 100 percent.

In additional embodiments of the present invention, a first doped GaN layer is disposed between the GaN barrier layer and the InGaN channel layer. The first doped GaN layer may comprise a Si, Sn, O and/or Ge doped GaN layer. The first doped GaN layer may have a thickness of from about 0.2 nm to about 10 nm. The first doped GaN layer may have a dopant concentration of from about 1×10^{16} cm^{-3} to about 1×10^{21} cm^{-3}. A first undoped GaN layer may be disposed between the first doped GaN layer and the InGaN channel layer. The first undoped GaN layer may have a thickness of from about 0.3 nm to about 5 nm.

In further embodiments of the present invention, a first doped GaN layer is disposed between the GaN cap layer and the InGaN channel layer. The first doped GaN layer disposed between the GaN cap layer and the InGaN channel layer may comprise a Si, Sn, O and/or Ge doped GaN layer. The first doped GaN layer disposed between the GaN cap layer and the InGaN channel layer may have a thickness of from about 0.2 nm to about 10 nm. The first doped GaN layer disposed between the GaN cap layer and the InGaN channel layer may have a dopant concentration of from about 1×10^{16} cm^{-3} to about 1×10^{21} cm^{-3}. A first undoped GaN layer may be disposed between the first doped GaN layer and the InGaN channel layer. The first undoped GaN layer disposed between the first doped GaN layer and the InGaN layer may have a thickness of from about 0.3 nm to about 5 nm. A second doped GaN layer may be disposed between the GaN barrier layer and the InGaN channel layer. The second doped GaN layer disposed between the GaN barrier layer and the InGaN channel layer may comprise a Si, Sn, O and/or Ge doped GaN layer. The second doped GaN layer disposed between the GaN barrier layer and the InGaN channel

layer may have a thickness of from about 0.2 nm to about 10 nm. The second doped GaN layer disposed between the GaN barrier layer and the InGaN channel layer may have a dopant concentration of from about 1 x 10^{16} cm^{-3} to about 1 x 10^{21} cm^{-3}. A second undoped GaN layer may be disposed between the second doped GaN layer and the InGaN channel layer. The second undoped GaN layer may have a thickness of from about 0.3 nm to about 5 nm.

In additional embodiments of the present invention, an InGaN layer is provided on the GaN cap layer opposite the InGaN channel layer. The InGaN layer on the GaN cap layer opposite the InGaN channel layer may have a thickness of from about 0.3 nm to about 100 nm.

In some embodiments of the present invention, a metal semiconductor field effect transistor (MESFET) is provided.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 is a cross-section of an aluminum free Group III-nitride based HEMT according to some embodiments of the present invention.

Figure 2 is a cross-section of an aluminum free GaN based HEMT according to some embodiments of the present invention.

Figures 3A through **3D** are cross-sections of aluminum free GaN based HEMTs according to further embodiments of the present invention.

Figures 4A through **4N** are graphs of carrier concentration and band diagrams from simulation models of transistors according to some embodiments of the present invention.

DETAILED DESCRIPTION OF EMBODIMENTS OF THE INVENTION

The present invention now will be described more fully hereinafter with reference to the accompanying drawings, in which embodiments of the invention are shown. However, this invention should not be construed as limited to the embodiments set forth herein. Rather, these embodiments are provided so that this disclosure will be thorough and complete, and will fully convey the scope of the invention to those skilled in the art. In the drawings, the thickness of layers and regions are exaggerated for clarity. Like numbers refer to like elements throughout. As used herein the term "and/or" includes any and all combinations of one or more of the associated listed items.

The terminology used herein is for the purpose of describing particular embodiments only and is not intended to be limiting of the invention. As used herein, the singular forms "a", "an" and "the" are intended to include the plural forms as well, unless the context clearly indicates otherwise. It will be further understood that the terms "comprises" and/or "comprising," when used in this specification, specify the presence of stated features, integers, steps, operations, elements, and/or components, but do not preclude the presence or addition of one or more other features, integers, steps, operations, elements, components, and/or groups thereof.

It will be understood that when an element such as a layer, region or substrate is referred to as being "on" or extending "onto" another element, it can be directly on or extend directly onto the other element or intervening elements may also be present. In contrast, when an element is referred to as being "directly on" or extending "directly onto" another element, there are no intervening elements present. It will also be understood that when an element is referred to as being "connected" or "coupled" to another element, it can be directly connected or coupled to the other element or intervening elements may be present. In contrast, when an element is referred to as being "directly connected" or "directly coupled" to another element, there are no intervening elements present. Like numbers refer to like elements throughout the specification.

It will be understood that, although the terms first, second, etc. may be used herein to describe various elements, components, regions, layers and/or sections, these elements, components, regions, layers and/or sections should not be limited by these terms. These terms are only used to distinguish one element, component, region, layer or section from another region, layer or section. Thus, a first element, component, region, layer or section discussed below could be termed a second element, component, region, layer or section without departing from the teachings of the present invention.

Furthermore, relative terms, such as "lower" or "bottom" and "upper" or "top," may be used herein to describe one element's relationship to another elements as illustrated in the Figures. It will be understood that relative terms are intended to encompass different orientations of the device in addition to the orientation depicted in the Figures. For example, if the device in the Figures is turned over, elements described as being on the "lower" side of other elements would then be oriented on "upper" sides of the other elements. The exemplary term "lower", therefore,

encompasses both an orientation of "lower" and "upper," depending of the particular orientation of the figure. Similarly, if the device in one of the figures is turned over, elements described as "below" or "beneath" other elements would then be oriented "above" the other elements. The exemplary terms "below" or "beneath" can, therefore, encompass both an orientation of above and below.

Embodiments of the present invention are described herein with reference to cross-section illustrations that are schematic illustrations of idealized embodiments of the present invention. As such, variations from the shapes of the illustrations as a result, for example, of manufacturing techniques and/or tolerances, are to be expected. Thus, embodiments of the present invention should not be construed as limited to the particular shapes of regions illustrated herein but are to include deviations in shapes that result, for example, from manufacturing. For example, an etched region illustrated as a rectangle will, typically, have tapered, rounded or curved features. Thus, the regions illustrated in the figures are schematic in nature and their shapes are not intended to illustrate the precise shape of a region of a device and are not intended to limit the scope of the present invention.

Unless otherwise defined, all terms (including technical and scientific terms) used herein have the same meaning as commonly understood by one of ordinary skill in the art to which this invention belongs. It will be further understood that terms, such as those defined in commonly used dictionaries, should be interpreted as having a meaning that is consistent with their meaning in the context of the relevant art and will not be interpreted in an idealized or overly formal sense unless expressly so defined herein.

It will also be appreciated by those of skill in the art that references to a structure or feature that is disposed "adjacent" another feature may have portions that overlap or underlie the adjacent feature.

Embodiments of the present invention provide aluminum free nitride-based HEMTs such as Group III-nitride based devices. As used herein, the term "Group III nitride" refers to those semiconducting compounds formed between nitrogen and the elements in Group III of the periodic table, gallium (Ga), and/or indium (In). As is well understood by those in this art, the Group III elements can combine with nitrogen to form binary (*e.g.*, GaN), ternary (*e.g.*, InGaN), and quaternary compounds. These compounds all have empirical formulas in which one mole of nitrogen is combined

with a total of one mole of the Group III elements. Accordingly, formulas such as $In_xGa_{1-x}N$ where $0 \leq x \leq 1$ are often used to describe them.

Furthermore, as used herein, aluminum free refers to the absence of Al intentionally incorporated into active layers of the Group III-nitride based device. For example, in some embodiments a region or layer with less than about 1% Al may be considered aluminum free. Thus, an active layer of a device may be Al free even if some Al is present in the active layer, for example, through unintentional incorporation by contamination during fabrication. Active layers of a device are the layers of the device where the 2DEG is formed and layers disposed between the layers where the 2DEG is formed and the source, drain and/or gate contacts and/or contact layers (*i.e.* layers on which a contact is directly formed) of the device. Aluminum is not, however, intentionally incorporated in the layers that form the 2DEG. Accordingly, in some embodiments of the present invention, Al may be present in layers between the layers that form the 2DEG and a substrate, in contacts and/or in the substrate. For example, Al may be in the substrate, nucleation and/or buffer layers and/or the ohmic contacts.

Figure 1 illustrates a HEMT structure according to some embodiments of the present invention. As seen in **Figure 1**, a substrate **10** is provided on which Group III-nitride based devices may be formed. In particular embodiments of the present invention, the substrate **10** may be a silicon carbide (SiC) substrate that may be, for example, 4H polytype of silicon carbide. Other silicon carbide candidate polytypes include the 3C, 6H, and 15R polytypes. In particular embodiments of the present invention, the substrate **10** may be semi-insulating. The term "semi-insulating" is used descriptively rather than in an absolute sense. In particular embodiments of the present invention, the silicon carbide bulk crystal has a resistivity equal to or higher than about $1x10^5$ Ω-cm at room temperature. In other embodiments of the present invention, the substrate **10** may be conductive.

Optional buffer, nucleation and/or transition layers (not shown) may be provided on the substrate **10**. For example, an AlN buffer layer may be provided to provide an appropriate crystal structure transition between the silicon carbide substrate and the remainder of the device. Additionally, strain balancing transition layer(s) may also be provided as described, for example, in commonly assigned U.S. Patent Publication No. 2003/0102482A1, filed July 19, 2002 and published June 5,

2003, and entitled "STRAIN BALANCED NITRIDE HETROJUNCTION TRANSISTORS AND METHODS OF FABRICATING STRAIN BALANCED NITRIDE HETEROJUNCTION TRANSISTORS," and/or United States Patent No. 6,841,001, entitled "STRAIN COMPENSATED SEMICONDUCTOR STRUCTURES AND METHODS OF FABRICATING STRAIN COMPENSATED SEMICONDUCTOR STRUCTURES," the disclosures of which are incorporated herein by reference as if set forth fully herein.

Appropriate SiC substrates are manufactured by, for example, Cree, Inc., of Durham, N.C., the assignee of the present invention, and methods for producing are described, for example, in U. S. Patent Nos. Re. 34,861; 4,946,547; 5,200,022; and 6,218,680, the contents of which are incorporated herein by reference in their entirety. Similarly, techniques for epitaxial growth of Group III nitrides have been described in, for example, U. S. Patent Nos. 5,210,051; 5,393,993; 5,523,589; and 5,592,501, the contents of which are also incorporated herein by reference in their entirety.

Although silicon carbide may be used as a substrate material, embodiments of the present invention may utilize any suitable substrate, such as sapphire, aluminum nitride, aluminum gallium nitride, gallium nitride, silicon, GaAs, LGO, ZnO, LAO, InP and the like. In some embodiments, an appropriate buffer layer also may be formed. For example, some embodiments of the present invention may utilize thick semi-insulating or insulating Group III-nitride layers and/or conducting substrates or layers as described in United States Patent Application Serial No. _____ (Attorney Docket No. 5308-551), filed April 11, 2005 and entitled "COMPOSITE SUBSTRATES OF CONDUCTIVE AND INSULTATING OR SEMI-INSULATING GROUP III-NITRIDES FOR GROUP III-NITRIDE DEVICES," and/or United States Patent Application Serial No. _____ (Attorney Docket No. 5308-553), filed April 11, 2005 and entitled "THICK SEMI-INSULATING OR INSULATING EPITAXIAL GALLIUM NITRIDE LAYERS AND DEVICES INCORPORATING SAME," the disclosures of which are incorporated herein by reference as if set forth in their entirety.

Returning to **Figure 1**, an aluminum free Group III nitride barrier layer **12** is provided on the substrate **10**. An aluminum free Group III-nitride channel layer **14** is provided on the barrier layer **12** and an aluminum free Group III-nitride cap layer **16** is provided on the channel layer **14**. The barrier layer **12** may be deposited on the substrate **10** using buffer layers, transition layers, and/or nucleation layers as

described above. The barrier layer **12** may be semi-insulating or insulating and/or may be unintentionally doped. In some embodiments, the barrier layer **12** and/or the cap layer **16** may include doped regions adjacent the channel layer **14**. Furthermore, the barrier layer **12**, channel layer **14**, cap layer **16** and/or buffer nucleation and/or transition layers may be deposited by MOCVD or by other techniques known to those of skill in the art, such as MBE or HVPE .

The barrier layer **12** may be undoped or unintentionally doped. In some embodiments, the barrier layer **12** may include a thick semi-insulating or insulating layer with an undoped or unintentionally doped region adjacent the channel layer **14**. The barrier layer **12** should be thick enough to prevent migration of Al in layers disposed opposite the channel layer **14** to the channel layer **14**. Thus, portions of the barrier layer **12** may unintentionally include Al while still being an aluminum free Group III-nitride layer. For example, in some embodiments of the present invention, the barrier layer **12** may be from about 1 nm to about 1 x 10^6 nm thick and may have less than about 1% aluminum. In some embodiments of the present invention, the barrier layer **12** is about 1000 Å thick. Furthermore, a portion of the barrier layer **12** distal from the channel layer **14** may be doped with Fe or other elements to make it more insulating or provide a larger barrier as described in the above referenced patent applications. The barrier layer **12** may be provided as part or all of the substrate **10** or as a separate layer on the substrate **10**.

In some embodiments of the present invention, the channel layer **14** is a Group III-nitride, such as $In_xGa_{1-x}N$, where $0 \leq x \leq 1$ provided that the energy of the conduction band edge of the channel layer **14** is less than the energy of the conduction band edge of the cap layer **16** at the interface between the channel and cap layers. In particular, the channel layer **14** may have a bandgap that is less than the bandgap of the cap layer **16** and the channel layer **14** may also have a larger electron affinity than the cap layer **16**. Embodiments of the present invention where the channel layer **14** is InN (*i.e.* x=1) may exhibit lower alloy scatter because InN is a binary material. The channel layer **14** may be undoped or unintentionally doped and may be grown to a thickness of greater than about 10 Å. For example, in some embodiments, the channel layer **14** may have a thickness of from about 10 Å to about 200 Å. The channel layer **14** may also be a multi-layer structure, such as a superlattice or combinations of GaN, InGaN or the like. In some embodiments of the present invention, the channel layer **14** has less than about 1% aluminum.

In particular embodiments of the present invention, the cap layer **16** is thick enough and/or has a high enough doping to induce a significant carrier concentration at the interface between the channel layer **14** and the cap layer **16** through polarization effects. As discussed above, the cap layer **16** may be a Group III-nitride and has a bandgap larger than that of the channel layer **14** and a smaller electron affinity than the channel layer **14**. For example, the cap layer **16** may be GaN or InGaN. If the cap layer **16** is InGaN the cap layer **16** should have a lower indium percentage than is present in the channel layer **14**. The cap layer **16** may, for example, be from about 5 nm to about 100 nm thick, but is not so thick as to cause cracking or substantial defect formation therein. The cap layer **16** may be thicker if the gate contact **24** is recessed into the cap layer **16**. In certain embodiments of the present invention, the cap layer **16** is undoped and/or doped with an n-type dopant to a concentration of 1×10^{16} cm^{-3} about 1×10^{21} cm^{-3}. In some embodiments of the present invention, the cap layer **16** has less than about 1% aluminum.

Source and drain ohmic contacts **20** and **22** are provided on the cap layer **16** and a gate contact **24** is disposed between the source and drain contacts **20** and **22**. Suitable ohmic contact materials may include, for example, Ti, Al, Ni and/orAu. Suitable gate materials may depend on the composition of the cap layer, however, in certain embodiments, conventional materials capable of making a Schottky contact to a nitride based semiconductor material may be used, such as Ni, Pt, $NiSi_x$, Cu, Pd, Cr, W and/or WSiN.

Figure 2 is a schematic diagram of HEMTs according to further embodiments of the present invention. As seen in **Figure 2**, a GaN barrier layer **112** is provided on a substrate **110**. The substrate **110** may be a substrate as described above with reference to the substrate **10**. Furthermore, optional buffer, nucleation and/or transition layers (not shown) may be provided on the substrate **110** as described above. These optional buffer, nucleation and/or transition layers may include aluminum. In particular embodiments of the present invention, the substrate **110** is a GaN substrate.

As is further illustrated in **Figure 2**, an InGaN channel layer **114** is provided on the GaN barrier layer **112**. A GaN cap layer **116** is provided on the InGaN channel layer **114**.

In particular embodiments of the present invention, the GaN barrier layer **112** is a thick GaN layer and may be undoped, unintentionally doped and/or semi-

insulating or insulating. For example, the GaN barrier layer **112** may be semi-insulating or insulating in a region proximate the substrate **110** and may be undoped or unintentionally doped in a region proximate the InGaN channel layer **114**. The GaN barrier layer **112** should be sufficiently thick to prevent migration of Al in layers disposed opposite the channel layer **114** to the channel layer **114**. Thus, portions of the barrier layer **112** may unintentionally include Al while still being an aluminum free layer. In some embodiments of the present invention, the barrier layer **112** may be from about 10 nm to about 1 x 10^6 nm thick. In particular embodiments of the present invention, the barrier layer **112** is at least about 1000 Å thick. In some embodiments of the present invention, the barrier layer **112** has less than about 1% aluminum.

The InGaN channel layer **114** may be $In_xG_{1-x}aN$, where $0<x\leq 1$ provided that the energy of the conduction band edge of the channel layer **114** is less than the energy of the conduction band edge of the cap layer **116** at the interface between the channel and cap layers. In particular, the channel layer **114** may have a bandgap that is less than the bandgap of the cap layer **116** and the channel layer **114** may also have a larger electron affinity than the cap layer **116**. The channel layer **114** may be undoped or unintentionally doped and may be grown to a thickness of greater than about 10 Å. For example, in some embodiments, the channel layer **114** may have a thickness of from about 10 Å to about 200 Å. The maximum thickness of the channel layer **114** may depend on the percentage of indium in the channel layer **114**. The lower the percentage of indium in the channel layer **114**, the thicker the channel layer **114** may be before an undesirable two dimensional hole gas is formed for Ga polar devices. A low or high indium percentage may be desirable to reduce or minimize impurity scattering. In particular embodiments of the present invention, the indium percentage is the channel layer **114** is about 30% or less. In some embodiments, the indium percentage is the channel layer **114** is about 20%. In some embodiments of the present invention, the channel layer **114** has less than about 1% aluminum.

The GaN cap layer **116** is thick enough and/or has a high enough doping to induce a significant carrier concentration at the interface between the channel layer **114** and the cap layer **116**. In some embodiments of the present invention, the GaN cap layer **116** is from about 1 nm to about 100 nm thick, but is not so thick as to cause cracking or substantial defect formation therein. In some embodiments of the present invention, the cap layer **116** has less than about 1% aluminum. As discussed above,

with reference to the cap layer **16**, the cap layer **116** may be thicker if the gate contact **24** is recessed into the cap layer **116**.

Optionally, an InGaN layer (not shown) may be provided on the GaN cap layer **116**. The InGaN layer may increase the barrier to the surface from the channel. If an InGaN layer is provided on the GaN cap layer **116**, the InGaN layer may have an indium composition of from about 1% to 100% and may have a thickness of from about 1 nm to about 100 nm.

Figures 3A through **3D** are schematic illustrations of further embodiments of HEMTs according the present invention having doped and/or spacer layers adjacent an InGaN channel layer **214**. As seen in **Figures 3A** through **3D** a GaN barrier layer **212** is provided on a substrate **210**. An InGaN channel layer **214** is provided on the GaN barrier layer **212** and a GaN cap layer **216** is provided on the InGaN channel layer **214**. The substrate **210**, GaN barrier layer **212**, InGaN channel layer **214** and GaN cap layer **216** may be provided as described above with reference to the substrate **110**, GaN barrier layer **112**, InGaN channel layer **114** and GaN cap layer **116** of **Figure 2**. The optional buffer, nucleation and/or transition layers described above may also be provided. An optional InGaN layer (not shown) may also be provided on the cap layer **216** as described above.

Figure 3A illustrates embodiments of the present invention where a doped GaN layer **230** is disposed between the GaN barrier layer **212** and the InGaN channel layer **214**. In some embodiments of the present invention, the doped GaN layer **230** may be doped with Si, Ge, Sn and/or O and may have a dopant concentration of from about 1×10^{16} cm^{-3} to about 1×10^{21} cm^{-3}. In particular embodiments, the dopant concentration may be about 1×10^{20} cm^{-3}. Furthermore, the doped GaN layer **230** may be from about 0.2 nm to about 10 nm thick. The doping concentration should be high enough and the layer thick enough to supply sufficient electrons to the 2DEG channel, but not so high or thick as to have additional, unintentional n-type regions outside of the channel region. In particular embodiments, the dopant may be Sn and/or Ge. In other embodiments, the dopant may be Si. The doped GaN layer **230** may be provided as a delta doped region. In particular embodiments of the present invention, the doped layer **230** provides a sheet density of from about 1×10^{12} cm^{-2} to about 1×10^{14} cm^{-2} at the interface with the channel layer **214**.

While the doped layer **230** is described above with reference to a GaN layer, in some embodiments of the present invention, the doped layer **230** may be provided

by an InGaN layer. Thus, for example, the doped layer **230** may be provided by a doped region of the InGaN channel layer **214**. In such a case, the InGaN channel layer **214** should be thick enough and the doped portion thin enough and doped lightly enough so that electrons from the doping are supplied to the 2DEG and do not form an n-type region in the doped region.

Figure 3B illustrates embodiments of the present invention where a doped GaN layer **230** is disposed between the GaN barrier layer **212** and the InGaN channel layer **214** and an undoped GaN layer **240** is disposed between the doped GaN layer **230** and the InGaN channel layer **214**. In some embodiments of the present invention, the undoped GaN layer **240** may be from about 0.5 nm to about 5 nm thick. The undoped GaN layer **240** may space the doped layer **230** from the channel layer **214** to reduce and/or minimize impurity scattering.

Figure 3C illustrates embodiments of the present invention where a doped GaN layer **250** is disposed between the GaN cap layer **216** and the InGaN channel layer **214**. In some embodiments of the present invention, the doped GaN layer **250** may be doped with Si, Sn, Ge and/or O and may have a dopant concentration of from about 1×10^{16} cm^{-3} to about 1×10^{21} cm^{-3}. Furthermore, the doped GaN layer **250** may be from about 0.2 nm to about 100 nm thick. The structure of **Figure 3C** could be used as a MESFET with the InGaN channel layer **214** acting more as a back barrier than a channel if the GaN layer **250** is doped heavily enough. Mobility may be better in the doped GaN layer **250** than in the InGaN channel layer **214** depending on the doping density and the indium percentage.

Figure 3D illustrates embodiments of the present invention where a doped GaN layer **250** is disposed between the GaN cap layer **216** and the InGaN channel layer **214** and an undoped GaN layer **260** is disposed between the doped GaN layer **250** and the InGaN channel layer **214**. In some embodiments of the present invention, the undoped GaN layer **260** may be from about 0.3 nm to about 10 nm thick. The undoped GaN layer **260** may space the doped layer **250** from the channel layer **214** to reduce and/or minimize impurity scattering.

While embodiments of the present invention are illustrated in **Figures 3A** through **3D** as including doped and/or undoped layers on one side or the other of the InGaN channel layer **214**, combinations and subcombinations of the structures illustrated in **Figures 3A** through 3D may also be provided. For example, a structure

with a doped layer between the cap layer **216** and the channel layer **214** may also have a doped layer between the barrier layer **212** and the channel layer **214**.

A passivation layer (not shown) may also be provided on the structures of **Figures 1** through **3D**. In certain embodiments of the present invention, the passivation layer may be silicon nitride, aluminum nitride, silicon dioxide, an ONO structure and/or an oxynitride. Furthermore, the passivation layer may be a single or multiple layers of uniform and/or non-uniform composition.

Figures 4A through **4N** are graphs of carrier concentration and band diagrams from simulation models of transistors according to some embodiments of the present invention. In the simulations depicted in **Figures 4A** through **4N**, the aluminum free layers are modeled as having 0% aluminum. These simulations are not meant to be exact but are provided to illustrate possible trends and to estimate properties of different designs. Accordingly, these graphs are provided as a rough estimate of possible characteristics of the simulated device structures but are only as accurate as the underlying assumptions and models. Accordingly, the properties of actual devices may differ from those illustrated in **Figures 4A** through **4N**.

Figure 4A illustrates a modeled band diagram and electron concentration for an aluminum free HEMT with a thick undoped GaN barrier layer, a 3 nm thick InGaN channel layer with 30% indium and a 10 nm thick undoped GaN cap layer. **Figure 4B** illustrates a modeled band diagram and electron concentration for an aluminum free HEMT with a thick undoped GaN barrier layer, a 3 nm thick InGaN channel layer with 30% indium and a 20 nm thick undoped GaN cap layer. By comparing **Figures 4A** and **4B**, an increase in peak electron concentration is predicted as a result of increasing the thickness of the GaN cap layer.

Figure 4C illustrates a modeled band diagram and electron concentration for an aluminum free HEMT with a thick undoped GaN barrier layer, a 1 nm thick doped GaN layer with a dopant concentration of 18×10^{19} cm^{-3} between the barrier layer and the channel layer, a 1 nm thick undoped GaN layer between the doped GaN layer and the channel layer, a 6 nm thick InGaN channel layer with 30% indium and a 60 nm thick undoped GaN cap layer. As seen in **Figure 4C**, the configuration of **Figure 4C** is predicted to have a higher peak electron concentration than either of the configurations of **Figures 4A** and **4B**.

Figure 4D illustrates a modeled band diagram and electron concentration for an aluminum free HEMT with a thick undoped GaN barrier layer, a 1 nm thick doped

GaN layer with a dopant concentration of 20 X 10^{19} cm^{-3} between the barrier layer and the channel layer, a 6 nm thick InGaN channel layer with 20% indium and a 60 nm thick undoped GaN cap layer. As seen in **Figure 4D**, the configuration of **Figure 4D** is predicted to have a higher peak electron concentration than either of the configurations of Figures **4A** and **4B** but may have a lower peak electron concentration than provided by the configuration of **Figure 4C**.

Figure 4E illustrates a modeled band diagram and electron concentration for an aluminum free HEMT with a thick undoped GaN barrier layer, a 1 nm thick doped GaN layer with a dopant concentration of 10 X 10^{19} cm^{-3} between the barrier layer and the channel layer, a 6 nm thick InGaN channel layer with 20% indium and a 60 nm thick undoped GaN cap layer. As seen in **Figure 4E**, by increasing the dopant concentration in the doped GaN layer and increasing the thickness of the GaN cap layer, the configuration of **Figure 4E** is predicted to have a higher peak electron concentration than either of the configurations of Figures **4A** and **4B** but may have a lower peak electron concentration than provided by the configuration of **Figures 4C** or **4D**. The configuration of **Figure 4E** is predicted to have a higher conduction band edge in the barrier layer than in **Figure 4D** due to the lower doping.

Figure 4F illustrates a modeled band diagram and electron concentration for an aluminum free HEMT with a thick undoped GaN barrier layer that is delta doped at 1 x 10^{13} cm^{-2} at the interface with the channel layer, a 6 nm thick InGaN channel layer with 20% indium and a 60 nm thick undoped GaN cap layer. As seen in **Figure 4F**, the configuration of **Figure 4F** is about the same as the configuration in **Figure 4E** due to the same sheet doping density in both structures with slightly lower conduction band bending in the barrier due to the reduced thickness of the doped region.

Figure 4G illustrates a modeled band diagram and electron concentration for an aluminum free HEMT with a thick undoped GaN barrier layer, a 3 nm thick doped GaN layer with a dopant concentration of 3 X 10^{19} cm^{-3} between the barrier layer and the channel layer, a 1 nm thick undoped GaN layer between the doped GaN layer and the channel layer, a 3 nm thick InGaN channel layer with 30% indium and a 20 nm thick undoped GaN cap layer. As seen in **Figure 4G**, the configuration of **Figure 4G** is predicted to have a higher peak electron concentration than either of the configurations of **Figures 4A** and **4B**.

Figure 4H illustrates a modeled band diagram and electron concentration for an aluminum free HEMT with a thick undoped GaN barrier layer, a 3 nm thick doped GaN layer with a dopant concentration of 3 X 10^{19} cm^{-3} between the barrier layer and the channel layer, a 1 nm thick undoped GaN layer between the doped GaN layer and the channel layer, a 3 nm thick InGaN channel layer with 30% indium and a 30 nm thick undoped GaN cap layer. As seen in **Figure 4H**, the configuration of **Figure 4H** is predicted to have a slightly higher peak electron concentration than the configuration of **Figure 4G** as a result of the thicker GaN cap.

Figure 4I illustrates a modeled band diagram and electron concentration for an aluminum free HEMT with a thick undoped GaN barrier layer, a 3 nm thick doped GaN layer with a dopant concentration of 3 X 10^{19} cm^{-3} between the barrier layer and the channel layer, a 1 nm thick undoped GaN layer between the doped GaN layer and the channel layer, a 3 nm thick InGaN channel layer with 20% indium and a 30 nm thick undoped GaN cap layer. As seen in **Figure 4I**, the configuration of **Figure 4I** is predicted to have a lower peak electron concentration than the configurations of **Figure 4H** due to the lower In percentage.

Figure 4J illustrates a modeled band diagram and electron concentration for an aluminum free HEMT with a thick undoped GaN barrier layer, a 3 nm thick doped GaN layer with a dopant concentration of 3 X 10^{19} cm^{-3} between the cap layer and the channel layer, a 1 nm thick undoped GaN layer between the doped GaN layer and the channel layer, a 3 nm thick InGaN channel layer with 20% indium and a 26 nm thick undoped GaN cap layer. As seen in **Figure 4J**, the configuration of **Figure 4J** is predicted to have two peaks in the electron concentration and has a lower peak electron concentration than configurations with a doped layer on the opposite side of the channel layer as seen in **Figure 4I**. A structure similar to that of **Figure 4J** could be used as a MESFET, as mentioned above.

Figure 4K illustrates a modeled band diagram and electron concentration for an aluminum free HEMT with a thick undoped GaN barrier layer, a 3 nm thick doped GaN layer with a dopant concentration of 3 X 10^{19} cm^{-3} between the barrier layer and the channel layer, a 1 nm thick undoped GaN layer between the doped GaN layer and the channel layer, a 6 nm thick InGaN channel layer with 20% indium and a 30 nm thick undoped GaN cap layer. In comparison to the structure of **Figure 4I**, the structure of **Figure 4K** has a higher back barrier due to the thicker InGaN layer. *See* United States Patent Application Serial No. 10/772,882, filed February 5, entitled

"NITRIDE HETEROJUNCTION TRANSISTORS HAVING CHARGE-TRANSFER INDUCED ENERGY BARRIERS AND METHODS OF FABRICATING THE SAME," the disclosure of which is incorporated herein as if set forth fully herein.

Figure 4L illustrates a modeled band diagram and electron concentration for an aluminum free HEMT with a thick undoped GaN barrier layer, a 3 nm thick doped GaN layer with a dopant concentration of 3 X 10^{19} cm^{-3} between the barrier layer and the channel layer, a 1 nm thick undoped GaN layer between the doped GaN layer and the channel layer, a 6 nm thick InGaN channel layer with 20% indium and a 60 nm thick undoped GaN cap layer. As seen in **Figures 4K** and **4L**, a thicker GaN cap may increase the charge in the channel.

Figures 4M and **4N** illustrate modeling of configurations that vary the thickness of the GaN doped layer. The structure of **Figure 4M** has a higher In concentration than the structure of **Figure 4L**, resulting in a higher carrier concentration and higher conduction band in the barrier, but a lower mobility due to increased alloy scattering is likely. As seen in **Figures 4M** and **4N**, **Figure 4N** has a thicker doped layer than **Figure 4M** and, therefore, a higher electron concentration in the channel and a lower conduction band energy in the barrier layer.

An aluminum free HEMT structure according to some embodiments of the present invention has been fabricated using a 60 nm GaN cap layer, a 6 nm InGaN channel layer with 20 % In and a 1.7 x 10^{13} cm^{-2} Si delta doped region at the interface with a thick GaN barrier layer. Such device structure exhibited a sheet resistivity of approximately 1200 Ω/□.

While embodiments of the present invention have been described herein with reference to particular HEMT structures, the present invention should not be construed as limited to such structures. For example, additional layers may be included in the HEMT device while still benefiting from the teachings of the present invention. In some embodiments, insulating layers such as SiN, an ONO structure or relatively high quality AlN may be deposited for making a MISHEMT and/or passivating the surface. The additional layers may also include a compositionally graded transition layer or layers.

Also, other structures, such as recessed or "T" gate structures, regrown contact regions or the like may also be provided. Accordingly, some embodiments of the present invention provide aluminum free embodiments of structures such as those described in, for example, U.S. Patent 6,316,793 and U.S. Patent Publication No.

2002/0066908A1 filed July 12, 2001 and published June 6, 2002, for "ALUMINUM GALLIUM NITRIDE/GALLIUM NITRIDE HIGH ELECTRON MOBILITY TRANSISTORS HAVING A GATE CONTACT ON A GALLIUM NITRIDE BASED CAP SEGMENT AND METHODS OF FABRICATING SAME," U. S. Patent No. 6,849,882 to Smorchkova *et al.*, entitled "GROUP-III NITRIDE BASED HIGH ELECTRON MOBILITY TRANSISTOR (HEMT) WITH BARRIER/SPACER LAYER", U.S. Patent Application Serial No. 10/617,843 filed July 11, 2003 for "NITRIDE-BASED TRANSISTORS AND METHODS OF FABRICATION THEREOF USING NON-ETCHED CONTACT RECESSES," U.S. Patent Application Serial No. 10/772,882 filed February 5, 2004 for "NITRIDE HETEROJUNCTION TRANSISTORS HAVING CHARGE-TRANSFER INDUCED ENERGY BARRIERS AND METHODS OF FABRICATING THE SAME," U.S. Patent Application Serial No. 10/897,726, filed July 23, 2004 entitled "METHODS OF FABRICATING NITRIDE-BASED TRANSISTORS WITH A CAP LAYER AND A RECESSED GATE," U.S. Patent Application Serial No. 10/849,617, filed May 20, 2004 entitled "METHODS OF FABRICATING NITRIDE-BASED TRANSISTORS HAVING REGROWN OHMIC CONTACT REGIONS AND NITRIDE-BASED TRANSISTORS HAVING REGROWN OHMIC CONTACT REGIONS," U.S. Patent Application Serial No. 10/849,589, filed May 20, 2004 and entitled "SEMICONDUCTOR DEVICES HAVING A HYBRID CHANNEL LAYER, CURRENT APERTURE TRANSISTORS AND METHODS OF FABRICATING SAME," U.S. Patent Publication No. 2003/0020092 filed July 23, 2002 and published January 30, 2003 for "INSULATING GATE ALGAN/GAN HEMT", U.S. Patent Application Serial No.10/996,249, filed November 23, 2004 and entitled "CAP LAYERS AND/OR PASSIVATION LAYERS FOR NITRIDE-BASED TRANSISTORS, TRANSISTOR STRUCTURES AND METHODS OF FABRICATING SAME," United States Patent Application Serial No. _____ (Attorney Docket No. 5308-516), filed March 15, 2005 and entitled "GROUP III NITRIDE FIELD EFFECT TRANSISTORS (FETs) CAPABLE OF WITHSTANDING HIGH TEMPERATURE REVERSE BIAS TEST CONDITIONS," United States Patent Application Serial No. 11/005,107, filed December 6, 2004 and entitled " HIGH POWER DENSITY AND/OR LINEARITY TRANSISTORS," and United States Patent Application Serial No. 11/005,423, filed December 6, 2004 and entitled "FIELD EFFECT TRANSISTORS (FETs) HAVING

MULTI-WATT OUTPUT POWER AT MILLIMETER-WAVE FREQUENCIES," the disclosures of which are incorporated herein as if described in their entirety. Embodiments of the present invention may also be utilized with HEMT structures such as described in, for example, Yu et al., "Schottky barrier engineering in III–V nitrides via the piezoelectric effect," Applied Physics Letters, Vol. 73, No. 13, 1998, or in U.S. Patent No. 6,584,333 filed July 12, 2001, for "ALUMINUM GALLIUM NITRIDE/GALLIUM NITRIDE HIGH ELECTRON MOBILITY TRANSISTORS HAVING A GATE CONTACT ON A GALLIUM NITRIDE BASED CAP SEGMENT AND METHODS OF FABRICATING SAME," the disclosures of which are incorporated herein by reference as if set forth fully herein.

In the drawings and specification, there have been disclosed typical embodiments of the invention, and, although specific terms have been employed, they have been used in a generic and descriptive sense only and not for purposes of limitation, the scope of the invention being set forth in the following claims.

THAT WHICH IS CLAIMED IS:

1. A high electron mobility transistor (HEMT), comprising:
an aluminum free Group III-nitride barrier layer;
an aluminum free Group III-nitride channel layer on the barrier layer; and
an aluminum free Group III-nitride cap layer on the channel layer.

2. The HEMT of Claim 1, wherein the barrier layer comprises a doped Group III-nitride region adjacent the aluminum free Group III-nitride channel layer.

3. The HEMT of Claim 2, further comprising an undoped Group III-nitride layer disposed between the doped Group III-nitride region and the channel layer.

4. The HEMT of Claim 2, wherein the cap layer comprises a first doped Group III-nitride region adjacent the aluminum free Group III-nitride channel layer.

5. The HEMT of Claim 4, further comprising an undoped Group III-nitride layer disposed between the first doped Group III-nitride region and the channel layer.

6. The HEMT of Claim 1, wherein the cap layer comprises a first doped Group III-nitride region adjacent the aluminum free Group III-nitride channel layer.

7. The HEMT of Claim 6, further comprising an undoped Group III-nitride layer disposed between the first doped Group III-nitride region and the channel layer.

8. The HEMT of Claim 1, wherein the barrier layer comprises a GaN layer, the channel layer comprises an InGaN layer and the cap layer comprises a GaN layer.

9. The HEMT of Claim 8, wherein the barrier layer has a thickness of from about 1 nm to about 1 mm, the channel layer has a thickness of from about 0.3

nm to about 50 nm and the cap layer has a thickness of from about 1 nm to about 100 nm.

10. The HEMT of Claim 8, wherein the InGaN layer has a percentage of indium of from about 1 % to about 100 %.

11. The HEMT of Claim 8, further comprising a first doped GaN layer disposed between the GaN barrier layer and the InGaN channel layer.

12. The HEMT of Claim 11, wherein the first doped GaN layer comprises a Si, Sn, O and/or Ge doped GaN layer.

13. The HEMT of Claim 11, wherein the first doped GaN layer has a thickness of from about 0.2 nm to about 10 nm.

14. The HEMT of Claim 11, wherein the first doped GaN layer has a dopant concentration of from about 1×10^{17} cm^{-3} to about 1×10^{21} cm^{-3}.

15. The HEMT of Claim 11, further comprising a first undoped GaN layer disposed between the first doped GaN layer and the InGaN channel layer.

16. The HEMT of Claim 15, wherein the first undoped GaN layer has a thickness of from about 0.3 nm to about 10 nm.

17. The HEMT of Claim 8, further comprising a first doped GaN layer disposed between the GaN cap layer and the InGaN channel layer.

18. The HEMT of Claim 17, wherein the first doped GaN layer comprises a Si, Sn, O and/or Ge doped GaN layer.

19. The HEMT of Claim 17, wherein the first doped GaN layer has a thickness of from about 0.2 nm to about 10 nm.

20. The HEMT of Claim 17, wherein the first doped GaN layer has a dopant concentration of from about 1×10^{17} cm^{-3} to about 1×10^{21} cm^{-3}.

21. The HEMT of Claim 17, further comprising a first undoped GaN layer disposed between the first doped GaN layer and the InGaN channel layer.

22. The HEMT of Claim 21, wherein the first undoped GaN layer has a thickness of from about 0.3 nm to about 10 nm.

23. The HEMT of Claim 17, further comprising a second doped GaN layer disposed between the GaN barrier layer and the InGaN channel layer.

24. The HEMT of Claim 23, wherein the second doped GaN layer comprises a Si, Sn, O and/or Ge doped GaN layer.

25. The HEMT of Claim 23, wherein the second doped GaN layer has a thickness of from about 0.2 nm to about 10 nm.

26. The HEMT of Claim 23, wherein the second doped GaN layer has a dopant concentration of from about 1 x 10^{17} cm^{-3} to about 1 x 10^{21} cm^{-3}.

27. The HEMT of Claim 23, further comprising a second undoped GaN layer disposed between the second doped GaN layer and the InGaN channel layer.

28. The HEMT of Claim 27, wherein the second undoped GaN layer has a thickness of from about 0.3 nm to about 10 nm.

29. The HEMT of Claim 8, further comprising an InGaN layer on the GaN cap layer opposite the InGaN channel layer.

30. The HEMT of Claim 29, wherein the InGaN layer on the GaN cap layer opposite the InGaN channel layer has a thickness of from about 0.3 nm to about 50 nm.

31. A method of fabricating a high electron mobility transistor (HEMT), comprising:

forming an aluminum free Group III-nitride barrier layer;

forming an aluminum free Group III-nitride channel layer on the barrier layer; and

forming an aluminum free Group III-nitride cap layer on the channel layer.

32. The method of Claim 31, wherein the barrier layer comprises a doped Group III-nitride region adjacent the aluminum free Group III-nitride channel layer.

33. The method of Claim 32, further comprising forming an undoped Group III-nitride layer disposed between the doped Group III-nitride region and the channel layer.

34. The method of Claim 32, wherein the cap layer comprises a first doped Group III-nitride region adjacent the aluminum free Group III-nitride channel layer.

35. The method of Claim 34, further comprising forming an undoped Group III-nitride layer disposed between the first doped Group III-nitride region and the channel layer.

36. The method of Claim 31, wherein the cap layer comprises a first doped Group III-nitride region adjacent the aluminum free Group III-nitride channel layer.

37. The method of Claim 36, further comprising forming an undoped Group III-nitride layer disposed between the first doped Group III-nitride region and the channel layer.

38. The method of Claim 31, wherein the barrier layer comprises a GaN layer, the channel layer comprises an InGaN layer and the cap layer comprises a GaN layer.

39. The method of Claim 38, wherein the barrier layer has a thickness of from about 1 nm to about 1 mm, the channel layer has a thickness of from about 0.3 nm to about 50 nm and the cap layer has a thickness of from about 1 nm to about 100 nm.

40. The method of Claim 38, wherein the InGaN layer has a percentage of indium of from about 1 % to about 100 %.

41. The method of Claim 38, further comprising a first doped GaN layer disposed between the GaN barrier layer and the InGaN channel layer.

42. The method of Claim 41, wherein the first doped GaN layer comprises a Si, Sn, O and/or Ge doped GaN layer.

43. The method of Claim 41, wherein the first doped GaN layer has a thickness of from about 0.2 nm to about 10 nm.

44. The method of Claim 41, wherein the first doped GaN layer has a dopant concentration of from about 1 x 10^{17} cm^{-3} to about 1 x 10^{21} cm^{-3}.

45. The method of Claim 41, further comprising forming a first undoped GaN layer disposed between the first doped GaN layer and the InGaN channel layer.

46. The method of Claim 45, wherein the first undoped GaN layer has a thickness of from about 0.3 nm to about 10 nm.

47. The method of Claim 38, further comprising forming a first doped GaN layer disposed between the GaN cap layer and the InGaN channel layer.

48. The method of Claim 47, wherein the first doped GaN layer comprises a Si, Sn, O and/or Ge doped GaN layer.

49. The method of Claim 47, wherein the first doped GaN layer has a thickness of from about 0.2 nm to about 10 nm.

50. The method of Claim 47, wherein the first doped GaN layer has a dopant concentration of from about 1 x 10^{17} cm^{-3} to about 1 x 10^{21} cm^{-3}.

51. The method of Claim 47, further comprising a first undoped GaN layer disposed between the first doped GaN layer and the InGaN channel layer.

52. The method of Claim 51, wherein the first undoped GaN layer has a thickness of from about 0.3 nm to about 10 nm.

53. The method of Claim 47, further comprising forming a second doped GaN layer disposed between the GaN barrier layer and the InGaN channel layer.

54. The method of Claim 53, wherein the second doped GaN layer comprises a Si, Sn, O and/or Ge doped GaN layer.

55. The method of Claim 53, wherein the second doped GaN layer has a thickness of from about 0.2 nm to about 10 nm.

56. The method of Claim 53, wherein the second doped GaN layer has a dopant concentration of from about 1×10^{17} cm^{-3} to about 1×10^{21} cm^{-3}.

57. The method of Claim 53, further comprising forming a second undoped GaN layer disposed between the second doped GaN layer and the InGaN channel layer.

58. The method of Claim 57, wherein the second undoped GaN layer has a thickness of from about 0.3 nm to about 10 nm.

59. The method of Claim 38, further comprising forming an InGaN layer on the GaN cap layer opposite the InGaN channel layer.

60. The method of Claim 59, wherein the InGaN layer on the GaN cap layer opposite the InGaN channel layer has a thickness of from about 0.3 nm to about 50 nm.

61. The method of Claim 36, wherein the transistor comprises a metal semiconductor field effect transistor (MESFET).

62. The HEMT of Claim 6, wherein the transistor comprises a metal semiconductor field effect transistor (MESFET).

63. The HEMT of Claim 1, wherein the channel layer comprises a doped Group III-nitride region adjacent the aluminum free Group III-nitride barrier layer.

64. The HEMT of Claim 63, wherein the channel layer comprises an InGaN channel layer and the barrier layer comprises a GaN barrier layer, the InGaN channel layer comprising a doped region adjacent the GaN barrier layer.

65. The HEMT of Claim 1, wherein the aluminum free Group III-nitride barrier layer comprises a substantially relaxed $In_xGa_{1-x}N$ layer where $x > 0$, the aluminum free Group III-nitride channel layer on the barrier layer comprises an $In_yGa_{1-y}N$ layer where $y > x$ and the aluminum free Group III-nitride cap layer on the channel layer comprises an $In_zGa_{1-z}N$ layer where $z < x$.

66. The HEMT of Claim 65, wherein the barrier layer, channel layer and cap layer are strain balanced.

67. The HEMT of Claim 65, wherein $y=1$.

68. The HEMT of Claim 65, wherein $z=0$.

69. The HEMT of Claim 68, wherein $y=1$.

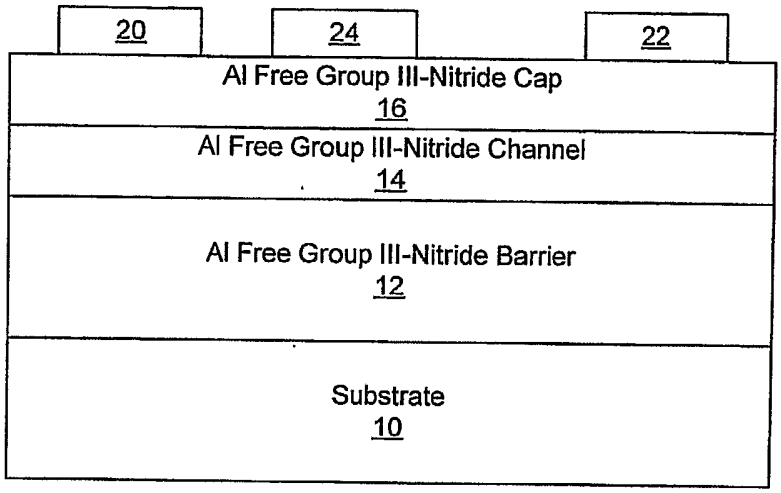


Figure 1

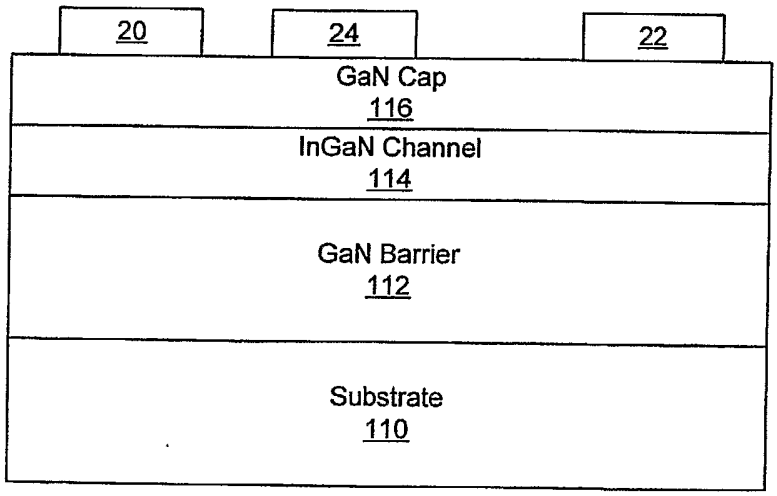


Figure 2

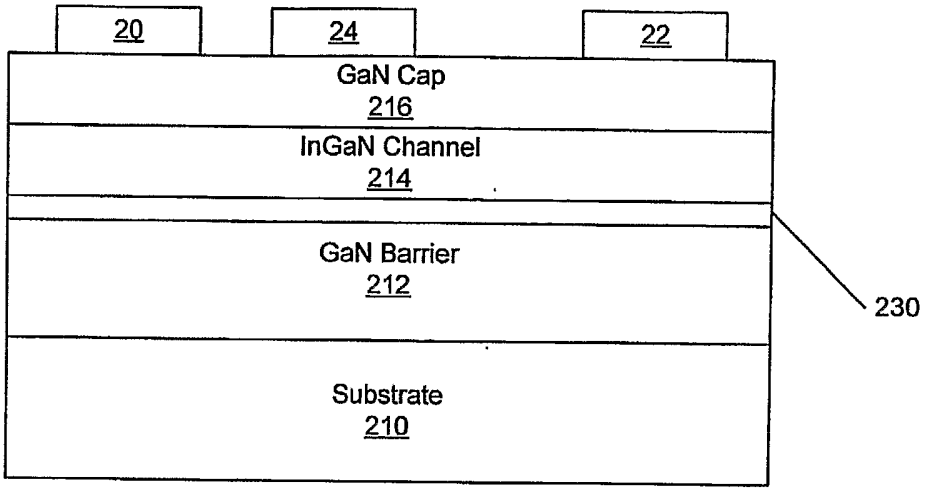


Figure 3A

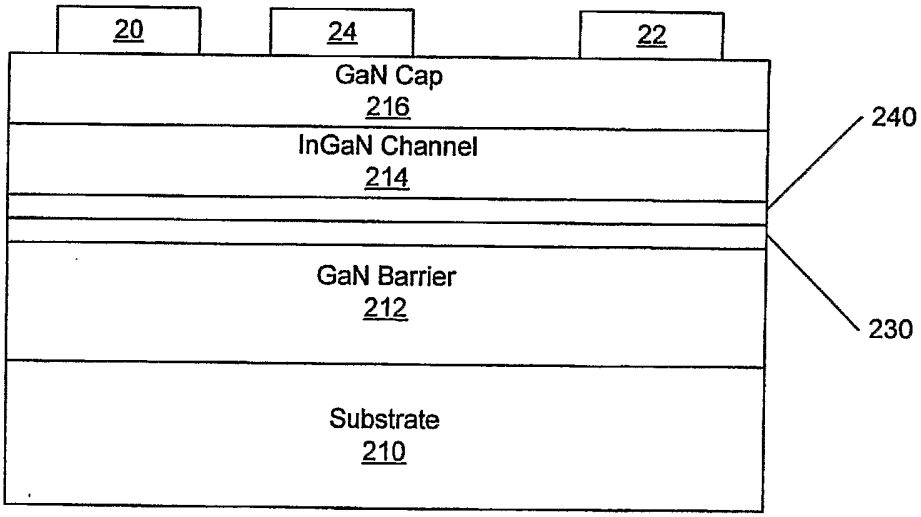


Figure 3B

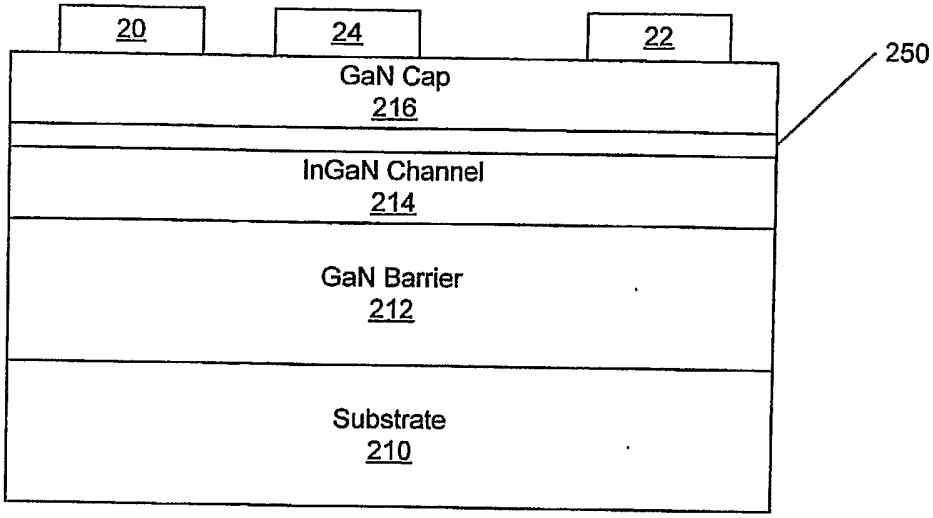


Figure 3C

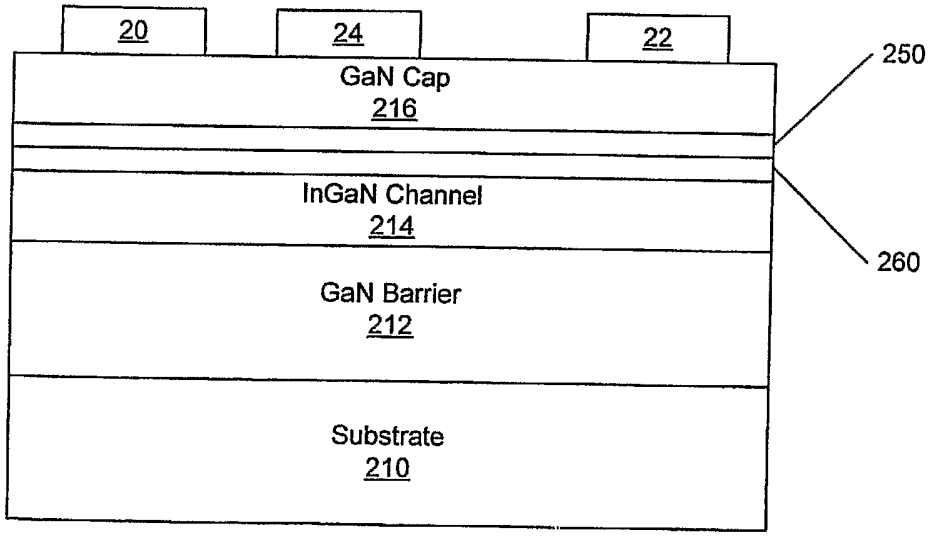


Figure 3D

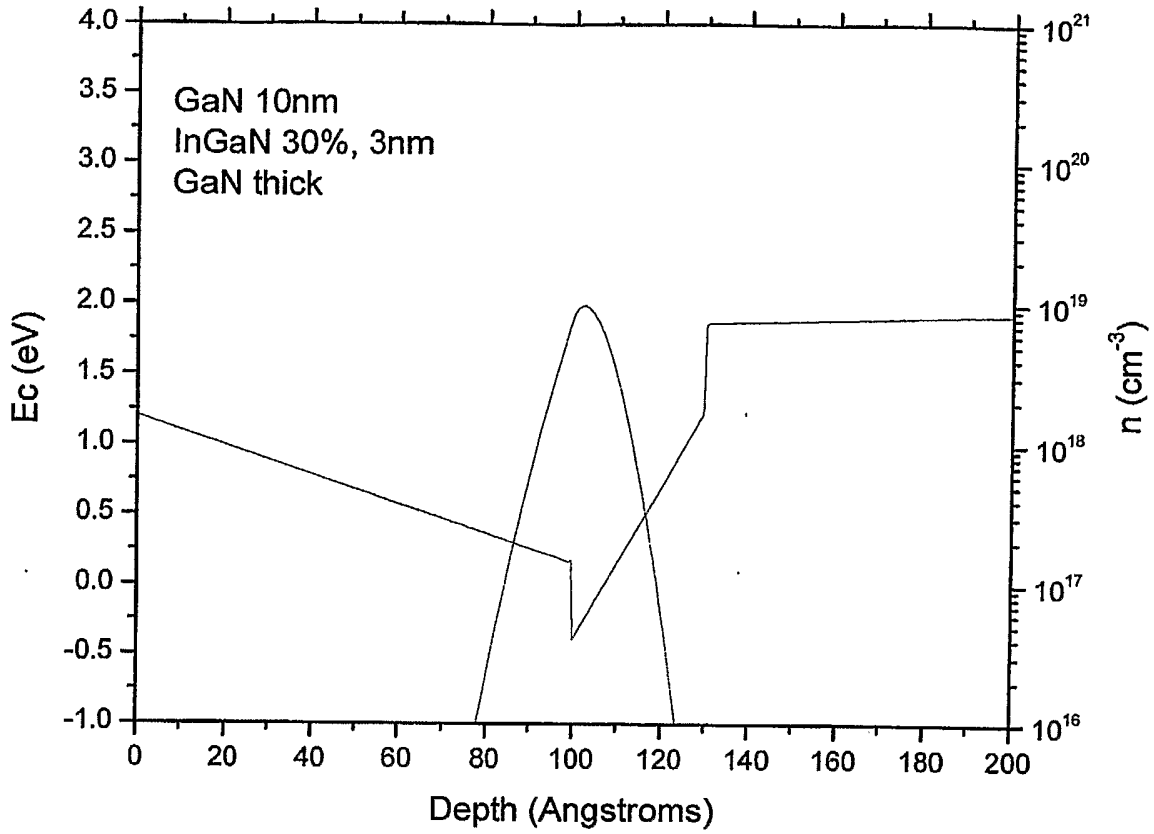


Figure 4A

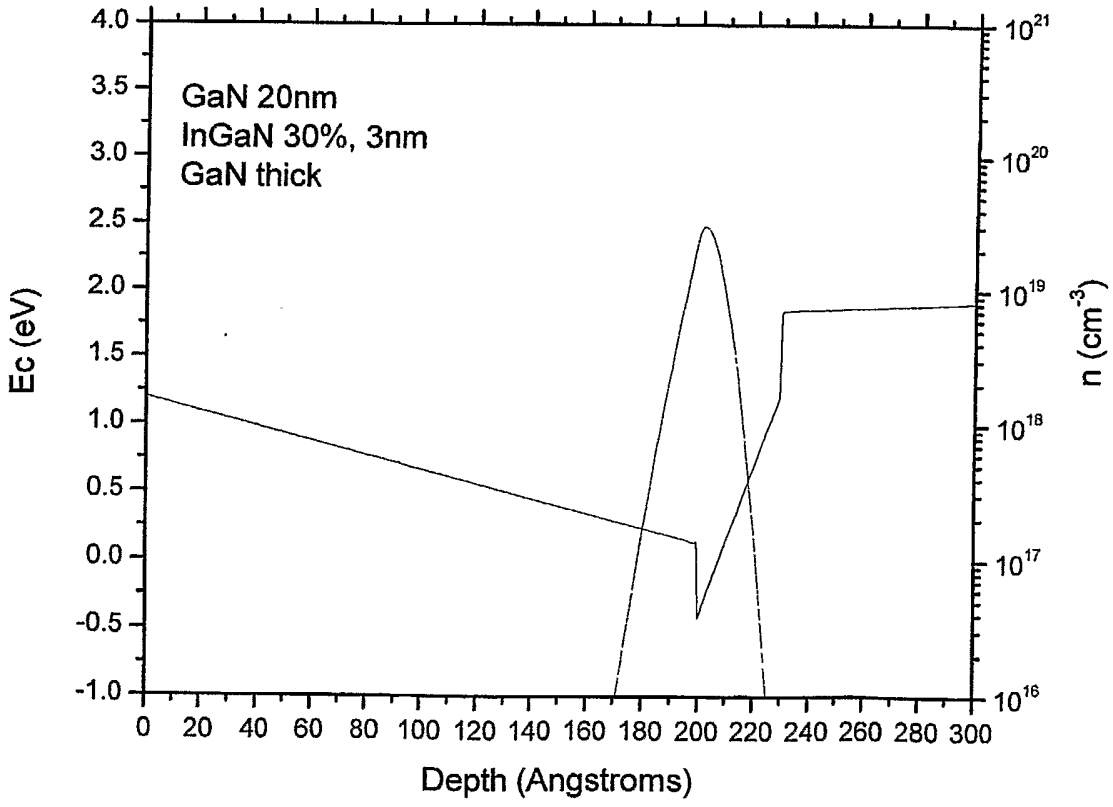


Figure 4B

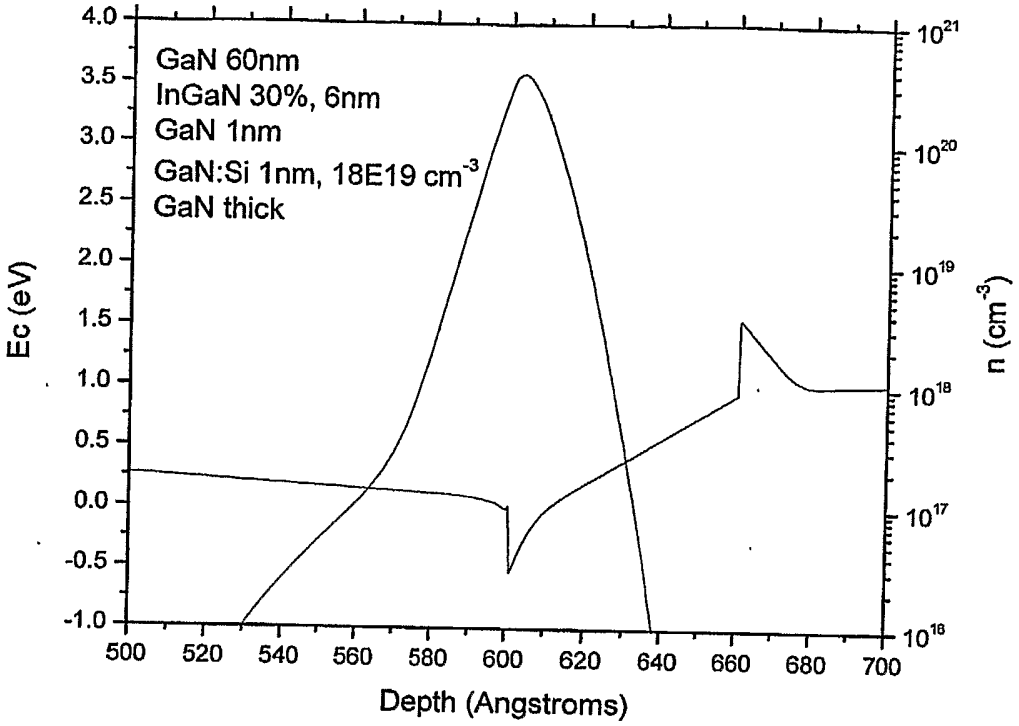


Figure 4C

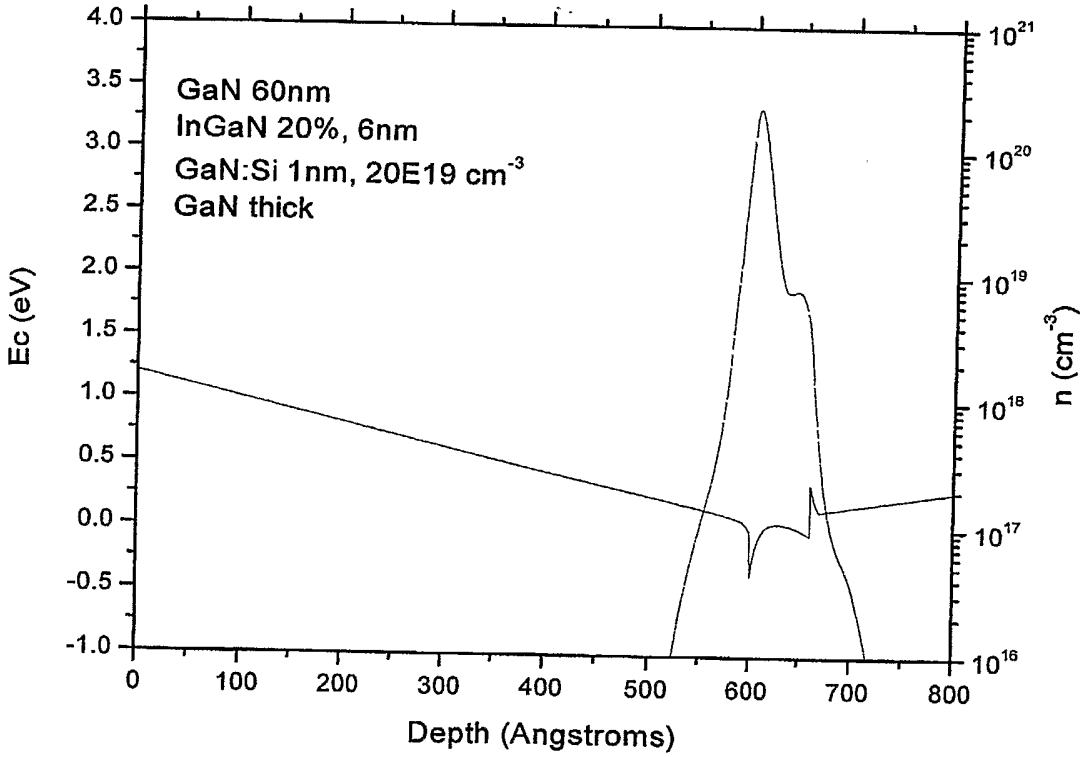


Figure 4D

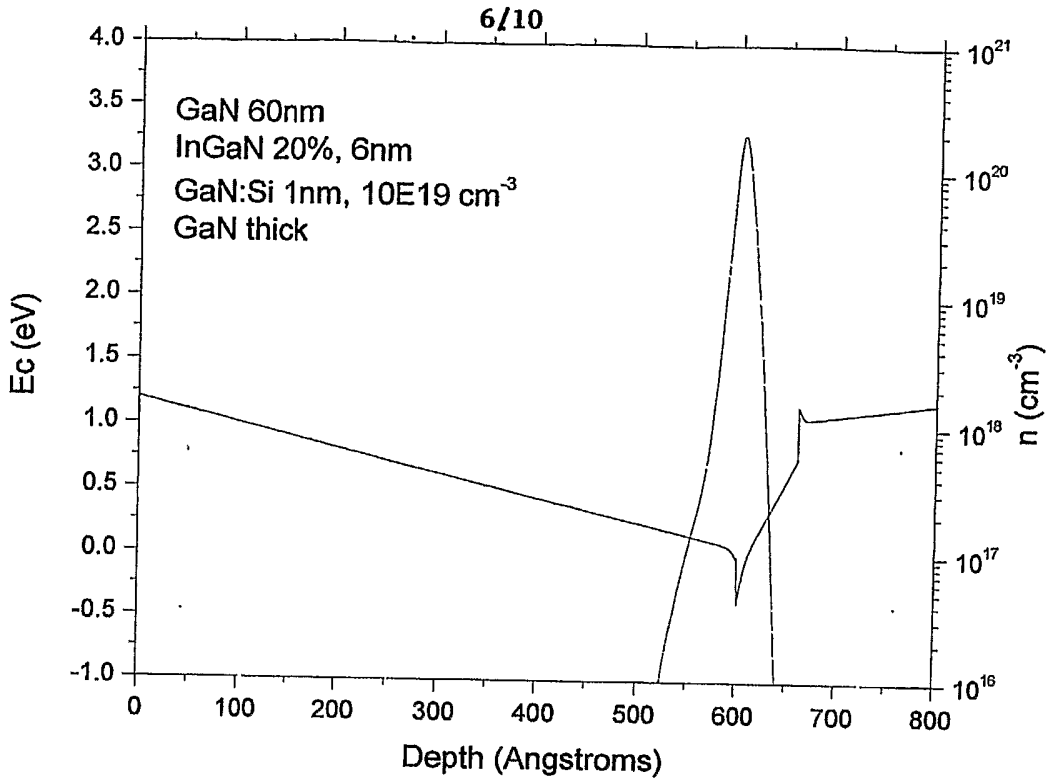


Figure 4E

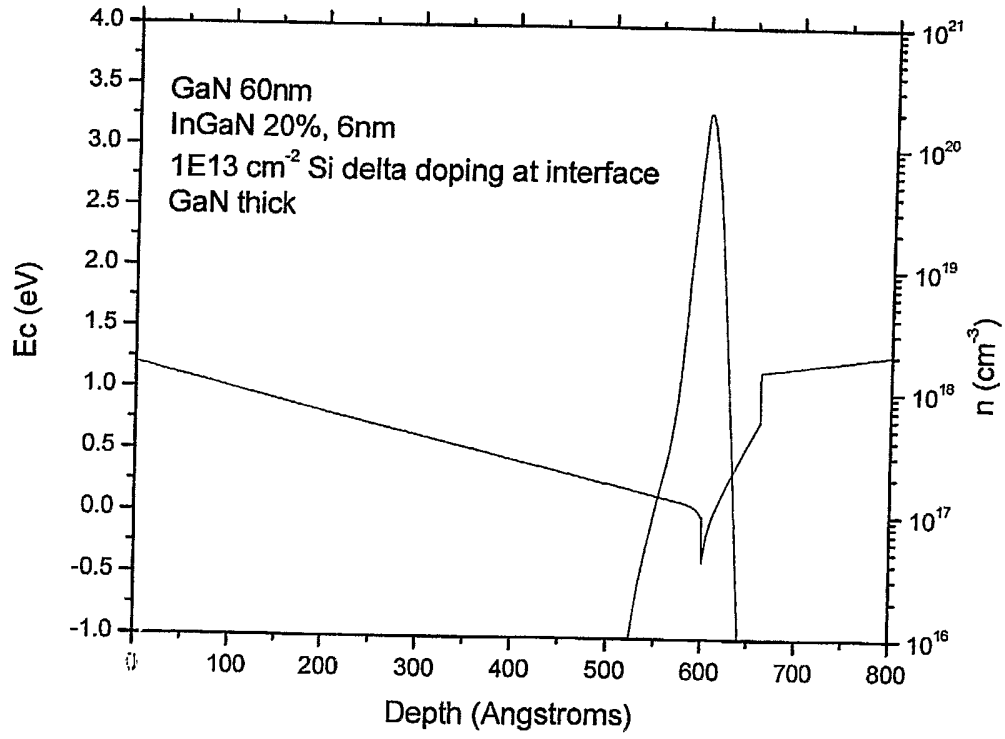


Figure 4F

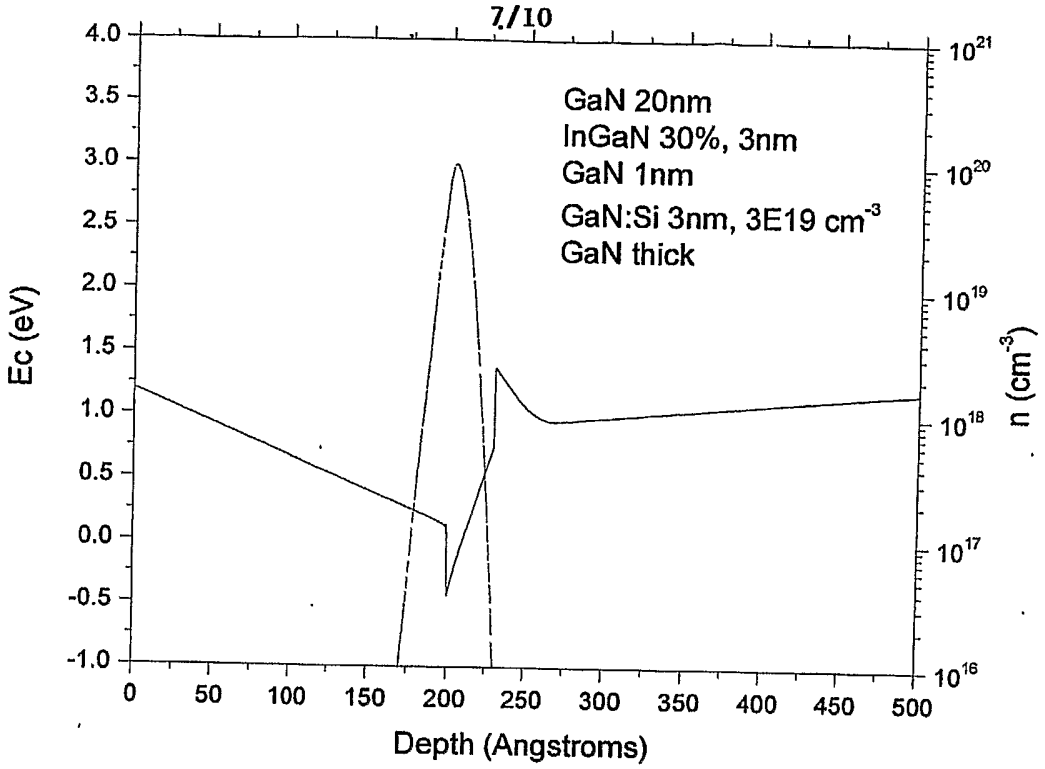


Figure 4G

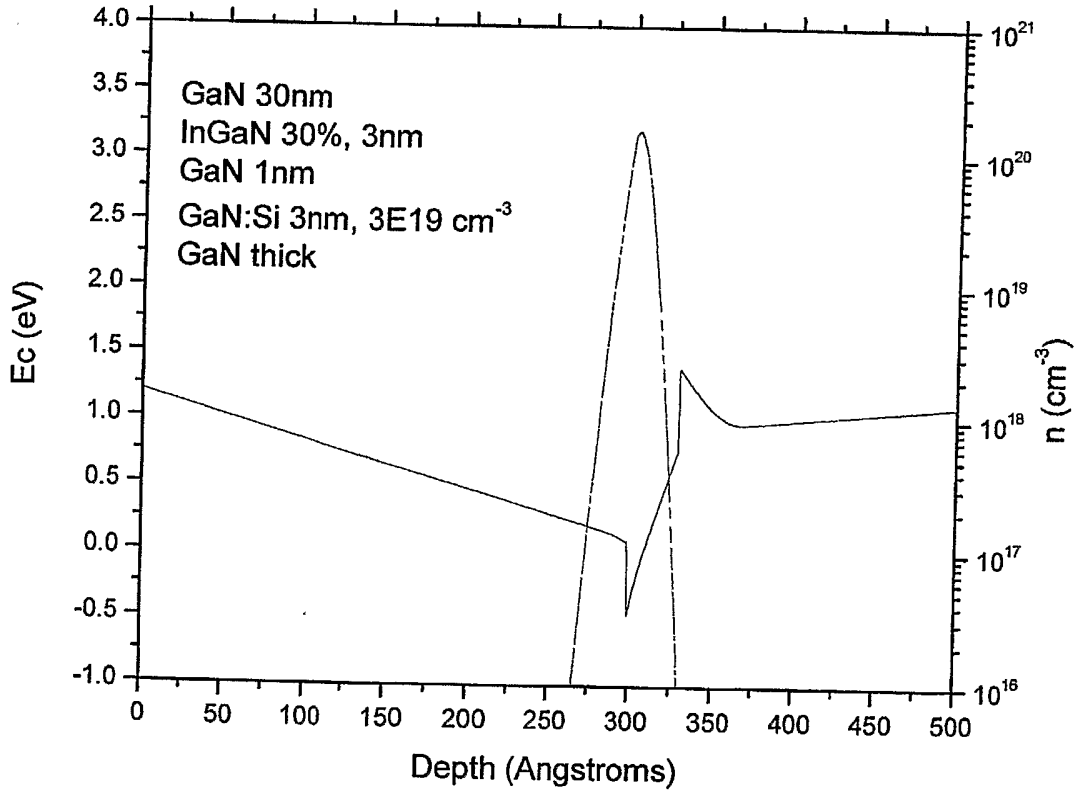


Figure 4H

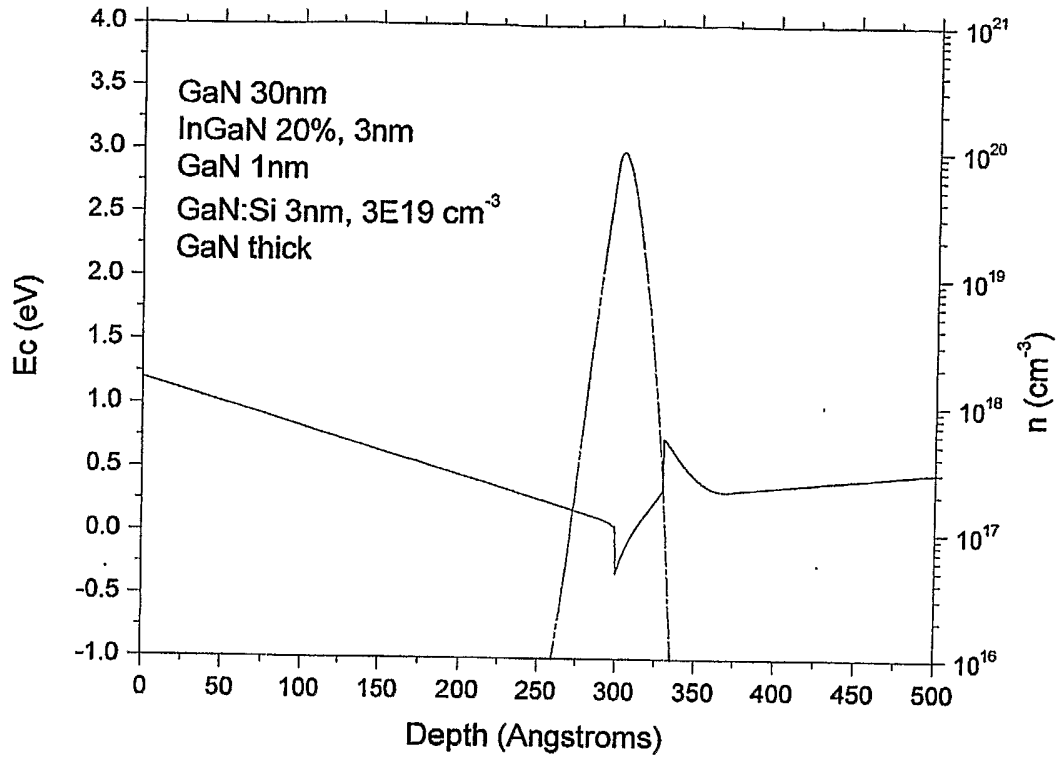


Figure 4I

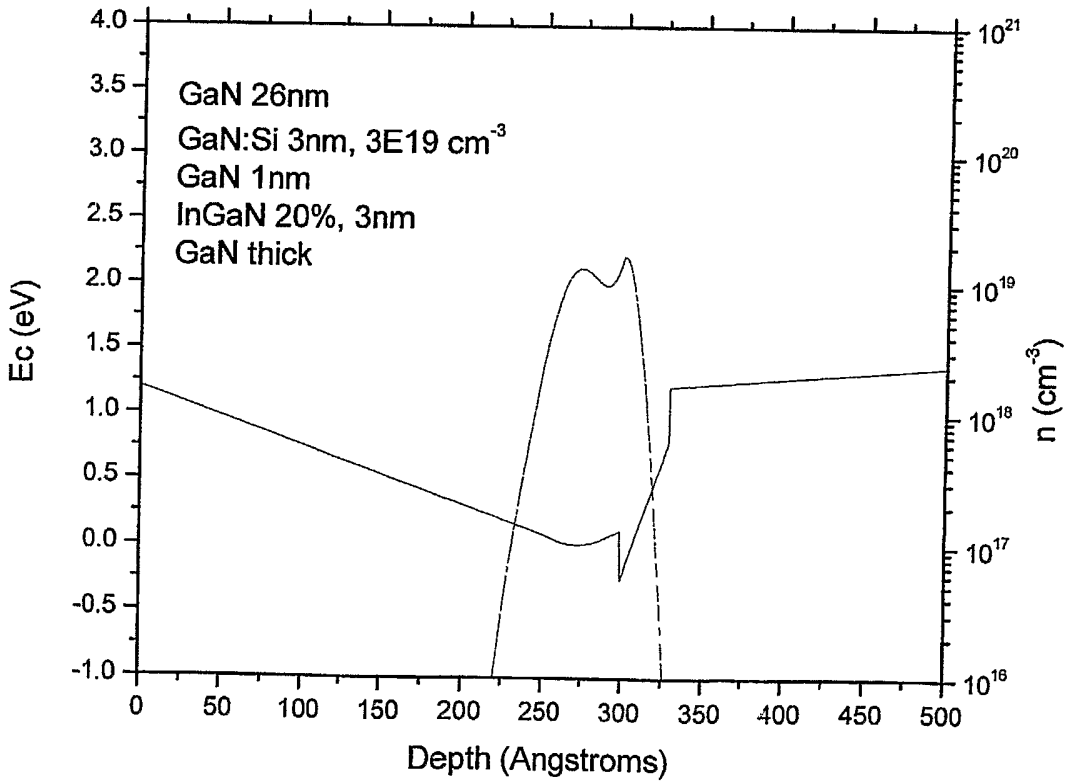


Figure 4J

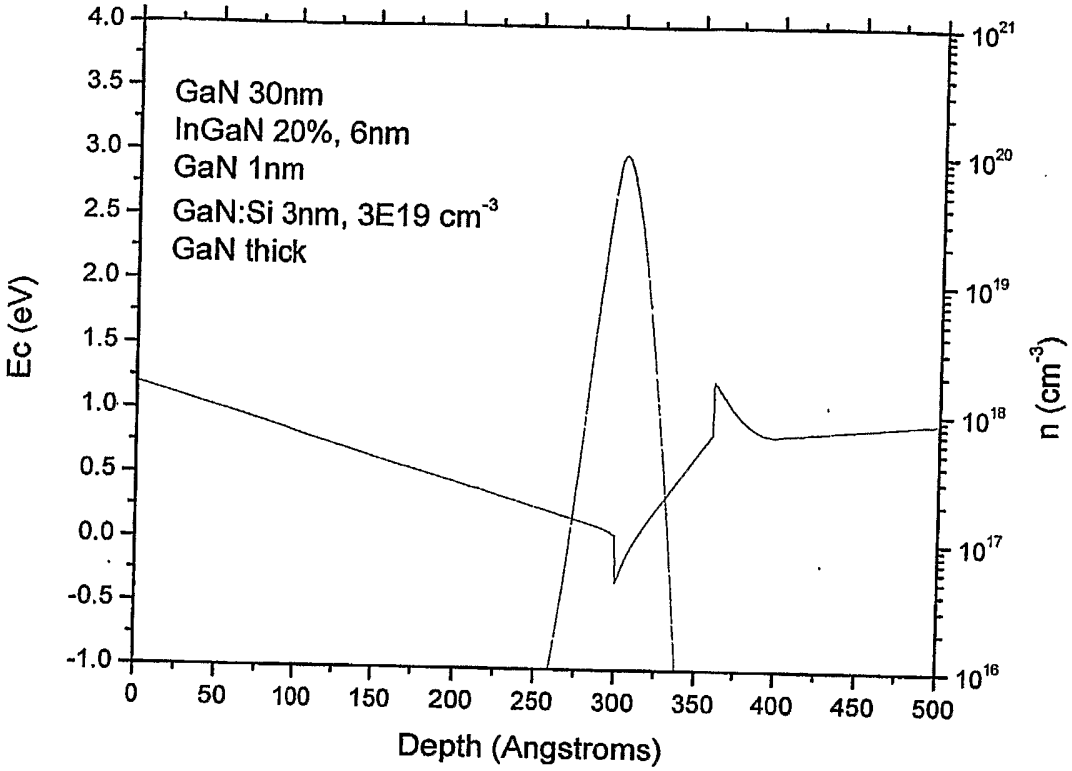


Figure 4K

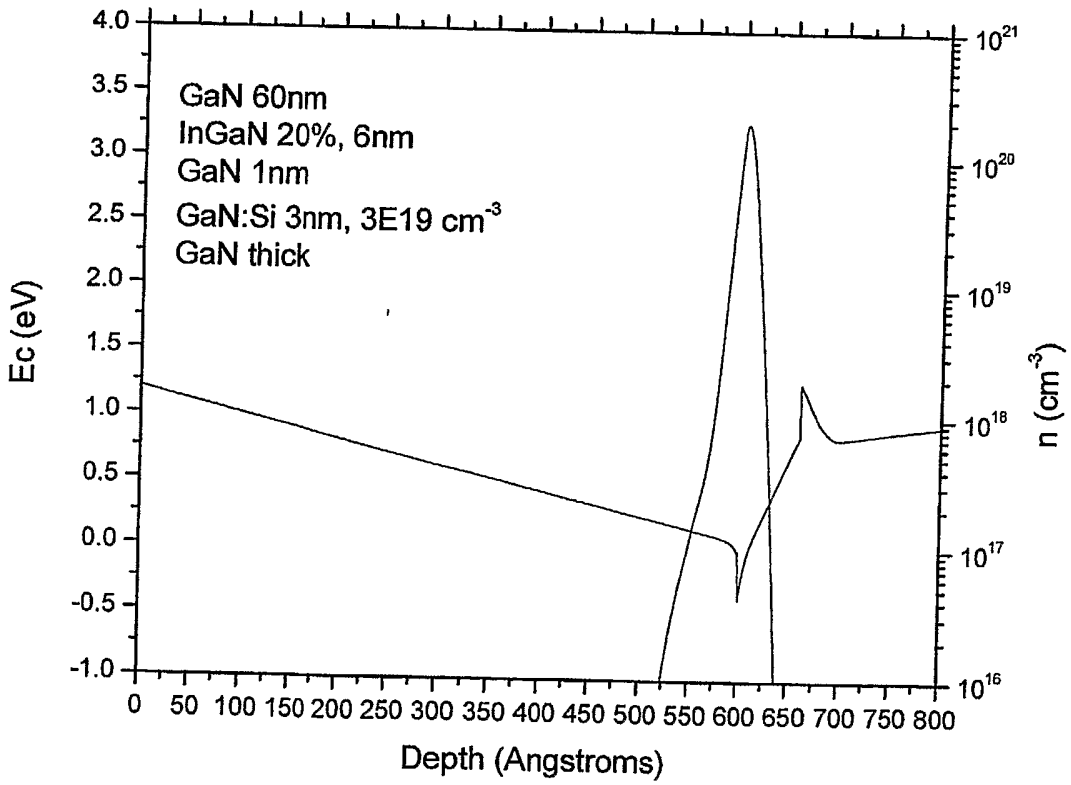


Figure 4L

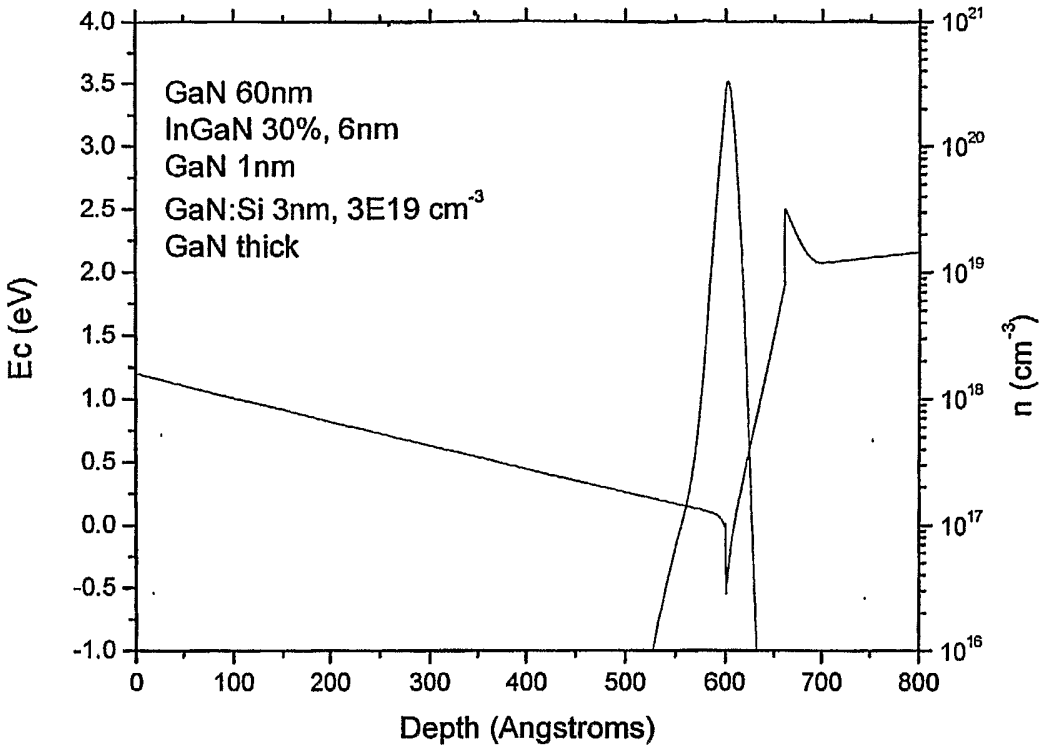


Figure 4M

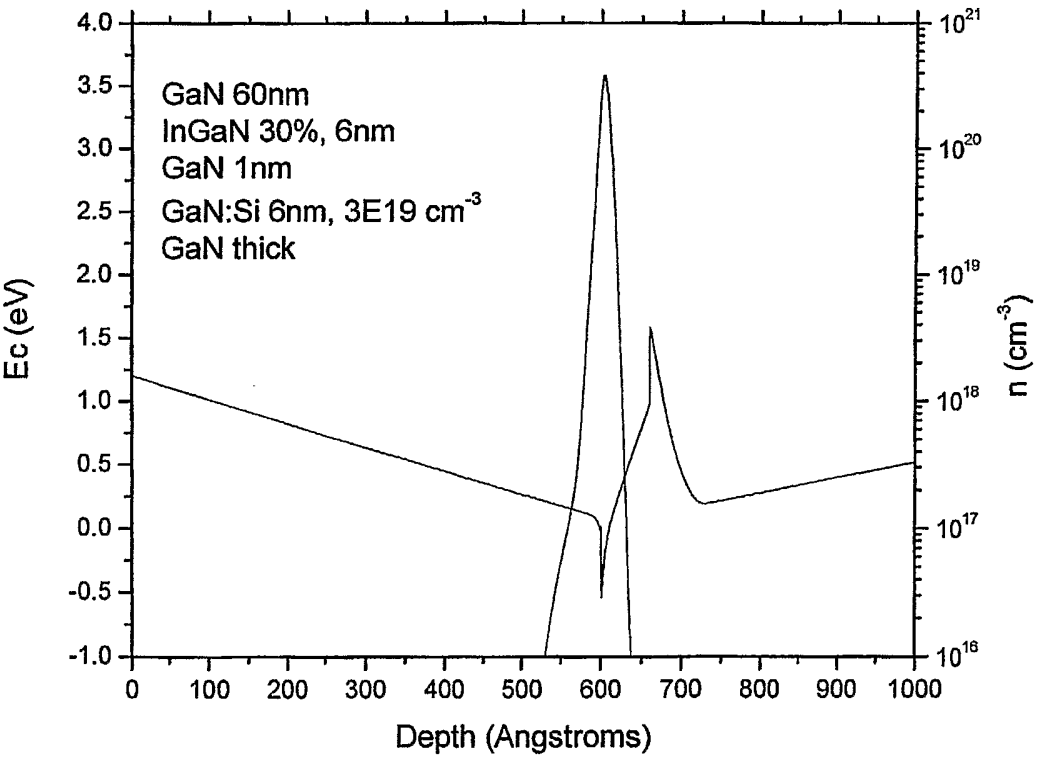


Figure 4N

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2006/006146

A. CLASSIFICATION OF SUBJECT MATTER
INV. H01L29/778 H01L29/812 H01L29/10 H01L29/20
ADD. H01L29/205

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal, WPI Data, INSPEC, COMPENDEX, IBM-TDB

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	WO 01/92428 A (KOHN ET AL.) 6 December 2001 (2001-12-06)	1-3, 6-17, 19-21, 29-33, 36-47, 49-51, 59,60, 63,64
Y	figures 1,5,8,11 page 6, lines 17-19 page 7, lines 15,16 page 8, lines 15-18	4,5, 23-28, 34,35, 53-58,68
	----- -/--	

[X] Further documents are listed in the continuation of Box C.

[X] See patent family annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
14 September 2006	25/09/2006

Name and mailing address of the ISA/	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL – 2280 HV Rijswijk Tel. (+31–70) 340–2040, Tx. 31 651 epo nl, Fax: (+31–70) 340–3016	Moehl, Sebastian

Form PCT/ISA/210 (second sheet) (April 2005)

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2006/006146

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 2003/218183 A1 (MICOVIC MIROSLAV ET AL) 27 November 2003 (2003-11-27) figure 18	29,30, 59,60
X	US 6 177 685 B1 (TERAGUCHI NOBUAKI ET AL) 23 January 2001 (2001-01-23)	1,6,7, 17,18, 20-22, 31,36, 37,47, 48, 50-52, 61,62
Y	figure 1 column 3, lines 29-43	4,5, 23-28, 34,35, 53-58,69
X	KONG Y C ET AL: "A novel InxGa1-xN/InN heterostructure field-effect transistor with extremely high two-dimensional electron-gas sheet density" SOLID STATE ELECTRONICS, ELSEVIER SCIENCE PUBLISHERS, BARKING, GB, vol. 49, no. 2, February 2005 (2005-02), pages 199-203, XP004645013 ISSN: 0038-1101	1,31, 65-67
Y	abstract	68,69

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No
PCT/US2006/006146

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
WO 0192428 A	06-12-2001	AU 8572901 A	11-12-2001
		EP 1292648 A2	19-03-2003
		JP 2003535481 T	25-11-2003
		US 2003155578 A1	21-08-2003
		US 2006113564 A1	01-06-2006
US 2003218183 A1	27-11-2003	NONE	
US 6177685 B1	23-01-2001	NONE	