United States Patent [19]

Sweeney

[11] **3,850,097**

[45] **Nov. 26, 1974**

[54] **HIGH SPEED PRINTERS WITH STAGGERED FONTS**

[75] Inventor: **David F. Sweeney,** Alamo, Calif.

[73] Assignee: **Mohawk Data Sciences Corporation,** East Herkimer, N.Y.

[22] Filed: **Apr. 18, 1973**

[21] Appl. No.: **352,162**

Related U.S. Application Data

[63] Continuation of Ser. No. 178,371, March 8, 1962, abandoned.

[52] **U.S. Cl.** ..... **101/93 C,** 197/49, 178/32, 340/172.5, 235/61.9

[51] **Int. Cl.** **B41j 5/00**

[58] **Field of Search** ..... 101/93 C, 99, 110, 94; 346/141; 235/58, 60, 61.9; 340/172.5, 318; 197/44–47, 49; 178/28–30, 32, 34

[56] **References Cited**

UNITED STATES PATENTS

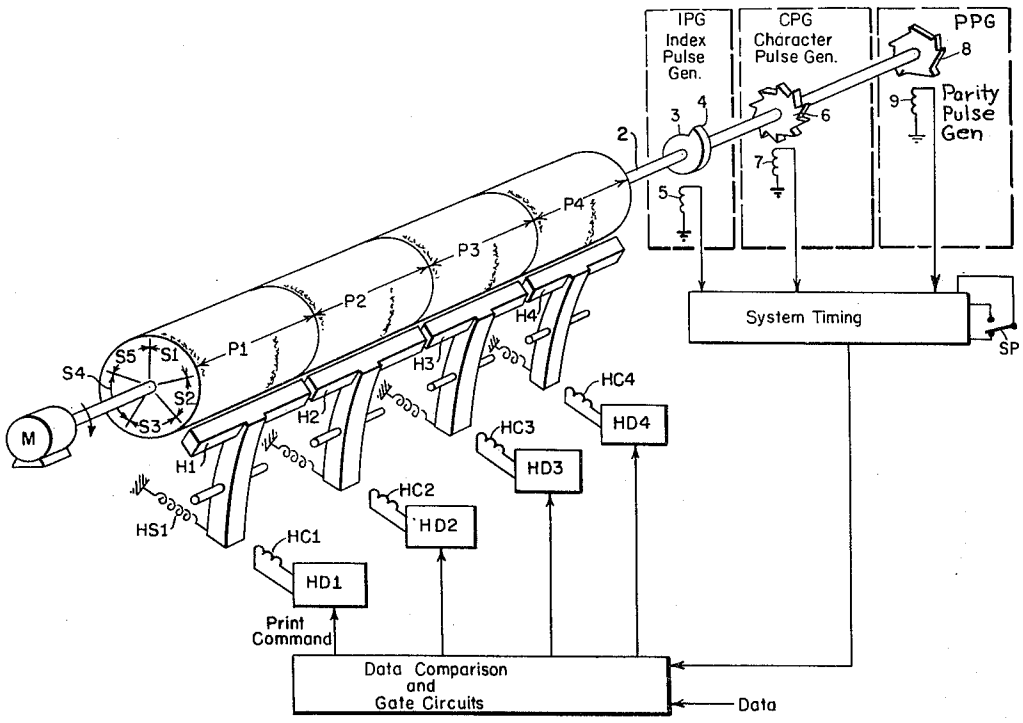
373,508	11/1887	Wiley	178/32 X
1,838,584	12/1931	Smith	101/94
1,933,650	11/1933	Bascom	340/318
2,658,106	11/1953	Hell	178/30
2,757,605	8/1956	Dumey	101/93 C
2,796,830	6/1957	Hilton	101/93 C
2,915,967	12/1959	Gehring et al.	101/93 C
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R26,240	7/1967	Wasserman	101/93 C

Primary Examiner—Robert E. Pulfrey
Assistant Examiner—E. H. Eickholt
Attorney, Agent, or Firm—Robert R. Hubbard; Richard H. Smith

[57] **ABSTRACT**

A high speed on-the-fly line printer employs print hammers which span five print positions and which are actuatable in sync with a continuously rotating print drum such that each hammer is adapted to print a character in each of the five print positions which it spans. The print drum has a separate font of type characters for each print position, the fonts associated with any one hammer being staggered about the periphery of the drum such that they scan past the hammer one font at a time (all the types of one font passing the hammer before any type of another font passes the hammer). The hammers are driven by electronic control means which generate hammer firing pulses through comparison of the data to be printed against character codes representing the print drum type characters as they come into alignment with the different print positions. The control means operate to fire each hammer a plurality of times to print a plurality of characters during a single revolution of the print drum. The control means inhibits the generation of hammer firing pulses during passage of alternate type fonts past each hammer, thereby permitting adequate hammer recovery time after each firing and enabling each hammer to print its five characters in less than two complete revolutions of the drum.

19 Claims, 34 Drawing Figures



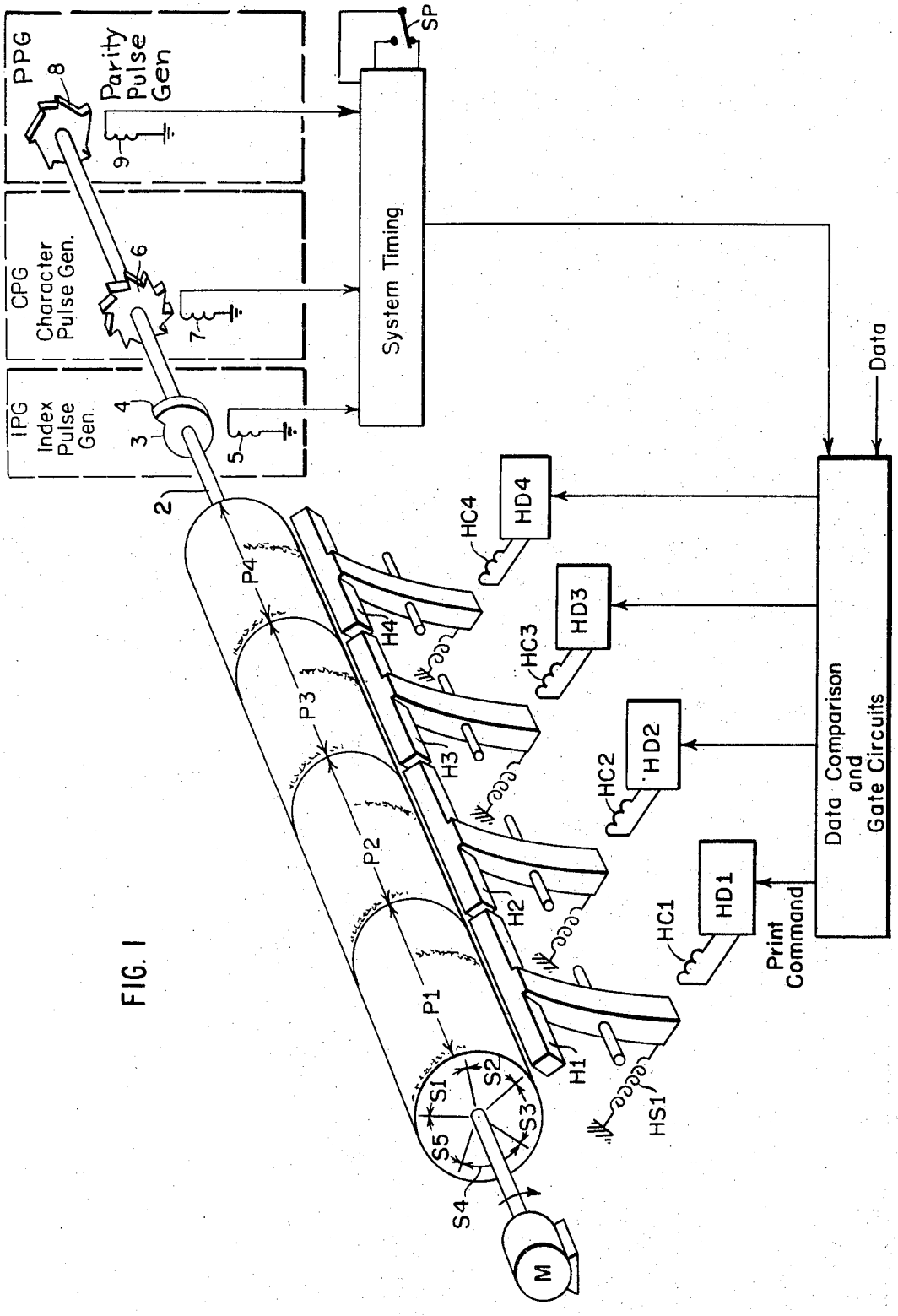

PPG
Parity Pulse Gen
8
9
CPG
Character Pulse Gen.
6
7
IPG
Index Pulse Gen.
4
3
5
2
SP
System Timing
Data
HC4
HD4
H4
HC3
HD3
H3
HC2
HD2
H2
HC1
HD1
H1
HS1
Print Command
Data Comparison and Gate Circuits
P4
P3
P2
P1
S1
S2
S3
S4
S5
M

FIG. 1

FIG. 2

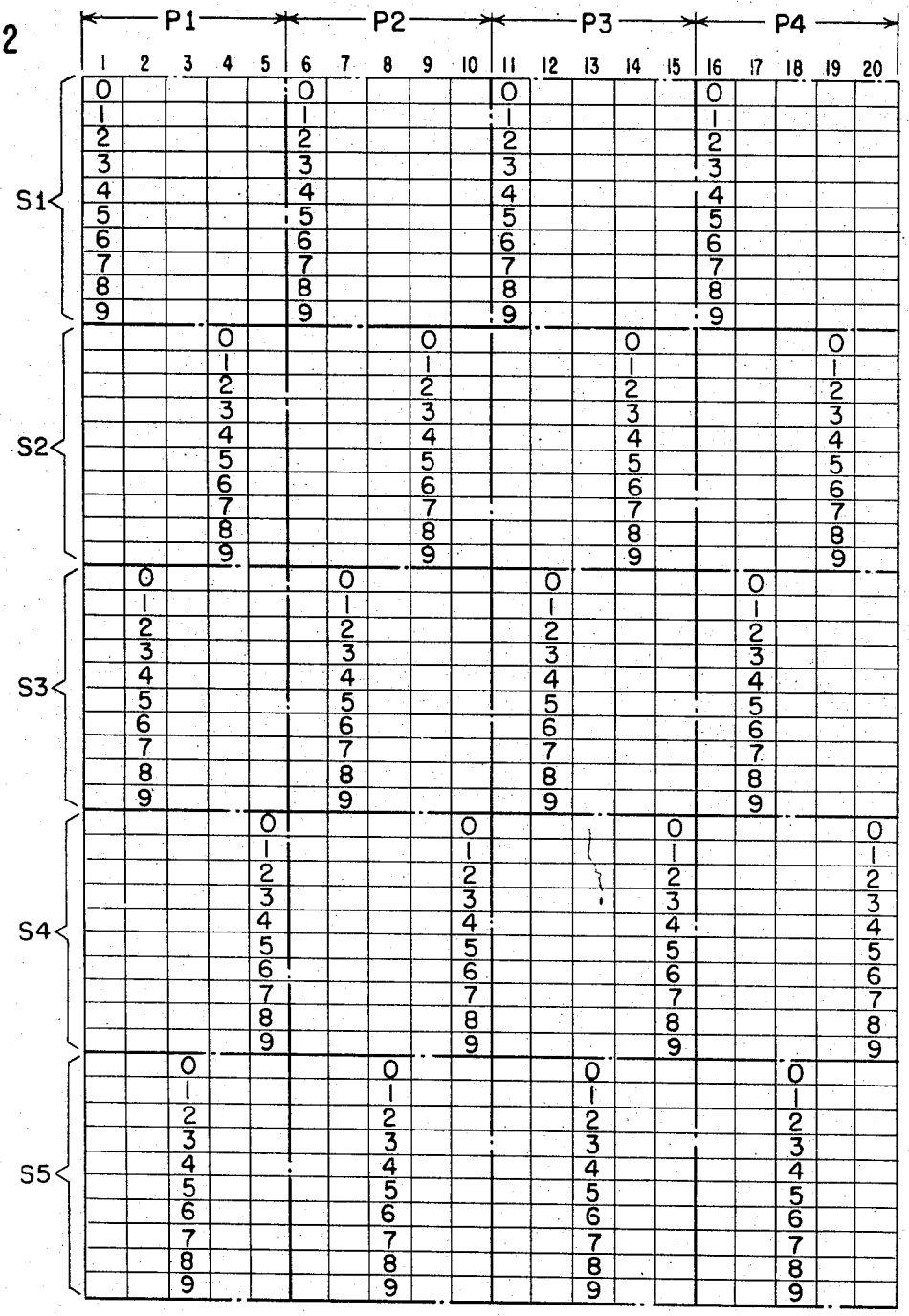

P1
P2
P3
P4
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20
S1
S2
S3
S4
S5

FIG. 3

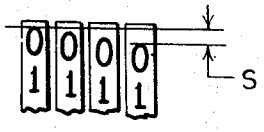
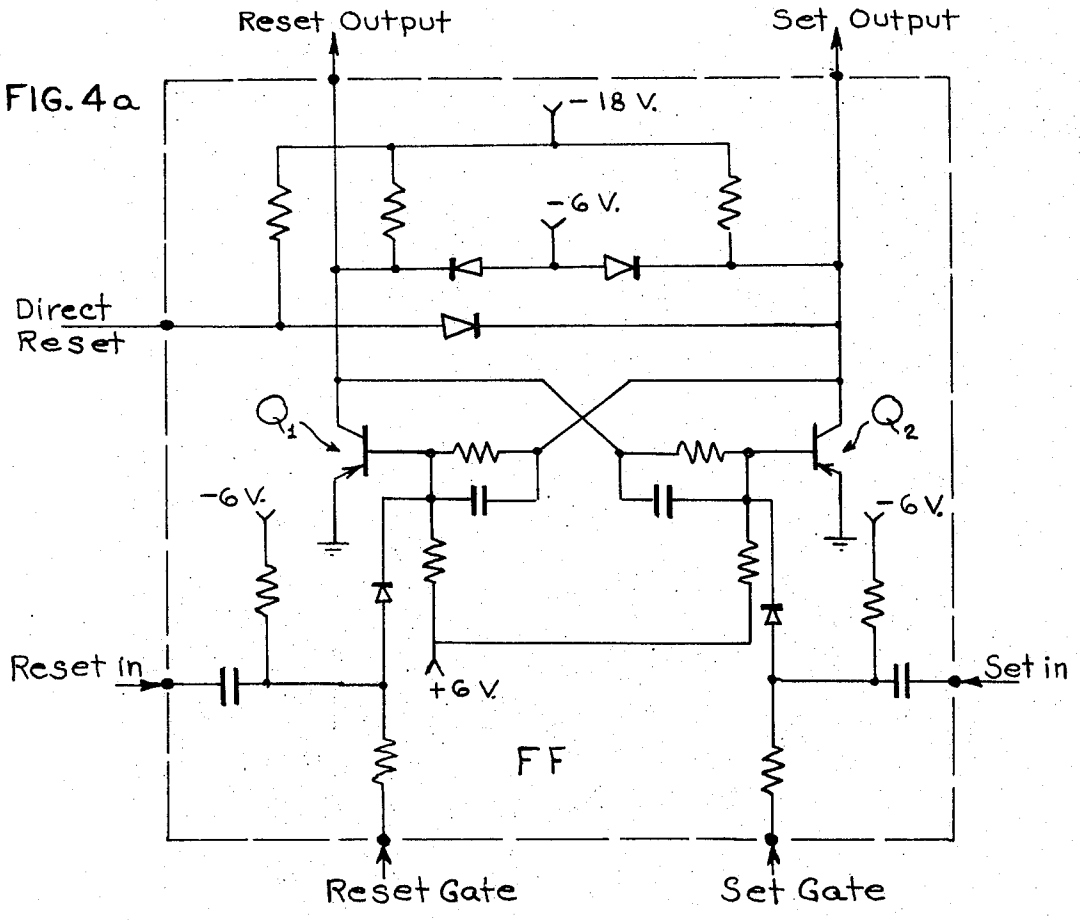

S

FIG. 4a



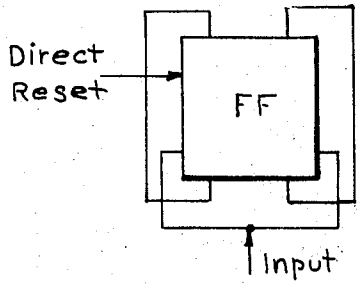


FIG. 4b

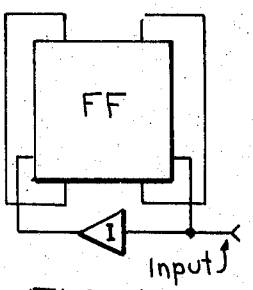


FIG. 4c

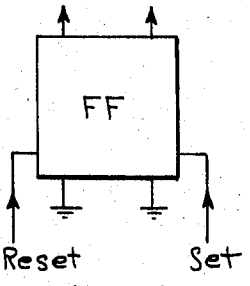


FIG. 4d

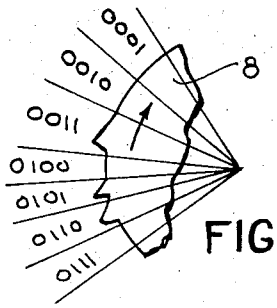


FIG. 5

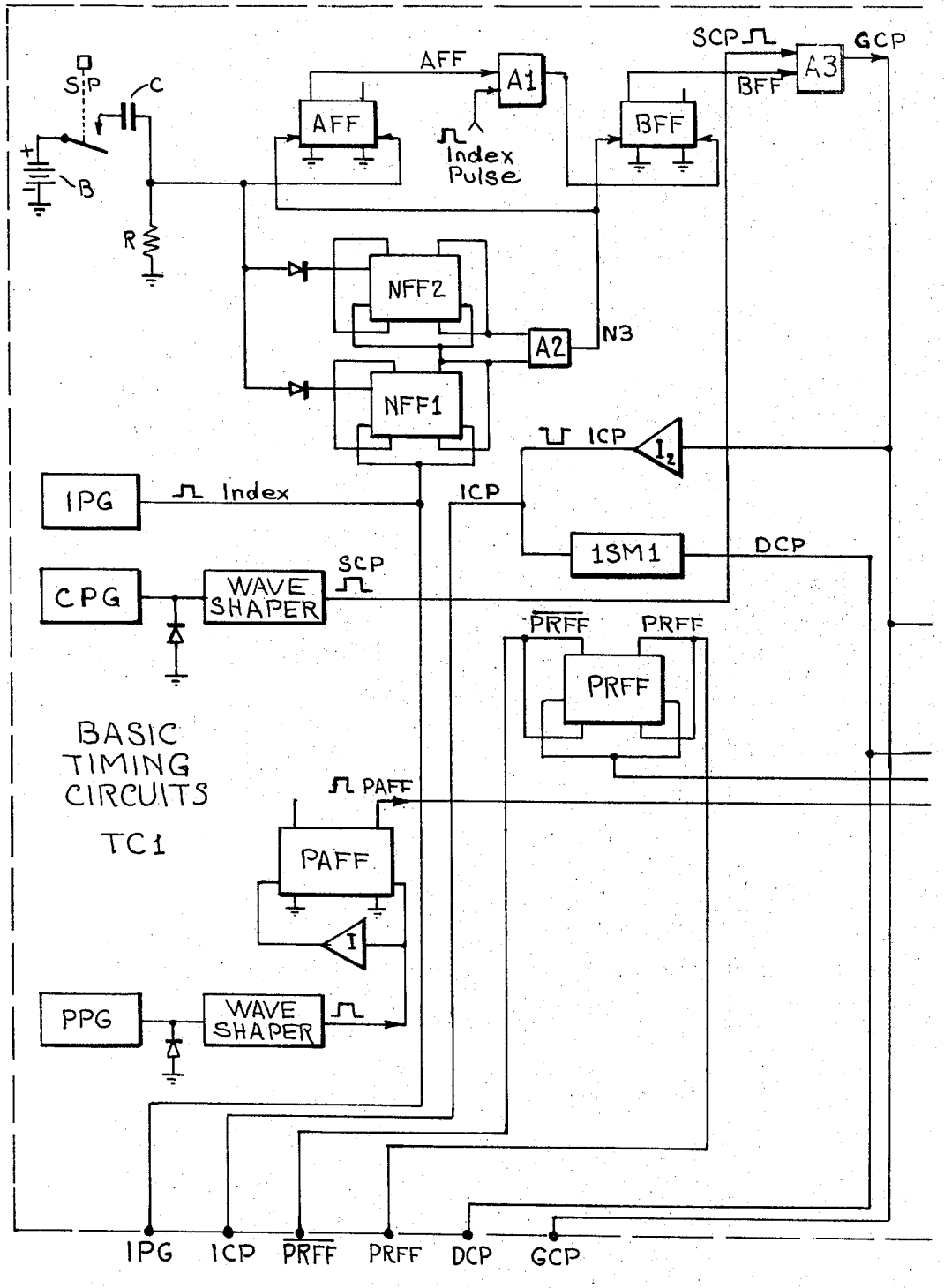

SCP
GCP
AFF
A1
A3
BFF
S
P
C
B
R
Index Pulse
NFF2
A2
N3
NFF1
ICP
I_2
IPG
Index
1SM1
DCP
CPG
WAVE SHAPER
PRFF
PAFF
I
PPG
BASIC TIMING CIRCUITS
TC1
IPG
ICP
PRFF
PRFF
DCP
GCP

FIG. 6a

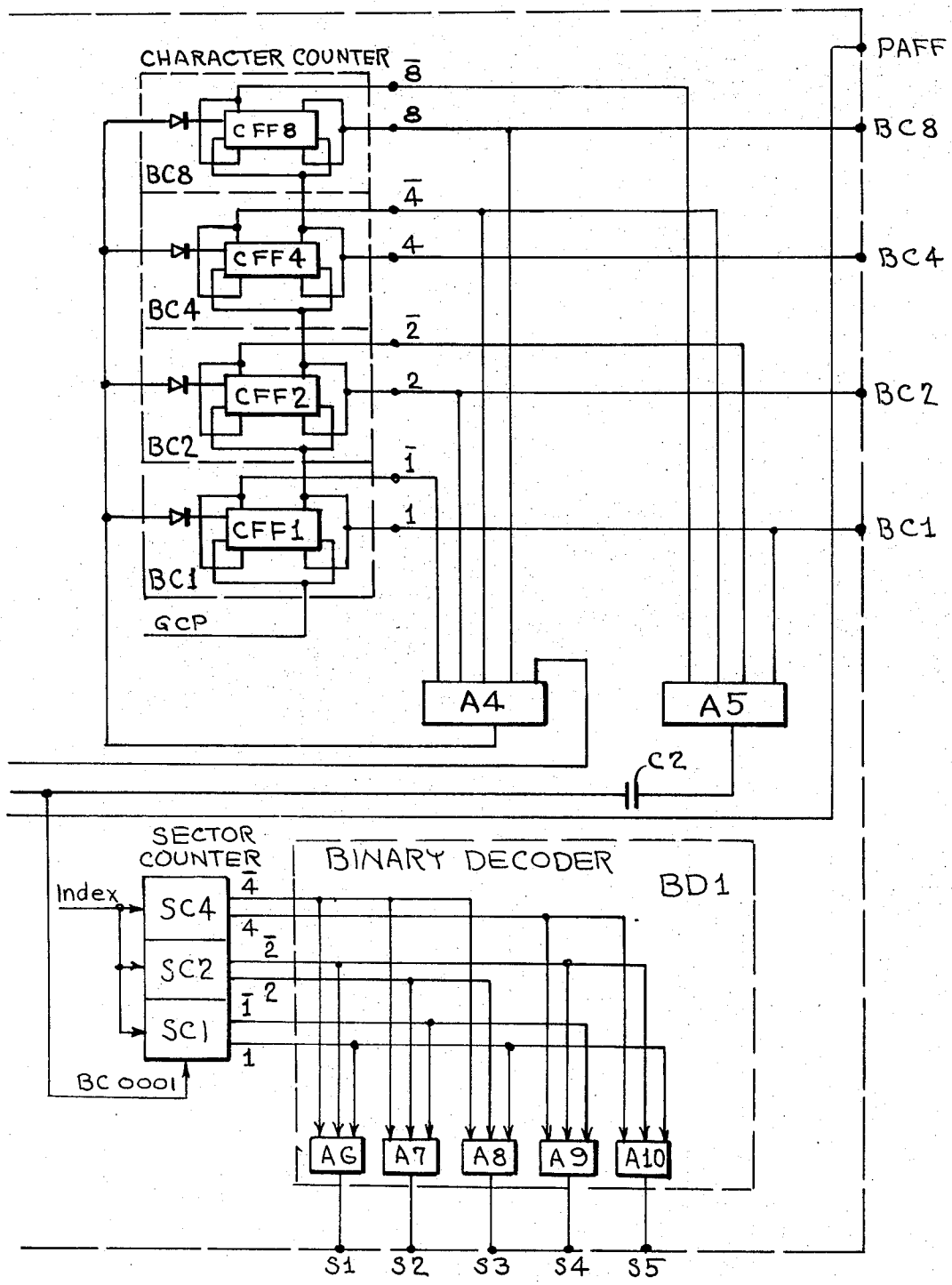

CHARACTER COUNTER
CFF8
CFF4
CFF2
CFF1
BC8
BC4
BC2
BC1
GCP
PAFF
A4
A5
C2
SECTOR COUNTER
Index
SC4
SC2
SC1
BC 0001
BINARY DECODER
BD1
A6
A7
A8
A9
A10
S1
S2
S3
S4
S5

FIG. 6 b

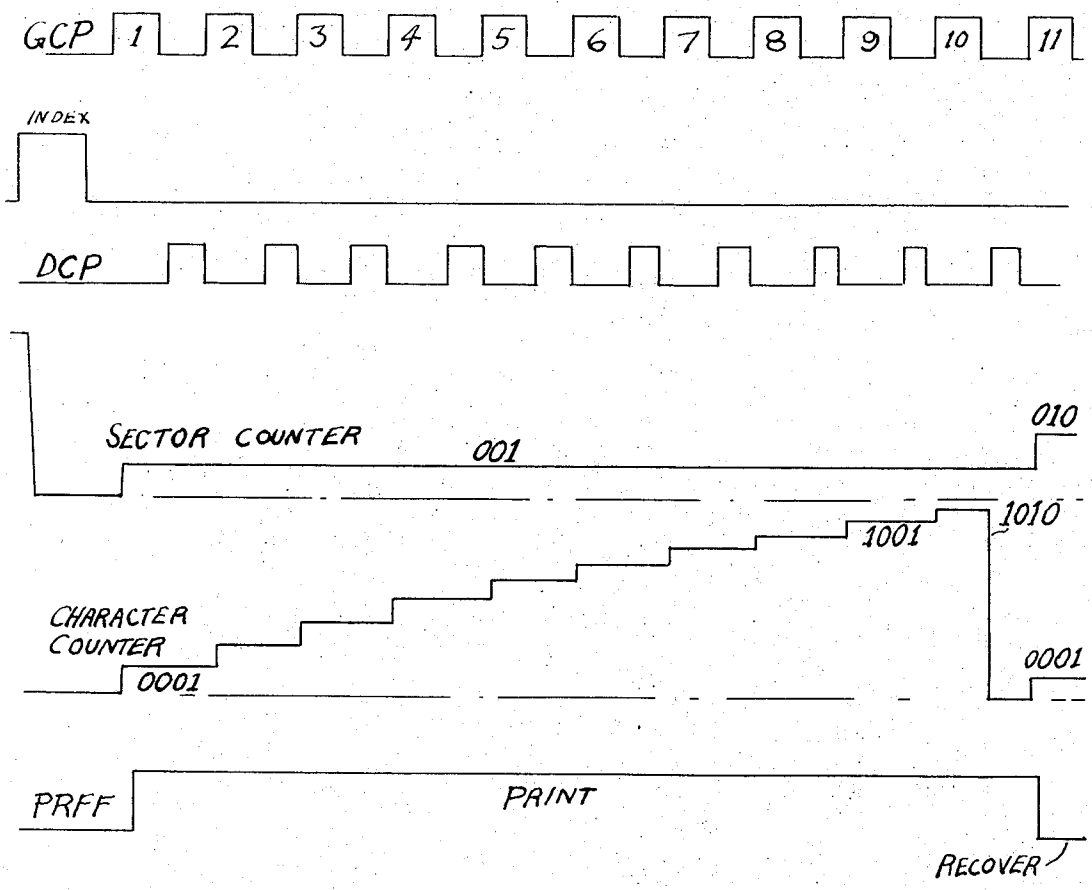

GCP
1
2
3
4
5
6
7
8
9
10
11
INDEX
DCP
SECTOR COUNTER
001
010
1001
1010
CHARACTER COUNTER
0001
0001
PRFF
PRINT
RECOVER

FIG. 7

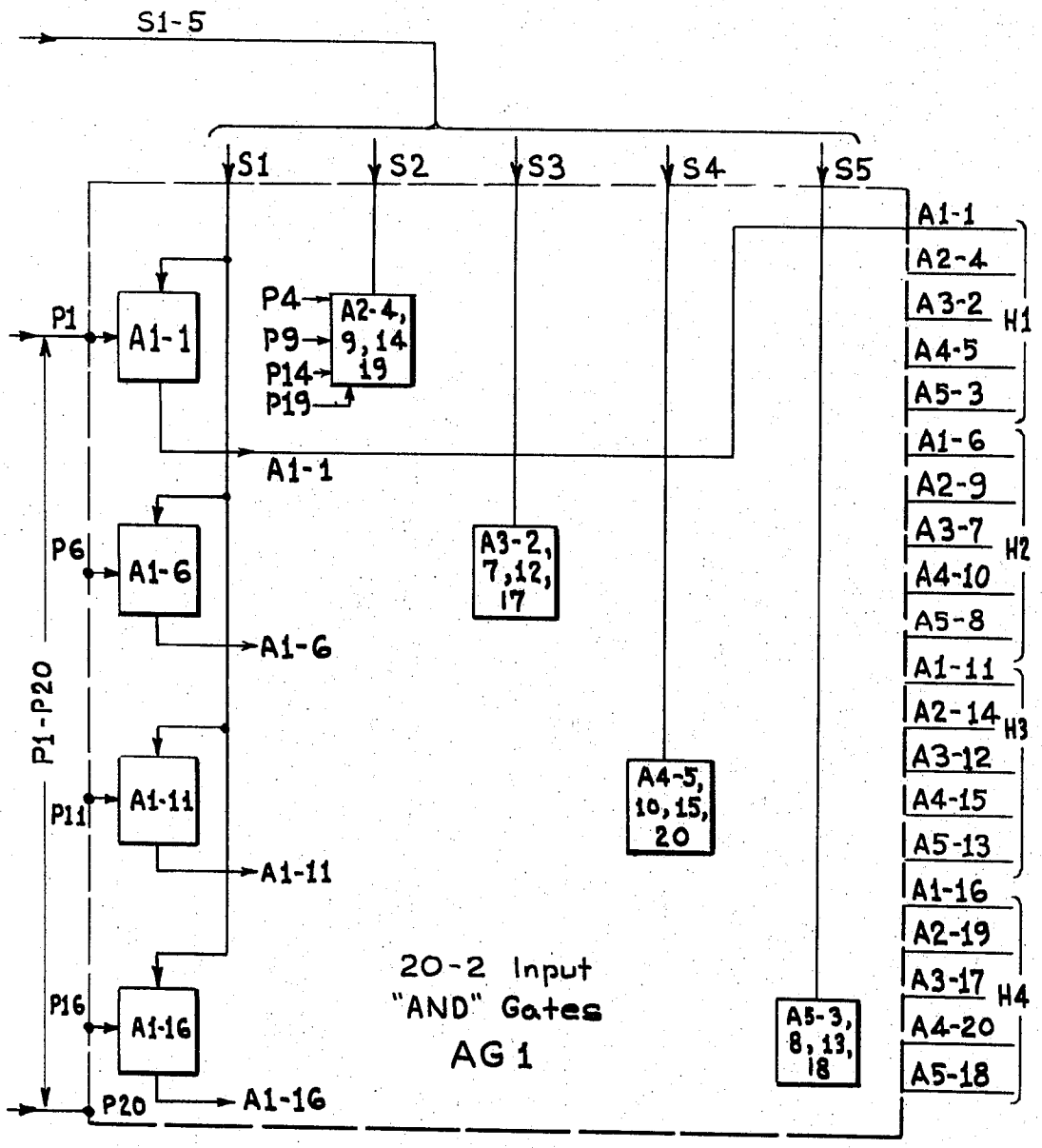

S1-5
S1
S2
S3
S4
S5
P1
A1-1
P4
P9
P14
P19
A2-4, 9, 14 19
A1-1
P6
A1-6
A1-6
A3-2, 7, 12, 17
P1-P20
P11
A1-11
A1-11
A4-5, 10, 15, 20
P16
A1-16
A1-16
P20
20-2 Input "AND" Gates
AG 1
A5-3, 8, 13, 18
A1-1
A2-4
A3-2
A4-5
A5-3
H1
A1-6
A2-9
A3-7
A4-10
A5-8
H2
A1-11
A2-14
A3-12
A4-15
A5-13
H3
A1-16
A2-19
A3-17
A4-20
A5-18
H4

FIG. 8 b

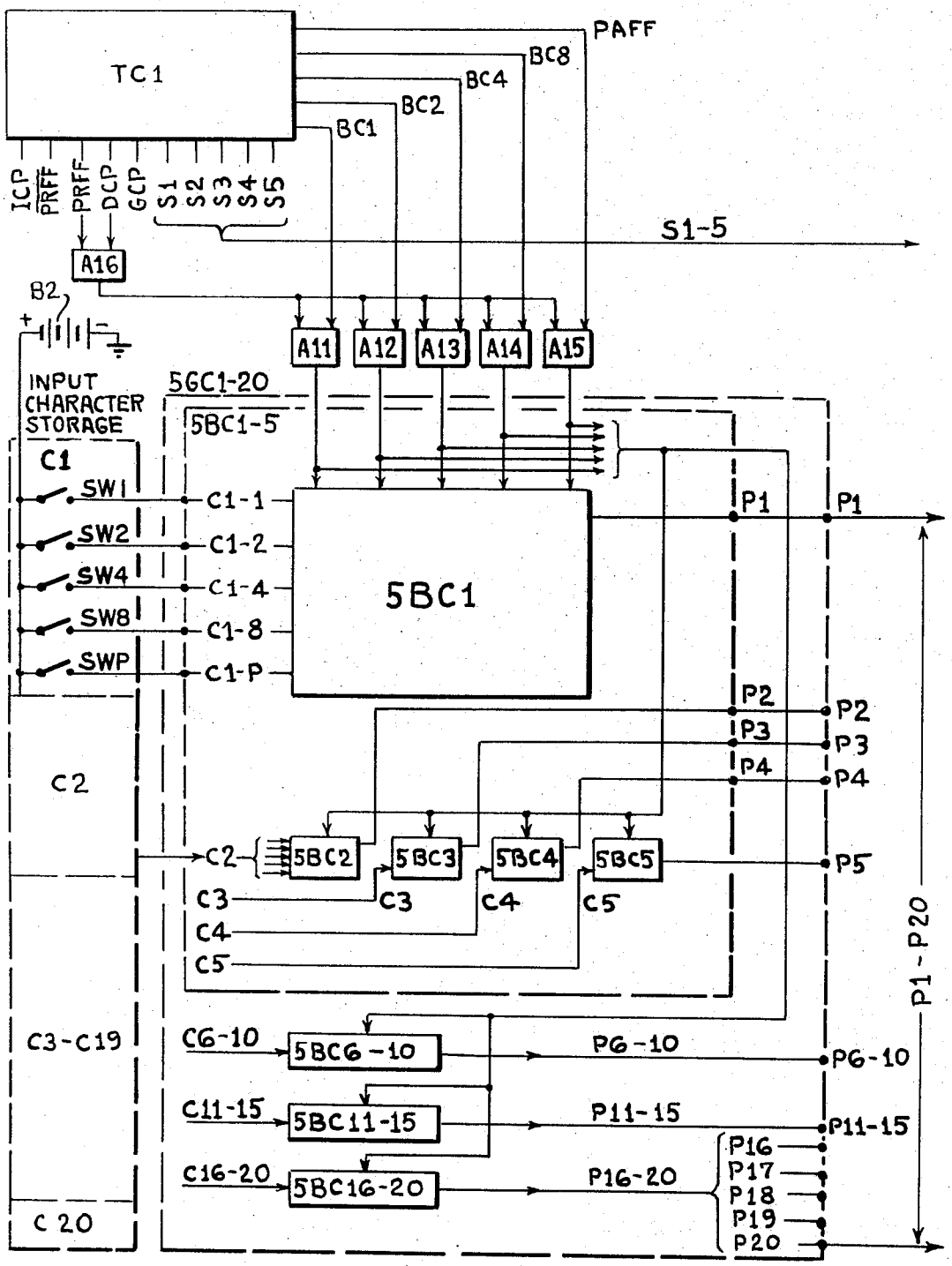

TC1
PAFF
BC8
BC4
BC2
BC1
ICP
PRFF
PRFF
DCP
GCP
S1
S2
S3
S4
S5
S1-5
A16
B2
A11
A12
A13
A14
A15
INPUT CHARACTER STORAGE
5GC1-20
5BC1-5
C1
SW1
SW2
SW4
SW8
SWP
C1-1
C1-2
C1-4
C1-8
C1-P
5BC1
P1
P1
P2
P2
P3
P3
P4
P4
P5
C2
C2
5BC2
5BC3
5BC4
5BC5
C3
C3
C4
C4
C5
C5
P1-P20
C3-C19
C6-10
5BC6-10
P6-10
P6-10
C11-15
5BC11-15
P11-15
P11-15
C16-20
5BC16-20
P16-20
P16
P17
P18
P19
P20
C 20

FIG. 8a

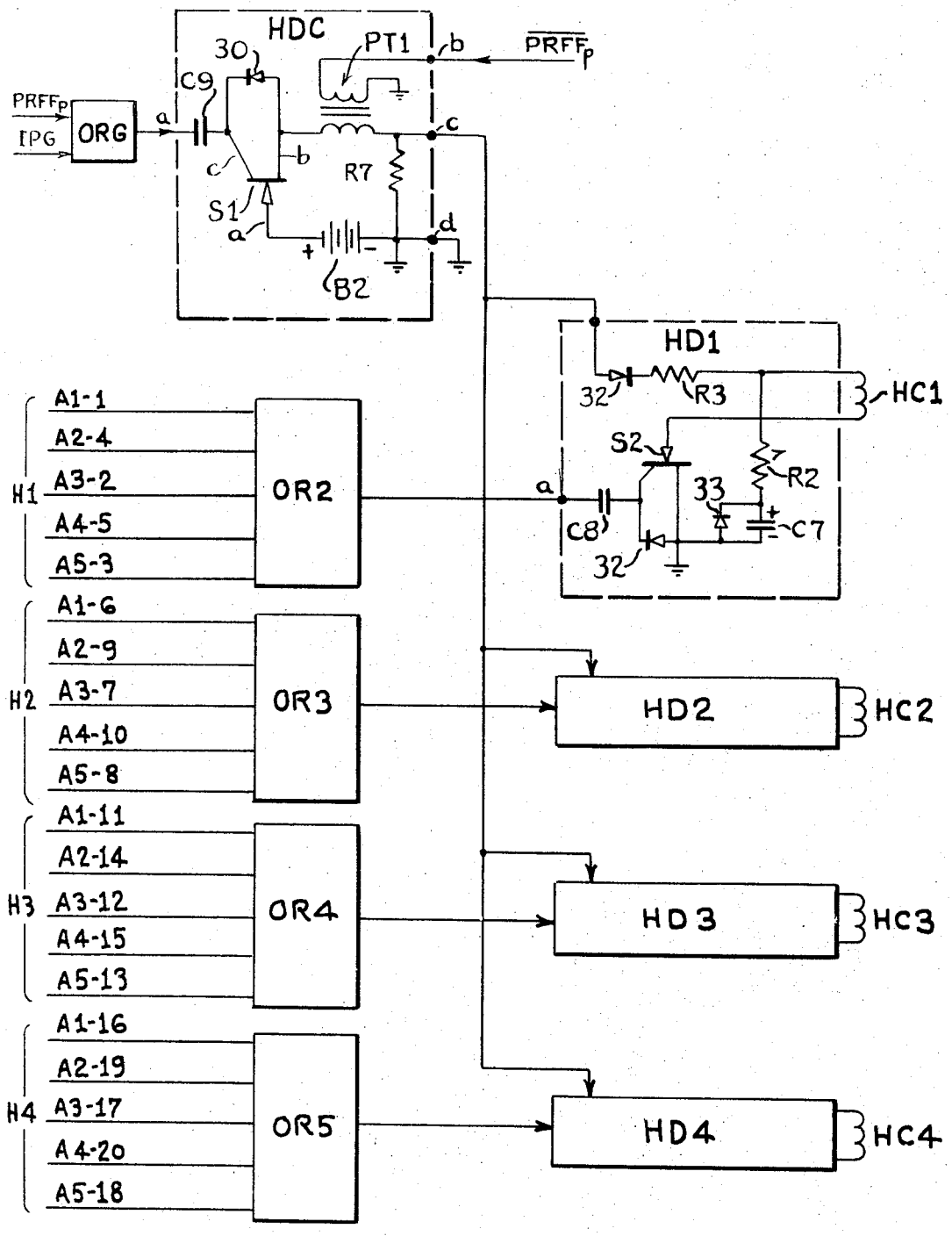

HDC
PT1
30
C9
PRFF$_P$
IPG
ORG
a
b
c
R7
S1
d
B2
HD1
32
R3
HC1
S2
R2
33
C8
C7
H1
A1-1
A2-4
A3-2
A4-5
A5-3
OR2
H2
A1-6
A2-9
A3-7
A4-10
A5-8
OR3
HD2
HC2
H3
A1-11
A2-14
A3-12
A4-15
A5-13
OR4
HD3
HC3
H4
A1-16
A2-19
A3-17
A4-20
A5-18
OR5
HD4
HC4

FIG. 8 c

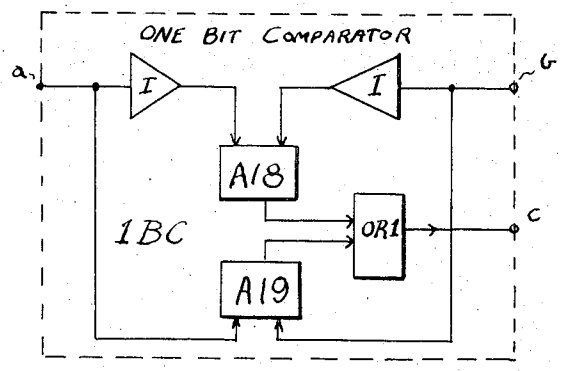


FIG. 9

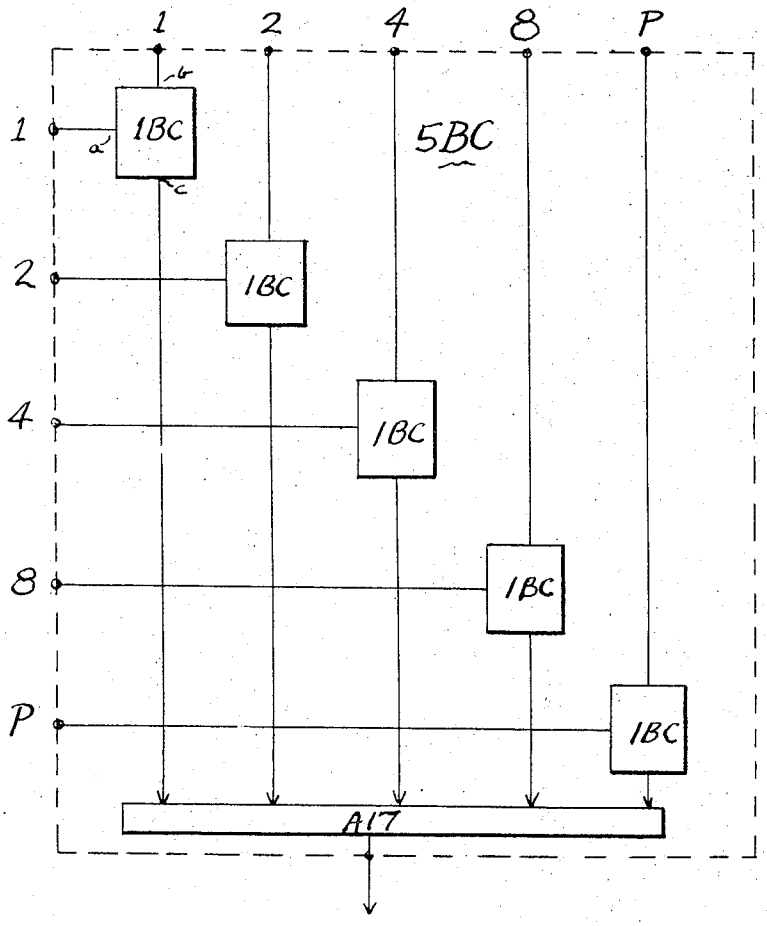


FIG. 10

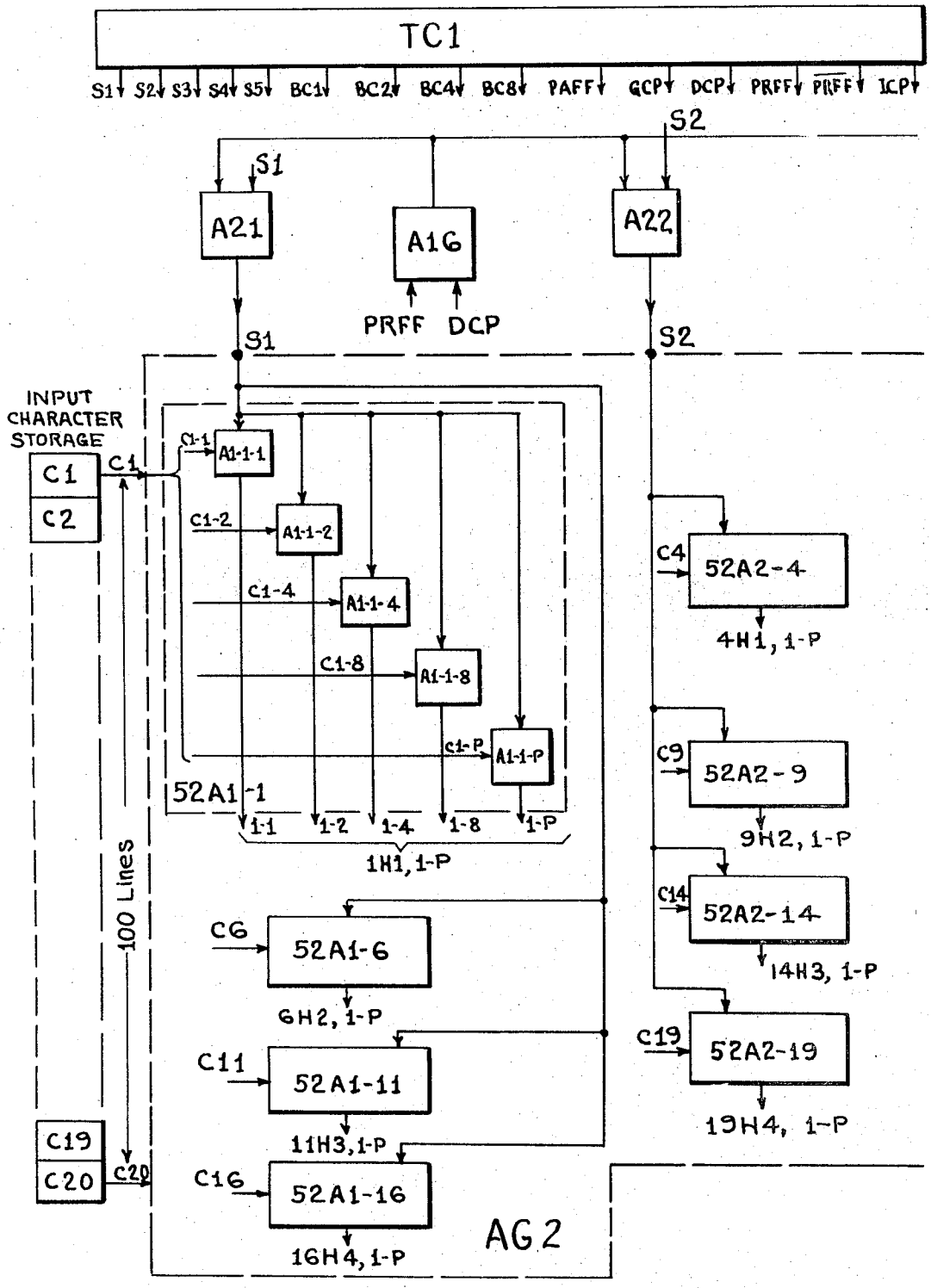

TC1
S1 S2 S3 S4 S5 BC1 BC2 BC4 BC8 PAFF GCP DCP PRFF PRFF ICP
S2
S1
A21
A16
A22
PRFF DCP
S1
S2
INPUT CHARACTER STORAGE
C1
C2
C1
C1-1
A1-1-1
C1-2
A1-1-2
C1-4
A1-1-4
C1-8
A1-1-8
C1-P
A1-1-P
52A1-1
1-1 1-2 1-4 1-8 1-P
1H1, 1-P
100 Lines
C19
C20
C20
C4
52A2-4
4H1, 1-P
C9
52A2-9
9H2, 1-P
C14
52A2-14
14H3, 1-P
C19
52A2-19
19H4, 1-P
C6
52A1-6
6H2, 1-P
C11
52A1-11
11H3, 1-P
C16
52A1-16
16H4, 1-P
AG2

FIG. 11a

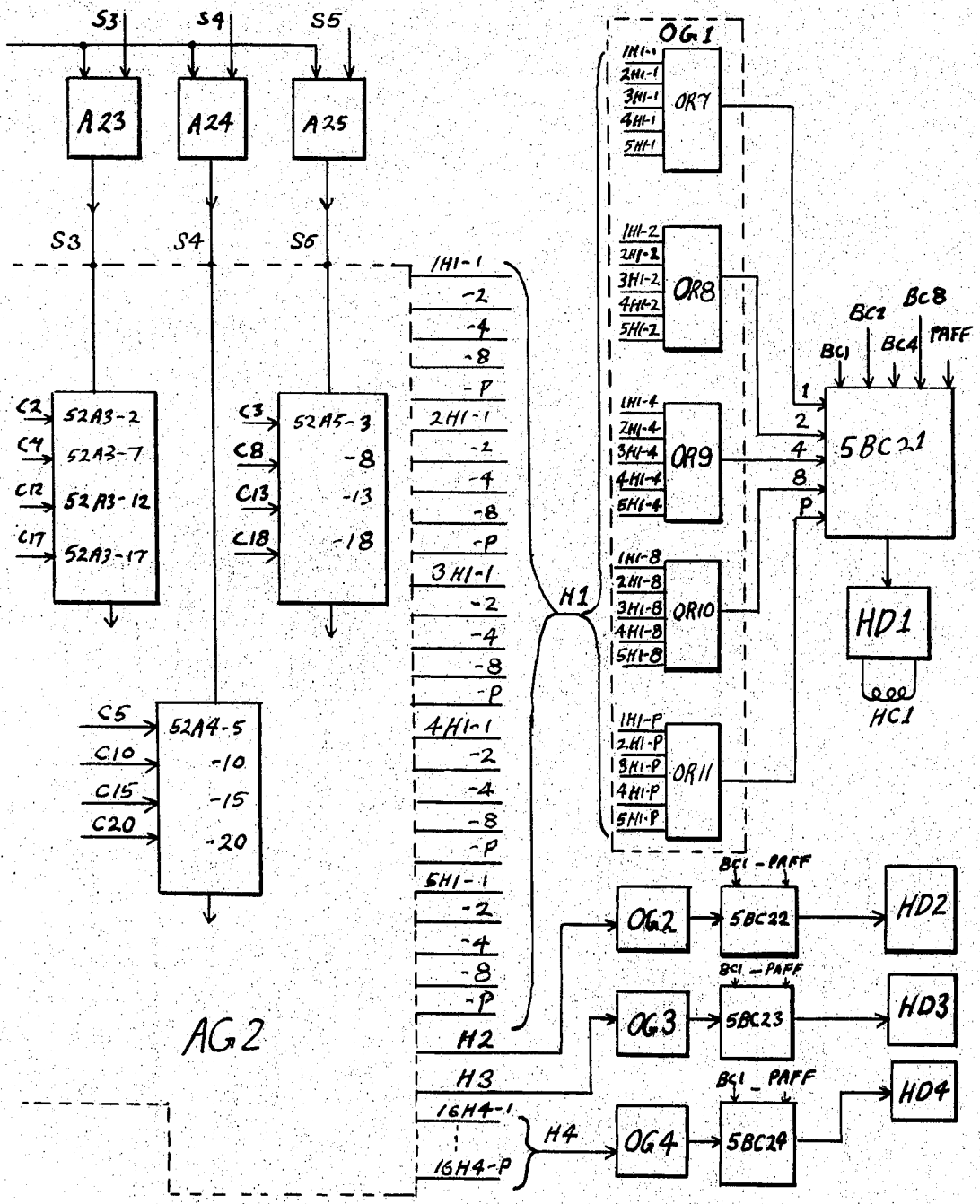

S3
S4
S5
A23
A24
A25
S3
S4
S6
1H1-1
-2
-4
-8
-P
2H1-1
-2
-4
-8
-P
3H1-1
-2
-4
-8
-P
4H1-1
-2
-4
-8
-P
5H1-1
-2
-4
-8
-P
H1
H2
H3
16H4-1
16H4-P
H4
C2
C4
C12
C17
52A3-2
52A3-7
52A3-12
52A3-17
C3
C8
C13
C18
52A5-3
-8
-13
-18
C5
C10
C15
C20
52A4-5
-10
-15
-20
AG2
OG1
1H1-1
2H1-1
3H1-1
4H1-1
5H1-1
OR7
1H1-2
2H1-2
3H1-2
4H1-2
5H1-2
OR8
1H1-4
2H1-4
3H1-4
4H1-4
5H1-4
OR9
1H1-8
2H1-8
3H1-8
4H1-8
5H1-8
OR10
1H1-P
2H1-P
3H1-P
4H1-P
5H1-P
OR11
BC1
BC2
BC4
BC8
PAFF
1
2
4
8
P
5BC21
HD1
HC1
OG2
5BC22
HD2
OG3
5BC23
HD3
OG4
5BC24
HD4
BC1 - PAFF

FIG. 11b

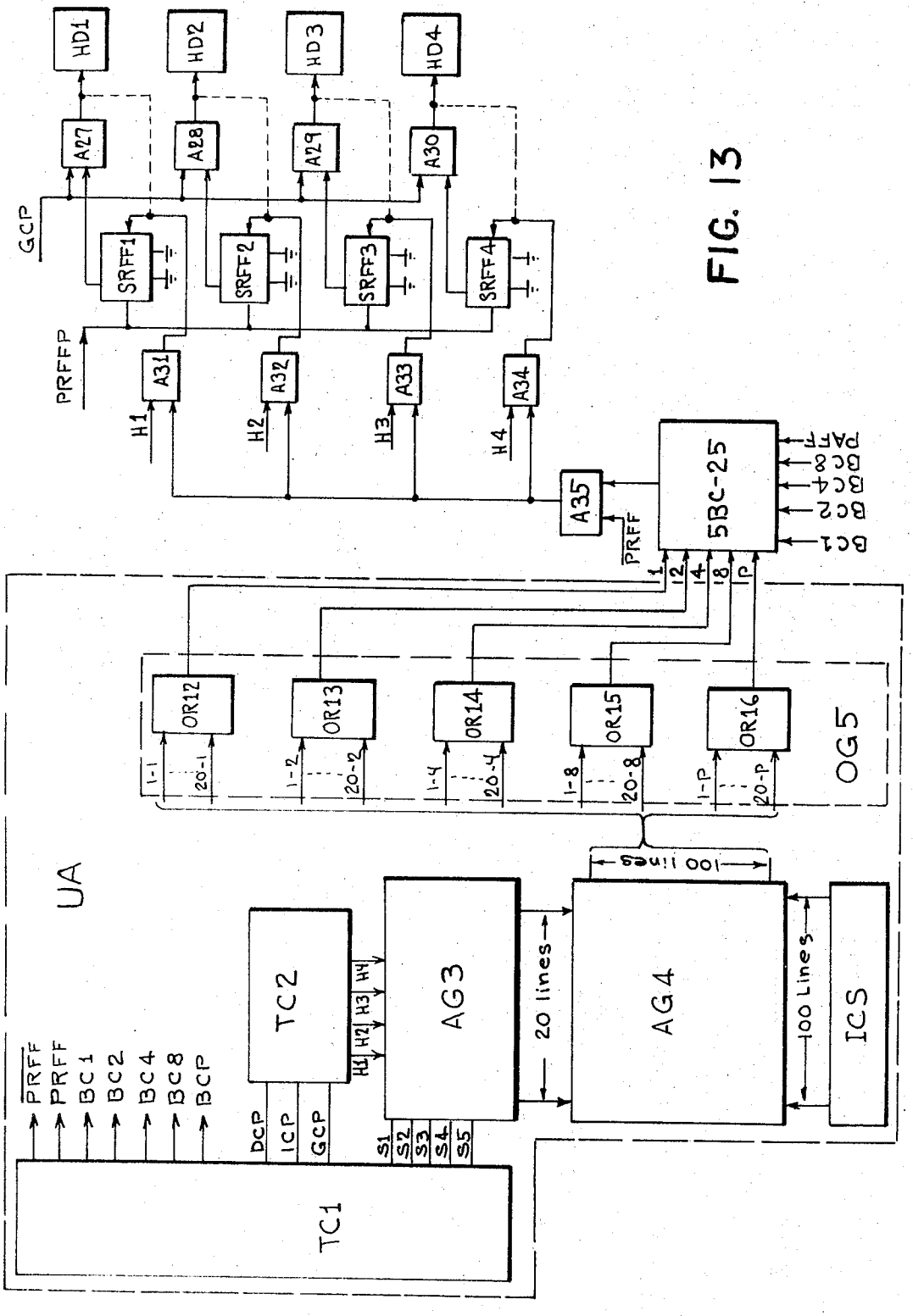

HD1
HD2
HD3
HD4
A27
A28
A29
A30
GCP
SRFF1
SRFF2
SRFF3
SRFF4
PRFFP
A31
A32
A33
A34
H1
H2
H3
H4
A35
PRFF
5BC-25
PAFF
BC8
BC4
BC2
BC1
1
12
14
8
1P
OR12
OR13
OR14
OR15
OR16
1-1
20-1
1-2
20-2
1-4
20-4
1-8
20-8
1-P
20-P
OG5
100 lines
UA
TC2
AG3
AG4
ICS
20 lines
100 Lines
PRFF
PRFF
BC1
BC2
BC4
BC8
BCP
DCP
ICP
GCP
H1
H2
H3
H4
S1
S2
S3
S4
S5
TC1

FIG. 13

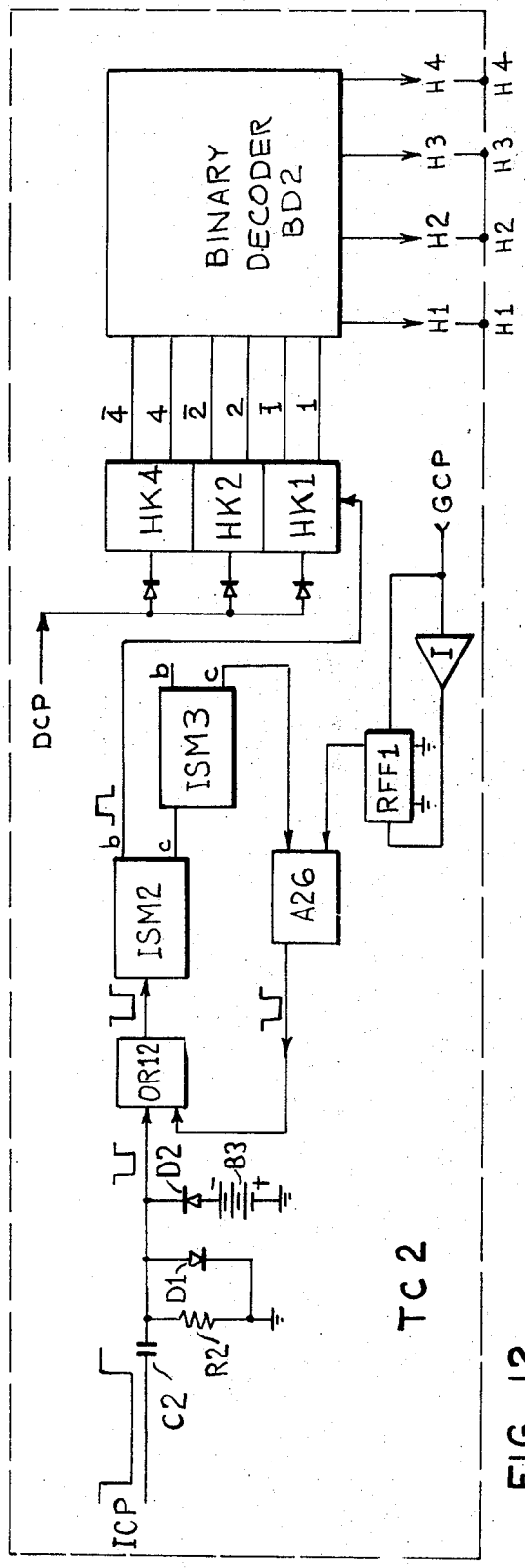

BINARY DECODER BD2
H4
H3
H2
H1
4̄
4
2̄
2
1̄
1
HK4
HK2
HK1
GCP
DCP
ISM3
ISM2
A26
RFF1
I
OR12
D2
B3
D1
R2
C2
ICP
TC 2

FIG. 12

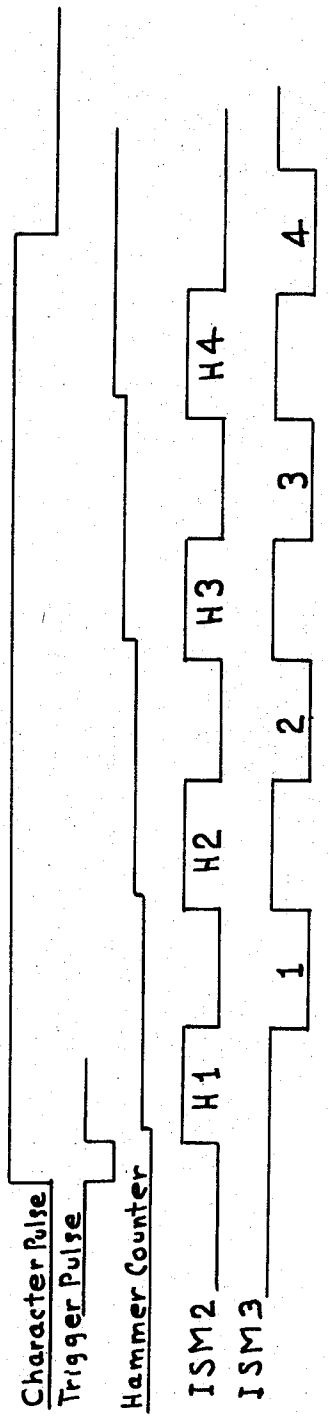

Character Pulse
Trigger Pulse
Hammer Counter
ISM2
ISM3
H1
H2
H3
H4
1
2
3
4

FIG. 16

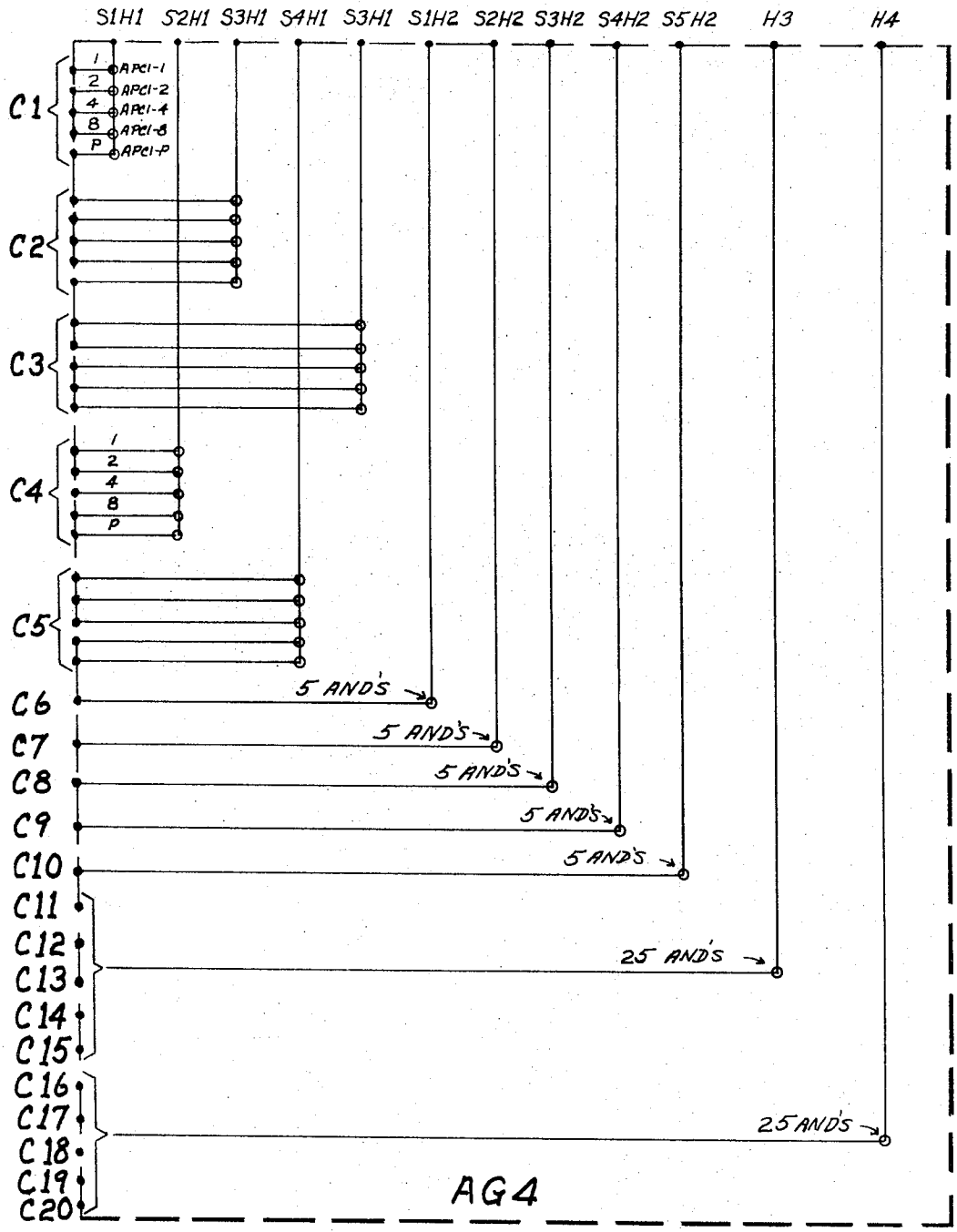

S1H1
S2H1
S3H1
S4H1
S3H1
S1H2
S2H2
S3H2
S4H2
S5H2
H3
H4
C1
1
2
4
8
P
APc1-1
APc1-2
APc1-4
APc1-8
APc1-P
C2
C3
C4
1
2
4
8
P
C5
C6
C7
C8
C9
C10
C11
C12
C13
C14
C15
C16
C17
C18
C19
C20
5 AND'S
5 AND'S
5 AND'S
5 AND'S
5 AND'S
25 AND'S
25 AND'S
AG4

FIG. 15

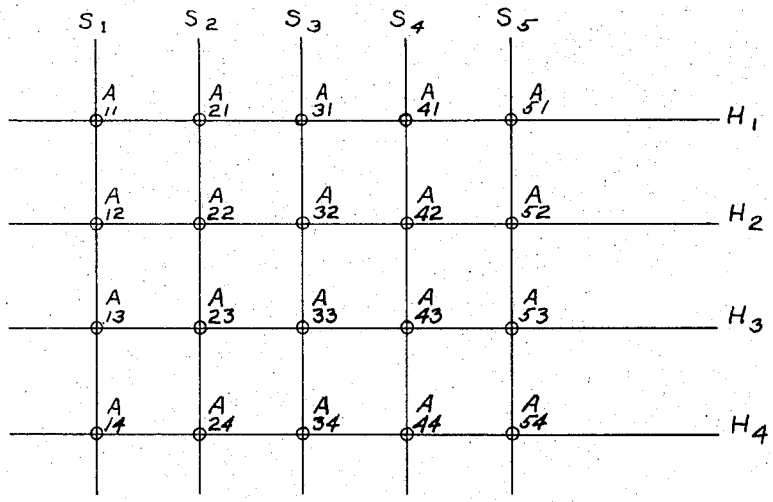

S1
S2
S3
S4
S5
A11
A21
A31
A41
A51
H1
A12
A22
A32
A42
A52
H2
A13
A23
A33
A43
A53
H3
A14
A24
A34
A44
A54
H4

FIG. 14

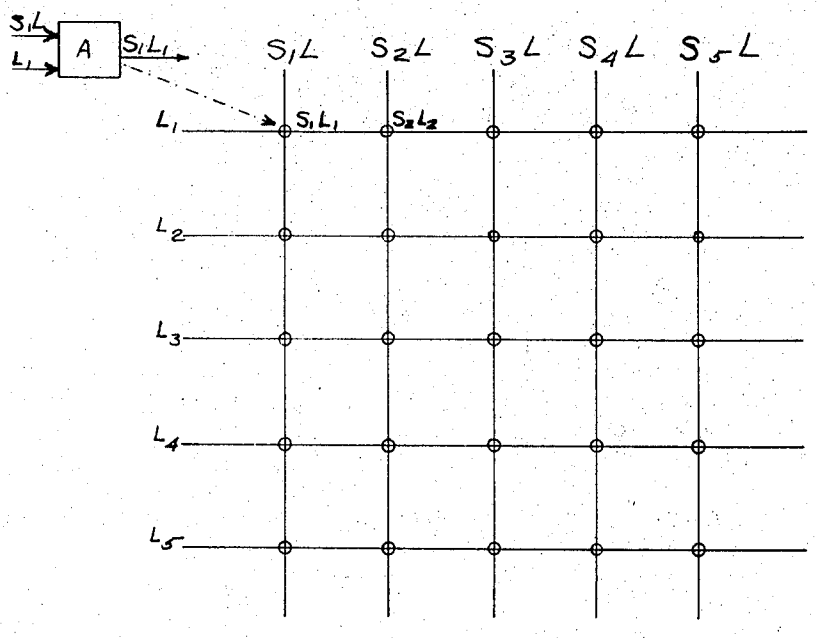

S1L
L1
A
S1L1
S1L
S2L
S3L
S4L
S5L
L1
S1L1
S2L2
L2
L3
L4
L5

FIG. 23

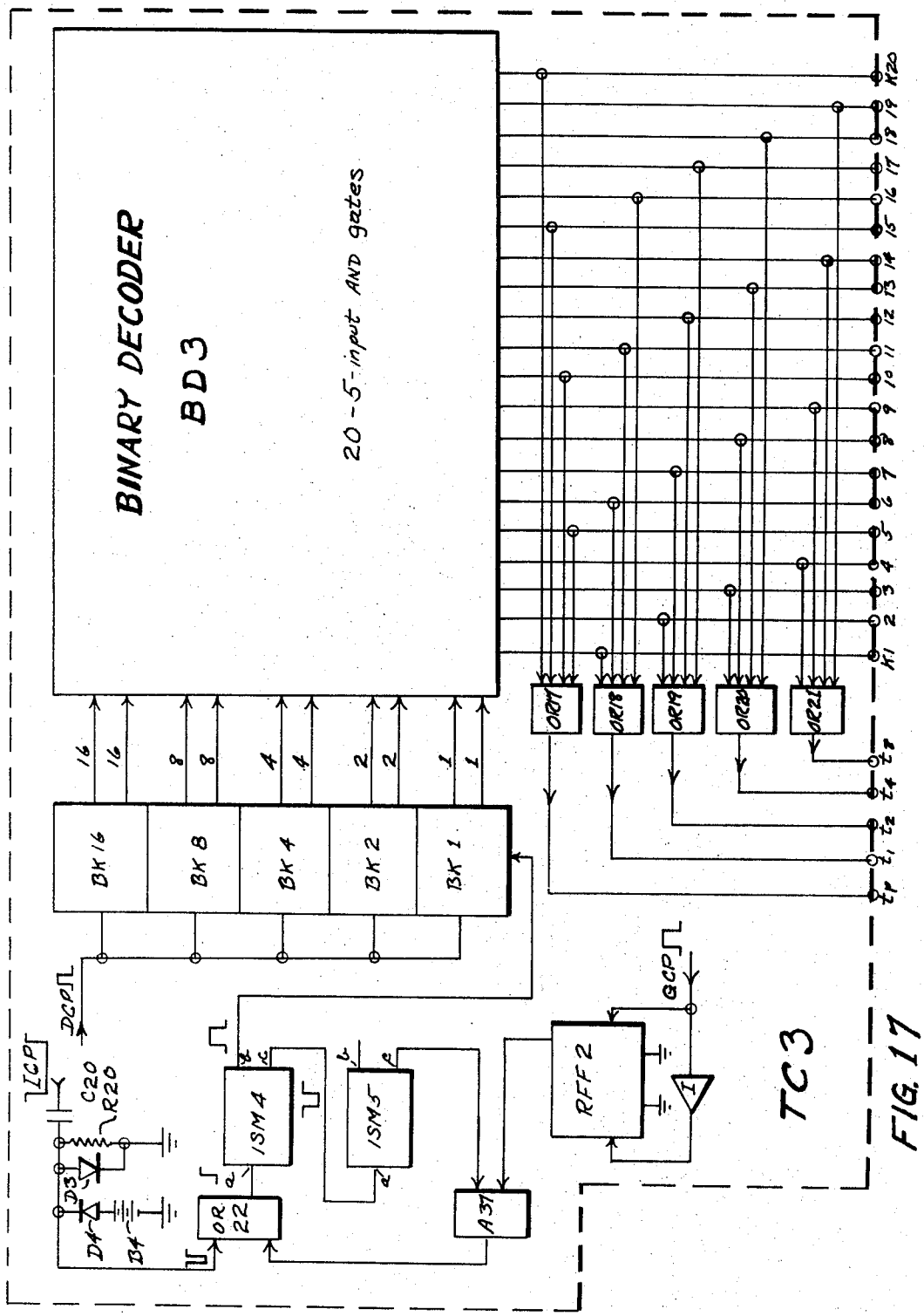

BINARY DECODER
BD3
20-5-input AND gates
BK 16
BK 8
BK 4
BK 2
BK 1
OR 22
ISM 4
ISM 5
A31
RFF 2
C20
R20
D3
D4
D5
DCP
ICP
GCP
TC3

FIG. 17

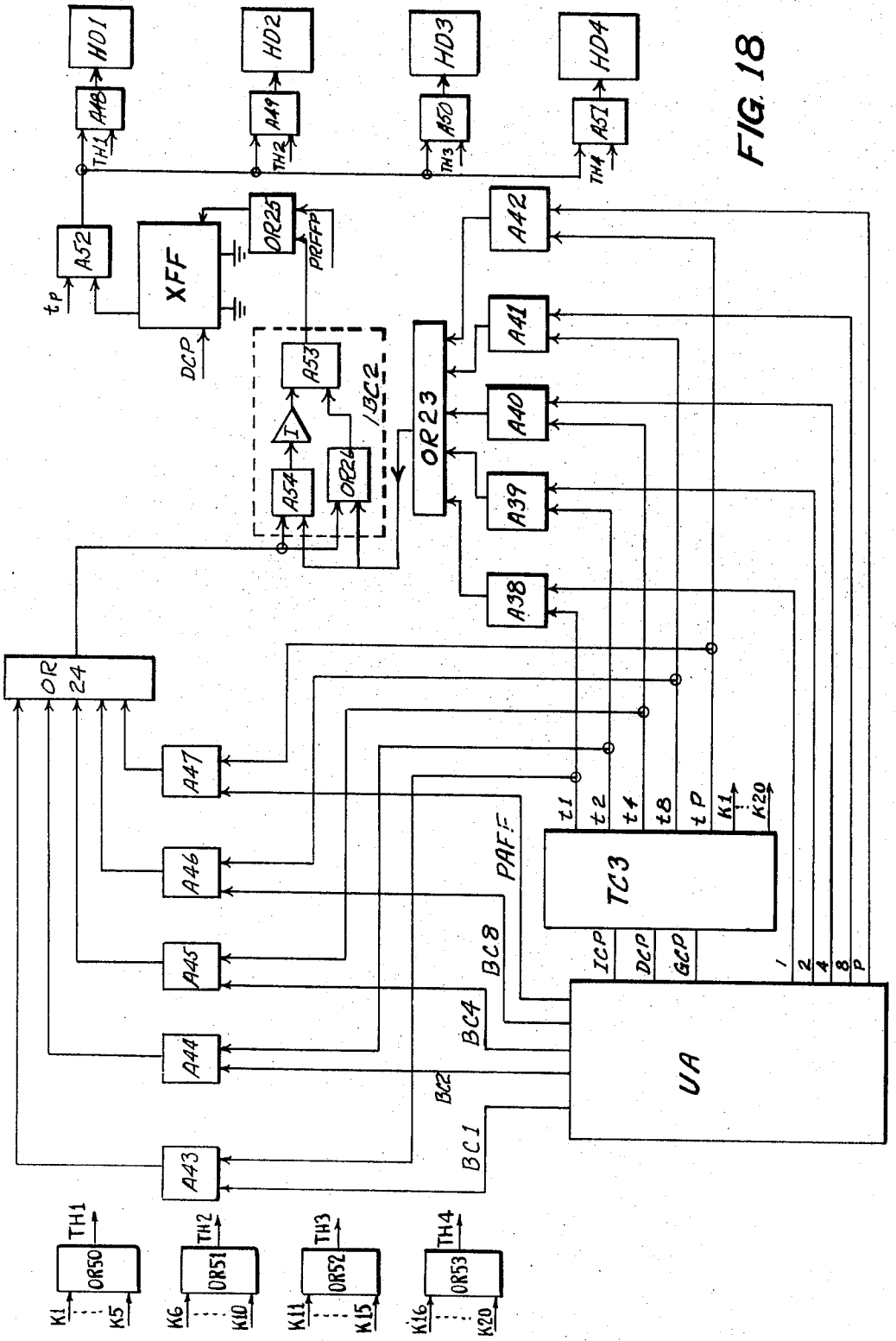

HD1
HD2
HD3
HD4
A48
A49
A50
A51
TH1
TH2
TH3
TH4
A52
XFF
OR25
PREFP
tP
DCP
A53
A54
OR24
/BC2
OR23
A42
A41
A40
A39
A38
OR 24
A47
A46
A45
A44
A43
t1
t2
t4
t8
tP
K1
K20
TC3
PAF
ICP
DCP
GCP
BC8
BC4
BC2
BC1
UA
1
2
4
8
P
TH1
TH2
TH3
TH4
OR50
OR51
OR52
OR53
K1
K5
K6
K10
K11
K15
K16
K20

FIG. 18

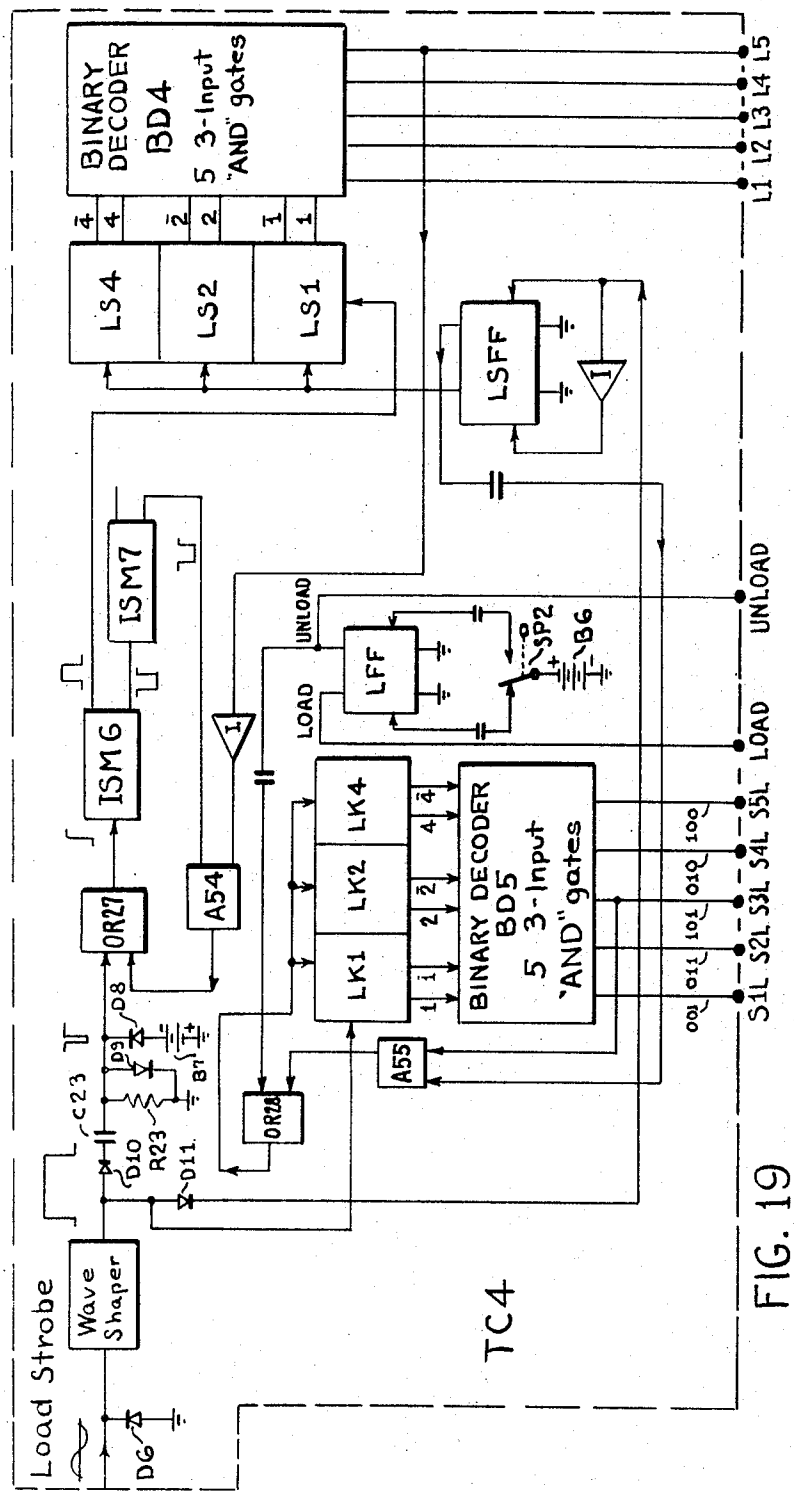

BINARY DECODER BD4 5 3-Input "AND" gates
L1 L2 L3 L4 L5
LS4
LS2
LS1
LSFF
ISM7
ISM6
OR27
A54
UNLOAD
LOAD
LFF
SP2
B6
LK4
LK2
LK1
BINARY DECODER BD5 5 3-Input "AND" gates
S1L S2L S3L S4L S5L
A55
OR28
C23
D8
D9
B7
D10
R23
D11
Load Strobe
Wave Shaper
DG
TC4

FIG. 19

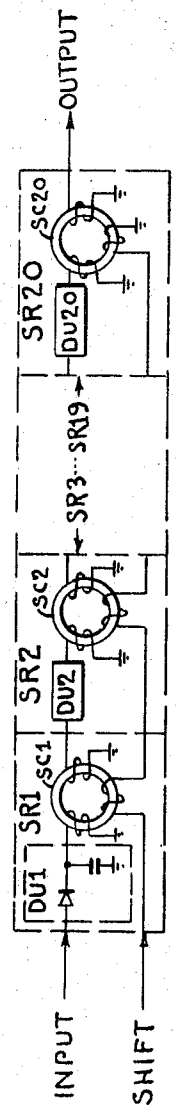

OUTPUT
SR20
SC20
DU20
SR3···SR19
SR2
SC2
DU2
SR1
SC1
DU1
INPUT
SHIFT

FIG. 21

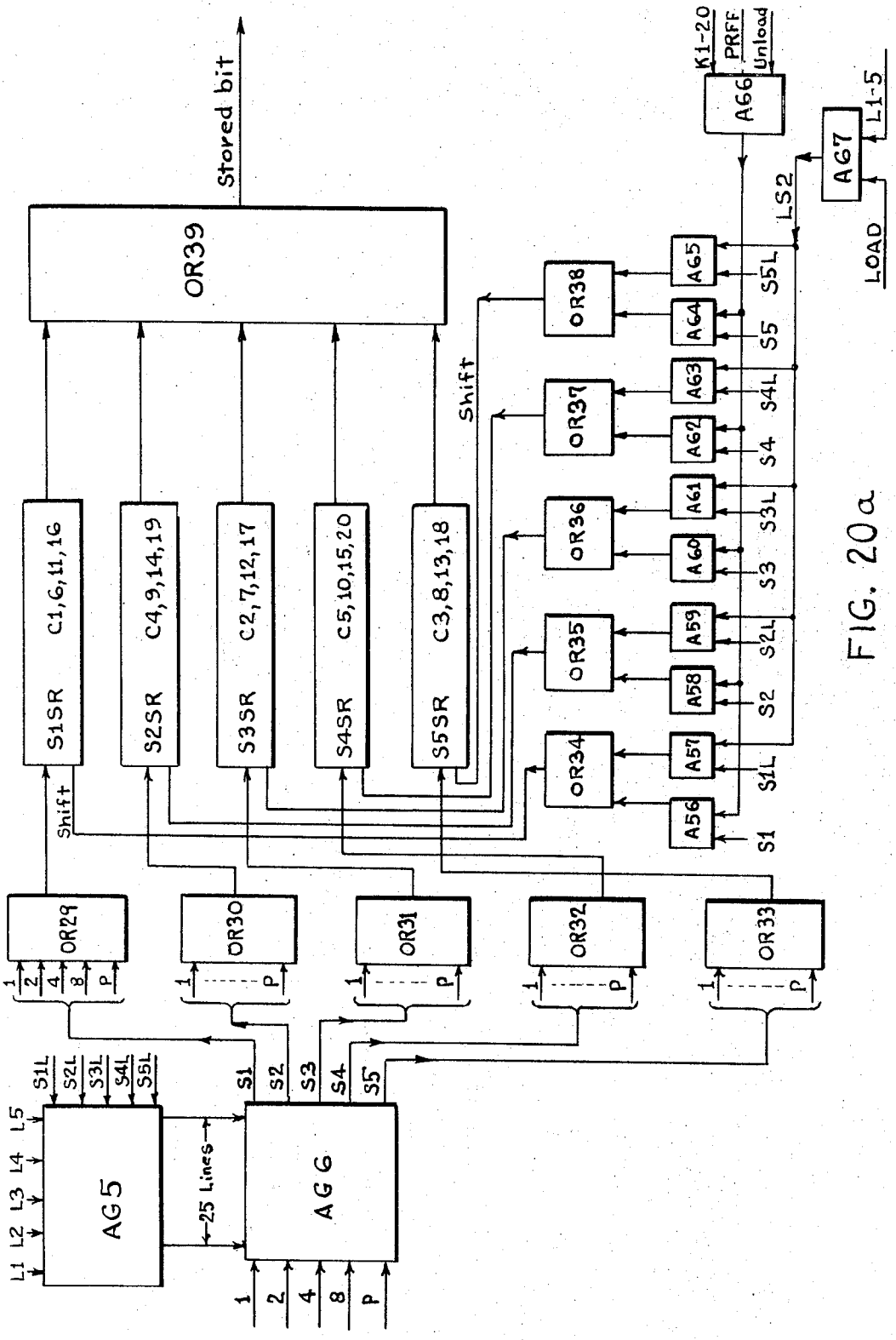

Stored bit
OR39
S1SR C1,6,11,16
S2SR C4,9,14,19
S3SR C2,7,12,17
S4SR C5,10,15,20
S5SR C3,8,13,18
Shift
Shift
OR38
OR37
OR36
OR35
OR34
A65
A64
A63
A62
A61
A60
A59
A58
A57
A56
S5L
S5
S4L
S4
S3L
S3
S2L
S2
S1L
S1
LS2
K1-20
PRFF
Unload
A66
A67
L1-5
LOAD
OR29
OR30
OR31
OR32
OR33
1
2
4
8
P
S1L
S2L
S3L
S4L
S5L
S1
S2
S3
S4
S5
L1 L2 L3 L4 L5
AG5
25 Lines
AG6

FIG. 20a

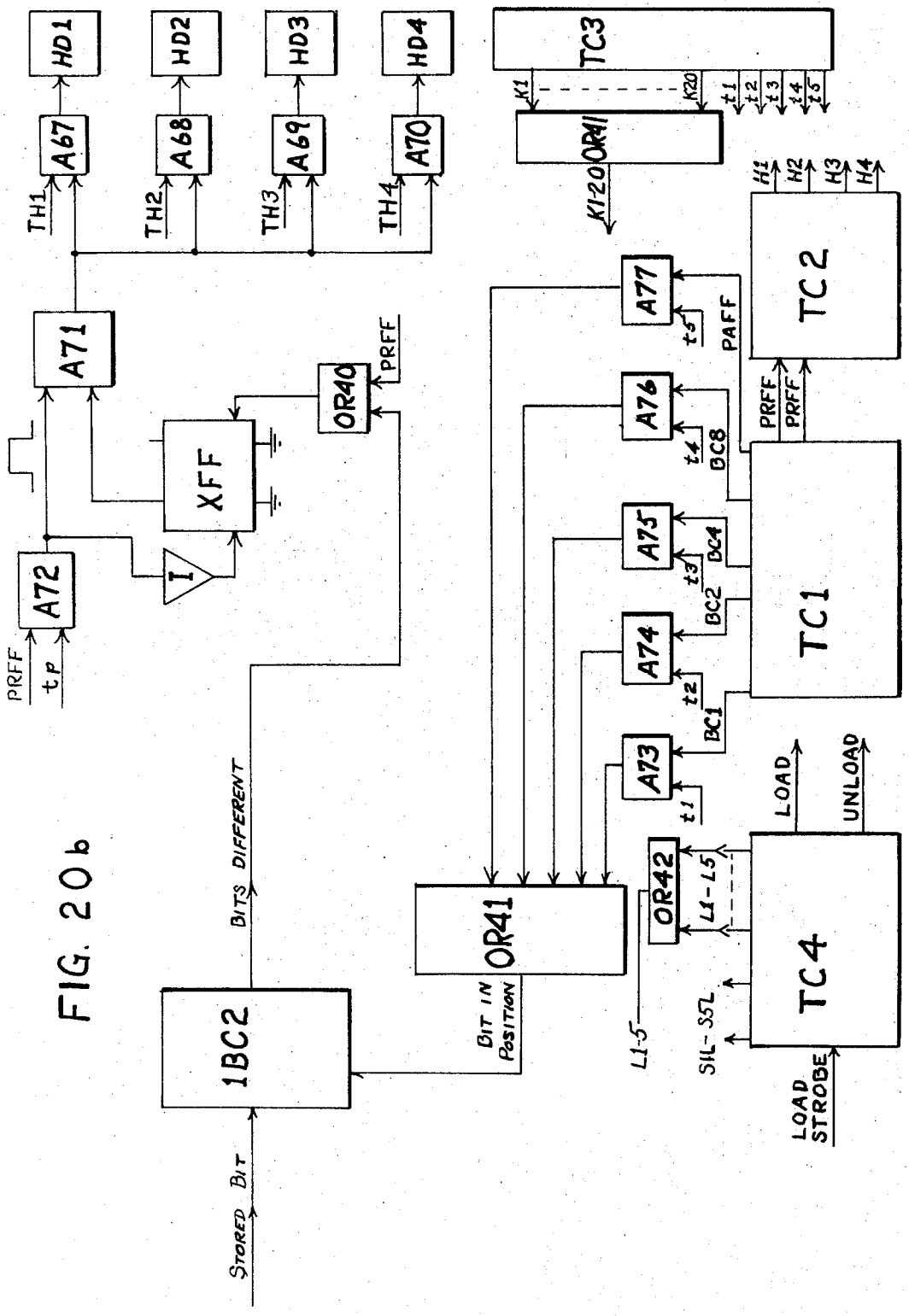

HD1
HD2
HD3
HD4
A67
A68
A69
A70
TH1
TH2
TH3
TH4
A71
A72
XFF
I
PRFF
tp
OR40
PRFF
TC3
K1
K120
t1
t2
t3
t4
t5
OR41
K120
H1
H2
H3
H4
TC2
A77
t5
PAFF
A76
t4
BC8
A75
t3
BC4
A74
t2
BC2
A73
t1
BC1
PRFF
PRFF
TC1
LOAD
UNLOAD
OR42
L1-L5
TC4
SIL-SSL
LOAD STROBE
L1-5
BIT IN POSITION
OR41
BITS DIFFERENT
1BC2
STORED BIT

FIG. 20b

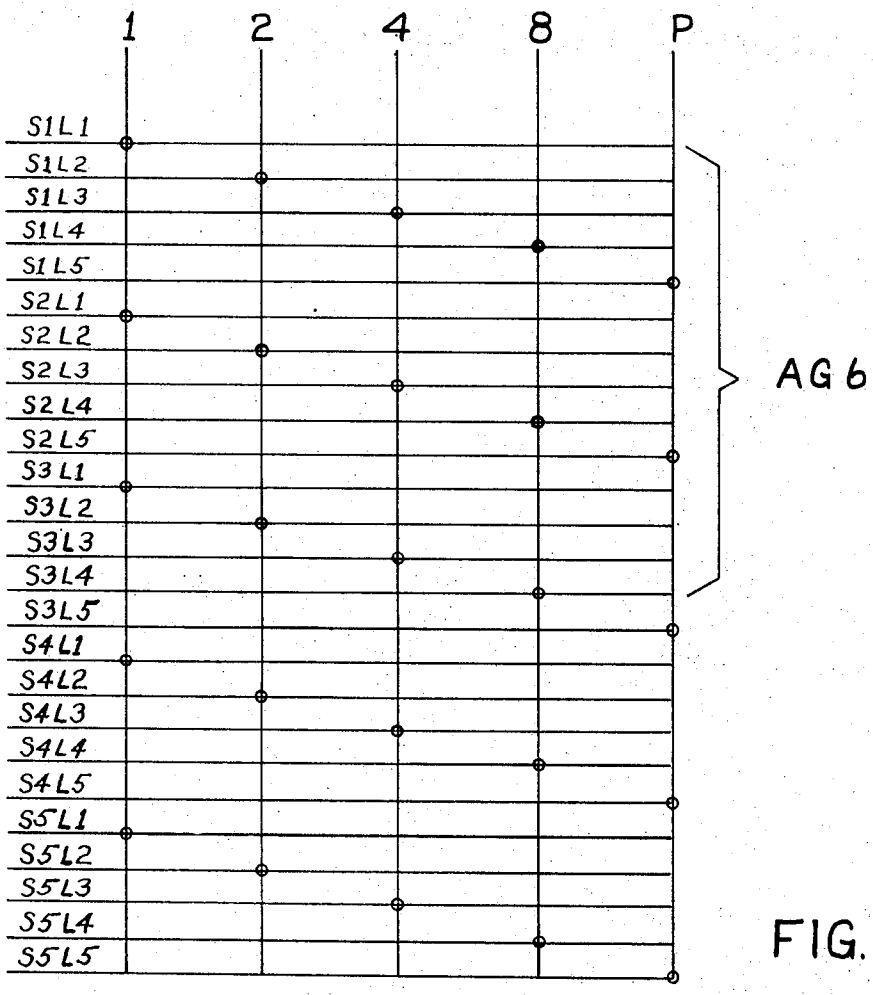

1
2
4
8
P
S1L1
S1L2
S1L3
S1L4
S1L5
S2L1
S2L2
S2L3
S2L4
S2L5
S3L1
S3L2
S3L3
S3L4
S3L5
S4L1
S4L2
S4L3
S4L4
S4L5
S5L1
S5L2
S5L3
S5L4
S5L5
AG 6

FIG. 24

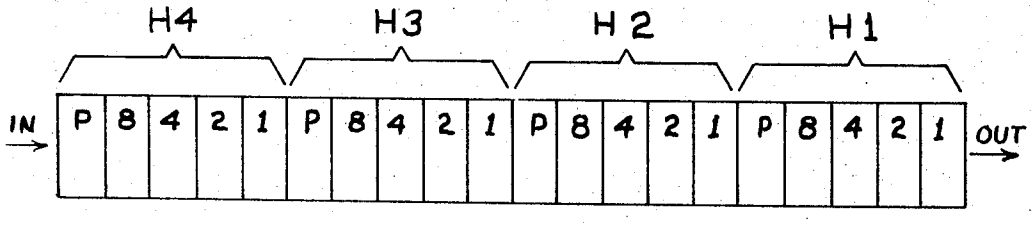

H4
H3
H2
H1
IN
P 8 4 2 1 P 8 4 2 1 P 8 4 2 1 P 8 4 2 1
OUT

FIG. 22

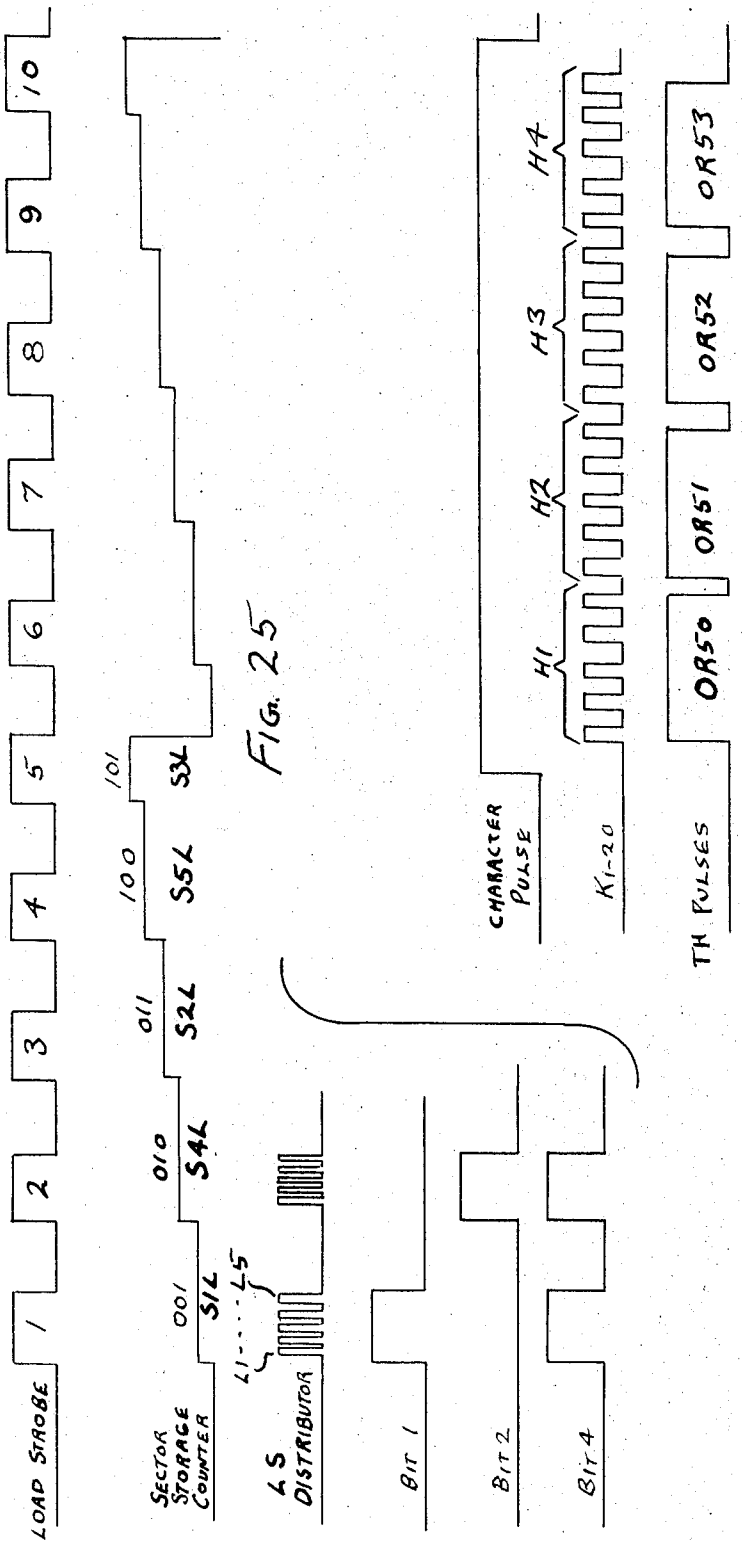

LOAD STROBE
1
2
3
4
5
6
7
8
9
10
SECTOR STORAGE COUNTER
001
S1L
010
S4L
011
S2L
100
S5L
101
S3L
4S DISTRIBUTOR
BIT 1
BIT 2
BIT 4
CHARACTER PULSE
H1
H2
H3
H4
K1-20
TH PULSES
OR50
OR51
OR52
OR53

FIG. 25

FIG. 26

HIGH SPEED PRINTERS WITH STAGGERED FONTS

RELATED APPLICATIONS

This application is a continuation of an application for "High Speed Printers," Ser. No. 178,371 filed Mar. 8, 1962 by David F. Sweeney and now abandoned.

SUMMARY OF THE INVENTION

High speed printers are currently in use which are capable of printing information a line at a time at speeds up to 1,200 lines per minute. These high speeds are now obtained, for example, in printers of the class in which a recording sheet, of paper or the like, is passed between a series of constantly rotating print wheels bearing fonts of characters and a row of print hammers, one for each column in the line to be printed. Frequently, a transfer sheet, such as a carbon ribbon or the like, is placed between the print wheels and the recording sheet, so that when a hammer is struck against the associated print wheel, an image of the character then in position on the print wheel is transferred from the transfer sheet to the recording sheet. Since the print wheel continues to move during the image transfer process, the hammer impact must be short and sharp to prevent smudging. The hammers are usually actuated electromagnetically by a coil, and in view of the necessity for transferring a relatively large amount of energy to the hammer in a short time interval, a relatively large coil is required. The size of this coil basically determines the minimum size of each hammer assembly. For this reason, it is conventional to place hammer assemblies on both sides of the line of printing, with alternate columns being actuated by hammers on opposite sides of the line. Also, the hammer assemblies are frequently interlocked mechanically, so that the length of the line may be reduced. With this arrangement, the last line printed cannot be seen until several additional lines have been printed. Also, in servicing one of the hammers, it is necessary to remove the entire row. For many purposes, these requirements are not onerous, and in fact they are necessary to the attainment of the very highest printing speeds. However, for many applications a somewhat lower printing speed would be acceptable if the same minimum spacing between characters could be obtained and the last line of printing could be readily observed immediately after it was formed. One object of my invention is to make it possible to inspect a line of print just after it has been formed. Additional objects of my invention are to simplify the construction of high speed printers, and to reduce the size and amount of apparatus required to print a given number of characters.

Basically, in accordance with my invention I provide a series of print hammers for use in a printer of the type described above, each of which has an actuating face broad enough to cover a plurality of columns of print. Such a hammer would be useless with a conventional arrangement of character fonts on the print wheels, because it would only be by accident that all of the characters which could be struck at a given time by a hammer would be in the desired sequence. Accordingly, I modify the arrangement of the fonts of characters on the print wheels such that only one font of characters is presented to a hammer at a given time, the remaining fonts being distributed in other sectors on their respective print wheels. Electronic timing means are provided for gating the characters stored for a line of print in the proper sequence to comparison circuits for determining when to actuate each hammer. In order to maintain relatively high printing speeds, means are provided for actuating the hammers a plurality of times during each revolution of the print wheels. Since the hammer drive coils must be allowed time in which to recover after each energization, I provide cycle timing means for allowing each hammer to recover during the passage of a given font of characters in order to print the next font. Preferably, I provide an odd number of character fonts for each hammer, such that the skipped fonts of characters are different for two successive revolutions of the print wheel. Accordingly, it is possible to print a line on only two revolutions of the print wheels.

My invention will best be understood by reference to the accompanying drawings, together with the following detailed description, of various preferred embodiments thereof suited to different specific requirements.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** is a schematic diagram of a high speed printing system in accordance with my invention;

FIG. **2** is a development of the print wheels of the system of FIG. **1**, showing the manner in which fonts of characters are arranged on the print wheels;

FIG. **3** is a fragmentary schematic diagram of a series of print wheels arranged in accordance with an alternative embodiment of my invention;

FIG. **4***a* is a schematic wiring diagram of a typical flip-flop suitable for use in the printer control system of my invention, and FIGS. **4***b*, **4***c* and **4***d* show various ways in which the external terminals of the flip-flop of FIG. **4***a* may be interconnected to perform different functions;

FIG. **5** is a fragmentary diagram of a parity generator disc shown in FIG. **1**, showing the manner in which the teeth are arranged;

FIGS. **6***a* and **6***b*, when arranged vertically side by side with FIG. **6***a* at the left, comprise a schematic wiring diagram of basic timing circuits suitable for use in a system in accordance with my invention;

FIG. **7** is a chart illustrating the operation of the system of FIGS. **6***a* and **6***b*;

FIGS. **8***a*, **8***b* and **8***c*, when arranged vertically side by side with FIG. **8***a* at the left, comprise a schematic wiring diagram of one embodiment of my invention;

FIG. **9** is a schematic wiring diagram of a one-bit comparator suitable for use in the five-bit comparator of FIG. **10**;

FIG. **10** is a schematic wiring diagram of a five-bit comparator suitable for use in the system of FIGS. **8***a*, **8***b* and **8***c*;

FIGS. **11***a* and **11***b*, when arranged vertically side by side with FIG. **11***a* at the left, comprise a schematic wiring diagram of a second embodiment of my invention;

FIG. **12** is a schematic wiring diagram of additional timing circuits suitable for use in the system of FIG. **13**;

FIG. **13** is a schematic wiring diagram of a print control system in accordance with a third embodiment of my invention;

FIG. **14** is a schematic wiring diagram of a group of AND gates suitable for use in the system of FIG. **13**;

FIG. 15 is a schematic wiring diagram of a second group of AND gates suitable for use in the system of FIG. 13;

FIG. 16 is a timing chart illustrating the mode of operation of the system of FIG. 13;

FIG. 17 is a schematic wiring diagram of additional timing circuits used in the system shown in FIG. 18;

FIG. 18 is a schematic wiring diagram of a preferred embodiment of my invention;

FIG. 19 is a schematic wiring diagram of additional timing circuits needed to convert the system of FIG. 18 for use with a serial-parallel data input system;

FIGS. 20*a* and 20*b*, when arranged horizontally side by side with FIG. 20*a* at the left, comprise a schematic wiring diagram of the preferred embodiment of my invention adapted for serial-parallel data inputs;

FIG. 21 comprises a schematic wiring diagram of a shift register suitable for use in the system of FIGS. 20*a* and 20*b*;

FIG. 22 is a schematic diagram of the shift register of FIG. 21, showing the manner in which data is stored;

FIG. 23 is a schematic wiring diagram of a group of AND gates shown in the system of FIGS. 20*a* and 20*b*;

FIG. 24 is a schematic wiring diagram of a second group of AND gates used in the system of FIGS. 20*a* and 20*b*;

FIG. 25 is a timing chart showing the mode of operation during the load cycle of the system of FIGS. 20*a* and 20*b*; and

FIG. 26 is a timing chart showing the mode of operation of the system of FIGS. 20*a* and 20*b* during the unload cycle.

DETAILED DESCRIPTION

Referring first to FIG. 1, a high speed printer in accordance with my invention is provided with a group 1 of print wheels P1, P2, P3 and P4. These print wheels are fixed on a shaft 2, which is rotated at constant speed by a conventional motor M.

Also disposed on shaft 2 are the movable elements of an index pulse generator IPG, a character pulse generator CPG and a parity pulse generator PPG. These pulse generators each comprise a disc of ferromagnetic material having one or more teeth magnetically polarized with respect to the body of the discs, which disc is fixed for rotation with the shaft 2, and an output coil which produces an electrical pulse each time a tooth moves past it. Thus, the index pulse generator IPG comprises a disc 3 having a single tooth 4 which actuates the coil 5 once during each revolution of the shaft 2 to mark the beginning of the revolution. The character pulse generator CPG comprises a disc 6 provided with a tooth marking the approach of each character on the print wheels to printing position, and a coil 7 energized once for each passage of a tooth. The parity pulse generator PPG comprises a disc 8 having teeth, located in a manner to be described, to actuate a coil 9 when the binary code describing the character coming into position has an even number of 1's, to provide an odd parity check.

The outputs of the pulse generators just described are applied to system timing circuits, to be described. The basic system cycle is controlled by conventional means here shown as a manual switch SP, which divides operational printer time into two basic periods: a first period in which paper is moved and information for a new line is stored, and a second period in which the paper is held stationary and the stored line is printed.

Disposed adjacent each of the print wheels P1, P2, P3 and P4 are print hammers H1, H2, H3 and H4, respectively. These hammers each have a striking face wide enough to span the associated print wheel. As schematically indicated, each hammer is pivoted for movement toward and away from the associated print wheels, and is urged away from the print wheel by a biasing spring such as the spring HS1 for the hammer H1. An actuating coil is located adjacent each hammer, to cause the hammer to strike the associated print wheel when the coil is energized with an applied electrical pulse. Thus, the coils HC1, HC2, HC3 and HC4 are arranged to actuate the hammers H1, H2, H3 and H4, respectively.

The hammer actuating coils HC1-HC4 are connected to the output terminals of hammer driver circuits HD1-HD4, respectively. These hammer driver circuits provide a pulse of actuating current for the associated hammer actuating coil in response to a print command signal from data comparison and gate circuits in the system, as schematically indicated in FIG. 1. These circuits compare stored data, defining characters to be printed in each column of a line, with a code representing the characters coming into printing position on command signals to the hammers at the proper time.

As schematically indicated in FIG. 1, each of the ring wheels is provided with five fonts of characters staggered around the periphery of the print wheel in five sectors S1, S2, S3, S4 and S5 and horizontally disposed in five columns. Thus, the illustrated printer is arranged to print a line of twenty characters. Referring to FIG. 2, the manner in which typical character fonts, each comprising the numerals O-9, are arranged on the print wheels, is shown in detail.

In general, each hammer is energized when the stored character for the column in the sector then in position matches the character coming into position in that column on the print wheel. However, time must be provided between actuations of the hammer driver circuits to permit them to be recharged. Thus, it would be impractical to print 9 in column 1 and sector S1 and then to print 0 in column 4 and sector S2 by successive actuations of the hammer H1. Accordingly, I prefer to inhibit printing during every other sector time. Thus, by means to be described in detail below, during a first revolution of the print wheels, the columns in sectors S1, S3 and S5 are printed, and during the next revolution the columns in sectors S2 and S4 are printed. In this manner a complete line may be printed in only two revolutions of the print wheels, and very high printing speeds may be attained if the character fonts are not unduly long. In this regard, it may be well to note that while I have illustrated my invention with reference to a system in which each hammer covers five columns, the hammers could be made to cover only two, or any higher number of columns, without departing from the scope of my invention.

As indicated in FIG. 2, the print wheels P1, P2, P3 and P4 may be disposed with fonts in registry on the shaft 2. However, for some purposes it is desirable to displace the wheels angularly with respect to each other, such that corresponding fonts on successive wheels come successively later into printing position, as shown in FIG. 3. The purpose of this displacement, as

will appear, is to permit the characters for the different hammers to be compared one at a time, within the time of a character pulse. The total displacement of the fonts, regardless of the number of wheels employed, is slightly less than one character space, as indicated by the displacement S in FIG. 3.

FIG. 4*a* shows a conventional flip-flop used for various purposes in the timing and gating circuits of my invention, to be described. As will be apparent to those skilled in the art, the circuit comprises conventional connections to a pair of transistors Q1 and Q2 to form a bistable circuit, which is shown in some detail only to make it clear how the circuit will operate in the system to be described. Basically, the set output terminal will be negative, representing logical **1**, when the transistor Q2 is cut off, and at ground potential, representing logical **0**, when the transistor Q2 is conducting. The reset output terminal similarly reacts to the state of the transistor Q1, to indicate logical **0** by a negative potential and logical **1** by ground potential. The collectors and bases of the transistors are interconnected so that if one is conducting, the other is cut off. The circuit can be reset directly to the logical **0** state by a positive-going pulse applied to the direct reset terminal. To set the flip-flop, a positive (or ground) level is applied to the set gate terminal, and a positive-going pulse applied thereafter to the set input terminal will cut off the transistor Q2. The circuit will respond on the leading edge of a positive pulse, and on the trailing edge of a negative pulse. The flip-flop may be reset in a similar manner by a pulse applied to its reset input terminal after a ground or positive level has been applied to its reset gate terminal.

FIGS. 4*b*, 4*c* and 4*d* show various ways in which the external terminals of the flip-flop FF of FIG. 4*a* may be interconnected to perform different functions. Specifically, the connections of FIG. 4*b* provide a flip-flop which will change state on each applied input pulse. FIG. 4*c* shows the connections used to cause the flip-flop to set on the leading edge of an applied positive pulse, and to reset on the trailing edge. As shown, an inverter I is inserted between the input terminal and the reset input terminal. FIG. 4*d* shows a flip-flop which may be set by one line and reset by a second line.

Referring next to FIG. 5, the detailed construction of the parity pulse generator disc **8** is indicated. While various codes and parity checks may be employed within the scope of my invention, for purposes of illustration I have shown means for making an odd parity check of a conventional ascending binary code. The parity bits required for an odd parity check are shown in the following table, for a four-bit character code corresponding to the characters on the fonts in FIG. 2:

Character	Character Code	Parity Bit
0	0001	0
1	0010	0
2	0011	1
3	0100	0
4	0101	1
5	0110	1
6	0111	0
7	1000	0
8	1001	1
9	1010	1

As shown in FIG. 5, these parity bits are produced by teeth appropriately located on the periphery of the disc **8**.

Referring now to FIGS. 6*a* and 6*b*, the basic timing circuits for the print control system of my invention will next be described. As my invention is not concerned with the events taking place during the portion of the operating cycle in which paper is moved, which are controlled in a conventional manner, I have indicated the means for initiating the print cycle as a manually controlled switch SP. Of course, other conventional means, including automatic means, for timing the print cycle could be employed without departing from the scope of my invention.

As shown, closure of the print switch SP applies energy from the positive terminal of a battery B to a differentiator comprising a capacitor C and a resistor R. A start-print pulse appearing across the resistor R is thereby applied to set a flip-flop AFF to its logical **1** state, causing its reset output terminal (see FIGS. 4*a* and 4*d*) to go from negative potential to ground and enabling an AND gate A**1**, of any conventional construction, to pass the next index pulse.

In connection with the AND gate A**1**, and other AND gates and OR gates to be described, details of suitable circuits for the purpose are so well understood in the art that I feel it unnecessary to linger on them. In general, conventional gates comprising diodes, transistors, saturable core reactors or switch cores may be employed, and where necessary to provide the proper polarity, a stage of inversion may be included. Suitable gates for use in the circuits to be described are considered in more detail in U.S. Application Ser. No. 106,840, filed on May 1, 1961, by Lynn W. Marsh for Pulse Retiming System, now U.S. Pat. No. 3,189,835, and assigned to the assignee of my invention.

A convention employed in the drawings, which is illustrated in the connections to the AND gate A**1**, may well be pointed out here. Specifically, I have not shown the wire connecting the output of the index pulse generator IPG to the input of the AND gate A**1**, but have appropriately marked the input terminal of the AND gate to signify that such a wire is intended. This convention is frequently employed in the drawings to avoid a confusing maze of crossing lines, and should be understood to imply the necessary wire connections.

In response to the first index pulse occurring after the flip-flop AFF has been set, the AND gate A**1** emits a pulse to set a second flip-flop BFF. The purpose of the flip-flop BFF is to mark a time during which a stored line is to be printed. Since this time must include time for at least two complete revolutions of the print wheels, I have provided for resetting the flip-flop BFF in response to the third index pulse received during the print cycle. For this purpose, I have shown an index pulse counter comprising two flip-flops NFF**1** and NFF**2**, which re interconnected to form a binary counter. As shown, the start print pulse appearing across the resistor R resets both flip-flops to logical **0** through isolating diodes connected to their direct reset input terminals. From the previous discussion, it will be clear that the first index pulse occurring thereafter will set the flip-flop NFF**1**, causing its set output terminal to go to ground. The resulting positive-going pulse on the set output terminal will set the flip-flop NFF**2** to its logical **1** state. The third index pulse will set the flip-flop NFF**1** to logical **1**, and so on.

An AND gate A2 is connected to respond to the 11 state of the counter comprising the flip-flop NFF1 and NFF2 by producing a positive pulse. This pulse will reset the flip-flops AFF and BFF, terminating the print cycle.

The output of the character pulse generator CPG may contain transients, and it is preferably clamped by a diode and applied to a suitable wave shaper, as indicated in FIG. 6*a*, to produce a square pulse of predetermined characteristics. This function may be performed by any suitable conventional circuits, comprising, for example, a one-shot multivibrator, a triggered blocking oscillator or the like.

The squared character pulse is applied to one input terminal of an AND gate A3. The other input terminal of the gate A3 is connected to the reset output terminal of the flip-flop BFF, which indicates the logical 1 state of the flip-flop by a ground potential. As will be obvious, a negative potential for the same purpose could be taken from the set output terminal, if it was desired to employ a negative character pulse, or if a mixed polarity AND gate was used.

The output of the AND gate A3 is a gated character pulse GCP. This pulse is employed to step a character counter comprising four flip-flops CFF1, CFF2, CFF4 and CFF8 interconnected to form a binary counter comprising four stages BC1, BC2, BC4 and BC8. The dotted lines surrounding the counter stages are replaced by full lines in other counters to be described, and these should be understood to imply the internal circuitry shown for the character counter.

As indicated, the character counter supplies four signals BC1, BC2, BC4 and BC8, which make up a binary code indicating the character then coming into printing position on the print wheels. The character counter is required to count to 1010 and then begin again once for each font in the five sectors on the print wheels. To perform the resetting function, I have shown an AND gate A4 to which the logical 1 output terminals of the flip-flops CFF8 and CFF2, and the logical 0 outputs of the flip-flops CFF1 and CFF4 are applied. In order to prevent the premature clearing of the character counter, a delayed character pulse DCP is also applied to this gate. The DCP pulse is derived from the gated character pulse GCP by application of the latter to an inverter 12, which provides an inverted pulse to a character multivibrator ISMI to provide the delayed character pulse DCP. The one-shot multivibrator may be of any conventional construction, but for example, may be of the type shown and described in the above-cited patent of Lynn W. Marsh. As shown, the output of the AND gate A4 is applied to the direct reset terminals of the flip-flops comprising the character counter.

An AND gate A5 is connected to produce an output pulse on each 0001 count of the character counter. This pulse is applied through a suitable coupling capacitor C2 to perform two functions.

First, the output of the gate A5 sets a flip-flop PRFF which divides the print cycle into print and recover intervals. In the print interval, the characters in one sector are printed, while in the recover interval one sector is allowed to pass without printing to enable the hammer driver circuits to be recharged.

The second function of the AND gate A5 is to step a sector counter comprising three stages SC1, SC2 and SC4. This counter may be wired in the manner shown in detail for the character counter described above. As shown, the outputs of the sector counter are connected to a binary decoder BD1, comprising five AND gates A6, A7, A8, A9 and A10. These gates produce five signals S1, S2, S3, S4 and S5, in the corresponding binary states of the sector counter, which are employed to gate information to character comparison circuits in a manner to be described. Other decoders to be described will be shown in block diagram form, and can be assumed to be wired in the manner indicated in detail for the decoder BD1.

As indicated in FIG. 6*a*, the output of the parity pulse generator PPG is shaped into rectangular pulses in the manner described above for the character pulse generator. Each parity pulse is then applied to a flip-flop PAFF, which is wired in the manner described in connection with FIG. 4*c* to set on the leading edge of the shaped parity pulse and to reset on the trailing edge. The output of the flip-flop PAFF makes up the parity bit of the character-in-position code, the remaining bits comprising the character counter output bits BC1, BC2, BC4 and BC8.

FIG. 7 comprises a timing chart showing the sequence of operation of the circuits of FIGS. 6*a* and 6*b*. As indicated, an index pulse begins a print cycle. The character pulses and their delayed mates continue throughout the cycle. The sector counter begins its count on the first gated character pulse, and continues to count through the cycle. The character counter is reset on each delayed pulse DCP following a count of ten or 1010. The print flip-flop PRFF is alternately set and reset on successive groups of ten character pulses, being set or reset on each 0001 count of the character counter.

Referring next to FIGS. 8*a*, 8*b* and 8*c*, a first embodiment of the print control system of my invention is shown in detail. Any desired form of character code storage may be employed if so desired; however, since the details of storage equipment of this kind do not form a part of my invention, I have shown apparatus for storing codes identifying a line of twenty characters to be printed as simply comprising a group of manual switches, which may be closed or opened to represent logical 1's or 0's, respectively, in a desired character code, here assumed to be the ascending binary code. Specifically, the input character storage is shown to comprise five switches SW1, SW2, SW4, SW8 and SWP for each character to be stored. These switches each function, when closed, to apply a positive potential from a battery B2, or other conventional source of energy, to a code bit line. The character storage is divided into twenty units C1 through C20, only the first of which is shown in detail.

The outputs of the input character storage unit are applied to a group of twenty five-bit comparators, one for each character in storage. As illustrated for the comparator 5BC1, each bit of the character associated with the comparator is supplied to one of five first input terminals, and a set of second input terminals is supplied from the character-in-position code terminals of the basic timing circuits TC1 through a group of AND gates A11, A12, A13, A14 and A15.

In the embodiment of my invention illustrated in FIGS. 8*a*, 8*b* and 8*c*, the character comparisons are made on the delayed pulse DCP following each gated character pulse GCP. These comparisons are made, however, only during every other sector time. To accomplish this purpose, each of the AND gates A11-

A15 has one input terminal supplied by the output of an AND gate A16. The gate A16 has two inputs, one the delayed character pulse DCP, and the other the set output of the print-recover flip-flop PRFF. The other inputs to the gates A11-A15 are supplied by the BC1, BC2, BC4, BC8 and PAFF bits of the character-in-position code from the timing circuits TC1.

The five-bit comparators 5BC1-5BC20 each produce an output when each bit of the applied stored character code is identical to the corresponding bit of the character-in-position code. Thus, twenty outputs, labeled P1 through P20, re provided, each energized when the corresponding stored character corresponds to the character coming into position on the print wheels. In order to provide proper registry in this embodiment of my invention, the character fonts are staggered from the teeth of the character generator by a space which allows for the hammer flight time plus the delay of the delayed character pulse DCP.

Referring now to FIG. 10, a five-bit comparator 5BC may comprise five one-bit comparators 1BC, each producing an output in response to equality of one applied stored character code bit and one corresponding character-in-position code bit. The outputs of the comparators 1BC are collected and applied to an AND gate A17, which responds when all of the comparators register bit agreement.

FIG. 9 shows a suitable construction for the one-bit comparator 1BC. The bits to be compared are applied to input terminals *a* and *b*, which are both connected to input terminals of two AND gates A18 and A19. A18 receives the inputs through a pair of inverters I. The output of the gate A19 is connected to one input terminal of a conventional OR gate OR1, and the output of the gate A18 is connected to a second input terminal of the gate OR1. By this arrangement the gate OR1 will produce an output if the input bits are both zero or both 1, but not if they are different.

Returning to FIGS. 8*a*, 8*b* and 8*c*, the twenty output lines P1-P20 are each connected to one input terminal of twenty 2-input AND gates collectively designated as AG1. The second input terminal of each of these AND gates is supplied by one of the sector lines S1, S2, S3, S4 and S5 from the timing circuits TC1. The purpose of this arrangement is to pass a character agreement signal on one of the lines P1-P20 only when the sector on which the corresponding character is located is in printing position. Thus, the S1 line is connected to gates A1-1, A1-6, A1-11 and A1-16, corresponding to the columns in printing position when sector S1 is in printing position. The gates are designated by a first number representing the sector and a second number designating the columns, as will be apparent from the gates for sector S1; the remaining gates, schematically shown in FIG. 8*b*, are as follows:

A2-4	A3-2	A4-5	A5-3
A2-9	A3-7	A4-10	A5-8
A2-14	A3-12	A4-15	A5-13
A2-19	A3-17	A4-20	A5-18

The outputs of the AND gates just described are grouped in accordance with the hammer associated with the columns represented by the gate output, and applied to four OR gates OR2, OR3, OR4 and OR5. Thus, the columns 1, 2, 3, 4 and 5, printed by hammer H1, are represented by the gate outputs A1-1, A2-4, A3-2, A4-5 and A5-3, which are connected to the input of the OR gate OR2. The connections to the remaining gates are shown in FIG. 8*c*.

The OR gates OR2, OR3, OR4 and OR5 control the hammer driver circuits HD1, HD2, HD3 and HD4, respectively. While these hammer driver circuits may be of any conventional design suitable for actuating a print hammer drive coil in response to an applied pulse, they are preferably of the types shown in my copending U.S. Application Ser. No. 178,445, filed on Mar. 8, 1962 for Control System for High Speed Printers, now U.S. Pat. No. 3,215,985. As there described in more detail, each circuit such as HD1 comprises an input terminal *a* connected through a suitable capacitor C8 to the control terminal of a silicon controlled rectifier S2. The control base terminal is connected to the load base terminal through a reverse-biased diode 32, and the load base terminal is grounded as shown. A series circuit including the load terminals of the controlled rectifier S2 extends through the hammer actuating coil HC1, a variable resistor R2, and through a capacitor C7 and a reverse biased diode 33 in parallel to ground. If the capacitor C7 is charged, a positive pulse applied to the input terminal *a* of the circuit HD1 will cause the controlled rectifier S2 to conduct, allowing the capacitor C7 to discharge through the coil HC1.

A charging circuit for the capacitor such as C7 in the hammer drive circuits HD1 is provided which extends from an output terminal *c* of a hammer driver control circuit HDC through a diode 32, a resistor R3, the resistor R2, and the capacitor C7 to ground. The hammer driver control circuit HDC comprises a battery B2 in series with the load terminals of a silicon controlled rectifier S1, the secondary winding of a pulse transformer PT1 and a load resistor R7. A back-biased diode 30 is connected across the base terminals of the controlled rectifier, and the control terminal is connected through a coupling capacitor C9 to an input terminal *a* of the circuit HDC. An input terminal *b* is connected through the primary winding of the pulse transformer PT1 to ground.

The set terminal of the flip-flop PRFF, in going to the logical 0 state of the flip-flop, produces a positive going pulse labeled PRFFp. This pulse, together with the shaped index pulse IPG, is applied to an OR gate OR6. The output of the gate OR6 is applied to the input terminal *a* of the hammer driver control circuit HDC, to cause the controlled rectifier S1 to conduct.

Conduction of the controlled rectifier S1 supplies current to charge the capacitors of the hammer drive circuits, such as the capacitor C7 of the circuit HD1. The charge cycle is interrupted when the flip-flop PRFF goes to its logical 1 state, at which time the reset output terminal produces a positive pulse labeled PRFFp. This pulse, applied to the input terminal *b* of the control circuit HDC, cuts off the controlled rectifier S1. Thereafter, each hammer drive circuit HD1-HD4 may fire only once until it is recharged after the flip-flop PRFF goes to its logical 0 state.

In the description of the various modifications of the print control system of my invention that follow, the hammer drive circuits may be assumed to operate in the manner described above, although the control circuit HDC will not be shown to avoid unduly complicating the drawings.

The operation of the first embodiment of my invention during the print cycle is as follows: Referring to FIGS. 6*a* and 6*b*, the cycle is begun by closing the print

switch SP, causing the flip-flop AFF to be set to its logical 1 state. The next index pulse will set the flip-flop BFF through the AND gate A1, enabling the AND gate A3 to pass the next fifty character pulses. The first of these will set the character counter to binary 1, causing the sector counter to step to S1 through the gate A5. At the same time the flip-flop PRFF is set to its print state. These S1 and PRFF states are held while the character counter cycles through a count of ten.

Referring to FIG. 8*a*, the counter states are supplied from the timing circuits TC1 to five AND gates A11, A12, A13, A14 and A15. At each delayed character pulse DCP, the AND gate A16 enables the gates A11-A15 to apply the character-in-position code to one set of input terminals of each of the twenty comparators 5BC1-5BC20. When the stored character for a given column corresponds to the character-in-position code, the associated comparator produces an output pulse on its output line in the group P1-P20. If this output corresponds to a column in the sector then in position, it will be passed by the corresponding gate in the group AG1 to the OR gate in the group OR2-OR5 for the hammer which prints the selected column. The OR gate will then actuate the hammer drive circuit, causing the hammer to fire. Each hammer will thus be actuated at some time during the first ten delayed character pulses.

The delayed character pulse following the tenth character pulse will reset the character counter to zero. At the eleventh character pulse the character counter will step to binary 1, resetting the flip-flop PRFF to its recover state and stepping the sector counter to S2. As the flip-flop PRFF goes to its recover state the set output terminal, labeled PRFF, will produce the pulse PRFFp to begin recharging the hammer drive circuits by setting the hammer driver control circuit HDC to its charge state.

At the twenty-first character pulse, the sector counter will step to S3 and the flip-flop PRFF will be set to its print state. In the transition the pulse PRFFp will be produced by the reset output terminal of the flip-flop PRFF and cut off the hammer driver control circuit HDC, leaving the capacitors such as C7 in the hammer drive circuit HD1 in their charged states. Printing of the columns in the third sector will then proceed as for the first sector.

When the sector counter goes to its S4 state, a second recovery period will begin, and the columns in the fourth sector will not be printed at this time. The fifth sector will be printed, however, on the first revolution of the print wheels.

After the next index pulse, the next 0001 count of the character counter will reset the flip-flop PRFF to its recover state, so that the first sector will be skipped. The second sector and fourth sector will therefore be encountered with this flip-flop in its print state, so that the columns in those sectors will be printed during the second revolution of the print wheels. The third and fifth sectors will be skipped, to allow for hammer drive circuit recharging.

At the third index pulse, the index pulse counters NFF1 and NFF2 will be in their binary 11, or 3, state, resetting the flip-flops AFF and BFF. The print cycle will then be terminated, with the apparatus restored to its initial condition after the print switch SP is opened.

Referring now to FIGS. 11*a* and 11*b*, I have shown a second embodiment of my invention in which a more economical arrangement of the comparison circuits is employed. The same basic timing circuits described in connection with the first embodiment of my invention are employed. However, the comparison of the stored character codes with character-in-position codes is deferred until the stored codes have first been gated by sector and by order within the code. For this purpose, the 100 lines representing the four information bits and one parity bit of each of twenty characters stored for the line to be printed are first each connected to one input terminal of a different one of one hundred 2-input AND gates. These gates are divided into twenty groups of five, each group corresponding to the five bits of one stored character. Thus, the stored character for the first column C1 has each of its lines corresponding to the bits 1, 2, 4, 8 and P connected to one of the AND gates A1-1-1, A1-1-2, A1-1-4, A1-1-8 and A1-1-P, respectively. These gates are labeled by a first number representing the sector in which the font for the columns to be printed lies, a second number representing the column in which the character to be printed lies, and a third number representing the bit order of the character code for the stored character. The gates just described accordingly have a second input terminal connected to the sector line S1 from the basic timing circuits TC1. As before, these sector line outputs are gated to the gate group AG2 by the print-recover flip-flop PRFF and the delayed character pulse DCP. For this purpose, the gate A16, responding to the levels PRFF and DCP as previously described, is employed to supply a gate signal to AND gates A21-A25, the other input terminals of which are supplied by the sector output lines S1, S2, S3, S4 and S5.

AND gates in the group AG2 other than the group for the first column character just described are schematically indicated in FIG. 11*a*. In general, as each sector comes into printing position, each bit of each stored character for the columns in the sector is gated to the output of the group AG2. These outputs are collected in terms of the hammers which will print the associated characters. The outputs for the hammer H1 are explicitly shown, and the outputs for the other hammers will be obviously, similarly collected. It should be borne in mind that the character data for each column is simultaneously presented, as its sector comes into position, and that the data for the columns 1-2-3-4-5, for example, come into position in the order in which the columns appear on the wheel; that is, in the order 1-4-2-5-3, for the first hammer.

The outputs of the gates AG2 are supplied to the inputs of five OR gates OR7, OR8, OR9, OR10 and OR11. These gates comprise a group labeled OG1. Each gate responds to a different bit of the stored character code in a column associated with a given hammer. It will be recalled that the stored character data is gated by sector in the gates AG2, so that only one character code will be applied to the gates OG1 at a time, and at a given time the character applied will be that character to be printed in the column then in position.

The outputs of the OR gates OG1, OG2, OG3 and OG4 are applied to the first input terminals of five-bit comparators 5BC21, 5BC22, 5BC23 and 5BC24, respectively. The other input terminals of these comparators are connected to the character-in-position code

terminals BC1, BC2, BC4, BC8 and PAFF of the timing circuits TC1. With these connections, each five-bit comparator will produce an output pulse during the delayed character pulse in which the applied stored code matches the character-in-position code, and cause the associated hammer drive circuit HD1-HD4 to actuate its associated hammer.

The overall operation of the embodiment of my invention just described will be apparent from the above description. Specifically, referring first to FIG. 8*a*, assume that a series of characters is stored in the input character storage unit by closure of appropriate switches, such as the switches SW1-SWP in the storage CS1 for the column 1 character. Next, assume that the print switch SP in FIG. 6*a* is closed to initiate a print cycle. This action will cause the flip-flop AFF to set. At the next index pulse the AND gate A1 will produce a pulse, setting the flip-flop BFF and enabling the AND gate A3. Character pulses from the character pulse generator CPG will now be applied to step the character counter in FIG. 6*b*.

At the first step of the character counter, the sector counter in FIG. 6*b* will be set through the AND gate A5, which will also set the flip-flop PRFF to its print state. Referring now to FIG. 11*a*, the AND gate A16 is now enabled to pass the next delayed character pulse. When this occurs the AND gate A21 will transmit the sector 1 indication S1 to enable the AND gates 52A1-1, 52A1-6, 52A1-11 and 52A1-16 to pass the characters for columns 1, 6, 11 and 16 which occur in sector 1. The outputs of these gates comprise the lines 1H1-1, 1H1-2, 1H1-4, 1H1-8 and 1H1-P, applied to the input terminals of OR gates OR7, OR8, OR9, Or10 and OR11, respectively; the lines 6H2-1, 6H2-2, 6H2-4, 6H2-8 and 6H2-P, applied to successive ones of the corresponding OR gates in the group OG2, respectively; the lines 11H3-1, 11H3-2, 11H3-4, 11H3-8 and 11H3-P, applied to corresponding gates in the group OG3; and the lines 16H4-1, 16H4-2, 16H4-4, 16H4-8 and 16H4-P, applied to the gates of the group OG4.

When the characters appearing at the outputs of the groups OG1, OG2, OG3 and OG4 match the output of the character counter of the timing circuits TC1, the corresponding five bit comparator 5BC21, 5BC22, 5BC23 or 5BC24 will respond by energizing its associated hammer drive circuit HD1, HD2, HD3 or HD4, respectively, to print the character then in position. It will be recalled that the character counter is stepped at each character pulse, and the stored data from the gates AG2 will be represented to the comparators at each delayed character pulse. This action will continue, with the actuation of each hammer on some character of the font for the columns in position, until one sector has been covered and the tenth character has been presented to the hammers. At this time the character counter will be in the state 1010, and the next delayed character pulse will cause it to reset to binary zero.

The next character pulse will step the counter to 0001, causing the sector counter to step to S2 and the flip-flop PRFF to reset to its recover state. The print hammer drive circuits will be recharged during the passage of the second sector, and no data will be printed because the AND gate A16 will not be enabled at this time.

When the sector counter is stepped to S3, the flip-flop PRFF will be set to its print state, and the columns 2, 7, 12 and 17 will be printed in the manner just described for the first sector, with appropriate ones of the gates AG2 being enabled to pass the stored character data for these columns.

The operation will continue in the manner outlined above, with hammer recovery occurring during S4 and printing of columns 3, 8, 13 and 18 during S5. At the beginning of the next revolution of the print wheels the flip-flop PRFF will be reset to its recover state, skipping the sector S1. The sector S2 will then be printed, sector S3 skipped, sector S4 printed and S5 skipped. After the end of the second revolution the next index pulse will step the index pulse counter comprising the flip-flops NFF1 and NFF2 to their binary three state, 11, which will reset the flip-flops AFF and BFF and terminate the print cycle. If desired, the resetting of either of these flip-flops may be used as a signal to start the move-paper, store next line period of operation.

In the embodiment of my invention next to be described, only a single five-bit comparator is employed. In order to schedule the use of this comparator to sequentially process data for each of the four hammers, an additional timing circuit is employed; this circuit is indicated as TC2 in FIG. 12. As shown, the inverted character pulse ICP from the timing circuits TC1 in FIGS. 6*a* and 6*b* is employed as the input to the circuit TC2. This pulse is applied to a differentiator comprising a capacitor C2 and a resistor R2. A clamping diode D1 prevents the junction of the capacitor C2 and the resistor R2 from going above ground, and a diode D2 is blocked by a battery B3 to prevent the excursion of the junction below ground by more than the potential of the battery B3. A negative rectangular pulse is thus provided at the junction of the resistor R2 and the capacitor C2 for each ICP pulse leading edge. This pulse is applied to one input terminal of an OR gate OR12.

The output terminal of the gate OR12 is connected to the input terminal of a one-shot multivibrator 1SM2, which may be identical with the monostable unit described in the above-cited copending application Ser. No. 106,840, or of other conventional construction. This circuit produces a positive pulse on one output terminal and a negative pulse on the other output terminal in response to each applied positive-going pulse; specifically, on the trailing edge of each output pulse of the gate OR12. Thus, these pulses are delayed by a time selected by the time constants of the circuit 1SM2 from the leading edge of the inverted character pulse ICP. As will appear, these time constants should be selected to provide four pulses during each character pulse time.

The negative pulse output terminal of the one-shot multivibrator 1SM2 is connected to the input terminal of a second one-shot multivibrator 1SM3. The negative pulse output terminal of this multivibrator is connected to one input terminal of an AND gate A26. The other input terminal of the gate A26 is connected to the set output terminal of a flip-flop RFF1.

The flip-flop RFF1 is connected to set on the leading edge of each gated character pulse GCP, and to reset on the trailing edge. When set, the gate A26 is enabled to pass pulses from the multivibrator 1SM3 to the gate OR2. Thus, after the leading edge of each gated character pulse, the one-shot multivibrators 1SM2 and 1SM3 will oscillate until the trailing edge of the gated character pulse closes the gate A26. The circuit constants are selected so that four pulses will be produced

at the output of the multivibrator 1SM2 during this time.

The positive pulse output of the one-shot multivibrator 1SM2 is connected to the input terminal of a binary counter comprising three stages HK1, HK2 and HK4. The outputs of the counter are applied to a binary decoder BD2, of the type previously described, in which a separate line H1, H2, H3 and H4 is energized in the 001, 010, 011 and 100 states of the counter, respectively. These lines indicate by their energized state that the associated hammer is to take possession of the comparator, to be described. As shown, the counter is cleared by each delayed character pulse DCP from the timing circuits TC1.

FIG. 13 shows an embodiment of my invention in which only one five-bit comparator, 5BC25, is employed. As shown, the input character storage ICS, which may be the same as previously described, has its 100 output lines, for twenty characters each represented by four information bits plus one parity bit, connected to a group of AND gates AG4. The gates AG4 will be described below; in general, they are divided into twenty groups, one for each stored character, each group comprising five gates, one for each bit in the character. A second input to each of these one hundred AND gates is provided by one of the outputs of a group AG3 of twenty 2-input AND gates. These gates each have as inputs one of the sector timing outputs S1-S5 of the basic timing circuit TC1 and one of the hammer scheduling outputs H1-H4 of the timing circuits TC2.

Referring to FIG. 14, the detailed connection of the AND gates in the group AG3 is shown. Each of the AND gates is represented by a circle at the intersection of the two input lines which supply it; the output lines are not shown, but would correspond to the twenty-five lines identified by the reference characters assigned to the gates, as gates A11, A23 and A43, for example, would have output lines energized for logical 1 values of both S1 and H1, S2 and H3, and S4 and H3, respectively. These output lines are indicated across the top of FIG. 15 as one set of inputs to the AND gates of the group AG4. As shown in detail for the first column character C1, five AND gates are provided for each character, such as the gates APC1-1, APC1-2, APC1-4, APC1-8 and APC1-P for the 1, 2, 4, 8 and parity bits of the stored character code for the first column. Energization of the output line of any gate means that the associated bit is for a column in a sector then in position controlled by a hammer then in possession of the comparator 5BC25.

Referring again to FIG. 13, the outputs of the gates AG4 are collected into four groups each identified with one bit of the character code and one group identified with the parity bit of the character code. Each group of twenty output lines so formed is connected to the input terminals of one of five twenty-input OR gates OR12, OR13, OR14, OR15 and OR16. Thus, the one bits of the codes for characters 1-20 are applied to the gate OR12, the two bits to gate OR13 and so on, as shown in FIG. 13.

The outputs of the gates OR12-OR16, comprising the group OG5, are applied to one set of input terminals of a single five-bit comparator 5BC-25. The other inputs to the comparator comprise the character-in-position code output terminals of the timing circuit TC1.

The output of the comparator 5BC-25 is connected to one input terminal of an AND gate A35, the other input terminal being energized in the print state of the flip-flop PRFF. During the print portions of a revolution, the output of the comparator is thus gated to the inputs of a group of AND gates A31, A32, A33 and A34, one for each hammer. The other inputs to these gates are supplied by the lines H1, H2, H3 and H4 from the timing circuit TC2.

The outputs of the gates A31-A34 are stored in a series of flip-flops SRFF1, SRFF2, SRFF3 and SRFF4, of the set-reset type. These flip-flops are reset on the positive pulse PRFFp produced by the set terminal of the flip-flop PRFF when it goes from the print state to the recover state. When set, the reset output terminal of each flip-flop is at ground potential, enabling one of a group of AND gates A27, A28, A29 and A30 to pass the next gated character pulse GCP to actuate the associated hammer driver circuit HD1, HD2, HD3 and HD4, respectively.

The operation of this embodiment of my invention is substantially the same in basic respects as that of the embodiments previously described. The differences are in the gating of the code bits to the comparison circuit. Reference to FIG. 16 is made to show the basic timing of the circuit TC2, which controls the assignment of the comparator to the successive hammers. As each hammer takes possession of the comparator, the characters gated to the comparator are restricted to those for the column in its group which is then in printing position, and no characters are gated to the comparator during the skipped sectors in the printing cycle, during which the hammer drive circuits are recharged.

A simplification of the circuiting of the system shown in FIG. 13 is possible if the fonts on the columns for the successive hammers are staggered one from the other a sufficient amount to allow time for each successive comparison made by the comparator 5BC-25. If this is done, the flip-flops SRFF1, SRFF2, SRFF3 and SRFF4, or other storage which may be provided, and the AND gates A27, A28, A29 and A30, may be omitted and the outputs of the gates A31-A34 connected directly to the input terminals of the hammer drive circuits HD1-HD4, respectively, in the manner shown by the dotted lines in FIG. 13. Specifically, the fonts are initially staggered from the character pulse generator teeth to allow one character pulse to be emitted before the first character on the first font is encountered, this first character occurring just after the second character pulse. The delay after the second pulse is to account for the hammer flight time, so that the hammer will strike just as the character comes into print position. The first character in the sixth column is placed after the first character in the first column, as indicated in FIG. 3, and so on. Thus, each column is printed on the same line, although the hammers are acutated in sequence.

In the preferred embodiment of my invention next to be described, only a single one-bit comparator is required. In this embodiment, data is gated to the comparator one bit at a time. The additional timing circuits TC3 required for this embodiment are shown in FIG. 17. While various known circuits could be employed to provide the necessary timing pulses, I have shown a distributor similar to that employed in the timing circuit TC2, except that the time constants are selected to produce twenty pulses within each character pulse time.

The counting cycle for the timing circuits TC3 is established by a flip-flop RFF2, which has its set terminal connected to the gated character pulse output terminal GCP of the basic timing circuit TC1 and its reset terminal supplied from the same terminal through an inverter I, so that the flip-flop is set on the leading edge of each gated character pulse and reset on the trailing edge of the same pulse.

The set output terminal of the flip-flop RFF2 is connected to one input terminal of an AND gate A37. In the set state of the flip-flop, the gate A37 is enabled to pass pulses circulating through a delay line comprising two one-shot multivibrators 1SM4 and 1SM5. As in the timing circuit TC2, an OR gate OR22 receives the output of the AND gate A37 and the output of a pulsing circuit, to be described, which provides a starting trigger pulse. The output of the OR gate OR22 is connected to the input terminal *a* of the multivibrator 1SM4, and the negative pulse output terminal of the multivibrator 1SM4 is connected to the input terminal *a* of the multivibrator 1SM5. The negative pulse output terminal of the multivibrator 1SM5 is connected to one input terminal of the AND gate A37 to complete the loop.

A starting pulse is provided by the leading edge of the inverted character pulse ICP from the timing circuit TC1. This pulse is applied to a differentiator comprising a capacitor C20 and a resistor R20. A diode D3 prevents the junction of the resistor and capacitor from going above ground, and a diode D4 reverse-biased by a battery B4 limits the negative excursion of the junction to provide a rectangular negative pulse adjacent the leading edge of the character pulse. The trailing edge of this pulse, delayed a predetermined time after the leading edge of the character pulse, triggers the multivibrator 1SM4 to start a series of progressively delayed pulses circulating through the loop. The circuits constants are chosen to provide twenty of these pulses for each gated character pulse.

The positive pulses produced at the output terminal *b* of the multivibrator 1SM4 are counted in a binary counter having five stages BK1, BK2, BK4, BK8 and BK16. This counter is reset after each character pulse by the delayed character pulse DCP from the timing circuit TC1.

The outputs of the binary counter from 00001 to 10100 are gated to twenty output lines K1-K20 by a decoder BD3 similar to those previously described, comprising twenty five-input AND gates each connected to the appropriate logical 1 or logical 0 output terminals of the counter to respond to the proper count code. These output terminals are used directly in a later described embodiment, but in the embodiment next to be described are collected in groups of four, each group representing the time corresponding to a particular bit of the character code, and each group is applied to the input terminals of one of five OR gates OR17, OR18, OR19, OR20 and OR21. As will appear, during each character pulse time it is desired to sample four character codes, one for each hammer. Since there are five bits in each code, if the bits are scanned in the order 1, 2, 4, 8, P, the times 1, 6, 11 and 16 will correspond to 1 bits, the times 2, 7, 12 and 17 will correspond to 2 bits, the times 3, 8, 13 and 18 will correspond to 4 bits, the times 4, 9, 14 and 19 will correspond to 8 bits, and the times 5, 10, 15 and 20 will correspond to parity bits. The gate OR17 output is accordingly labeled tp, and the outputs of the gates OR18-OR21 are labeled t_1, t_2, t_4 and t_8, respectively.

Referring now to FIG. 18, I have shown a preferred embodiment of my invention in which only a single one-bit comparator is employed. In FIG. 18, the block UA corresponds in structure to the circuits surrounded by the dotted line and labeled UA in FIG. 13, since this portion of the system may be the same as that previously described. In this regard it will be recalled that the five 20-input OR gates in the circuit portion UA presented at their outputs terminals the five bits of four character codes per character pulse, one for each hammer. In the embodiment of my invention shown in FIG. 18, each character code output is sampled one bit at a time in the times t_1, t_2, t_4, t_8 and t_p provided by the timing circuit TC3. Specifically, the character code outputs of the unit UA are each connected to one of five AND gates A38, A39, A40, A41 and A42. The other input to each AND gate is provided by one of the output lines t_1, t_2, t_4, t_8 and t_p of the timing circuit TC3.

The outputs of the AND gates A38-A42 are collected in a five input OR gate OR23. The output of this gate is connected to one input terminal of a one-bit comparator 1BC2.

The states of the character-in-position code output terminals of the timing circuit TC1 are also serially presented to the one-bit comparator 1BC2, in time with the corresponding bits of the stored character codes. For this purpose the character counter output terminals BC1, BC2, BC4, BC8 and the parity flip-flop output PAFF, are each connected to one of five AND gates A43, A44, A45, A46 and A47. The other input terminal of each of these gates is connected to the corresponding output terminal t_1, t_2, t_4, t_8 and t_p of the timing circuit TC3.

The output terminals of the gates A43-A47 are applied to the input terminals of an OR gate OR24, the output terminal of which is connected to the other input terminal of the one-bit comparator 1BC2. Thus, at each of the twenty timing pulses supplied by the timing circuit TC3, one bit of a stored character code is compared with the corresponding bit of the character-in-position code for the associated character pulse. As previously described, the fonts for successive hammers are staggered in the manner shown in FIG. 3, so that the print command signal for each hammer occurs at the proper time even though the hammers are actuated at different times.

For the purposes of this embodiment of my invention a one-bit comparator different than that previously described is required. As shown in FIG. 18, the comparator comprises two AND gates A53 and A54, an OR gate OR26 and an inverter I interconnected to produce an output pulse when the applied input signals are not in agreement. For this purpose, the outputs of the gates OR23 and OR24 are each connected to one input terminal of the gates A54 and OR26. The output of the gate OR26 is connected to one input terminal of the gate A53, and the output of the gate A54 is connected to the other input terminal of the gate A53 through the inverter I. Thus, the gate A53 will produce a pulse if gate OR26 produces a pulse, unless gate A54 produces a pulse. Both of these conditions can occur only if one but not both of the input bits is logical 1.

The output of the comparator 1BC2 is applied to one input terminal of an OR gate OR25. The other input terminal of the gate OR25 is energized by the positive-

going pulse produced when the flip-flop PRFF goes to its recover state, and is employed to prevent printing during the hammer recovery cycle.

The output of the gate OR25 is connected to the set input terminal of a flip-flop XFF. This flip-flop is reset on each delayed character pulse if it has been set during the preceding character pulse. The reset output terminal of the flip-flop XFF is connected to one input terminal of an AND gate A52. The other terminal of the gate A52 is energized during each parity pulse time t_p, and causes a pulse to be transmitted to a group of four AND gates A48-A51 if the flip-flop XFF has not been set to its logical 1 state by a discrepancy between two applied bits of the group 1, 2, 4, 8 and P associated with each character code.

The other input terminals of the gates A48-A51 are connected to the lines TH1-TH4, respectively, from the OR gates OR50-OR53. These gates are each supplied with five pulses, K1-5 being supplied to the gate OR50, K6-10 being supplied to the gate OR51, and so on. These gates provide four lines TH1-TH4, which lines are energized successively during each character pulse, to enable each hammer to be successively actuated.

The operation of this embodiment of my invention is identical with those previously described except for the serial comparison of the character codes. As each bit of each character for the sector in position and hammer in possession of the comparator is presented to the comparator, it will produce a pulse or not according as the bit matches or does not match, respectively, the corresponding bit of the character-in-position code. If each bit matches, the flip-flop XFF will remain in its reset state, allowing the corresponding hammer to be actuated during the parity pulse time t_p. However, any bit that does not match will set the flip-flop XFF, preventing printing until the next character for the next hammer is compared.

The embodiment of my invention next to be described preserves the advantages of serial bit comparison possessed by the previously described embodiment, but is adapted for use with character codes presently serially a character at a time. As will be apparent, only minor modifications would be necessary to make it usable with data presented serially one bit at a time.

In order to process serially presented data, it is necessary to provide specific data loading circuits which will cooperate with the serial comparison circuits used during the print cycle. FIG. 19 shows one form of timing circuit suitable for the purpose. Basically, the timing circuit TC4 to FIG. 19 comprises means for producing a load signal, an unload signal, five bit loading time signals L1, L2, L3, L4 and L5, and five storage sequencing signals S1L, S2L, S3L, S4L and S5L.

It is assumed that data is presented to the system in the form of a pulse for 1 and not pulse for 0 for each of four information bits plus a parity bit, and for each group of bits so presented a load strobe pulse is supplied by conventional means to indicate the presence of a character to be stored. As shown in FIG. 19, this load strobe pulse is clamped by a suitable diode D6, and formed into a rectangular pulse having a duration less than or equal to the duration of each information pulse. This shaped pulse performs three functions in the system.

First, a counter comprising three stages LK1, LK2 and LK4 is stepped to count the individual load strobe pulses. The outputs of the counter are applied to a binary decoder BD5, comprising five 3-input AND gates, to energize the lines S1L, S2L, S3L, S4L and S5L on selected counting states from 001 to 101. As will appear, it is desired to load each character into a storage for the sector in which its column lies, and to load four characters into each sector storage, one for each hammer, in the order in which the hammers take possession of the serial comparator. Since the columns appear in the sectors in the order 1-4-2-5-3, 6-9-7-10-8, 11-14-12-15-13 and 16-19-17-20-18, the storage sequence must be in the same order so that the sector storage loading signals S1L-S5L correspond to the binary counter 001, 011, 101, 010 and 100, respectively.

During the loading cycle the counter is reset after each fifth load strobe pulse. For this purpose, a flip-flop LSFF is provided which is set on the leading edge of each load strobe pulse and reset on the trailing edge. Thus, a positive-going pulse is provided at its set output terminal at the trailing edge of each load strobe pulse. This pulse is applied to an AND gate A55, which is enabled when the counter is set to 101, so that the counter is reset at the end of the load strobe pulse in which it is set to 101 through an OR gate OR28. A second input to the gate OR28 is provided by a flip-flop LFF which divides the machine cycle into load and unload periods. This flip-flop is set and reset by a pulse applied through a suitable coupling capacitor from a switch SP2, which may be assumed to be ganged with the print switch SP, and which is closed to the right to initiate the print cycle and closed to the left to initiate the load character, move paper cycle. When reset to the load state the unload terminal produces a positive-going pulse to make sure that the counter is reset.

Each load strobe pulse is used to generate five bit timing pulses L1, L2, L3, L4 and L5 for the loading of the 1, 2, 4, 8 and P bits, respectively, of each character. For this purpose a delay line comprising two oneshot multivibrators 1SM6 and 1SM7 is provided. These multivibrators are interconnected in a manner previously described to produce a train of five successively delayed counting pulses for each load strobe pulse. Specifically, a shaped pulse corresponding to the leading edge is formed as previously described by a differentiator, comprising a capacitor C23 and a resistor R3, a clamping diode D9 and a limiting circuit comprising a diode D8 blocked by a battery or other source of potential B7. The pulse so formed is applied through an OR gate OR27 to the multivibrator 1SM6, which in turn is connected to the multivibrator 1SM7. The output of the multivibrator 1SM7 is connected to one input terminal of an AND gate A54. The other input to the gate A54 is supplied through an inverter I from the L5 terminal, which is energized on the fifth delayed pulse. The output of the gate A54 is connected to the other input terminal of the gate OR27.

The positive pulse output terminal of the multivibrator 1SM6 is connected to the input terminal of a counter comprising three stages LS1, LS2 and LS4. This counter is reset at the end of each load strobe pulse by the ground level appearing at the reset output terminal of the flip-flop LSFF.

The outputs of the counter are supplied to a decoder BD4, of the type previously described, which energizes the lines L1-L5 on the successive states of the counter from 001 to 101. At the fifth count the gate A54 is dis-

abled, and the pulses circulating through the delay line are shut off.

Referring now to FIGS. **20***a* and **20***b*, each character input group **1, 2, 4, 8** and P is applied to a group of AND gates AG**6** (FIG. **20***a*) as a load strobe pulse is applied to the timing circuits TC**4** (FIG. **20***b*). The bits of the characters presented to the gates AG**6** are gated in a manner that will best be understood after a consideration of FIGS. **23** and **24.**

FIG. **23** shows the detailed manner of connecting the AND gates of the group AG**5.** As shown, each sector storage load line S1L-S5L is connected to one input terminal of five AND gates, indicated by the small circles, and the other terminal of each such gate is connected to one of the load timing lines L**1,** L**2,** L**3,** L**4** and L**5.** Thus, a separate line for the loading of each bit into each sector is provided.

As shown in FIG. **24,** the outputs of the gates of the group AG**5** are each applied to one input terminal of one AND gate of the group AG**6.** The other terminal of each such gate is connected to one of the character code bit supply lines **1, 2, 4, 8** and P. These gates thus provide five lines for each sector storage, one for each bit of the stored code.

Referring again to FIG. **20***a*, the output lines of the group of gates AG**6** are collected by sector and applied to one of five OR gates OR**29**-OR**33,** one for each sector storage. The output of each of these gates is connected to the information input terminal of one of five shift registers S1SR, S2SR, S3SR, S4SR and S5SR, one for each sector.

The shift pulses for the shift registers S1SR-S5SR are provided by five gates OR**34,** OR**35,** OR**36,** OR**37** and OR**38.** These gates are actuated during the character loading cycle by one of five AND gates A**57,** A**59,** A**61,** A**63** and A**65.** Each of these gates is enabled by a strobe LS2 from an AND gate A**67.** The inputs to the gate A**67** comprise the load signal from the timing circuit TC**4** and a strobe pulse formed by collecting the individual load lines L**1**-L**5** in an OR gate OR**42,** as shown in FIG. **20***b*.

A second input to each of the gates A**57,** A**59,** A**61,** A**63** and A**65** is provided by a different one of the sector load lines S1L, S2L, S3L, S4L and S5L. Thus, the proper sector shift register is shifted in time with the information applied from the associated gate OR**29**-OR**33** during the load cycle.

During the unload cycle, when character comparison and printing are carried out, the gates OR**34**-OR**38** are controlled by a second group of gates A**56,** A**58,** A**60,** A**62** and A**64.** Each of these gates is provided with one sector count input S**1**-S**5,** and one input from an unload strobe gate A**66.** This gate is enabled by the flip-flop PRFF and the unload signal from the timing circuit TC**4,** when the flip-flop is in its print state, to pass strobe pulses K**1**-K**20** from an OR gate OR**41** (FIG. **20***b*). The latter gate collects the twenty count lines K**1**-K**20** from the timing circuit TC**3.**

The outputs of the shift register S1SR-S5SR are applied to an OR gate OR**39.** The output of this gate is connected to one input terminal of the one-bit comparator **1**BC**2,** previously described, which functions to produce an output pulse when two applied input pulses are different.

The second input to the comparator **1**BC**2** is provided by an OR gate OR**41.** Each bit of the character-in-position code is strobed to this gate by one of AND gates A**73,** A**74,** A**75,** A**76** and A**77.** These gates each receive one of the bit timing signals t_1-t_5 from the timing circuit TC**3,** and one output terminal of the character-in-position code output of the timing circuit TC**1.**

In the manner previously described, the output of the comparator **1**BC**2** is connected to set a flip-flop XFF through an OR gate OR**40.** The other input to this gate OR**40** is energized when the flip-flop PRFF is in its recover state, as indicated in FIG. **20***b*. The output of the flip-flop XFF is sampled in the parity pulse time when the flip-flop PRFF is in the print state. For this purpose, a gate A**72** is enabled at this time, and enables a gate A**71** if the flip-flop XFF has not been set by a mismatched bit pair during the preceding five bits, including the parity bit. As shown, the flip-flop XFF is reset at the trailing edge of the parity time pulse t_p through an inverter I.

As before, the output of the gate A**71** controls the individual hammers through four AND gates A**67,** A**68,** A**69** and A**70,** which are enabled by the individual hammer scheduling lines H**1,** H**2,** H**3** and H**4** from the timing circuit TC**2.** When enabled, a pulse to any of these gates actuates the corresponding hammer driver circuit to print the character then in position.

Referring now to FIG. **21,** I have shown a typical shift register suitable for use in the embodiment of FIGS. **20***a* and **20***b*. As shown, the shift register comprises a group of twenty stages, each including a delay unit such as DU**1** and a ferromagnetic saturable switch core such as SC**1.** The delay units may comprise a diode and a capacitor as shown, and serve to delay the application of an information pulse to the input winding of the switch core while the state of the switch core is shifted to the next stage of the register by energization of the shift winding. EAch core is provided with an output winding connected to the input winding of the next stage core, except for the last core which supplies an output pulse. FIG. **22** shows the manner in which information is stored in a typical register in the system of FIGS. **20***a* and **20***b*.

FIG. **25** illustrates the operation of the system of FIGS. **20***a* and **20***b* during the load cycle. As shown, the sector storage counter cycles through a count of five for each five successive load pulses, and resets at the trailing edge of the fifth load pulse. The manner in which the load strobe pulses are generated during each load strobe pulse is shown, and typical **1, 2** and **4** bits of the character codes presented to the system are illustrated.

FIG. **26** shows the basic operation of the system during the unload cycle. As shown, the hammer scheduling pulses TH**1,** TH**2,** TH**3** and TH**4,** formed from the timing pulses K**1-5,** K**6-10,** K**11-15** and K**16-20** as shown in FIG. **18,** bridge each group of five counting pulses and enable the associated hammer at that time.

While I have described various embodiments of my invention in detail, many changes and variations will be apparent to those skilled in the art after reading my description, and such can obviously be made without departing from the scope of my invention.

I claim:

1. A printer comprising:

a print wheel bearing two fonts of character types on different sectors of the wheel and in different columns of its circumferential surface;

a hammer having a face positioned to strike against said character types and having a width sufficient to span each column;

means for rotating said print wheel so that the fonts pass by the hammer face one at a time sequentially;

means for actuating said hammer when a selected character type in either of said fonts is in striking position; and

means for inhibiting the operation of said actuating means during the passage of one of said fonts for at least those wheel revolutions in which the actuating means is operated to actuate said hammer during the passage of the other of said fonts.

2. A printer comprising:

a print wheel bearing two pluralities of character types on different sectors of the wheel and in different columns of its circumferential surface;

a hammer having a face positioned to strike against said character types and having a width sufficient to span each column;

means for rotating said print wheel so that the character type pluralities pass by the hammer face one at a time sequentially;

means for actuating said hammer when a selected character in either of said pluralities is in striking position; and

means for inhibiting the operation of said actuating means during the passage of one of said pluralities for at least those wheel revolutions in which the actuating means is operated to actuate said hammer during the passage of the other of said pluralities.

3. In a high speed printer, a type carrier assembly including:

a movable type carrier adapted to support a plurality of printing type arranged in rows in the direction of movement;

a plurality of printing hammers supported in positions to strike the printing type, each of the printing hammers including a head portion arranged to span at least two rows of the printing type;

circuit means to actuate the printing hammers in accordance with a predetermined logic;

the two rows spanned by a head portion comprising:

a first plurality of printing type positioned in one row;

a second plurality of like printing type positioned in the other of the two rows; and

one printing type in the first plurality being displaced relative to the corresponding printing type in the second plurality by a distance at least equal to the length of one of said pluralities of printing type, so that the head portion of the associated printing hammer can strike any of the printing type in the first plurality before striking any of the printing type in the second plurality; and

inhibit means for preventing said circuit means from actuating said hammers for the duration of hammer recovery intervals, said hammer recovery intervals for each hammer occurring at least after it has been actuated during the passage by it of the type plurality in one of its associated rows and each said recovery interval lasting until the type plurality in the other of its associated rows has passed it by.

4. In a high speed printer, a type carrier assembly including:

a movable carrier means adapted to support a plurality of printing type arranged in rows extending in the direction of movement of the carrier means;

a plurality of printing hammers supported in positions to strike the printing type, each of the printing hammers including a head portion arranged to span at least two rows of the printing type;

a circuit means to actuate the printing hammers in accordance with a predetermined logic;

the two rows spanned by a head portion comprising:

all the printing type in one of the two rows being arranged sequentially in a linear group with a space after the end of the group at least equal to the length of the group;

all the printing type in the other of the two rows being arranged sequentially in a linear group similar to the arrangement in the one of the two rows; and

the two groups of printing type being displaced in the direction of movement of the carrier means so that the second-mentioned group is positioned adjacent the space after the first-mentioned group, so that the head portion of the associated printing hammer can strike each printing type in the first-mentioned group before striking any printing type in the second-mentioned group; and

inhibit means for preventing said circuit means from actuating said hammers for the duration of hammer recovery intervals, said hammer recovery intervals for each hammer occurring at least after it has been actuated during the passage by it of the plurality of printing type in one of its associated rows and each said recovery interval lasting until the plurality of printing type in the other of its associated rows has passed it by.

5. In a high speed printer, a type carrier assembly including:

a movable carrier means adapted to support a plurality of printing type arranged in rows extending in the direction of movement of the carrier means;

a plurality of printing hammers supported in positions to strike the printing type, ach of the printing hammers including a head portion arranged to span at least three rows of the printing type;

circuit means to actuate the printing hammers in accordance with a predetermined logic;

the three rows spanned by a head portion comprising:

all the printing type in each respective row being arranged sequentially in a linear group with a space after each group at least equal to twice the length of the group, the spacing between the types within said groups being equal to the spacing between the first and last types in groups which are adjacent to one another in the direction of movement of said carrier means; and

each group being displaced relative to the other groups in the direction of movement of the carrier means, so that the head portion of the associated printing hammer can strike the printing type in only one group during any one stroke; and

inhibit means for preventing said circuit means from actuating said hammers during hammer recovery

intervals, said hammer recovery intervals for each hammer occurring at least after it has been actuated during the passage by it of the type plurality in one of its associated rows and said recovery interval lasting until the next adjacent type plurality in another of its associated rows in the direction of carrier movement has passed it by.

6. A printer for printing data in a row of data positions on a document comprising:

a hammer positioned adjacent said row and having a striking face spanning a plurality of adjacent data positions;

a type carrier movable past said hammer and positioned with respect to said hammer and said document so as to cause printing of a selected character on said document when said hammer is actuated, the type being arranged on said carrier in a plurality of fonts which pass said hammer one font at a time sequentially as the carrier moves, the type characters within said fonts being spaced so as to be presented to said hammer one character at a time;

means for moving said carrier;

timing means operating in synchronism with the movement of said carrier for generating a series of output code characters identifying the sequence in which the type characters of at least two of said fonts are presented to said hammer;

actuating means responsive to the identity of said selected character with one of said output code characters for actuating said hammer to cause printing of the selected character corresponding to said selected code in one of said data positions spanned by said hammer; and

means for inhibiting the operation of said actuating means during hammer recovery intervals, said hammer recovery intervals occurring at least after each hammer actuation which occurs during the passage by said area of a first of said fonts and said recovery interval lasting until the next sequentially presented font has scanned past said area.

7. The printer set forth in claim **6** wherein the plurality of type fonts on said carrier is at least equal in number to the number of data positions spanned by said hammer, and wherein said actuating means includes control means for causing said character printed in said row of data positions by said hammer to be printed from a different one of said type fonts.

8. A printer for printing data in a row of data positions on a document, comprising:

a hammer positioned adjacent said row and having a striking face spanning a plurality of adjacent data positions;

a moving type character member positioned adjacent said row and having on its surface a plurality of identical, multi-character type fonts arranged to scan past the area defined by said spanned data positions, said fonts being oriented such that the characters thereof pass said area one at a time and such that all the characters of one font pass said area before any of the characters of another font pass said area;

code means operating in synchronism with the motion of said member for generating a sequence of code signals representing the type characters of a font in the order in which they passes said area, said sequence of signals being repeated as each font passes said area;

means for storing coded input data representing characters to be printed in said spanned data positions;

signal comparison means for generating pulses to actuate said hammer;

means for controlling said signal comparison means to compare different sequences of said code signals with different ones of said stored input data characters whereby each equal comparison results in actuation of said hammer, pressing said document against said member to print a character in one of said data positions; and

inhibit means for preventing said control means from actuating said hammer during recovery intervals, said recovery intervals occurring at least after each hammer actuation which occurs during the passage of a first font by said area and said recovery interval lasting until the next sequentially presented font has passed said area.

9. The printer set forth in claim **8** wherein said control means presents said different stored input data characters for comparison in a predetermined sequence determined by the arrangement of said fonts on said type character member.

10. The printer set forth in claim **8** wherein said inhibiting time interval commences at the termination of a series of said code signals and lasts at least as long as a series of said code signals.

11. A printer for printing data in a row of data positions on a document, comprising:

a plurality of print hammers positioned adjacent said document, each said hammer spanning a set of adjacent ones of the data positions;

a rotating type drum positioned on the opposite side of said document from said hammers, said drum having on its surface a plurality of identical, multi-character type fonts arranged such that each font passes serial-by-character behind a different one of said data positions as said drum rotates, the fonts associated with the set of data positions spanned by any one of said hammers being oriented such that all the characters of one font pass their data position before any characters of another font pass their respective data position;

code means operating in synchronism with the rotation of the drum for generating a series of code signals representing the characters of a font in the order in which they move past said row of data positions, said series of code signals being repeated as each new type font passes a set of said data positions;

means for storing coded input data representing characters to be printed in said data positions, each said character being stored in said storage means at a location corresponding to the data position in which the character is to be printed;

signal comparison means for generating pulses to actuate said hammers;

means for controlling said comparison means to perform successive comparison sequences, each said sequence effecting the comparison of one series of said code signals with a selected plurality of said input data characters, said plurality of characters being selected from those locations in said storage means corresponding to the data positions then

being passed by a font on said type drum, each equal comparison resulting in actuation of an associated one of said hammers whereby said document is pressed against said drum to print a character; and

means for inhibiting said comparison operation during hammer recovery intervals, said hammer recovery intervals for each hammer occurring at least after it has been actuated during passage of a font in one of its associated data positions and said hammer recovery intervals lasting for at least the period of time required to generate one of said comparison sequences.

12. A printer for printing data in a row of data positions on a document, comprising:

a print hammer positioned adjacent said row and having a striking face spanning a plurality of adjacent ones of the data positions;

a continuously rotatable type drum positioned adjacent said row and mounted for rotation about an axis parallel thereto, said type drum having on its surface a plurality of groups of type characters positioned to scan, as said drum rotates, past the area defined by the data positions spanned by said hammer, a different type group being associated with each different data position, said different groups being arranged to move past their respective data positions in series such that all characters of a group are presented to a data position before any characters of another group are presented to any other data position;

means for actuating said hammer a plurality of times during one revolution of said drum, each said actuation operating to force said document into printing engagement with a different one of said type groups to print a character in a different one of said data positions; and

inhibit means for preventing said actuating means from actuating said hammer during hammer recovery intervals, said hammer recovery intervals occurring at least after said hammer has been actuated during the passage by said area of one of said fonts and said hammer recovery interval lasting until the next sequentially presented font has passed by said area.

13. A printer for printing data in a row of data positions on a document, comprising:

a print hammer positioned adjacent said row and having a striking face spanning a plurality of adjacent ones of the data positions;

a continuously rotatable type drum positioned adjacent said row and mounted for rotation about an axis parallel thereto, said type drum having on its surface a plurality of groups of type characters positioned to scan, as said drum rotates, past the area defined by the data positions spanned by said hammer, a different type group being associated with each different data position, said different groups being arranged to move past their respective data positions in series such that all characters of a group are presented to a data position before any characters of another group are presented to an other data position;

means for actuating said hammer a plurality of times during one revolution of said drum, said actuations operating to force said document into printing engagement in a predetermined print sequence with different ones of said type groups to print characters in different ones of said data positions, the spacing between said different ones of said type groups, measured along the circumference of said drum from the last character of one group to the first character of the next said group in said print sequence, being at least equal to the distance traversed by a point on the surface of the drum during a time interval equal to the minimum cycle time of said hammer and hammer actuating means; and

inhibit means for preventing the actuating means from actuating said hammer during hammer recovery intervals, said hammer recovery intervals occurring at least after said hammer has been actuated during the passage by said area of one of said type character groups and said hammer recovery intervals lasting until the next sequentially presented type character group has passed by said area.

14. The printer set forth in claim **13** wherein the spacing between individual type characters within each type group is no greater than that required to prevent the striking face of said hammer from striking an edge portion of the character adjacent the character being printed.

15. A printer for printing data in a row of data positions on a document, comprising:

a print hammer positioned adjacent said row and having a striking face spanning a plurality of adjacent ones of the data positions;

a type drum positioned adjacent said row and mounted for rotation about an axis parallel thereto;

means for rotating said type drum at a substantially constant velocity to move the surface thereof past said row in a direction perpendicular thereto;

said type drum having on its surface a plurality of groups of type characters positioned to scan past the area defined by the data positions spanned by said hammer, a different type group being associated with each different data position, said different groups being arranged to move past their respective data positions in series such that all characters of a group are presented to a data position before any characters of another group are presented to any other data position;

means for actuating said hammer to force said document into printing engagement with said type drum to print a character in a selected one of said data positions; and

control means including character position means for generating code signals identifying the characters passing said area and comparing means for comparing said code signals with data to be printed, said comparing means operating to generate output signals to activate said hammer actuating means in response to said comparisons, said character position means operating to present said code signals to said comparing means in a sequence wherein each series of code signals representing a type group is separated by a recovery interval having a duration at least equal to the time required to generate an entire series of code signals to permit said print hammer and said hammer actuating means to recover to their original condition in preparation for the next print operation.

16. A printer for printing data in a row of data positions on a document, comprising:
a print hammer positioned adjacent said row and having a striking face spanning a plurality of adjacent ones of the data positions;
a type carrier positioned adjacent said row;
means for moving said type carrier at a substantially constant velocity past said row;
said type carrier having on its surface a plurality of groups of type characters positioned to scan past the area defined by the data positions spanned by said hammer, said characters being spaced from one another in the direction of movement of said type carrier by substantially equal amounts, said characters further being arranged such that they move past said area one at a time with each of said spanned data positions being sequentially presented with all the characters of at least one of said type groups such that they scan past said area one group at a time whereby all the characters of one group move past a data position before any characters of another group move past any other data position;
means for actuating said hammer to force said document and said type carrier into printing engagement;
character position means for generating code signals identifying the type characters passing said area;
control means responsive to said code signals for operating said hammer actuating means to print selected characters in said data positions spanned by said hammer; and
inhibit means for preventing said control means from responding to said code signals during a recovery interval following each operation of said hammer actuating means, said recovery interval being of sufficient duration to permit said print hammer and said hammer actuating means to recover to their original condition in preparation for the next print operation, said recovery interval lasting until the next sequentially presented character group has passed said area.

17. In a printer for printing data in a row of data positions on a document, the combination comprising:
a rotating print wheel positioned adjacent said row and bearing a number of fonts of character types arranged on different wheel sectors and in different columns of its circumferential surface, so that the fonts scan past the area defined by said data positions sequentially;
a hammer positioned adjacent said row and having a striking face spanning all of the wheel columns;
control means operating in synchronism with the print wheel rotation for selectively actuating said hammer to strike said document against said character types; and
inhibit means for preventing said control means from actuating said hammer during hammer recovery intervals, said hammer recovery intervals occurring at least after each hammer actuation which occurs during the passage by said area of a first of said fonts and said recovery interval lasting until the next sequentially presented font has scanned past said area.

18. In a printer as set forth in claim 17 wherein said number is an odd number.

19. In a printer as set forth in claim 18 wherein said recovery intervals occur during the passage by said area of every other font.

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