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CONTROL OF STORED SIGNALS

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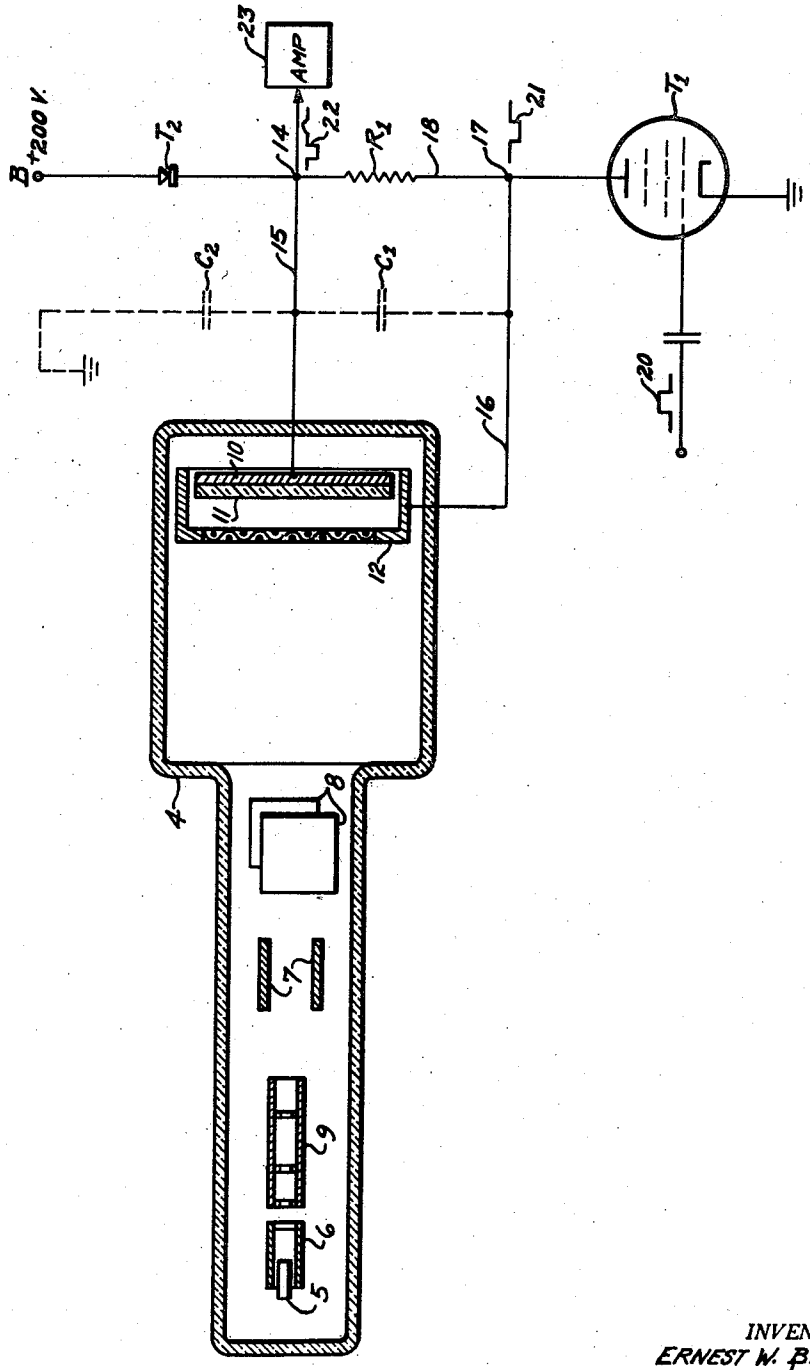

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CONTROL OF STORED SIGNALS

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The invention described herein may be manufactured and used by or for the United States Government for governmental purposes without payment to me of any royalty thereon.

The invention relates to the storage of electrical signals, and particularly to methods and means for controlling the signal storing and signal delivering ("writing" and "reading out") operations as performed through the instrumentality of a cathode ray type of storage tube incorporating a barrier grid between the electron gun and the target electrode assembly.

The invention is characterized by the modification of the read-write circuit of a barrier grid type of storage tube in such manner as to achieve a marked increase in the amplitude of the output signals read out of the tube; the signal level being increased on the order of 5000 percent, in comparison with the performance heretofore obtained.

This marked amplification of the output signal is attained, in the embodiment of the invention herein illustrated, by arranging the read-write circuit so that during the reading portion of the cycle the signal being taken off the storage surface is compelled to flow over a path of extremely high impedance, the effect of which is to build up the potential of the read circuit to a value that is far beyond that prevailing in prior art storage tube operations. Moreover, this tremendous increase in the impedance characteristic of the circuit is limited to the "read" portion of the cycle, the "write" portion of the operation being accomplished with relative electrical values substantially the same as have obtained heretofore.

Other characteristics and purposes of the invention will be understood upon reference to the following description of the embodiment of the invention illustrated in the accompanying drawing, in which the single figure is a longitudinal sectional view of a storage tube and associated circuitry embodying the invention.

The drawing shows a cathode ray tube **4** having a cathode **5**, a control grid **6**, and beam-deflecting plates **7** and **8**, co-operating with an accelerating electrode **9** to focus the beam upon the surface of the target assembly. The latter includes a metallic plate **10** to receive the signal input, a dielectric layer **11**, and a barrier grid **12**.

The function of the barrier grid in electrostatic storage may be summarized as follows: If an insulating surface is bombarded by an electron beam, the secondary emission ratio will vary with the energy of the bombarding electrons. If the energy is such that the secondary emission ratio is greater than unity, then the potential of the target surface will change with respect to the electrode which collects the secondaries, until the net number of secondaries leaving the target surface is exactly equal to the number of primaries arriving there. The surface potential, at which this action takes place, is known as the equilibrium potential. The remaining secondary electrons collect in the form of a space charge and rain back on the insulating surface, charging the unbombarded

parts of the surface to a negative potential. Thus, a charge pattern is built up on the surface in the absence of any applied signal. The returning electrons, of course, partially neutralize any charges already on the surface and, thus, would make any comparison of signals from scan to scan impossible. To eliminate this electron redistribution effect, there is interposed a short distance in advance of the target surface, a barrier grid or screen, which operates as a collector of returning electrons, and by thus minimizing potential differences between target and grid, tends to correct the difficulty above described. On the other hand, the proximity of the barrier grid to the signal energy-receiving plate **10** creates another problem in that the capacity factor thereby introduced tends to limit the output level, during signal read-out, to a very low value, bearing a ratio to the write-in signal that may be as low as 1 to 10,000. The present invention provides a remedy in the form of a new method of controlling the successive writing and reading portions of each cycle, which new method involves the utilization of widely divergent impedance factors for the two operations with the pulse write-in operation being performed at relatively low impedance, and the read-out operation against relatively high impedance.

Referring to the drawing, the signal write-in path includes pentode T_1, a plate voltage source B, a crystal diode T_2, and a tap-off connection **15** from junction **14** to plate **10**, so that upon delivery of the signal input pulse **20** to the control grid of tube T_1 a current flows from the positive voltage source B to plate **10**, and establishes the desired potential difference between plate **10** and barrier grid **12**, which is connected by conductor **16** to junction **17** in the tube plate circuit **18**. The capacity factor prevailing between the plate **10** and the barrier grid **12** is represented at C_1, while the stray capacity to ground is represented at C_2. In the embodiment illustrated C_1 will have a value of about 500 mmf., and C_2 about 15 mmf. Source B may be of 200 volts, resistor R_1 of 1 kilohm, and diode T_2 and IN56 crystal.

In operation, a positive pulse **20** applied to the grid of tube T_1 and of sufficient amplitude to trigger said tube, will cause a "write" pulse **21** of about 20 volts to be transmitted along branch line **15** to plate **10**, thence across the target ante-space to barrier grid **12**. If the cathode beam is in operation during this "write" pulse flow, any target spot which has had information stored thereon will deliver up its accumulated electrons, thus leaving an electron deficiency at said spot. During the subsequent operation of reading out the stored signal, the electron-deficient spot will attract a new charge from the barrier grid **12**; but as the return flow path for the electrons includes the extremely high impedance constituted by the back resistance of diode T_2, the output energy available to the output amplifier **23** will be of much higher magnitude than in prior art read-out circuitry, wherein there was no corresponding impedance differential between the read and write operations. Thus, whereas with prior art circuitry the ratio of the write signal to the read signal was on the order of 10,000 to 1, the circuitry illustrated herein provides a ratio of approximately 10 to 1, and a read signal whose amplitude is fifty times that heretofore obtainable.

The trigger and plate pulses may be square pulses of positive and negative polarity, respectively, as indicated, while the output to amplifier **23** will alternate, with positive "read-out" pulses of sine wave form followed by negative square wave pulses coinciding in time with the "write-in" intervals. The three wave forms referred to are illustrated at **20**, **21**, and **22**.

It will be understood that the cathode ray tube **4** includes electrical and structural elements additional to those illustrated, which elements have been omitted as

not essential to an understanding of the present invention.

What is claimed is:

1. In a signal storing system, a signal-receiving element, means for directing an electron beam towards said signal-receiving element, means for applying a signal storing potential to said signal-receiving element during operation of said electron beam-directing means, said means comprising a source of energy and a relatively low-impedance circuit from said source to said signal-receiving element, and means subsequently operable and responsive to the potential developed at said signal-receiving element for transmitting a signal proportional to said developed potential, said last-named means including a second circuit of relatively high impedance said second circuit coinciding in part with said first-named circuit.

2. In a signal storing system, a signal-receiving element, means for storing a signal-representing charge on said signal-receiving element, said means including a source of electrical energy and a circuit from said source to said signal-receiving element, said circuit being of relatively low impedance, and means including a relatively high-impedance circuit coinciding in part with said first-named circuit for subsequently transferring an electrical impulse proportional to said previously stored signal-representing charge.

3. In a signal storing system, a signal-receiving element, a signal utilizing element, means including a relatively low-impedance circuit for temporarily storing a signal in said signal-receiving element, and means including a relatively high-impedance circuit for subsequently delivering to said utilizing element an electrical impulse representative of the signal previously stored in said signal-receiving element, wherein said relatively low-impedance circuit includes a unidirectionally conductive element having a relatively high resistance to electrical energy flow in a reverse direction, and wherein said relatively high-impedance circuit is operative by way of said element in said reverse direction.

4. In a signal storing system, a signal-receiving element, a signal utilizing element, means including a relatively low-impedance circuit for temporarily storing a signal in said signal-receiving element, and means including a relatively high-impedance circuit for subsequently delivering to said utilizing element an electrical impulse representative of the signal previously stored in said signal-receiving element, wherein said relatively low-impedance circuit includes electronic amplifying means, and means for triggering said electronic amplifying means to initiate the signal storing cycle.

5. In a signal storing system, a signal-receiving element, a signal utilizing element, means including a relatively low-impedance circuit for temporarily storing a signal in said signal-receiving element, and means including a relatively high-impedance circuit for subsequently delivering to said utilizing element an electrical impulse representative of the signal previously stored in said signal-receiving element, including an impedance load common to said relatively low-impedance circuit and said relatively high-impedance circuit, and additional impedance means in said relatively high-impedance circuit.

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