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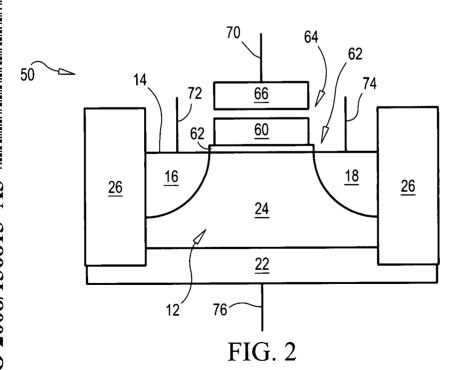
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(57) Abstract: Semiconductor memory having both volatile and non-volatile modes and methods of operation. A semiconductor memory cell includes a floating gate or trapping layer positioned in between first and second locations and above a surface of the substrate and insulated from the surface by an insulating layer; the floating gate or trapping layer being configured to receive transfer of data stored by the volatile memory and store the data as nonvolatile memory in the floating gate or trapping layer upon interruption of power to the memory cell.



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A. CLASSIFICATION OF SUBJECT MATTER IPC(8) - G11C 11/34 (2008.04) USPC - 365/185.01			
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B. FIELDS SEARCHED			
Minimum documentation searched (classification system followed by classification symbols) USPC:365/185.01			
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Electronic data base consulted during the international search (name of data base and, where practicable, search terms used) PubWEST(PGPB, USPT, USOC, EPAB, JPAB); GOOGLE Search Terms Used: power interrupt, RAM or ROM or volatile or nonvolatile, substrate, floating body or gate, insulating, trapping layer, binary, column, grid.			
C. DOCUMENTS CONSIDERED TO BE RELEVANT			
Category*	Citation of document, with indication, where ap	propriate, of the relevant passages	Relevant to claim No.
Υ	US 2006/0125010 A1 (Bhattacharyya) 15 June 2006 (15.06.2006), entire document, especially; abstract, para. [0001]-[0003], [0013]-[0023], [0059], [0060], [0104]-[0123], [0137], [0146]-[0155].		1-53
Y	US 5,519,831 A (Holzhammer) 21 May 1996 (21.05.1996), entire document, especially; abstract, Col. 3 in 59 - Col. 4 in 11; Col. 4 in 12-52.		1-53
A	US 2005/0024968 A1 (Lee et al.) 03 February 2005 (03.02.2005), entire document.		1-53
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Further documents are listed in the continuation of Box C.			
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