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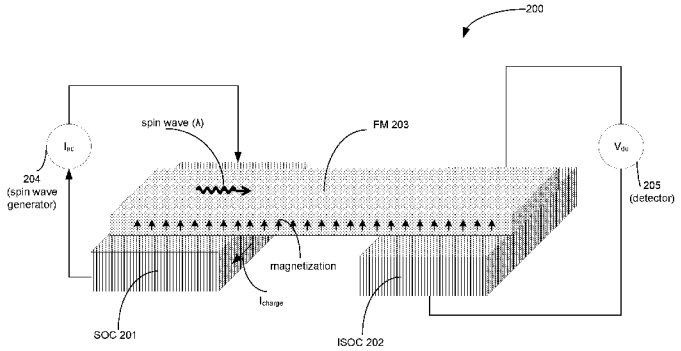

Fig. 2

(57) Abstract: Described is an apparatus which comprises: a first ferromagnet (FM) layer having a first end and a second end; a spin-orbit-coupling (SOC) layer adjacent to the first FM layer near the first end; and an inverse SOC (ISOC) layer adjacent to the first FM layer near the second end. Described is a system which comprises: a memory; a processor coupled to the memory, the processor having a spin wave device, which comprises an apparatus according to the apparatus described above; and a wireless interface for allowing the processor to communicate with another device.

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SPIN HALL EXCITED SPIN WAVE APPARATUS AND METHOD

BACKGROUND

[0001] Multiple exploratory logic devices are based on ferromagnetic (FM) elements. AC (Alternating Current) perturbations of magnetization in a FM are spin waves (e.g., propagating disturbances in the ordering of magnetic materials). These spin waves are akin to lattice waves in a solid system. Spin waves are also referred to as magnons. Spin logic and magnetic memory can enable a new class of logic circuits and architectures for beyond-CMOS (Complementary Metal Oxide Semiconductor) computing. One basic component of logic circuits are interconnects for connecting various nodes of the logic circuits. For seamless interconnection, it is advantageous to build interconnects which are magnetic/spintronic too. One of the promising interconnects are spin wave interconnects. However, experimentally demonstrated spin wave structures rely on magnetic field of RF (Radio Frequency) antennas. The RF antennas are too large and consume too much power to be competitive with electrical interconnects.

BRIEF DESCRIPTION OF THE DRAWINGS

[0002] The embodiments of the disclosure will be understood more fully from the detailed description given below and from the accompanying drawings of various embodiments of the disclosure, which, however, should not be taken to limit the disclosure to the specific embodiments, but are for explanation and understanding only.

[0003] **Fig. 1** illustrates a scheme of spin wave excitation and detection by RF antennas.

[0004] **Fig. 2** illustrates a spin wave interconnect with spin orbit coupling (SOC) for generating spin waves and inverse SOC (ISOC) for detecting spin waves, in accordance with some embodiments of the disclosure.

[0005] **Fig. 3** illustrates a spin wave interconnect with capping layers and with SOC for generating spin waves and with ISOC for detecting spin waves, in accordance with some embodiments of the disclosure.

[0006] **Fig. 4** illustrates a portion of the spin wave interconnect as it is coupled to a SOC material, in accordance with some embodiments of the disclosure.

[0007] **Fig. 5A** illustrates a multi-input logic device using spin wave interconnects, in accordance with some embodiments of the disclosure.

[0008] **Fig. 5B** illustrates a multi-input logic device using in-plane spin wave interconnects, in accordance with some embodiments of the disclosure.

[0009] **Fig. 6** illustrates a flowchart of a method of using the spin wave interconnect scheme, according to some embodiments of the disclosure.

[0010] **Fig. 7** illustrates a plot showing magnetization precession versus time at different points along the spin wave interconnect, according to some embodiments of the disclosure.

[0011] **Fig. 8** illustrates a smart device or a computer system or a SoC (System-on-Chip) with a spin wave interconnect, according to some embodiments of the disclosure.

DETAILED DESCRIPTION

[0012] Spin waves can be generated by DC current applied to an (Radio Frequency) RF antenna, where the resulting magnetic field generates the spin waves. These spin waves in turn generate AC magnetic field which is detected by another antenna. **Fig. 1** illustrates scheme 100 of spin wave excitation and detection by RF antennas. The scheme consists of a layer of silicon (Si) substrate adjacent to a silicon oxide (SiO_2) layer which is adjacent to a FM layer (e.g., CoFe). The FM can behave as interconnect for spin waves which are generated by RF excitation and detected by detection antennas formed over the FM layer in a layer of SiO_2. As shown, the RF antennas are large structures (as compared to integrated circuits used in processors). For example, each of the RF excitation and detection antennas can be a few microns in size. Further, large current (e.g., several mili-Amperes (mA)) is required to generate spin waves in the scheme of **Fig. 1**.

[0013] Some embodiments describe spin wave interconnects that use spin Hall effect (SHE) (more generally, spin-orbit coupling (SOC)) both to generate and detect spin waves. In some embodiments, on one end of an FM interconnect, conducting AC current in a SHE material exerts spin torque on the FM and excites spin waves. These spin waves propagate along the FM interconnect. The spin wave (e.g., oscillating magnetization) creates spin-polarized current in the FM interconnect. In an inverse SOC (ISOC) material, the spin polarized current of the spin wave is converted to charge current and then to voltage which is detected, in accordance with some embodiments.

[0014] In the following description, numerous details are discussed to provide a more thorough explanation of embodiments of the present disclosure. It will be apparent, however, to one skilled in the art, that embodiments of the present disclosure may be practiced without these specific details. In other instances, well-known structures and devices are shown in

block diagram form, rather than in detail, in order to avoid obscuring embodiments of the present disclosure.

[0015] Note that in the corresponding drawings of the embodiments, signals are represented with lines. Some lines may be thicker, to indicate more constituent signal paths, and/or have arrows at one or more ends, to indicate primary information flow direction. Such indications are not intended to be limiting. Rather, the lines are used in connection with one or more exemplary embodiments to facilitate easier understanding of a circuit or a logical unit. Any represented signal, as dictated by design needs or preferences, may actually comprise one or more signals that may travel in either direction and may be implemented with any suitable type of signal scheme.

[0016] Throughout the specification, and in the claims, the term "connected" means a direct connection, such as electrical, mechanical, or magnetic connection between the things that are connected, without any intermediary devices. The term "coupled" means a direct or indirect connection, such as a direct electrical, mechanical, or magnetic connection between the things that are connected or an indirect connection, through one or more passive or active intermediary devices. The term "circuit" or “module” may refer to one or more passive and/or active components that are arranged to cooperate with one another to provide a desired function. The term "signal" may refer to at least one current signal, voltage signal, magnetic signal, or data/clock signal. The meaning of "a," "an," and "the" include plural references. The meaning of "in" includes "in" and "on."

[0017] The term “scaling” generally refers to converting a design (schematic and layout) from one process technology to another process technology and subsequently being reduced in layout area. The term “scaling” generally also refers to downsizing layout and devices within the same technology node. The term “scaling” may also refer to adjusting (e.g., slowing down or speeding up – i.e. scaling down, or scaling up respectively) of a signal frequency relative to another parameter, for example, power supply level. The terms “substantially,” “close,” “approximately,” “near,” and “about,” generally refer to being within +/- 10% of a target value.

[0018] Unless otherwise specified the use of the ordinal adjectives “first,” “second,” and “third,” etc., to describe a common object, merely indicate that different instances of like objects are being referred to, and are not intended to imply that the objects so described must be in a given sequence, either temporally, spatially, in ranking or in any other manner.

[0019] For the purposes of the present disclosure, phrases “A and/or B” and “A or B” mean (A), (B), or (A and B). For the purposes of the present disclosure, the phrase “A, B,

and/or C" means (A), (B), (C), (A and B), (A and C), (B and C), or (A, B and C). The terms "left," "right," "front," "back," "top," "bottom," "over," "under," and the like in the description and in the claims, if any, are used for descriptive purposes and not necessarily for describing permanent relative positions.

[0020] **Fig. 2** illustrates apparatus 200 showing spin wave interconnect with SOC for generating spin waves and with ISOC for detecting spin waves, in accordance with some embodiments of the disclosure. In some embodiments, apparatus 200 comprises a layer of SOC material 201, a layer of ISOC material 202, ferromagnet (FM) interconnect 203, spin wave generator 204, and spin wave detector 205.

[0021] In some embodiments, the layer of SOC material 201 is adjacent to FM interconnect 203 at one end of FM interconnect 203. In some embodiments, the layer of SOC material 201 is directly below or under FM interconnect 203. In some embodiments, the layer of ISOC material 202 is adjacent to FM interconnect 203 at another end of FM interconnect 203. In some embodiments, the layer of ISOC material 202 is directly below or under FM interconnect 203. In some embodiments, spin wave generator 204 is coupled to the layer of SOC material 201 such that one terminal of spin wave generator 204 is coupled to one end of the layer of SOC material 201 while another terminal of spin wave generator 204 is coupled to another end of the layer of SOC material 201, where the two ends are substantially opposite to one another. In some embodiments, the two ends of the layer of SOC material 201 have metal regions for coupling to spin wave generator 204. If a charge current is injected to SOC materials, it produces a spin polarized current at its surface (i.e., direct SOC effect). In some embodiments, spin wave generator 204 is a current source I_{ac} that provides charge current I_{charge}. This charge current flows along the length of the layer of SOC material 201.

[0022] In some embodiments, the layer of SOC material 201 is operable to exhibit spin Hall effect (SHE). In some embodiments, the layer of SOC material 201 is made of one or more of β-Tantalum (β-Ta), Ta, β-Tungsten (β-W), W, Pt, Copper (Cu) doped with elements such as Iridium, Bismuth and any of the elements of 3d, 4d, 5d, 4f, and 5f periodic groups in the Periodic Table which may exhibit high spin orbit coupling, α-Sn, Bi_2O_3, MoS_2, Bi and Ag multilayers, and 2D dichalocgenides of the form MX_2, where 'X' is one of S, Se, or Te, and where 'M' are transition elements. In some embodiments, ISOC materials are desired to be of high resistivity, while the SOC materials are desired to have lower resistivity.

[0023] In some embodiments, the layer of SOC material 201 is coupled to high conductivity non-magnetic metal(s) (e.g., spin injection layer) to reduce the resistance of the

layer of SOC material 201. In some embodiments, the non-magnetic metals are formed from one or more of: Cu, Co, α-Ta, Al, CuSi, or NiSi, and these non-magnetic metals are coupled to the terminals of spin wave generator 204.

[0024] In some embodiments, FM 203 is formed of CFGG (i.e., Cobalt (Co), Iron (Fe), Germanium (Ge), or Gallium (Ga) or a combination of them). In some embodiments, FM 203 is formed from Heusler alloys. Heusler alloys are ferromagnetic metal alloys based on a Heusler phase. Heusler phases are intermetallic with certain composition and face-centered cubic crystal structure. The ferromagnetic property of the Heusler alloys are a result of a double-exchange mechanism between neighboring magnetic ions.

[0025] In some embodiments, FM 203 is formed of one of: Heusler alloy, Co, Fe, Ni, Gd, B, Ge, Ga, permalloy, Yttrium Iron Garnet (YIG), or a combination of them. In some embodiments, Heusler alloys are one of: Cu_2MnAl, Cu_2MnIn, Cu_2MnSn, Ni_2MnAl, Ni_2MnIn, Ni_2MnSn, Ni_2MnSb, Ni_2MnGa Co_2MnAl, Co_2MnSi, Co_2MnGa, Co_2MnGe, Pd_2MnAl, Pd_2MnIn, Pd_2MnSn, Pd_2MnSb, Co_2FeSi, Co_2FeAl, Fe_2VAl, Mn_2VGa, Co_2FeGe, MnGa, or MnGaRu.

[0026] In some embodiments, FM 203 is formed with a sufficiently high anisotropy (H_k) and sufficiently low magnetic saturation (M_s) to increase injection of spin currents. Magnetic saturation M_s is generally the state reached when an increase in applied external magnetic field H cannot increase the magnetization of the material (i.e., total magnetic flux density B substantially levels off). Here, sufficiently low M_s refers to M_s less than 200 kA/m (kilo-Amperes per meter). Anisotropy H_k generally refers to the material property which is directionally dependent. Materials with high H_k are materials with material properties that are highly directionally dependent. Here, sufficiently high H_k in context of Heusler alloys is considered to be greater than 2000 Oe (Oersted).

[0027] In some embodiments, FM 203 is a free magnetic layer. The thickness of a ferromagnetic layer may determine its magnetization direction. For example, when the thickness of the ferromagnetic layer is above a certain threshold (depending on the material of the magnet, e.g., approximately 1.5 nm for CoFe), then the ferromagnetic layer exhibits magnetization direction which is in-plane. Likewise, when the thickness of the ferromagnetic layer is below a certain threshold (depending on the material of the magnet), then the ferromagnetic layer exhibits magnetization direction which is perpendicular to the plane of the magnetic layer. Other factors may also determine the direction of magnetization.

[0028] For example, factors such as surface anisotropy (depending on the adjacent layers or a multi-layer composition of the ferromagnetic layer) and/or crystalline anisotropy

(depending on stress and the crystal lattice structure modification such as FCC (face centered cubic) lattice, BCC (body centered cubic) lattice, or L10-type of crystals, where L10 is a type of crystal class which exhibits perpendicular magnetizations), can also determine the direction of magnetization.

[0029] In some embodiments, FM 203 has perpendicular magnetic anisotropy (PMA). For example, FM 203 is magnetized perpendicular to the plane of the chip having apparatus 200. In some embodiments, magnets with PMA are formed with multiple layers in a stack. The multiple thin layers can be layers of Cobalt and Platinum (i.e., Co/Pt), for example. Other examples of the multiple thin layers include: Co and Pd; Co and Ni; MgO, CoFeB, Ta, CoFeB, and MgO; MgO, CoFeB, W, CoFeB, and MgO; MgO, CoFeB, V, CoFeB, and MgO; MgO, CoFeB, Mo, CoFeB, MgO; Mn_xGa_y; Materials with L10 crystal symmetry; or materials with tetragonal crystal structure. In some embodiments, the perpendicular magnetic layer is formed of a single layer of one or more materials (e.g., $Mn_xRu_yGa_zGe_k$). In some embodiments, the single layer is formed of MnGa. In some embodiments, the perpendicular magnetic layer is formed of one of: a Heusler alloy, Co, Fe, Ni, Gd, B, Ge, Ga, permalloy, YIG, or a combination of them.

[0030] In some embodiments, when spin wave generator 204 provides charge current I_{charge} which flows along the length of SOC 201, spin polarized current I_s is generated. The spin polarized current is generated at the surface of SOC 201 which is adjacent to FM 203, in accordance with some embodiments. This spin polarized current exerts an AC torque on the magnetization in plane direction. As such, polarized current cause spin wave (with wavelength λ) to be generate in FM 203 which has PMA. A spin wave is a harmonic perturbation propagating along FM 203 in which magnetization is around its average direction. The spin wave propagates from one end of FM 203 to the other end of FM 203. In some embodiments, a layer of ISOC material 202 is positioned adjacent to the other end of FM 203. In some embodiments, the layer of ISOC material 202 is under FM 203. In some embodiments, the spin wave and its associated spin current reaches the layer of ISOC material 202.

[0031] In some embodiments, the layer of ISOC material 202 is made of one or more of β-Tantalum (β-Ta), Ta, β-Tungsten (β-W), W, Pt, Copper (Cu) doped with elements such as Iridium, Bismuth and any of the elements of 3d, 4d, 5d, 4f, and 5f periodic groups in the Periodic Table which may exhibit high spin orbit coupling, α-Sn, Bi_2O_3, MoS_2, Bi and Ag multilayers, and 2D dichalocgenides of the form MX_2, where 'X' is one of S, Se, or Te, and where 'M' are transition elements. In some embodiments, the layer of ISOC materials 202

are desired to be of higher resistivity, while the layer of SOC materials 201 are desired to be of comparatively lower resistivity.

[0032] In some embodiments, spin-to-charge conversion is achieved by the layer of ISOC material 202 via spin orbit interaction in metallic interfaces (i.e., using Inverse Rashba-Edelstein Effect (IREE) and/or Inverse SHE (ISHE)), where a spin current injected from an input magnet produces a charge current I_c. In some embodiments, Spin Orbit Coupling (e.g., spin Hall effect) is used for transduction from both magnet state to current and back. Spin Orbit Coupling is more efficient switching mechanism for transduction from the magnetization direction to current and for switching magnetization.

[0033] **Table 1** summarizes transduction mechanisms for converting spin current to charge current and charge current to spin current for bulk materials and interfaces.

Table 1: Transduction mechanisms for Spin to Charge and Charge to Spin Conversion using SOC

	Charge → Spin	**Spin → Charge**
Bulk	e.g., Spin Hall Effect	e.g., Inverse Spin Hall Effect
Interface	e.g., Rashba-Edelstein Effect	e.g., Inverse Rashba-Edelstein effect

[0034] In some embodiments, the layer of ISOC material 202 comprises layers of materials exhibiting inverse spin orbit coupling such as one of inverse SHE (ISHE) or inverse Rashba-Edelstein effect (IREE). In some embodiments, the layer of ISOC material 202 comprises a stack of layers with materials exhibiting IREE and ISHE effects. In some embodiments, the layer of ISOC material 202 comprises a metal layer, such as a layer of Copper (Cu), Silver (Ag), or Gold (Au), which is coupled to FM 203. In some embodiments, the metal layer is a non-alloy metal layer.

[0035] In some embodiments, the layer of ISOC material 202 acts as the appropriate template for creating FM layer 203 or provides a suitable atomic structure for high spin injection and low lattice mismatch. In some embodiments, the layer of ISOC material 202 comprises elements of 5d transition series or materials with high spin to orbit coupling (topological materials) such as BiSe and BiTe. In some embodiments, the layer of ISOC material 202 comprises a bulk layer which is directly coupled to FM layer 203. In some embodiments, the layer of ISOC material 202 is defined as a layer formed of surface alloy layer and bulk layer, where the surface alloy is adjacent to the bulk layer (e.g., the bulk layer is below the surface layer).

[0036] In some embodiments, the surface alloy is a templating metal layer (also referred to as an interface layer) to provide a template for forming FM layer 203. In some

embodiments, the surface alloy is formed of Bismuth (Bi) on Ag coupled to a metal layer. In some embodiments, the metal of the metal layer is directly coupled to FM 203. In some embodiments, the metal of the metal layer is a noble metal (e.g., Ag, Cu, or Au) doped with other elements for group 4d and/or 5d of the Periodic Table. In some embodiments, the surface alloy is one of: Bi-Ag, Antimony-Bismuth (Sb-Bi), Sb-Ag, Lead-Nickel (Pb-Ni), Bi-Au, Pb-Ag, Pb-Au, β-Ta; β-W; Pt; or Bi_2Te_3. In some embodiments, one of the metals of the surface alloy is an alloy of heavy metal or of materials with high SOC strength, where the SOC strength is directly proportional to the fourth power of the atomic number of the metal.

[0037] In some embodiments, the bulk layer is a stack of materials such as a stack of Ag-Bi-Ag; Cu-Bi-Ag; Cu-Bi-Ag-$[Cu\text{-}Bi\text{-}Ag]_n$ (where 'n' is an integer); Cu-Bi-Ag-[Cu-Bi-Ag][PbAg-SbAg]; Cu and Cu-Bi-Ag-β-Ta; Cu and Cu-Bi-Ag, β-W; Cu and Cu-Bi-Ag- β-Hf; Cu and Cu-Bi-Ag-Bi_xSe_y, etc.

[0038] Here, the crystals of Ag and Bi of the layer of ISOC material 202 have lattice mismatch (i.e., the distance between neighboring atoms of Ag and Bi is different). In some embodiments, the surface alloy is formed with surface corrugation resulting from the lattice mismatch, (e.g., the positions of Bi atoms are offset by varying distance from a plane parallel to a crystal plane of the underlying metal). In some embodiments, the surface alloy is a structure not symmetric relative to the mirror inversion defined by a crystal plane. This inversion asymmetry and/or material properties lead to spin-orbit coupling in electrons near the surface (also referred to as the Rashba effect).

[0039] In some embodiments, when the spin current I_s from FM 203 flows through the 2D (two dimensional) electron gas between Bi and Ag in ISOC layer 202 with high SOC, charge current I_c is generated. In some embodiments, the interface surface alloy of $BiAg_2$ or $PbAg_2$ of ISOC layer 202 comprises of a high density 2D electron gas with high Rashba SOC. The spin orbit mechanism responsible for spin-to-charge conversion is described by Rashba effect in 2D electron gases. In some embodiments, 2D electron gases are formed between Bi and Ag, and when current flows through the 2D electron gases, it becomes a 2D spin gas because as charge flows, electrons get polarized.

[0040] The Hamiltonian energy H_R of the SOC electrons in the 2D electron gas corresponding to the Rashba effect is expressed as:

$$H_R = \alpha_R(k \times \hat{z}).\dot{\sigma} \quad \ldots (3)$$

where α_R is the Rashba coefficient, 'k' is the operator of momentum of electrons, $\hat{z}$ is a unit vector perpendicular to the 2D electron gas, and $\dot{\sigma}$ is the operator of spin of electrons.

[0041] The spin polarized electrons with direction of polarization in-plane (in the xy-plane) experience an effective magnetic field dependent on the spin direction which is given as:

$$B(\grave{k}) = \frac{\alpha_R}{\mu_B}(\grave{k} \times \hat{z}) \quad \ldots (4)$$

where μ_B is the Bohr magneton.

[0042] This results in the generation of a charge current in the interconnect proportional to the spin current I_s. The spin orbit interaction at the Ag and Bi interface (i.e., the Inverse Rashba-Edelstein Effect (IREE)) produces a charge current I_c in the horizontal direction which is expressed as:

$$I_c = \frac{\lambda_{IREE} I_s}{w_m} \quad \ldots (5)$$

where w_m is width of the magnet, and λ_{IREE} is the IREE constant (with units of length) proportional to α_R.

[0043] The IREE effect produces spin-to-charge current conversion around 0.1 with existing materials at 10nm magnet width. For scaled nanomagnets (e.g., 5 nm width) and exploratory SHE materials such as Bi_2Se_3, the spin-to-charge conversion efficiency can be between 1 and 2.5, in accordance with some embodiments. The net conversion of the drive charge current I_d to magnetization dependent charge current is:

$$I_c = \pm \frac{\lambda_{IREE} P I_d}{w_m} \quad \ldots (6)$$

where P is the spin polarization. The charge current I_c propagates through non-magnetic metal contacts coupled to the layer of ISOC material 202, in accordance with some embodiments. In some embodiments, this charge current is detected by detector 205, which is coupled to the non-magnetic contacts (which in turn are coupled to the layer of ISOC material 202). In some embodiments, the spin wave is detected at the interface between the layer of ISOC material 202 and FM 203. Precession of magnetization cause pin polarized current to be emitted by FM 203. This spin current is converted charged current or produces charge current by the layer of ISOC material 202, and this charge current can be converted to a representative voltage across the layer of ISOC material 202, in accordance with some embodiments.

[0044] **Fig. 3** illustrates apparatus 300 of a spin wave interconnect with capping layers and with SOC for generating spin waves and ISOC for detecting spin waves, in accordance with some embodiments of the disclosure. It is pointed out that those elements of **Fig. 3** having the same reference numbers (or names) as the elements of any other figure can

operate or function in any manner similar to that described, but are not limited to such. So as not to obscure the embodiments of the disclosure, differences between **Fig. 3** and **Fig. 2** are described.

[0045] **Fig. 3** is similar to **Fig. 2** except that a stack of layers is formed above FM 203. In some embodiments, the stack of layers include layer 301 (e.g., layer of Ru) which is adjacent to FM 203. In some embodiments, layer 302 (e.g., layer of Ta) is added which is adjacent to layer 301. In some embodiments, layer 303 (e.g., layer Ru) is added which is adjacent to layer 303. In some embodiments, layers 301, 302, and 303 are capping layers to protect FM 203 from oxidation.

[0046] **Fig. 4** illustrates a portion 400 of the spin wave interconnect as it is coupled to a SOC material, in accordance with some embodiments of the disclosure. It is pointed out that those elements of **Fig. 4** having the same reference numbers (or names) as the elements of any other figure can operate or function in any manner similar to that described, but are not limited to such. Here, non-magnetic metal terminals 401 and 402 are formed adjacent along the length of SOC 201. In some embodiments, non-magnetic metal terminals are also formed adjacent along the length of the layer of ISOC material 202. These non-magnetic metal terminals are used to electrically couple the spin wave generator 204 to the layer of SOC material 201, and also to electrically couple spin wave detector 205 to the layer of ISOC material 202. In some embodiments, the non-magnetic metals are formed from one or more of: Cu, Co, α-Ta, Al, CuSi, or NiSi.

[0047] **Fig. 5A** illustrates a multi-input logic device 500 using spin wave interconnects, in accordance with some embodiments of the disclosure. It is pointed out that those elements of **Fig. 5A** having the same reference numbers (or names) as the elements of any other figure can operate or function in any manner similar to that described, but are not limited to such.

[0048] In some embodiments, spin wave interconnects can be used to form a multi-input logic device. In some embodiments, the spin waves from each spin wave interconnect add or cancel each other at the interface of an ISOC layer and the spin wave interconnects to result in a final current. This final current indicates the logic value, in accordance with some embodiments. In some embodiments, multi-input logic device 500 comprises three spin wave interconnects FM502, FM 503, and FM 504 which converge on ISOC layer 501. In this example, spin wave interconnects FM502, FM 503, and FM 504 are shown in different levels (e.g., FM 503 being above FM 502, and FM 504 being above FM 503) and converging on to ISOC 501 through FM connections FM 505 and FM 506 as shown. However, the

embodiments are not limited to such topology. In some embodiments, spin wave interconnects FM502, FM 503, and FM 504 are on the same level and converge directly on to ISOC 501 from different directions.

[0049] So as not to obscure the embodiments, the spin wave generators and associated SOC layers adjacent to the respective FM interconnects are not shown. Regardless of how the spin waves are generated for each FM interconnect, these spin waves can be considered as input logic values (e.g., input 1, input 2, and input 3) to device 500, in accordance with some embodiments of the disclosure. While the embodiment of **Fig. 5A** is illustrated with reference to three inputs, fewer or more inputs can be used to form a multi-input logic spin wave device.

[0050] Depending on the wavelength (λ) of each spin wave on the respective FM interconnect, constructive or destructive interference may occur at the interfaces of the FM interconnects and ISOC layer 501. In this example, spin wave in FM 502 has wavelength $\lambda 1$, spin wave in FM 503 has wavelength $\lambda 2$, and spin wave in FM 504 has wavelength $\lambda 3$. For the case, where $\lambda 1$ is same as $\lambda 3$ (e.g., spin waves on FM 502 and FM 504 are in phase) while $\lambda 1$ is 90 degrees out of phase relative to $\lambda 2$ (e.g., spin waves on FM 502 and FM 504 are out of phase relative to spin wave of FM 503), the resultant voltage detected by a spin wave detector (not shown) will be determined by spin waves on FM 502, FM 503, and FM 504. In this example, spin waves on FM 504 and FM 502 add to one another while spin wave on FM 503 subtracts from the summed spin waves. As such, the resultant logic is determined by the logic value of spin waves of FM 502 or FM 504.

[0051] In one example, spin waves which are in-phase represent logic 1 and spin waves which are out of phase represent logic 0. As such, a majority spin wave function is achieved by multi-input logic device 500. In other embodiments, spin waves which are in-phase represent logic 0 and spin waves which are out of phase represent logic 1 to operate multi-input logic device 500.

[0052] **Fig. 5B** illustrates a multi-input logic device 520 using in-plane spin wave interconnects, in accordance with some embodiments of the disclosure. It is pointed out that those elements of **Fig. 5B** having the same reference numbers (or names) as the elements of any other figure can operate or function in any manner similar to that described, but are not limited to such. Multi-input logic device 520 is similar to **Fig. 5A** except that the spin interconnects 503, 504, and 505 are in-plane and coupled to ISOC layer 501.

[0053] **Fig. 6** illustrates flowchart 600 of a method of using the spin wave interconnect scheme, according to some embodiments of the disclosure. It is pointed out that

those elements of **Fig. 6** having the same reference numbers (or names) as the elements of any other figure can operate or function in any manner similar to that described, but are not limited to such.

[0054] Although the blocks in the flowchart with reference to **Fig. 6** are shown in a particular order, the order of the actions can be modified. Thus, the illustrated embodiments can be performed in a different order, and some actions/blocks may be performed in parallel. Some of the blocks and/or operations listed in **Fig. 6** are optional in accordance with certain embodiments. The numbering of the blocks presented is for the sake of clarity and is not intended to prescribe an order of operations in which the various blocks must occur. Additionally, operations from the various flows may be utilized in a variety of combinations.

[0055] At block 601, first spin wave is generated by the layer of SOC material 201 as described with reference to **Fig 2**, where the first spin wave is to propagate through a first FM 203 adjacent to the layer of SOC material 201. At block 606, the layer of ISOC material 202 converts the spin current associated with the first spin wave to charge current. In some embodiments, this charge current causes a voltage drop across the layer of ISOC material 202, and this voltage drop is detected by spin detector 205. Blocks 601 and 606 illustrate the case where a spin wave is generated, propagated, and then detected. Blocks 602-605 illustrate the logic computation from various spin waves on different FM interconnects as described with reference to **Figs. 5A-B**.

[0056] Referring back to **Fig. 6**, at block 602, a second spin wave is generated on FM 503, where the second FM is also adjacent to the layer of ISOC material 202 or 501 at the end of the second FM interconnect. In this example, the first spin wave is generated on FM 502. At block 603, a third spin wave is generated on FM 504, where the third FM is also adjacent to the layer of ISOC material 202 or 501 at the end of the third FM interconnect. Depending on the wavelengths of the first, second, and third spin waves and whether they cause constructive or destructive interference at the interface of the FM interconnects and the layer of ISOC material 202/501, a particular charge current magnitude is generated in the layer of ISOC material 202/501.

[0057] At block 604, a spin detector (e.g., a voltage detector) is applied across two ends of ISOC layer 501 to measure the voltage drop (and hence the current magnitude) in ISOC 501. The voltage level detected depends on the constructive or destructive interference of the first, second, and third spin waves. Different voltage levels may represent different logic levels, in accordance with some embodiments. At block 605, a logic value is determined according to the detected voltage.

[0058] **Fig. 7** illustrates plot 700 showing magnetization precession versus time at different points along the spin wave interconnect, according to some embodiments of the disclosure. It is pointed out that those elements of **Fig. 7** having the same reference numbers (or names) as the elements of any other figure can operate or function in any manner similar to that described, but are not limited to such. Here x-axis is time and y-axis is magnetization precession. Plot 700 demonstrates that a spin wave packet can propagate over a few microns.

[0059] **Fig. 8** illustrates a smart device or a computer system or a SoC (System-on-Chip) 1600 with an apparatus having spin wave interconnect, according to some embodiments of the disclosure. It is pointed out that those elements of **Fig. 8** having the same reference numbers (or names) as the elements of any other figure can operate or function in any manner similar to that described, but are not limited to such.

[0060] **Fig. 8** illustrates a block diagram of an embodiment of a mobile device in which flat surface interface connectors could be used. In some embodiments, computing device 1600 represents a mobile computing device, such as a computing tablet, a mobile phone or smart-phone, a wireless-enabled e-reader, or other wireless mobile device. It will be understood that certain components are shown generally, and not all components of such a device are shown in computing device 1600.

[0061] For purposes of the embodiments, the transistors in various circuits and logic blocks described here are metal oxide semiconductor (MOS) transistors or their derivatives, where the MOS transistors include drain, source, gate, and bulk terminals. The transistors and/or the MOS transistor derivatives also include Tri-Gate and FinFET transistors, Gate All Around Cylindrical Transistors, Tunneling FET (TFET), Square Wire, or Rectangular Ribbon Transistors, ferroelectric FET (FeFETs), or other devices implementing transistor functionality like carbon nanotubes or spintronic devices. MOSFET symmetrical source and drain terminals i.e., are identical terminals and are interchangeably used here. A TFET device, on the other hand, has asymmetric Source and Drain terminals. Those skilled in the art will appreciate that other transistors, for example, Bi-polar junction transistors (BJT PNP/NPN), BiCMOS, CMOS, etc., may be used without departing from the scope of the disclosure.

[0062] In some embodiments, computing device 1600 includes first processor 1610 with an apparatus having spin wave interconnect, according to some embodiments discussed. Other blocks of the computing device 1600 may also include an apparatus having spin wave interconnect, according to some embodiments. The various embodiments of the present disclosure may also comprise a network interface within 1670 such as a wireless interface so

that a system embodiment may be incorporated into a wireless device, for example, cell phone or personal digital assistant.

[0063] In some embodiments, processor 1610 can include one or more physical devices, such as microprocessors, application processors, microcontrollers, programmable logic devices, or other processing means. The processing operations performed by processor 1610 include the execution of an operating platform or operating system on which applications and/or device functions are executed. The processing operations include operations related to I/O (input/output) with a human user or with other devices, operations related to power management, and/or operations related to connecting the computing device 1600 to another device. The processing operations may also include operations related to audio I/O and/or display I/O.

[0064] In some embodiments, computing device 1600 includes audio subsystem 1620, which represents hardware (e.g., audio hardware and audio circuits) and software (e.g., drivers, codecs) components associated with providing audio functions to the computing device. Audio functions can include speaker and/or headphone output, as well as microphone input. Devices for such functions can be integrated into computing device 1600, or connected to the computing device 1600. In one embodiment, a user interacts with the computing device 1600 by providing audio commands that are received and processed by processor 1610.

[0065] In some embodiments, computing device 1600 comprises display subsystem 1630. Display subsystem 1630 represents hardware (e.g., display devices) and software (e.g., drivers) components that provide a visual and/or tactile display for a user to interact with the computing device 1600. Display subsystem 1630 includes display interface 1632, which includes the particular screen or hardware device used to provide a display to a user. In one embodiment, display interface 1632 includes logic separate from processor 1610 to perform at least some processing related to the display. In one embodiment, display subsystem 1630 includes a touch screen (or touch pad) device that provides both output and input to a user.

[0066] In some embodiments, computing device 1600 comprises I/O controller 1640. I/O controller 1640 represents hardware devices and software components related to interaction with a user. I/O controller 1640 is operable to manage hardware that is part of audio subsystem 1620 and/or display subsystem 1630. Additionally, I/O controller 1640 illustrates a connection point for additional devices that connect to computing device 1600 through which a user might interact with the system. For example, devices that can be attached to the computing device 1600 might include microphone devices, speaker or stereo

systems, video systems or other display devices, keyboard or keypad devices, or other I/O devices for use with specific applications such as card readers or other devices.

[0067] As mentioned above, I/O controller 1640 can interact with audio subsystem 1620 and/or display subsystem 1630. For example, input through a microphone or other audio device can provide input or commands for one or more applications or functions of the computing device 1600. Additionally, audio output can be provided instead of, or in addition to display output. In another example, if display subsystem 1630 includes a touch screen, the display device also acts as an input device, which can be at least partially managed by I/O controller 1640. There can also be additional buttons or switches on the computing device 1600 to provide I/O functions managed by I/O controller 1640.

[0068] In some embodiments, I/O controller 1640 manages devices such as accelerometers, cameras, light sensors or other environmental sensors, or other hardware that can be included in the computing device 1600. The input can be part of direct user interaction, as well as providing environmental input to the system to influence its operations (such as filtering for noise, adjusting displays for brightness detection, applying a flash for a camera, or other features).

[0069] In some embodiments, computing device 1600 includes power management 1650 that manages battery power usage, charging of the battery, and features related to power saving operation. Memory subsystem 1660 includes memory devices for storing information in computing device 1600. Memory can include nonvolatile (state does not change if power to the memory device is interrupted) and/or volatile (state is indeterminate if power to the memory device is interrupted) memory devices. Memory subsystem 1660 can store application data, user data, music, photos, documents, or other data, as well as system data (whether long-term or temporary) related to the execution of the applications and functions of the computing device 1600.

[0070] Elements of embodiments are also provided as a machine-readable medium (e.g., memory 1660) for storing the computer-executable instructions (e.g., instructions to implement any other processes discussed herein). The machine-readable medium (e.g., memory 1660) may include, but is not limited to, flash memory, optical disks, CD-ROMs, DVD ROMs, RAMs, EPROMs, EEPROMs, magnetic or optical cards, phase change memory (PCM), or other types of machine-readable media suitable for storing electronic or computer-executable instructions. For example, embodiments of the disclosure may be downloaded as a computer program (e.g., BIOS) which may be transferred from a remote computer (e.g., a

server) to a requesting computer (e.g., a client) by way of data signals via a communication link (e.g., a modem or network connection).

[0071] In some embodiments, computing device 1600 comprises connectivity 1670. Connectivity 1670 includes hardware devices (e.g., wireless and/or wired connectors and communication hardware) and software components (e.g., drivers, protocol stacks) to enable the computing device 1600 to communicate with external devices. The computing device 1600 could be separate devices, such as other computing devices, wireless access points or base stations, as well as peripherals such as headsets, printers, or other devices.

[0072] Connectivity 1670 can include multiple different types of connectivity. To generalize, the computing device 1600 is illustrated with cellular connectivity 1672 and wireless connectivity 1674. Cellular connectivity 1672 refers generally to cellular network connectivity provided by wireless carriers, such as provided via GSM (global system for mobile communications) or variations or derivatives, CDMA (code division multiple access) or variations or derivatives, TDM (time division multiplexing) or variations or derivatives, or other cellular service standards. Wireless connectivity (or wireless interface) 1674 refers to wireless connectivity that is not cellular, and can include personal area networks (such as Bluetooth, Near Field, etc.), local area networks (such as Wi-Fi), and/or wide area networks (such as WiMax), or other wireless communication. In some embodiments, Connectivity 1670 includes parallel sensing arrays as described with reference to **Figs. 10-13**.

[0073] In some embodiments, computing device 1600 comprises peripheral connections 1680. Peripheral connections 1680 include hardware interfaces and connectors, as well as software components (e.g., drivers, protocol stacks) to make peripheral connections. It will be understood that the computing device 1600 could both be a peripheral device ("to" 1682) to other computing devices, as well as have peripheral devices ("from" 1684) connected to it. The computing device 1600 commonly has a "docking" connector to connect to other computing devices for purposes such as managing (e.g., downloading and/or uploading, changing, synchronizing) content on computing device 1600. Additionally, a docking connector can allow computing device 1600 to connect to certain peripherals that allow the computing device 1600 to control content output, for example, to audiovisual or other systems.

[0074] In addition to a proprietary docking connector or other proprietary connection hardware, the computing device 1600 can make peripheral connections 1680 via common or standards-based connectors. Common types can include a Universal Serial Bus (USB) connector (which can include any of a number of different hardware interfaces), DisplayPort

including MiniDisplayPort (MDP), High Definition Multimedia Interface (HDMI), Firewire, or other types.

[0075] Reference in the specification to "an embodiment," "one embodiment," "some embodiments," or "other embodiments" means that a particular feature, structure, or characteristic described in connection with the embodiments is included in at least some embodiments, but not necessarily all embodiments. The various appearances of "an embodiment," "one embodiment," or "some embodiments" are not necessarily all referring to the same embodiments. If the specification states a component, feature, structure, or characteristic "may," "might," or "could" be included, that particular component, feature, structure, or characteristic is not required to be included. If the specification or claim refers to "a" or "an" element, that does not mean there is only one of the elements. If the specification or claims refer to "an additional" element, that does not preclude there being more than one of the additional element.

[0076] Furthermore, the particular features, structures, functions, or characteristics may be combined in any suitable manner in one or more embodiments. For example, a first embodiment may be combined with a second embodiment anywhere the particular features, structures, functions, or characteristics associated with the two embodiments are not mutually exclusive.

[0077] While the disclosure has been described in conjunction with specific embodiments thereof, many alternatives, modifications and variations of such embodiments will be apparent to those of ordinary skill in the art in light of the foregoing description. The embodiments of the disclosure are intended to embrace all such alternatives, modifications, and variations as to fall within the broad scope of the appended claims.

[0078] In addition, well known power/ground connections to integrated circuit (IC) chips and other components may or may not be shown within the presented figures, for simplicity of illustration and discussion, and so as not to obscure the disclosure. Further, arrangements may be shown in block diagram form in order to avoid obscuring the disclosure, and also in view of the fact that specifics with respect to implementation of such block diagram arrangements are highly dependent upon the platform within which the present disclosure is to be implemented (i.e., such specifics should be well within purview of one skilled in the art). Where specific details (e.g., circuits) are set forth in order to describe example embodiments of the disclosure, it should be apparent to one skilled in the art that the disclosure can be practiced without, or with variation of, these specific details. The description is thus to be regarded as illustrative instead of limiting.

[0079] The following examples pertain to further embodiments. Specifics in the examples may be used anywhere in one or more embodiments. All optional features of the apparatus described herein may also be implemented with respect to a method or process.

[0080] For example, an apparatus is provided which comprises: a first ferromagnet (FM) layer having a first end and a second end; a spin-orbit-coupling (SOC) layer adjacent to the first FM layer near the first end; and an inverse SOC (ISOC) layer adjacent to the first FM layer near the second end. In some embodiments, the SOC layer is formed of a material selected from a group consisting of: β-Ta, β-W, W, Pt, Cu doped with Iridium, Cu doped with Bismuth, Cu doped with an element of 3d, 4d, 5d, 4f, or 5f of periodic table groups, α-Sn, Bi_2O_3, MoS_2, Bi and Ag multilayers, and 2D dichalocgenides of the form MX_2, where 'X' is one of S, Se, or Te, and where 'M' are transition elements.

[0081] In some embodiments, the ISOC layer is formed of a material selected from a group consisting of: β-Ta, β-W, W, Pt, Cu doped with Iridium, Cu doped with Bismuth, Cu doped with an element of 3d, 4d, 5d, 4f, or 5f of periodic table groups, α-Sn, Bi_2O_3, MoS_2, Bi and Ag multilayers, and 2D dichalocgenides of the form MX_2, where 'X' is one of S, Se, or Te, and where 'M' are transition elements. In some embodiments, the apparatus comprises a spin injection layer adjacent to the ISOC layer, wherein the spin injection layer is formed of a material selected from a group consisting of: Copper (Cu), Silver (Ag), Gold (Au), and Aluminum (Al).

[0082] In some embodiments, the ISOC layer comprises a stack of: an interface layer which is coupled directly or indirectly to the FM layer; and a bulk layer coupled to the interface layer and a second conductor. In some embodiments, the interface layer is formed of a material selected from a group consisting of: Ag, Cu, Al, alloys of Ag, alloys of Cu, and alloys of Al. In some embodiments, the bulk layer is formed of a material selected from a group consisting of: Bi and Ag; Bi and Au; Bi and Cu; Pb and Ag; Pb and Au; β-Ta; β-W; Pt; Bi_2Te_3; elements from 5d series; elements from 4d series; alloys of elements from 5d series with 3d series; and alloys of elements from 4d series with 3d series, α-Sn, Bi_2O_3, MoS_2, Bi and Ag multilayers, and 2D dichalocgenides of the form MX_2, where 'X' is one of S, Se, or Te, and where 'M' are transition elements.

[0083] In some embodiments, the interface layer is operable to provide interface spin orbit effect via inverse Rashba-Edelstein (IREE) for spin to charge conversion. In some embodiments, the bulk layer is operable to provide bulk material spin orbit effect via inverse spin Hall effect (ISHE) for spin to charge conversion. In some embodiments, the apparatus comprises: a first layer of Ru adjacent to the layer of the first FM. In some embodiments, the

apparatus comprises a layer of Ta adjacent to the layer of Ru. In some embodiments, the apparatus comprises a second layer of Ta adjacent to the layer of Ru.

[0084] In some embodiments, the first FM layer comprises one or a combination of materials selected from a group consisting of a Heusler alloy, Co, Fe, Ni, Gd, B, Ge, Ga, permalloy, and Yttrium Iron Garnet (YIG). In some embodiments, the Heusler alloy is a material selected from a group consisting of: Cu_2MnAl, Cu_2MnIn, Cu_2MnSn, Ni_2MnAl, Ni_2MnIn, Ni_2MnSn, Ni_2MnSb, Ni_2MnGa Co_2MnAl, Co_2MnSi, Co_2MnGa, Co_2MnGe, Pd_2MnAl, Pd_2MnIn, Pd_2MnSn, Pd_2MnSb, Co_2FeSi, Co_2FeAl, Fe_2VAl, Mn_2VGa, Co_2FeGe, MnGa, MnGaRu, and Mn_3X, where 'X' is one of Ga and Ge. In some embodiments, the first FM magnet is formed of a stack of materials, wherein the materials for the stack are selected from a group consisting of: Co and Pt; Co and Pd; Co and Ni; MgO, CoFeB, Ta, CoFeB, and MgO; MgO, CoFeB, W, CoFeB, and MgO; MgO, CoFeB, V, CoFeB, and MgO; MgO, CoFeB, Mo, CoFeB, and MgO; Mn_xGa_y; Materials with L10 symmetry; and materials with tetragonal crystal structure.

[0085] In some embodiments, the first FM magnet is formed of a single layer of one or more materials. In some embodiments, the single layer is formed of $Mn_xRu_yGa_zGe_k$. In some embodiments, the first FM has a perpendicular magnetic anisotropy (PMA). In some embodiments, the apparatus comprises non-magnetic conductors adjacent to the SOC and ISOC layers. In some embodiments, the apparatus comprises a current source coupled to the non-magnetic conductors adjacent to the SOC layer. In some embodiments, the apparatus comprises a voltage detector coupled to the non-magnetic conductors adjacent to the ISOC layer. In some embodiments, the apparatus comprises: a second FM layer, a portion of which is adjacent to the first FM layer near the second end; and a third FM layer, a portion of which is adjacent to the first FM layer near the second end. In some embodiments, the second and third FMs have perpendicular magnetic anisotropy (PMA).

[0086] In another example, a system is provided which comprises: a memory; a processor coupled to the memory, the processor having a spin wave device, which comprises an apparatus according to the apparatus described above; and a wireless interface for allowing the processor to communicate with another device.

[0087] In another example, a method is provided which comprises: generating a first spin wave via a spin orbit coupling (SOC) layer, wherein the first spin wave is to propagate through a first ferromagnet (FM) adjacent to the SOC layer at one end of the first FM; and detecting a voltage across an inverse SOC (ISOC) layer, the ISOC layer being adjacent to the first FM at another end of the first FM, wherein the voltage is according to the generated first

spin wave. In some embodiments, generating the first spin wave comprises passing a charge current through the SOC layer, wherein the charge current causes the first spin wave to be generated in the first FM.

[0088] In some embodiments, detecting the voltage across the ISOC layer comprises applying a voltage detector across two ends along a length of the ISOC layer. In some embodiments, the method comprises: generating a second spin wave which propagates through a second FM, wherein the second FM is adjacent to the ISOC layer at one end of the second FM; and generating a third spin wave which propagates through a third FM, wherein the third FM is adjacent to the ISOC layer at one end of the third FM. In some embodiments, detecting the voltage across the ISOC layer comprises: applying a voltage detector across two ends along a length of the ISOC layer, and determining a logic value which is according to the voltage and the first, second, and third spin waves.

[0089] In another example, an apparatus is provided which comprises: means for generating a first spin wave via a spin orbit coupling (SOC) layer, wherein the first spin wave is to propagate through a first ferromagnet (FM) adjacent to the SOC layer at one end of the first FM; and means for detecting a voltage across an inverse SOC (ISOC) layer, the ISOC layer being adjacent to the first FM at another end of the first FM, wherein the voltage is according to the generated first spin wave. In some embodiments, the means for generating the first spin wave comprises means for passing a charge current through the SOC layer, wherein the charge current causes the first spin wave to be generated in the first FM.

[0090] In some embodiments, the apparatus comprises: means for detecting the voltage across the ISOC layer comprises means for applying a voltage detector across two ends along a length of the ISOC layer. In some embodiments, the apparatus comprises: means for generating a second spin wave which propagates through a second FM, wherein the second FM is adjacent to the ISOC layer at one end of the second FM; and means for generating a third spin wave which propagates through a third FM, wherein the third FM is adjacent to the ISOC layer at one end of the third FM. In some embodiments, the means for detecting the voltage across the ISOC layer comprises: means for applying a voltage detector across two ends along a length of the ISOC layer, and means for determining a logic value which is according to the voltage and the first, second, and third spin waves.

[0091] In another example, a system is provided which comprises: a memory; a processor coupled to the memory, the processor having a spin wave device, which comprises an apparatus according to the apparatus described above; and a wireless interface for allowing the processor to communicate with another device.

[0092] An abstract is provided that will allow the reader to ascertain the nature and gist of the technical disclosure. The abstract is submitted with the understanding that it will not be used to limit the scope or meaning of the claims. The following claims are hereby incorporated into the detailed description, with each claim standing on its own as a separate embodiment.

CLAIMS

We claim:

1. An apparatus comprising:
   a first ferromagnet (FM) layer having a first end and a second end;
   a spin-orbit-coupling (SOC) layer adjacent to the first FM layer near the first end; and
   an inverse SOC (ISOC) layer adjacent to the first FM layer near the second end.

2. The apparatus of claim 1, wherein the SOC layer is formed of a material selected from a group consisting of: β-Ta, β-W, W, Pt, Cu doped with Iridium, Cu doped with Bismuth, Cu doped with an element of 3d, 4d, 5d, 4f, or 5f of periodic table groups, α-Sn, Bi_2O_3, MoS_2, Bi and Ag multilayers, and 2D dichalocgenides of the form MX_2, where 'X' is one of S, Se, or Te, and where 'M' are transition elements.

3. The apparatus of claim 1, wherein the ISOC layer is formed of a material selected from a group consisting of: β-Ta, β-W, W, Pt, Cu doped with Iridium, Cu doped with Bismuth, Cu doped with an element of 3d, 4d, 5d, 4f, or 5f of periodic table groups, α-Sn, Bi_2O_3, MoS_2, Bi and Ag multilayers, and 2D dichalocgenides of the form MX_2, where 'X' is one of S, Se, or Te, and where 'M' are transition elements.

4. The apparatus of claim 1 comprises a spin injection layer adjacent to the ISOC layer, wherein the spin injection layer is formed of a material selected from a group consisting of: Copper (Cu), Silver (Ag), Gold (Au), and Aluminum (Al).

5. The apparatus of claim 1, wherein the ISOC layer comprises a stack of:
   an interface layer which is coupled directly or indirectly to the FM layer; and
   a bulk layer coupled to the interface layer and a second conductor.

6. The apparatus of claim 5, wherein the interface layer is formed of a material selected from a group consisting of: Ag, Cu, Al, alloys of Ag, alloys of Cu, and alloys of Al.

7. The apparatus of claim 5, wherein the bulk layer is formed of a material selected from a group consisting of: Bi and Ag; Bi and Au; Bi and Cu; Pb and Ag; Pb and Au; β-Ta; β-W; Pt; Bi_2Te_3; elements from 5d series; elements from 4d series; alloys of elements from 5d series with 3d series; and alloys of elements from 4d series with 3d series, α-Sn, Bi_2O_3,

MoS_2, Bi and Ag multilayers, and 2D dichalocgenides of the form MX_2, where 'X' is one of S, Se, or Te, and where 'M' are transition elements.

8. The apparatus of claim 5, wherein the interface layer is operable to provide interface spin orbit effect via inverse Rashba-Edelstein (IREE) for spin to charge conversion.

9. The apparatus of claim 5, wherein the bulk layer is operable to provide bulk material spin orbit effect via inverse spin Hall effect (ISHE) for spin to charge conversion.

10. The apparatus of claim 1 comprises a first layer of Ru adjacent to the layer of the first FM.

11. The apparatus of claim 10 comprises a layer of Ta adjacent to the layer of Ru.

12. The apparatus of claim 11 comprises a second layer of Ta adjacent to the layer of Ru.

13. The apparatus of claim 1, wherein the first FM layer comprises one or a combination of materials selected from a group consisting of a Heusler alloy, Co, Fe, Ni, Gd, B, Ge, Ga, permalloy, and Yttrium Iron Garnet (YIG).

14. The apparatus of claim 13, wherein the Heusler alloy is a material selected from a group consisting of: Cu_2MnAl, Cu_2MnIn, Cu_2MnSn, Ni_2MnAl, Ni_2MnIn, Ni_2MnSn, Ni_2MnSb, Ni_2MnGa Co_2MnAl, Co_2MnSi, Co_2MnGa, Co_2MnGe, Pd_2MnAl, Pd_2MnIn, Pd_2MnSn, Pd_2MnSb, Co_2FeSi, Co_2FeAl, Fe_2VAl, Mn_2VGa, Co_2FeGe, MnGa, MnGaRu, and Mn_3X, where 'X' is one of Ga and Ge.

15. The apparatus of claim 1, wherein the first FM magnet is formed of a stack of materials, wherein the materials for the stack are selected from a group consisting of: Co and Pt; Co and Pd; Co and Ni; MgO, CoFeB, Ta, CoFeB, and MgO; MgO, CoFeB, W, CoFeB, and MgO; MgO, CoFeB, V, CoFeB, and MgO; MgO, CoFeB, Mo, CoFeB, and MgO; Mn_xGa_y; Materials with L10 symmetry; and materials with tetragonal crystal structure.

16. The apparatus of claim 1, wherein the first FM magnet is formed of a single layer of one or more materials.

17. The apparatus of claim 16, wherein the single layer is formed of $Mn_xRu_yGa_zGe_k$.

18. The apparatus of claim 1, wherein the first FM has a perpendicular magnetic anisotropy (PMA).

19. The apparatus of claim 1 comprises non-magnetic conductors adjacent to the SOC and ISOC layers.

20. The apparatus of claim 19 comprises a current source coupled to the non-magnetic conductors adjacent to the SOC layer.

21. The apparatus of claim 1 comprises a voltage detector coupled to the non-magnetic conductors adjacent to the ISOC layer.

22. The apparatus of claim 1 comprises:

a second FM layer, a portion of which is adjacent to the first FM layer near the second end; and

a third FM layer, a portion of which is adjacent to the first FM layer near the second end, wherein the second and third FMs have perpendicular magnetic anisotropy (PMA).

23. A system comprising:

a memory;

a processor coupled to the memory, the processor having a spin wave device, which comprises an apparatus according to any one of apparatus claims 1 to 22; and

a wireless interface for allowing the processor to communicate with another device.

24. A method comprising:

generating a first spin wave via a spin orbit coupling (SOC) layer, wherein the first spin wave is to propagate through a first ferromagnet (FM) adjacent to the SOC layer at one end of the first FM; and

detecting a voltage across an inverse SOC (ISOC) layer, the ISOC layer being adjacent to the first FM at another end of the first FM, wherein the voltage is according to the generated first spin wave.

25. The method of claim 24, wherein generating the first spin wave comprises passing a charge current through the SOC layer, wherein the charge current causes the first spin wave to be generated in the first FM.

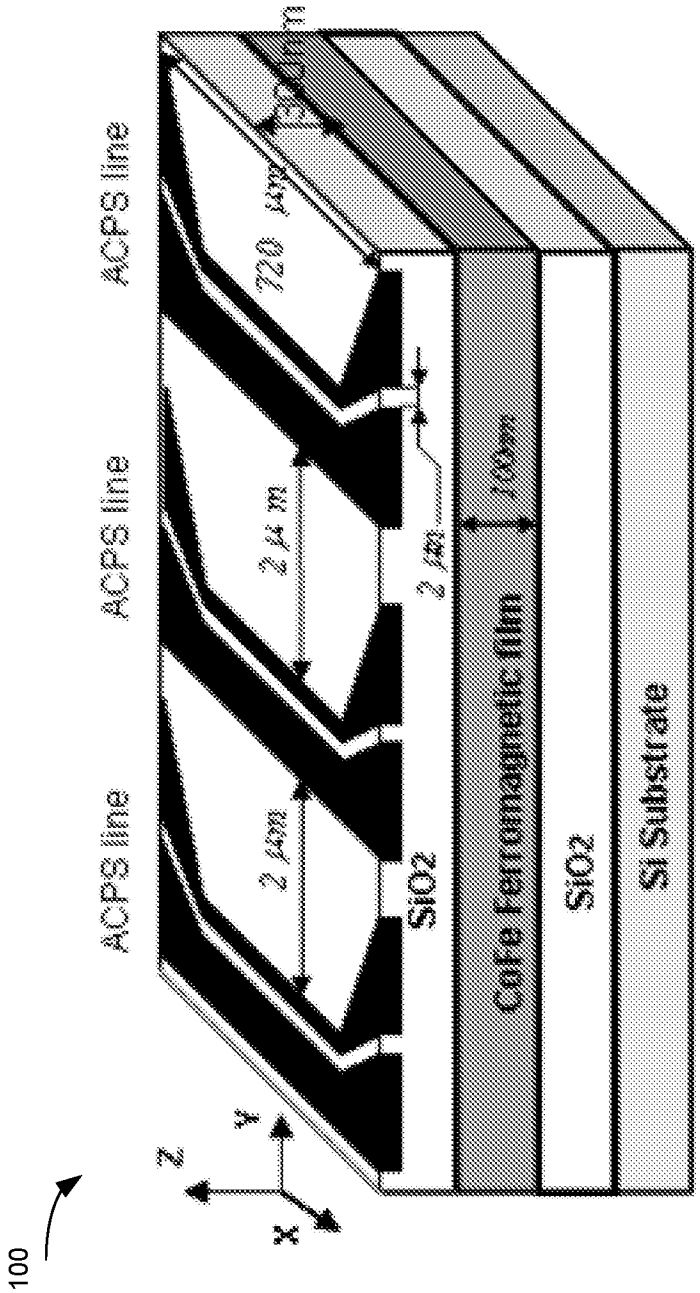

Fig. 1 (prior art)

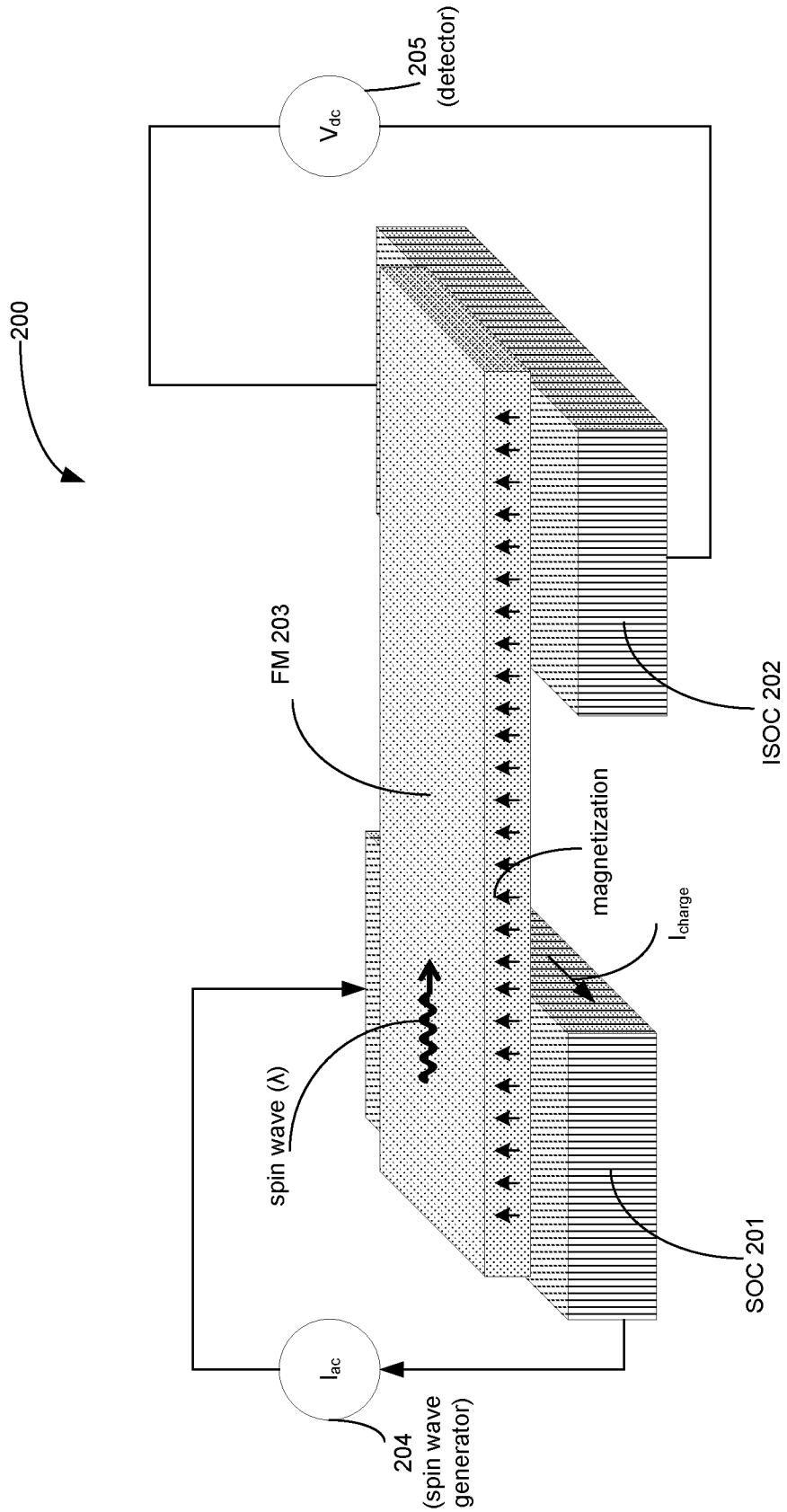
200
V_{dc}
205
(detector)
FM 203
ISOC 202
magnetization
I_{charge}
spin wave (λ)
SOC 201
I_{ac}
204
(spin wave
generator)

Fig. 2

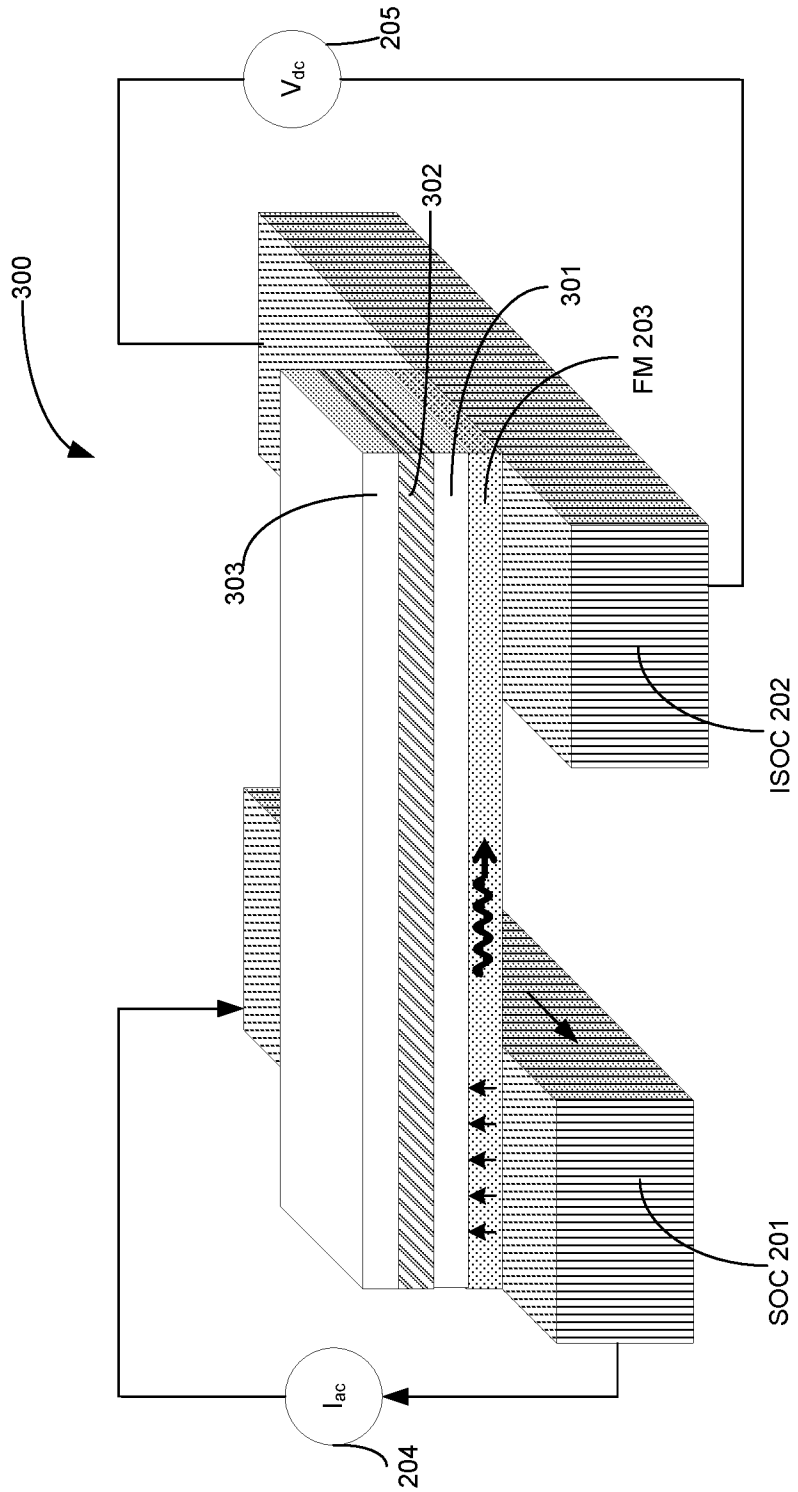

Fig. 3

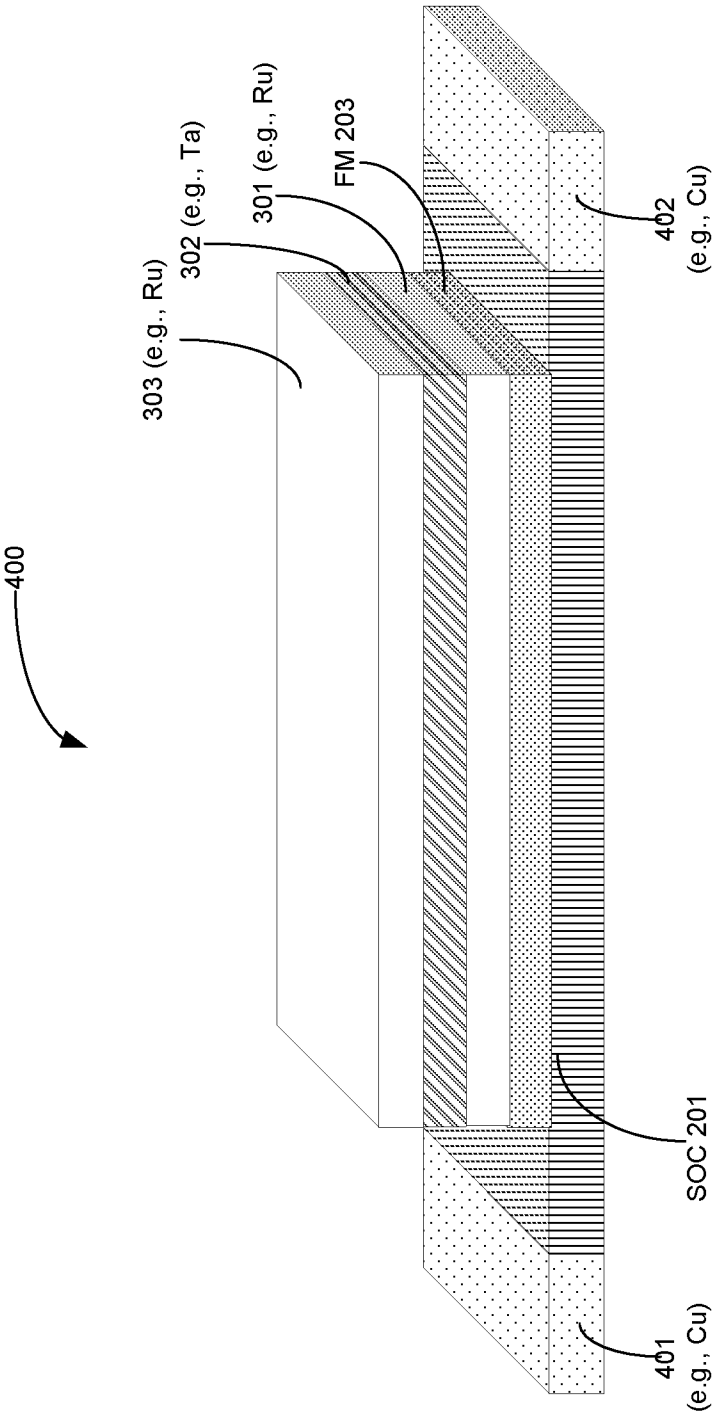

Fig. 4

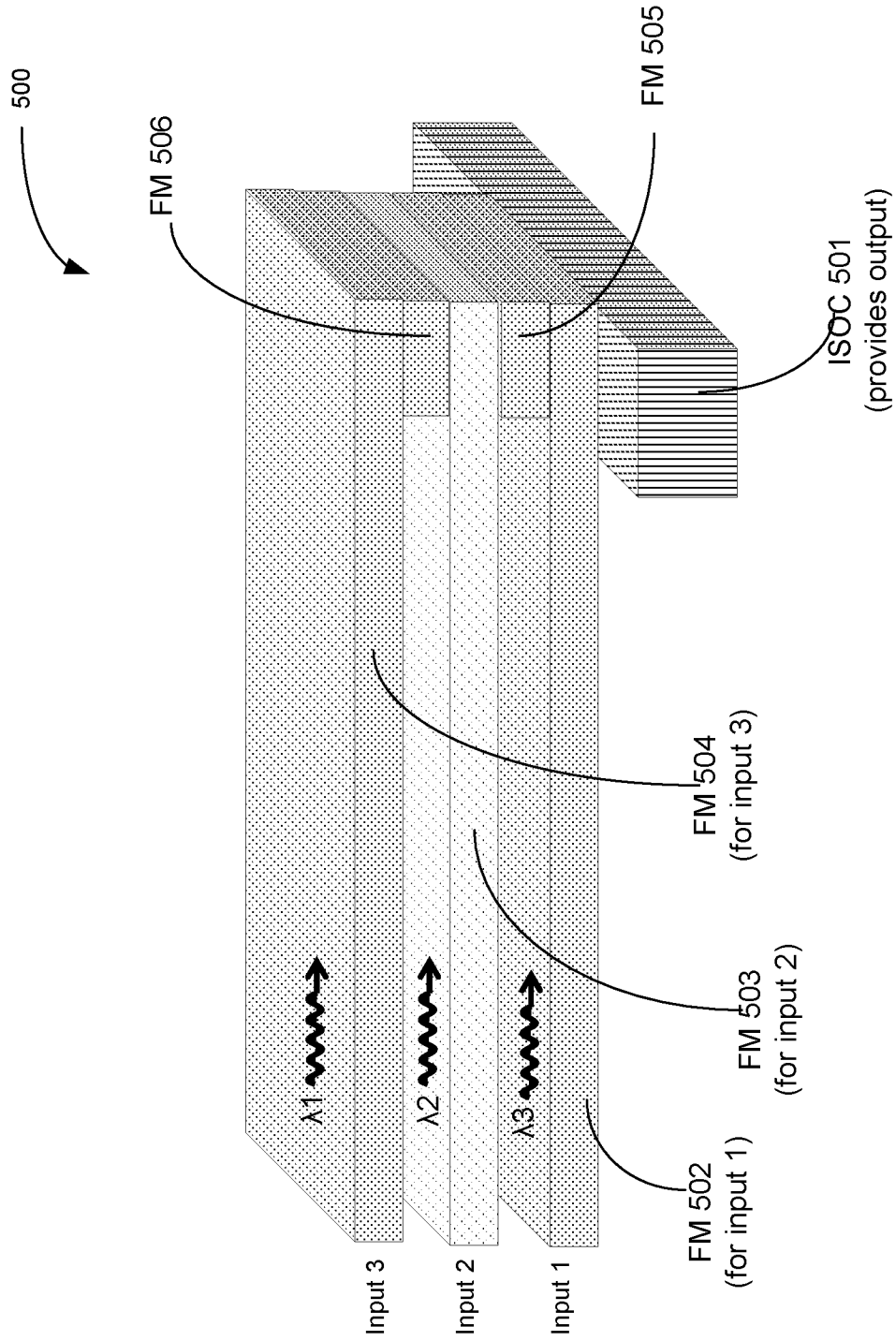
500
FM 506
FM 505
ISOC 501
(provides output)
FM 504
(for input 3)
FM 503
(for input 2)
FM 502
(for input 1)
λ1
λ2
λ3
Input 3
Input 2
Input 1

Fig. 5A

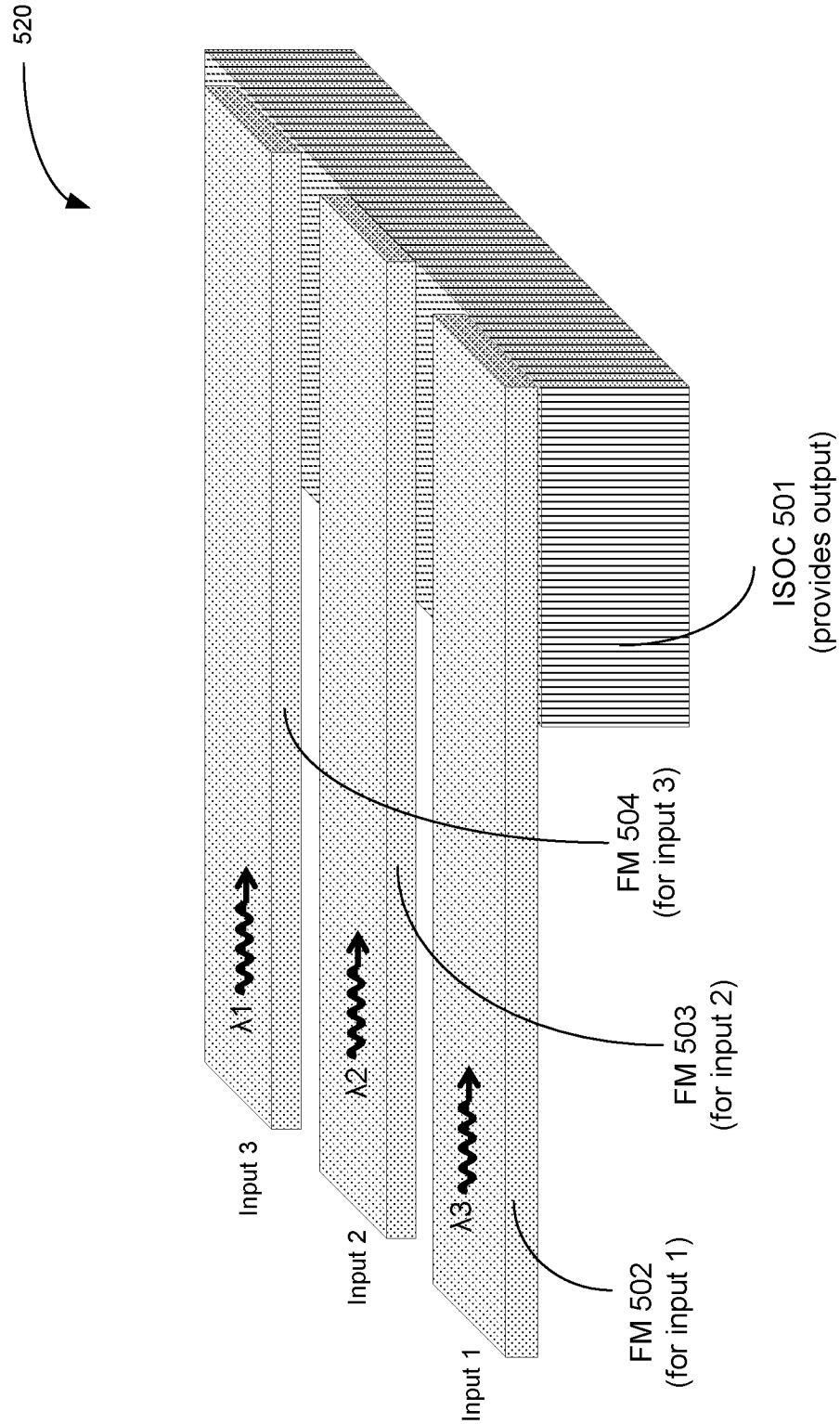
520
λ1
λ2
λ3
Input 3
Input 2
Input 1
FM 504
(for input 3)
FM 503
(for input 2)
FM 502
(for input 1)
ISOC 501
(provides output)

Fig. 5B

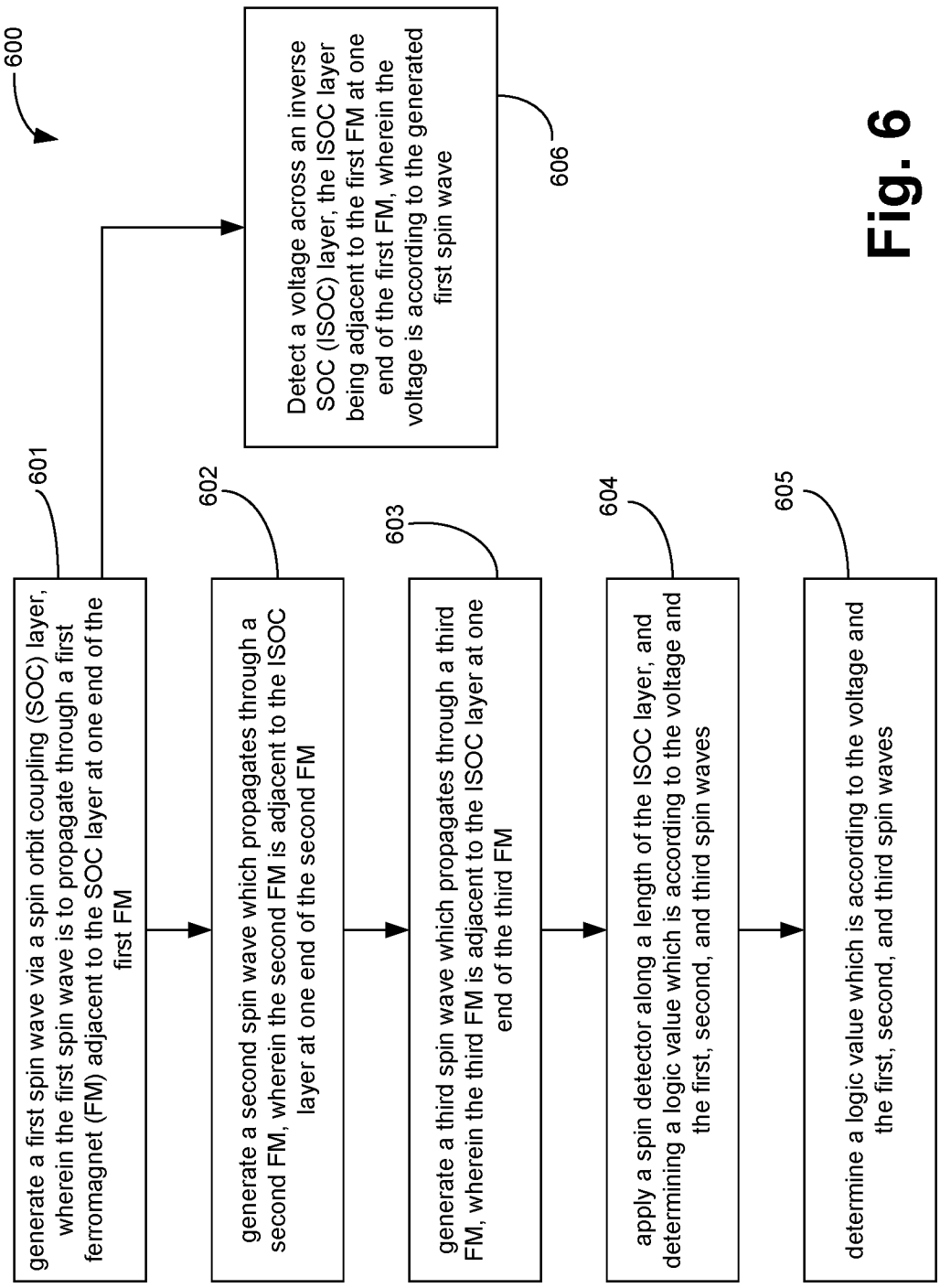
600
601
generate a first spin wave via a spin orbit coupling (SOC) layer, wherein the first spin wave is to propagate through a first ferromagnet (FM) adjacent to the SOC layer at one end of the first FM
602
generate a second spin wave which propagates through a second FM, wherein the second FM is adjacent to the ISOC layer at one end of the second FM
603
generate a third spin wave which propagates through a third FM, wherein the third FM is adjacent to the ISOC layer at one end of the third FM
604
apply a spin detector along a length of the ISOC layer, and determining a logic value which is according to the voltage and the first, second, and third spin waves
605
determine a logic value which is according to the voltage and the first, second, and third spin waves
606
Detect a voltage across an inverse SOC (ISOC) layer, the ISOC layer being adjacent to the first FM at one end of the first FM, wherein the voltage is according to the generated first spin wave

Fig. 6

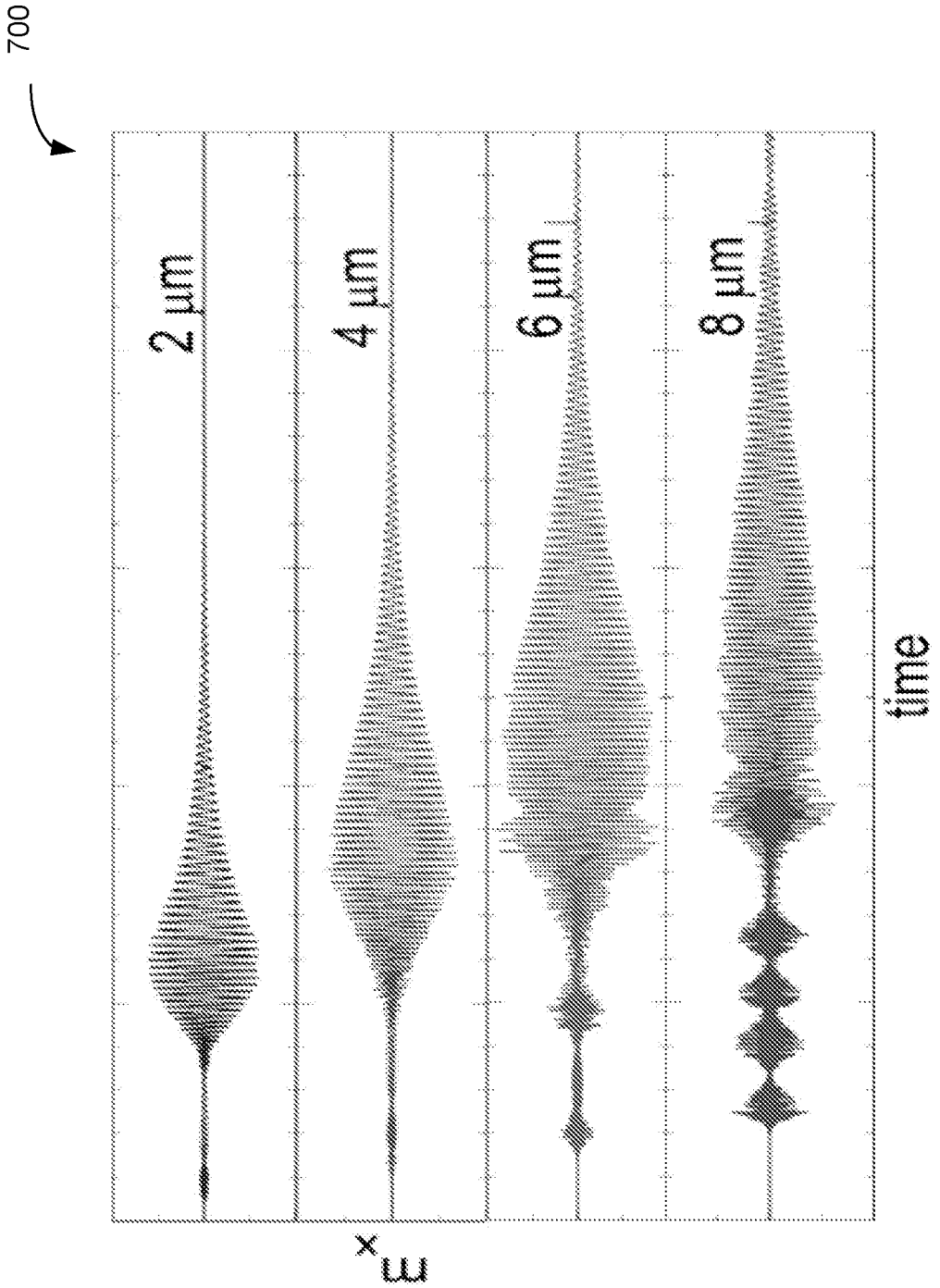

Fig. 7

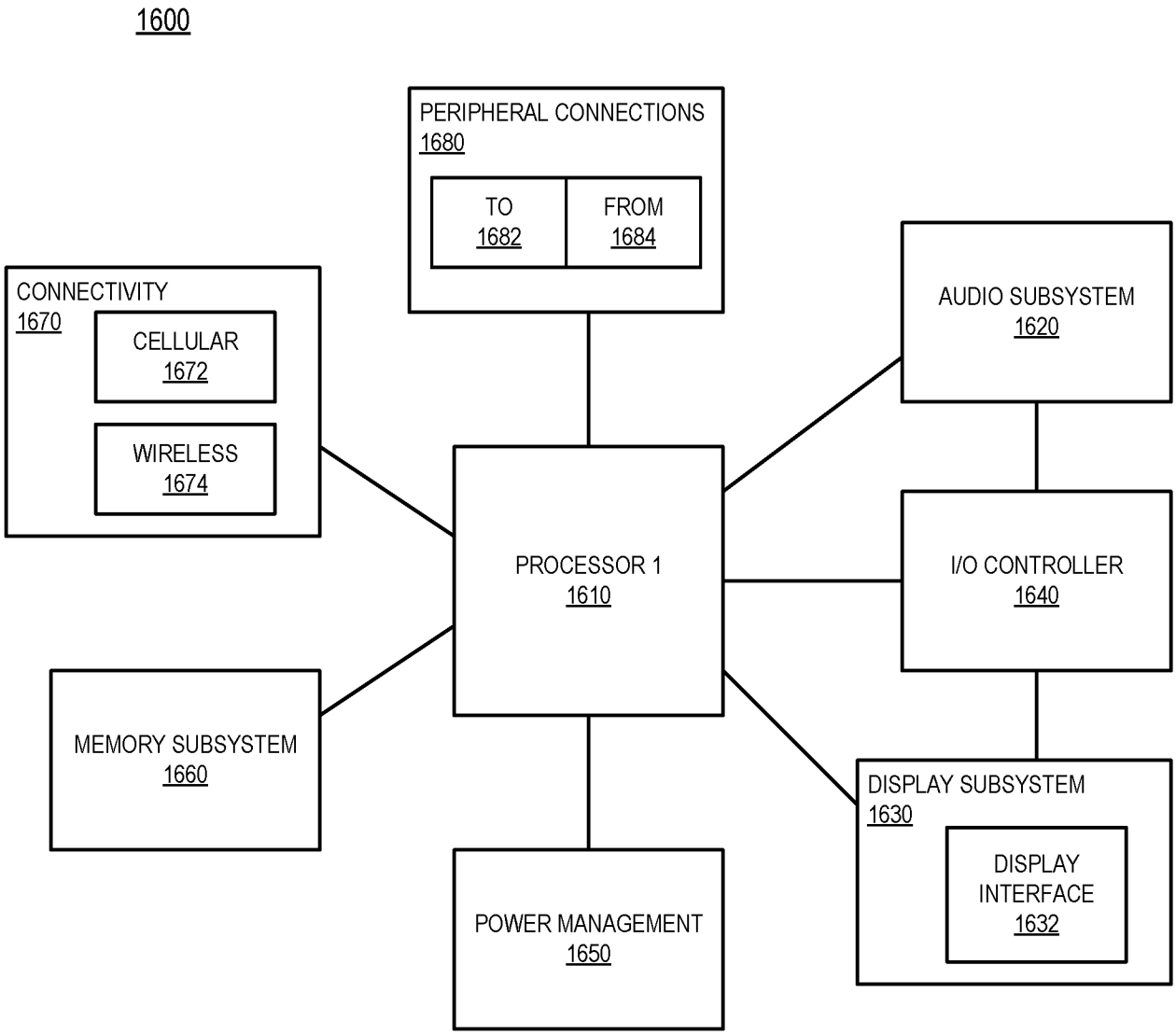
1600
PERIPHERAL CONNECTIONS
1680
TO
1682
FROM
1684
CONNECTIVITY
1670
CELLULAR
1672
WIRELESS
1674
AUDIO SUBSYSTEM
1620
PROCESSOR 1
1610
I/O CONTROLLER
1640
MEMORY SUBSYSTEM
1660
DISPLAY SUBSYSTEM
1630
DISPLAY
INTERFACE
1632
POWER MANAGEMENT
1650

Fig. 8

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2016/021262

A. CLASSIFICATION OF SUBJECT MATTER

H01L 43/02(2006.01)i, H01L 43/10(2006.01)i, H01L 43/12(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L 43/02; H01P 5/12; H01L 27/105; H01L 29/78; H01L 29/82; G01R 33/12; G01R 33/02; H01L 43/04; H01L 43/10; H01L 43/12

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
Korean utility models and applications for utility models
Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
eKOMPASS(KIPO internal) & Keywords:ferromagnet (FM), spin-orbit-coupling (SOC), spin wave, memory, detector

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2014-0231888 A1 (QUANTUM DEVICES, LLC. et al.) 21 August 2014 See paragraphs [0004]-[0012], [0023]-[0027], claim 1 and figures 1, 2.	1-3,23
Y		4,10-22,24,25
A		5-9
Y	US 2011-0234216 A1 (SHIHO NAKAMURA et al.) 29 September 2011 See paragraphs [0034]-[0045], [0086]-[0094], claim 8 and figures 3, 10.	4,10-18,21,22,24,25
Y	US 9128142 B1 (THE JOHNS HOPKINS UNIVERSITY) 08 September 2015 See column 1, lines 46-52, column 4, line 55 - column 5, line 11 and figure 4.	19,20
A	KR 10-0855105 B1 (KOREA INSTITUTE OF SCIENCE AND TECHNOLOGY) 29 August 2008 See paragraphs [0031]-[0036], claim 1 and figure 1.	1-25
A	US 2007-0296516 A1 (MARY M. ESHAGHIAN-WILNER et al.) 27 December 2007 See paragraphs [0048]-[0057], claim 1 and figures 1C-1F.	1-25

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"E" earlier application or patent but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents,such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
06 December 2016 (06.12.2016)	**06 December 2016 (06.12.2016)**

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INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.
PCT/US2016/021262

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		JP 2011-199190 A	06/10/2011
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US 9128142 B1	08/09/2015	None	
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		US 7535070 B2	19/05/2009
		US 8193598 B2	05/06/2012