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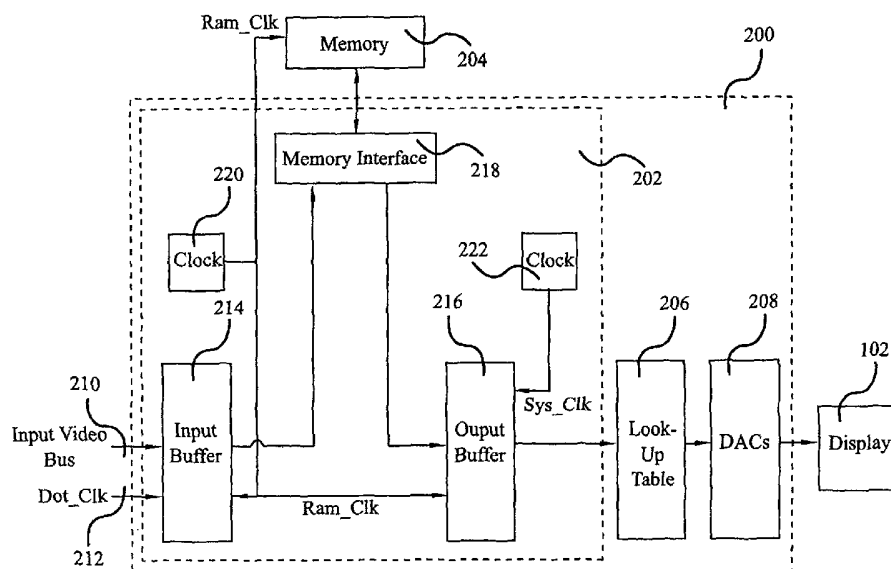
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(54) Title: FRAME MEMORY MANAGER AND METHOD OF MANAGING FRAME DATA FOR A DISPLAY SYSTEM



(57) Abstract: A memory management circuit manages frame data for a display system such as used in a projection television system or cellular phone. The frame data includes frames corresponding to a series of images for viewing by a user. The memory manager includes an input buffer to receive the frame data, a memory interface coupled to receive the frame data from the input buffer, and an output buffer coupled to receive the frame data from the memory interface and output the frame data to a display such as a liquid crystal (LCD) micro-display. The memory interface sends and receives the frame data as packets, with each packet having a size less than a full frame, to and from an external memory able to store at least one full frame of data.

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# INTERNATIONAL SEARCH REPORT

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**A. CLASSIFICATION OF SUBJECT MATTER**  
IPC 7 G09G3/20 G09G5/399 G09G5/393 G09G5/395

According to International Patent Classification (IPC) or to both national classification and IPC

**B. FIELDS SEARCHED**

Minimum documentation searched (classification system followed by classification symbols)  
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Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal, WPI Data, PAJ

**C. DOCUMENTS CONSIDERED TO BE RELEVANT**

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Further documents are listed in the continuation of box C.

Patent family members are listed in annex.

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