



(51) International Patent Classification:

H02M 1/40 (2007.01) H02M 3/337 (2006.01)  
H02M 3/335 (2006.01) H02M 1/08 (2006.01)  
H02M 1/36 (2007.01)

(21) International Application Number:

PCT/IB2016/053312

(22) International Filing Date:

6 June 2016 (06.06.2016)

(25) Filing Language:

English

(26) Publication Language:

English

(30) Priority Data:

62/314,126 28 March 2016 (28.03.2016) US

(71) Applicant: TELEFONAKTIEBOLAGET LM ERICSSON (PUBL) [SE/SE]; 164 83 Stockholm (SE).

(72) Inventors: KARLSSON, Magnus; Cedströms Väg 17, 572 50 Oskarshamn (SE). MALMBERG, Jonas; Sävsgatan 2, 386 33 Färjestaden (SE). WAHLEDOW, Fredrik; Morkullegatan 12, 386 30 Färjestaden (SE).

(74) Agents: SEKUL, Maria et al.; 6300 Legacy Drive, M/S EVR 1-C-11, Plano, Texas 75024 (US).

(81) Designated States (unless otherwise indicated, for every kind of national protection available):

AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IR, IS, JP, KE, KG, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SA, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

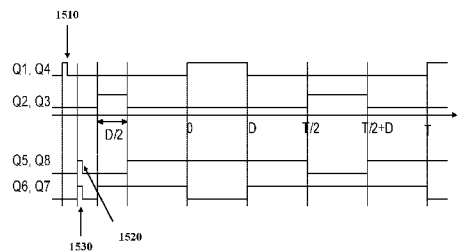
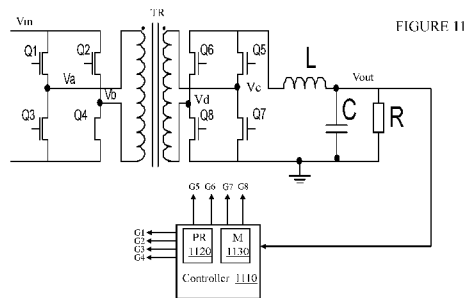
(84) Designated States (unless otherwise indicated, for every kind of regional protection available):

ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, ST, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, KM, ML, MR, NE, SN, TD, TG).

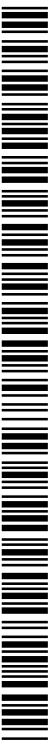
Published:

— with international search report (Art. 21(3))

(54) Title: CONTROLLER FOR USE WITH A POWER CONVERTER, AND METHOD OF OPERATING THE SAME



(57) Abstract: A controller for use with a power converter, and method of operating the same. In one embodiment, the power converter includes a power train having a first high-side switching device coupled in series at a first circuit node with a first low-side switching device. The controller of the power converter is coupled to a first bias voltage boot-strap capacitor having a first terminal couplable to a first bias voltage source and a second terminal coupled to the first circuit node. The controller includes a processor and a memory including computer program code that are collectively operable to apply a short control pulse to and momentarily turn on the first low-side switching device to charge up the first bias voltage boot-strap capacitor via the first bias voltage source at a start-up of the power converter.



## CONTROLLER FOR USE WITH A POWER CONVERTER, AND METHOD OF OPERATING THE SAME

This application claims the benefit of U.S. Provisional Application No. 62/314,126 entitled “Improved Prebias Start for Isolated SMPS with Secondary Full-Bridge,” filed March 28, 2016, which is incorporated herein by reference.

### TECHNICAL FIELD

The present invention is directed, in general, to the field of power electronics and, more specifically, to a controller for use with a power converter, and method of operating the same.

### BACKGROUND

A switched-mode power converter is a type of power converter having a diverse range of applications by virtue of its small size, weight and high efficiency. For example, switched-mode power converters are widely used in personal computers and portable electronic devices such as cellphones. A switching device (*e.g.*, a metal-oxide semiconductor field-effect transistor (“MOSFET”)) of a power train of the switched-mode power converter is controlled to convert an input voltage to a desired output voltage. The switched-mode power converters have for many years been designed for higher power conversion efficiency in a load range of 50 to 100 percent. This has led to the adoption of more efficient rectification techniques for the switched-mode power converters such as synchronous rectification, which yield high efficiency at high current levels.

An orderly start-up process of the switched-mode power converter is often employed to balance a magnetic flux of a transformer thereof around zero. The start-up process may include an application of a first voltage pulse of half a duty cycle to the power train. This is often referred to as half-pulse transformer balancing as described in U.S. Patent Application Publication No. 2011/0164438, entitled “Switch Mode Converter and a Method of Starting a Switched Mode Converter,” to Appelberg, published July 7, 2011, which is incorporated herein by reference. Unequal voltages resulting, for instance, from parasitic capacitances in the switching devices evident on a primary winding of the transformer within the switched-mode power converter may cause challenges to the operation of the half-pulse transformer balancing technique.

There have been other references directed to the start-up process for the switched-mode power converter. For instance, initialization of a control loop for a power converter is described in U.S. Patent Application Publication No. 2005/0212500, entitled "Control Circuit," to Bucheru, published September 29, 2005, which is incorporated herein by reference. Bucheru describes a process for reducing disturbances during a pre-bias start-up period. A start-up procedure for an isolated switched-mode power converter is described in U.S. Patent No. 8,456,867, entitled "Start-Up Procedure for an Isolated Switched Mode Power Supply," to Karlsson, *et al.*, issued June 4, 2013, which is incorporated herein by reference. Despite continued efforts to improve balancing of the magnetic flux in a transformer, a system and method is needed to overcome remaining magnetic flux unbalances, for instance, during start-up of a power converter.

#### SUMMARY

These and other problems are generally solved or circumvented, and technical advantages are generally achieved, by advantageous embodiments of the present invention for a controller for use with a power converter, and method of operating the same. In one embodiment, the power converter includes a power train having a first high-side switching device coupled in series at a first circuit node with a first low-side switching device. The controller of the power converter is coupled to a first bias voltage boot-strap capacitor having a first terminal couplable to a first bias voltage source and a second terminal coupled to the first circuit node. The controller includes a processor and a memory including computer program code that are collectively operable to apply a short control pulse to and momentarily turn on the first low-side switching device to charge up the first bias voltage boot-strap capacitor via the first bias voltage source at a start-up of the power converter.

The foregoing has outlined rather broadly the features and technical advantages of the present invention in order that the detailed description of the invention that follows may be better understood. Additional features and advantages of the invention will be described hereinafter, which form the subject of the claims of the invention. It should be appreciated by those skilled in the art that the conception and specific embodiment disclosed may be readily utilized as a basis for modifying or designing other structures or processes for carrying out the same purposes of the present invention. It should also be realized by those skilled in the art that such equivalent constructions do not depart from the spirit and scope of the invention as set forth in the appended claims.

## BRIEF DESCRIPTION OF THE DRAWINGS

For a more complete understanding of the present invention, reference is now made to the following descriptions taken in conjunction with the accompanying drawings, in which:

FIGURE 1 illustrates a schematic diagram of an embodiment of a power converter;

FIGUREs 2 and 3 illustrate timing diagrams demonstrating operations of the power converter of FIGURE 1;

FIGURE 4 illustrates a schematic diagram of an embodiment of a power converter;

FIGUREs 5 and 6 illustrate schematic diagrams of embodiments of portions of the power converter of FIGURE 4;

FIGUREs 7 to 10 illustrate timing diagrams demonstrating operations of the power converter of FIGUREs 4 to 6;

FIGURE 11 illustrates a schematic diagram of an embodiment of a power converter;

FIGUREs 12 and 13 illustrate schematic diagrams of embodiments of portions of the power converter of FIGURE 11;

FIGUREs 14 to 16 illustrate timing diagrams demonstrating operations of the power converter of FIGUREs 11 to 13; and

FIGURE 17 illustrates a flow diagram of an embodiment of a method of operating a power converter.

Corresponding numerals and symbols in the different figures generally refer to corresponding parts unless otherwise indicated, and may not be redescribed in the interest of brevity after the first instance. The FIGUREs are drawn to illustrate the relevant aspects of exemplary embodiments.

## DETAILED DESCRIPTION

The making and using of the present exemplary embodiments are discussed in detail below. It should be appreciated, however, that the embodiments provide many applicable inventive concepts that can be embodied in a wide variety of specific contexts. The specific embodiments discussed are merely illustrative of specific ways to make and use the systems, subsystems, and modules associated with controlling an operation during, for instance, a start-up of a power converter.

A process will be described herein with respect to exemplary embodiments in a specific context, namely, a system and method of controlling an operation of a power converter to reduce magnetic flux saturation in a transformer thereof. While the principles will be described in the environment of a power converter, any environment such as a motor controller that may benefit from such a system and method that enables these functionalities is well within the broad scope of the present disclosure.

Referring initially to FIGURE 1, illustrated is a schematic diagram of an embodiment of a power converter. A power train of the power converter receives an input voltage  $V_{in}$  and includes first and second high-side switching devices Q1, Q2, and first and second low-side switching devices Q3, Q4 arranged in a full bridge configuration and including parasitic capacitances (not shown). The first high-side switching device Q1 is coupled in series at a first circuit node Va with the first low-side switching device Q3. The second high-side switching device Q2 is coupled in series at a second circuit node Vb with the second low-side switching device Q4. The first and second circuit nodes Va, Vb are coupled to opposite ends of a primary winding of a transformer TR. A secondary winding of the transformer TR is coupled to a synchronous rectifier formed by a third high-side switching device Q5 (including a parasitic capacitance, not shown) and a third low-side switching device Q6 (including a parasitic capacitance, not shown). A center tap of the secondary winding of the transformer TR is coupled to an output filter including output inductor L and output capacitor C that filters an output voltage  $V_{out}$  provided to a load represented by a resistor R.

The first and second high-side switching devices Q1, Q2, and the first and second low-side switching devices Q3, Q4 are controlled to provide a high frequency alternating current (“ac”) voltage to the primary winding of the transformer TR. The high frequency ac voltage is impressed across to the secondary winding of the transformer TR and the third high-side switching device Q5 and the third low-side switching device Q6 are controlled to provide a rectified direct current (“dc”) voltage. The rectified dc voltage is

then filtered by the output filter, which provides the output voltage  $V_{out}$  to the load R. While the switching devices are illustrated as MOSFETs, it should be understood that any semiconductor switch technology can be used as the application dictates. Also, while the power train includes a full bridge configuration and synchronous rectifier, other topologies and rectification techniques may be employed to advantage.

As mentioned above, the half-pulse transformer balancing techniques are limited due to unequal voltages produced at the first and second circuit nodes Va, Vb. Unequal voltages are due to unbalances in a capacitive voltage divider formed by parasitic capacitances in the switching devices (see, *e.g.*, illustrated as parallel capacitances in FIGURE 4).

Turning now to FIGURE 2, illustrated are timing diagrams demonstrating an operation of the power converter of FIGURE 1. The timing diagrams represent the conduction intervals for the switching devices Q1, Q2, Q3, Q4, Q5, Q6 over a switching interval T as a function of time t (on the horizontal axis). The first high-side switching device Q1 and the second low-side switching device Q4 conduct for a duty cycle D delivering energy to the transformer TR. The third low-side switching device Q6 is also conducting during this time. During a freewheeling phase (from the duty cycle D to half the switching interval T/2), the first and second high-side switching devices Q1, Q2, and the first and second low-side switching devices Q3, Q4 are non-conducting, and a current in the output inductor L flows through the third high-side and low-side switching devices Q5, Q6 of the synchronous rectifier. During this period, a net magnetic flux in the transformer TR is zero (or about zero) as no energy is reflected back to the primary winding of the transformer TR.

For a period representing a duty cycle D (from half the switching interval T/2 to half the switching interval plus the duty cycle T/2+D), the second high-side switching device Q2 and the first low-side switching device Q3 conduct delivering energy to the transformer TR. The third high-side switching device Q5 is also conducting during this time. During another freewheeling phase (from half the switching interval plus the duty cycle T/2+D to the end of the switching interval T), the first and second high-side switching devices Q1, Q2, and the first and second low-side switching devices Q3, Q4 are non-conducting, and a current in the output inductor L flows through the third high-side and low-side switching devices Q5, Q6 of the synchronous rectifier. During this period, a net magnetic flux in the transformer TR is zero (or about zero) as no energy is reflected back to the primary winding of the transformer TR.

The application of full duty cycles to the transformer TR during a start-up of the power converter can produce saturation of the magnetic core thereof resulting in excessive currents. It is advantageous if both legs in the primary winding of the transformer TR transfer substantially the same amount of energy to keep the magnetic flux therein substantially balanced, thereby avoiding excessive currents in the power converter, particularly at start-up.

Turning now to FIGURE 3, illustrated are timing diagrams demonstrating an operation of the power converter of FIGURE 1. The timing diagrams represent the conduction intervals for the switching devices Q1, Q2, Q3, Q4, Q5, Q6 over a switching interval T as a function of time t (on the horizontal axis). During an initial period at start-up (representing half a duty cycle  $D/2$ ), the second high-side switching device Q2 and the first low-side switching device Q3 conduct delivering energy to the transformer TR. The third high-side switching devices Q5 is also conducting during this time. Then, the first and second high-side switching devices Q1, Q2, and the first and second low-side switching devices Q3, Q4 are non-conducting, and a current in the output inductor L flows through the third high-side and low-side switching devices Q5, Q6 of the synchronous rectifier. Thereafter, the timing diagrams of FIGURE 3 follow an analogous pattern as the timing diagrams of FIGURE 2. The application of half duty cycles for the second high-side switching device Q2 and the first low-side switching device Q3 at start-up of the power converter can avoid saturation of the magnetic core of the transformer TR and the large currents that can result from saturation of the magnetic core of transformer TR.

Turning now to FIGURE 4, illustrated is a schematic diagram of an embodiment of a power converter. A power train of the power converter receives an input voltage  $V_{in}$  and includes first and second high-side switching devices Q1, Q2, and first and second low-side switching devices Q3, Q4 arranged in a full bridge configuration and including parasitic capacitances (illustrated with dotted lines as parallel capacitances). The first high-side switching device Q1 is coupled in series at a first circuit node Va with the first low-side switching device Q3. The second high-side switching device Q2 is coupled in series at a second circuit node Vb with the second low-side switching device Q4. The first and second circuit nodes Va, Vb are coupled to opposite ends of a primary winding of a transformer TR. A secondary winding of the transformer TR is coupled to a synchronous rectifier formed by a third high-side switching device Q5 (including a parasitic capacitance, not shown) coupled to a third low-side switching device Q6

(including a parasitic capacitance, not shown). A center tap of the secondary winding of the transformer TR is coupled to an output filter including output inductor L and output capacitor C that filters an output voltage  $V_{out}$  provided to a load represented by a resistor R.

The first and second high-side switching devices Q1, Q2, and the first and second low-side switching devices Q3, Q4 are controlled to provide a high frequency ac voltage to the primary winding of the transformer TR. The high frequency ac voltage is impressed across to the secondary winding of the transformer TR and the third high-side switching device Q5 and the third low-side switching device Q6 are controlled to provide a rectified dc voltage. The rectified dc voltage is then filtered by the output filter, which provides the output voltage  $V_{out}$  to the load R. While the switching devices are illustrated as MOSFETs, it should be understood that any semiconductor switch technology can be used as the application dictates. Also, while the power train includes a full bridge configuration and synchronous rectifier, other topologies and rectification techniques may be employed to advantage.

A controller 410 including a processor (“PR”) 420 and memory (“M”) 430 controls and generates control signals for the first and second high-side switching devices Q1, Q2, and first and second low-side switching devices Q3, Q4 to regulate the output voltage  $V_{out}$  (an output characteristic of the power converter). The controller 410 also generates control signals for the synchronous rectifier formed by the third high-side switching device Q5 and the third low-side switching device Q6.

The processor 420 may be embodied as any type of processor and associated circuitry configured to perform one or more of the functions described herein. For example, the processor 420 may be embodied as or otherwise include a single or multi-core processor, an application specific integrated circuit, a collection of logic devices, or other circuits. The memory 430 may be embodied as read-only memory devices and/or random access memory devices. For example, the memory 430 may be embodied as or otherwise include dynamic random access memory devices (“DRAM”), synchronous dynamic random access memory devices (“SDRAM”), double-data rate dynamic random access memory devices (“DDR SDRAM”), and/or other volatile or non-volatile memory devices. The memory 430 may have stored therein programs including a plurality of instructions or computer program code for execution by the processor 420 to control particular functions of the power converter as discussed in more detail below.

The voltages at the first and second circuit nodes  $V_a$ ,  $V_b$  are about half the input voltage  $V_{in}$  during portions of the operation of the power train. At times, however, the voltages at the first and second circuit nodes  $V_a$ ,  $V_b$  may compromise half-pulse transformer magnetic flux balancing, since the resulting magnetic flux induced in the transformer TR at start-up does not correspond to half of the peak-to-peak magnetic flux.

Turning now to FIGURE 5, illustrated is a schematic diagram of an embodiment of portions of the power converter of FIGURE 4. The first high-side switching device Q1 is coupled in series at the first circuit node  $V_a$  with the first low-side switching device Q3. The power converter includes a first driver 510 for the first high-side switching device Q1 and a second driver 520 for the first low-side switching device Q3. The first driver 510 receives a control signal G1 from the controller 410 and provides a gate drive signal to the first high-side switching device Q1. A level shifter ("LS") enables the first driver 510 to drive the first high-side switching device Q1 referenced to local circuit ground. The second driver 520 receives a control signal G3 from the controller 410 and provides a gate drive signal to the first low-side switching device Q3. A first bias voltage boot-strap capacitor  $C_{B1}$  has a first terminal couplable to a first bias voltage source  $V_D$  and a second terminal coupled to the first circuit node  $V_a$ . A first blocking diode  $D_{B1}$  is couplable between the first bias voltage source  $V_D$  and the first terminal of the first bias voltage boot-strap capacitor  $C_{B1}$ . The first bias voltage boot-strap capacitor  $C_{B1}$  retains a bias voltage for the first driver 510. The first bias voltage source  $V_D$  is often about 5 to 10 volts ("V") and may be derived from a voltage divider that can be formed with capacitors from the input voltage  $V_{in}$  (which can be substantially higher such as 50 volts). Hence, the first bias voltage source  $V_D$  is produced and increases after application of the input voltage  $V_{in}$ .

During start-up when the input voltage  $V_{in}$  voltage is initially applied, the first circuit node  $V_a$  is capacitively divided to produce a driver voltage from the first bias voltage source  $V_D$ . The capacitance of the first bias voltage boot-strap capacitor  $C_{B1}$  is usually ten times or more than the parasitic capacitances of the first high-side switching device Q1 and the first low-side switching device Q3. Hence, the first bias voltage boot-strap capacitor  $C_{B1}$  may not be fully charged when initially applying the input voltage  $V_{in}$  to the power converter. An effective way of charging the first bias voltage boot-strap capacitor  $C_{B1}$  is to initially turn on the first low-side switching device Q3. Before this is done, the first high-side switching device Q1 cannot be turned on due to absence of an initial voltage across the first bias voltage boot-strap capacitor  $C_{B1}$ . Hence, charging of

the first bias voltage boot-strap capacitor  $C_{B1}$  should be performed before commencing a half-pulse transformer magnetic flux balancing procedure.

Turning now to FIGURE 6, illustrated is a schematic diagram of an embodiment of portions of the power converter of FIGURE 4. The second high-side switching device Q2 is coupled in series at the second circuit node Vb with the second low-side switching device Q4. The power converter includes a third driver 610 for the second high-side switching device Q2 and a fourth driver 620 for the second low-side switching device Q4. The third driver 610 receives a control signal G2 from the controller 410 and provides a gate drive signal to the second high-side switching device Q2. A level shifter ("LS") enables the third driver 610 to drive the second high-side switching device Q2 referenced to local circuit ground. The fourth driver 620 receives a control signal G4 from the controller 410 and provides a gate drive signal to the second low-side switching device Q4. A second bias voltage boot-strap capacitor  $C_{B2}$  has a first terminal couplable to the first bias voltage source  $V_D$  and a second terminal coupled to the second circuit node Vb. A second blocking diode  $D_{B2}$  is couplable between the first bias voltage source  $V_D$  and the first terminal of the second bias voltage boot-strap capacitor  $C_{B2}$ . The second bias voltage boot-strap capacitor  $C_{B2}$  retains a bias voltage for the third driver 610. The first bias voltage source  $V_D$  is often about 5 to 10 volts ("V") and may be derived from a voltage divider that can be formed with capacitors from the input voltage  $V_{in}$  (which can be substantially higher such as 50 volts). Hence, the first bias voltage source  $V_D$  is produced and increases after application of the input voltage  $V_{in}$ .

During start-up when the input voltage  $V_{in}$  voltage is initially applied, the second circuit node Vb is capacitively divided to produce a driver voltage from the first bias voltage source  $V_D$ . The capacitance of the second bias voltage boot-strap capacitor  $C_{B2}$  is usually ten times or more than the parasitic capacitances of the second high-side switching device Q2 and the second low-side switching device Q4. Hence, the second bias voltage boot-strap capacitor  $C_{B2}$  may not be fully charged when initially applying the input voltage  $V_{in}$  to the power converter. An effective way of charging the second bias voltage boot-strap capacitor  $C_{B2}$  is to initially turn on the second low-side switching device Q4. Before this is done, the second high-side switching device Q2 cannot be turned on due to absence of an initial voltage across the second bias voltage boot-strap capacitor  $C_{B2}$ . Hence, charging of the second bias voltage boot-strap capacitor  $C_{B2}$  should be performed before commencing a half-pulse transformer magnetic flux balancing procedure.

As provided herein, an improved magnetic flux balancing timing sequence for the transformer is employed for start-up in a pre-bias situation. The first energy transfer and transformer balancing pulse (a short control pulse) is improved by discharging parasitic capacitances of the first and second low-side switching devices Q3, Q4 of the power train, and charging the first and second bias voltage boot-strap capacitors  $C_{B1}$ ,  $C_{B2}$  for the first and second high-side switching devices Q1, Q2, respectively. As set forth below, a similar bias voltage boot-strap capacitor and accompanying components can be applied to the synchronous rectifier.

The operation of the power converter can be divided into multiple sections. Initially, a short control pulse is applied to at least one of the low-side switching devices (*e.g.*, the first low-side switching device Q3) to discharge a parasitic capacitance thereof, and charge a bias voltage boot-strap capacitor (*e.g.*, the first bias voltage boot-strap capacitor  $C_{B1}$ ) for the corresponding high-side switching device (*e.g.*, the first high-side switching device Q1). Then, a half-pulse magnetic flux balancing for the transformer TR is initiated. Thereafter, the controller 410 controls the operation of the first and second high-side switching devices Q1, Q2 and the first and second low-side switching devices Q3, Q4 and synchronous rectifier to regulate the output voltage  $V_{out}$ . Of course, many variants and orders of the short control pulses are possible.

Turning now to FIGURE 7, illustrated are timing diagrams demonstrating an operation of the power converter of FIGURES 4 to 6. The timing diagrams represent the conduction intervals for the switching devices Q1, Q2, Q3, Q4 over a switching interval T as a function of time t (on the horizontal axis). During an initialization period at start up, short control pulses 710, 720 are applied to briefly turn on (and then turn off) and discharge the parasitic capacitances of the first and second low-side switching devices Q3, Q4, respectively, of the power train. The first and second bias voltage boot-strap capacitors  $C_{B1}$ ,  $C_{B2}$  are also charged for the first and second high-side switching devices Q1, Q2, respectively. It should be noted that a duration of the short control pulses 710, 720 may be varied depending on the application. For instance, there may be times when the short control pulses 710, 720 are limited to one percent or five percent of the switching interval T. Additionally, the duration of the short control pulses 710, 720 may be different for the first and second low-side switching devices Q3, Q4, respectively. Thus, the duration of the short control pulses 710, 720 is limited to substantially maintain a magnetic flux balance in the transformer TR while sufficient to charge the first and second bias voltage boot-strap capacitors  $C_{B1}$ ,  $C_{B2}$ , respectively.

Thereafter, the second high-side switching device Q2 and the first low-side switching device Q3 conduct delivering energy to and maintain a magnetic flux balance of the transformer TR for a period representing half a duty cycle  $D/2$ . Then, the first and second high-side switching devices Q1, Q2, and the first and second low-side switching devices Q3, Q4 are non-conducting, and a current in the output inductor L flows through the synchronous rectifier.

Entering a standard operating region, the first high-side switching device Q1 and the second low-side switching device Q4 conduct for a duty cycle D delivering energy to the transformer TR. During a freewheeling phase (from the duty cycle D to half the switching interval  $T/2$ ), the first and second high-side switching devices Q1, Q2, and the first and second low-side switching devices Q3, Q4 are non-conducting, and a current in the output inductor L flows through the synchronous rectifier. During this period, a net magnetic flux in the transformer TR is zero (or about zero) as no energy is reflected back to the primary winding of the transformer TR.

For a period representing a duty cycle D (from half the switching interval  $T/2$  to half the switching interval plus the duty cycle  $T/2+D$ ), the second high-side switching device Q2 and the first low-side switching device Q3 conduct delivering energy to the transformer TR. During another freewheeling phase (from half the switching interval plus the duty cycle  $T/2+D$  to the end of the switching interval T), the first and second high-side switching devices Q1, Q2, and the first and second low-side switching devices Q3, Q4 are non-conducting, and a current in the output inductor L flows through the synchronous rectifier. During this period, a net magnetic flux in the transformer TR is zero (or about zero) as no energy is reflected back to the primary winding of the transformer TR.

As mentioned above, the application of full duty cycles to the transformer TR during a start-up of the power converter can produce saturation of the magnetic core thereof resulting in excessive currents. It is advantageous if both legs in the primary winding of the transformer TR transfer substantially the same amount of energy to keep the magnetic flux therein substantially balanced, thereby avoiding excessive currents in the power converter, particularly at start-up.

Turning now to FIGURE 8, illustrated are timing diagrams demonstrating an operation of the power converter of FIGURES 4 to 6. The timing diagrams represent the conduction intervals for the switching devices Q1, Q2, Q3, Q4 over a switching interval T as a function of time t (on the horizontal axis). During an initialization period at start

up, a short control pulse 810 is applied to briefly turn on (and then turn off) and discharge the parasitic capacitance of the second low-side switching device Q4 of the power train. The second bias voltage boot-strap capacitor  $C_{B2}$  is also charged for the second high-side switching device Q2. With this procedure, discharge of parasitic capacitance of the first low-side switching device Q3 is performed through the transformer TR, which may produce a small, possibly inconsequential, magnetic flux unbalance thereof. Again, the duration of the short control pulse 810 may be varied depending on the application. Thereafter, the timing diagrams of FIGURE 8 follow an analogous pattern as the timing diagrams of FIGURE 7.

Turning now to FIGURE 9, illustrated are timing diagrams demonstrating an operation of the power converter of FIGURES 4 to 6. The timing diagrams represent the conduction intervals for the switching devices Q1, Q2, Q3, Q4 over a switching interval T as a function of time t (on the horizontal axis). In the illustrated embodiment, the first high-side switching device Q1 and the second low-side switching device Q4 are controlled with the same control signal, and the second high-side switching device Q2 and the first low-side switching device Q3 are controlled with the same control signal, thereby reducing the number of control signals per the switching interval T.

During an initialization period at start up, a short control pulse 910 is applied to briefly turn on (and then turn off) and discharge the parasitic capacitance of the second low-side switching device Q4 of the power train. While the short control pulse 910 is also applied to the first high-side switching device Q1, it is sufficiently short in duration to avoid any damage to the power converter. It should be noted that the short-circuit current from the input voltage  $V_{in}$  (as a result of the simultaneous conduction of the switching devices Q1, Q4) that may cause the damage may also be limited by an input filter choke to the power converter. The second bias voltage boot-strap capacitor  $C_{B2}$  is also charged for the second high-side switching device Q2. With this procedure, discharge of parasitic capacitance of the first low-side switching device Q3 is performed through the transformer TR, which may produce a small, possibly inconsequential, magnetic flux unbalance thereof. Again, the duration of the short control pulse 910 may be varied depending on the application. Thereafter, the timing diagrams of FIGURE 9 follow an analogous pattern as the timing diagrams of FIGURE 7.

Turning now to FIGURE 10, illustrated are timing diagrams demonstrating an operation of the power converter of FIGURES 4 to 6. The timing diagrams represent the conduction intervals for the switching devices Q1, Q2, Q3, Q4 over a switching interval

T as a function of time t (on the horizontal axis). In the illustrated embodiment, the first high-side switching device Q1 and the second low-side switching device Q4 are controlled with the same control signal, and the second high-side switching device Q2 and the first low-side switching device Q3 are controlled with the same control signal, thereby reducing the number of control signals per the switching interval T.

During an initialization period at start up, short control pulses 1010, 1020 are applied to briefly turn on (and then turn off) and discharge the parasitic capacitances of the first and second low-side switching devices Q3, Q4, respectively, of the power train. While the short control pulses 1010, 1020 are also applied to the first and second high-side switching devices Q1, Q2, they are sufficiently short in duration to avoid any damage to the power converter. It should be noted that the short-circuit current from the input voltage  $V_{in}$  (as a result of the simultaneous conduction of the switching devices Q1, Q2, Q3, Q4) that may cause the damage may also be limited by an input filter choke to the power converter. The first and second bias voltage boot-strap capacitors  $C_{B1}$ ,  $C_{B2}$  are also charged for the first and second high-side switching devices Q1, Q2, respectively. Again, the application of the short control pulses 1010, 1020 reduce the magnetic flux unbalance in the transformer TR since the parasitic capacitances are discharged through the first and second low-side switching devices Q3, Q4 and not through the transformer TR. Again, the duration of the short control pulses 1010, 1020 may be varied depending on the application. Thereafter, the timing diagrams of FIGURE 10 follow an analogous pattern as the timing diagrams of FIGURE 7.

Turning now to FIGURE 11, illustrated is a schematic diagram of an embodiment of a power converter. A power train of the power converter receives an input voltage  $V_{in}$  and includes first and second high-side switching devices Q1, Q2, and first and second low-side switching devices Q3, Q4 arranged in a full bridge configuration and including parasitic capacitances (not shown). The first high-side switching device Q1 is coupled in series at a first circuit node Va with the first low-side switching device Q3. The second high-side switching device Q2 is coupled in series at a second circuit node Vb with the second low-side switching device Q4. The first and second circuit nodes Va, Vb are coupled to opposite ends of a primary winding of a transformer TR. A secondary winding of the transformer TR is coupled to a synchronous rectifier in a full bridge configuration formed by a third high-side switching device Q5 (including a parasitic capacitance, not shown) coupled to a third low-side switching device Q7 (including a parasitic capacitance, not shown) at a third circuit node Vc. The synchronous rectifier is

also formed by a fourth high-side switching device Q6 (including a parasitic capacitance, not shown) coupled to a fourth low-side switching device Q8 (including a parasitic capacitance, not shown) at a fourth circuit node Vd. The third and fourth circuit nodes Vc, Vd are coupled to the secondary winding of the transformer TR. The synchronous rectifier is coupled to an output filter including output inductor L and output capacitor C that filters an output voltage  $V_{out}$  provided to a load represented by a resistor R.

The first and second high-side switching devices Q1, Q2, and the first and second low-side switching devices Q3, Q4 are controlled to provide a high frequency ac voltage to the primary winding of the transformer TR. The high frequency ac voltage is impressed across to the secondary winding of the transformer TR and the third and fourth high-side switching devices Q5, Q6 and the third and fourth low-side switching devices Q7, Q8 are controlled to provide a rectified dc voltage. The rectified dc voltage is then filtered by the output filter, which provides the output voltage  $V_{out}$  to the load R. While the switching devices are illustrated as MOSFETs, it should be understood that any semiconductor switch technology can be used as the application dictates. Also, while the power train includes a full bridge configuration and synchronous rectifier, other topologies and rectification techniques may be employed to advantage.

A controller 1110 including a processor ("PR") 1120 and memory ("M") 1130 controls and generates control signals for the first and second high-side switching devices Q1, Q2, and first and second low-side switching devices Q3, Q4 to regulate the output voltage  $V_{out}$  (an output characteristic of the power converter). The controller 1110 also generates control signals for the synchronous rectifier formed by the third and fourth high-side switching devices Q5, Q6 and the third and fourth low-side switching devices Q7, Q8. A description of analogous controller 410 is described above with respect to FIGURE 4. The voltages at the first and second circuit nodes Va, Vb are about half the input voltage  $V_{in}$  during portions of the operation of the power train. At times, however, the voltages at the first and second circuit nodes Va, Vb may compromise half-pulse transformer magnetic flux balancing, since the resulting magnetic flux induced in the transformer TR at start-up does not correspond to half of the peak-to-peak magnetic flux.

Turning now to FIGURE 12, illustrated is a schematic diagram of an embodiment of portions of the power converter of FIGURE 11. The drivers and accompanying components for the first and second high-side switching devices Q1, Q2, and first and second low-side switching devices Q3, Q4 are analogous to the drivers as set forth above with respect to FIGURES 5 and 6 and, as such, will not be herein repeated. Regarding

the drivers for the synchronous rectifier, the third high-side switching device Q5 is coupled in series at the third circuit node Vc with the third low-side switching device Q7. The power converter includes a driver 1210 for the third high-side switching device Q5 and another driver 1220 for the third low-side switching device Q7. The driver 1210 receives a control signal G5 from the controller 1110 and provides a gate drive signal to the third high-side switching device Q5. A level shifter ("LS") enables the driver 1210 to drive the third high-side switching device Q5 referenced to local circuit ground. The another driver 1220 receives a control signal G7 from the controller 1110 and provides a gate drive signal to the third low-side switching device Q7. A bias voltage boot-strap capacitor  $C_{BS}$  has a first terminal couplable to a bias voltage source  $V_{DS}$  and a second terminal coupled to the third circuit node Vc. A blocking diode  $D_{BS}$  is couplable between the bias voltage source  $V_{DS}$  and the first terminal of the bias voltage boot-strap capacitor  $C_{BS}$ . The bias voltage boot-strap capacitor  $C_{BS}$  retains a bias voltage for the drivers 1210, 1220. The bias voltage source  $V_{DS}$  is often about 5 to 10 volts ("V") and may be derived from a voltage divider that can be formed with capacitors from the input voltage  $V_{in}$  (which can be substantially higher such as 50 volts). Hence, the bias voltage source  $V_{DS}$  is produced and increases after application of the input voltage  $V_{in}$ .

Turning now to FIGURE 13, illustrated is a schematic diagram of an embodiment of portions of the power converter of FIGURE 11. Regarding the drivers for the synchronous rectifier, the fourth high-side switching device Q6 is coupled in series at the fourth circuit node Vd with the fourth low-side switching device Q8. The power converter includes a driver 1310 for the fourth high-side switching device Q6 and another driver 1320 for the fourth low-side switching device Q8. The driver 1310 receives a control signal G6 from the controller 1110 and provides a gate drive signal to the fourth high-side switching device Q6. A level shifter ("LS") enables the driver 1310 to drive the fourth high-side switching device Q6 referenced to local circuit ground. The another driver 1320 receives a control signal G8 from the controller 1110 and provides a gate drive signal to the fourth low-side switching device Q8. A bias voltage boot-strap capacitor  $C_{BS}$  has a first terminal couplable to a bias voltage source  $V_{DS}$  and a second terminal coupled to the third circuit node Vd. A blocking diode  $D_{BS}$  is couplable between the bias voltage source  $V_{DS}$  and the first terminal of the bias voltage boot-strap capacitor  $C_{BS}$ . The bias voltage boot-strap capacitor  $C_{BS}$  retains a bias voltage for the drivers 1310, 1320. The bias voltage source  $V_{DS}$  is often about 5 to 10 volts ("V") and may be derived from a voltage divider that can be formed with capacitors from the input

voltage  $V_{in}$  (which can be substantially higher such as 50 volts). Hence, the bias voltage source  $V_{DS}$  is produced and increases after application of the input voltage  $V_{in}$ .

Turning now to FIGURE 14, illustrated are timing diagrams demonstrating an operation of the power converter of FIGURES 11 to 13. The timing diagrams represent the conduction intervals for the switching devices Q1, Q2, Q3, Q4, Q5, Q6, Q7, Q8 over a switching interval T as a function of time t (on the horizontal axis). In the illustrated embodiment, the first high-side switching device Q1 and the second low-side switching device Q4 are controlled with the same control signal, and the second high-side switching device Q2 and the first low-side switching device Q3 are controlled with the same control signal, thereby reducing the number of control signals per the switching interval T. Additionally, the third high-side switching device Q5 and the fourth low-side switching device Q8 are controlled with the same control signal, and the fourth high-side switching device Q6 and the third low-side switching device Q7 are controlled with the same control signal, thereby reducing the number of control signals for the synchronous rectifier per the switching interval T.

During an initialization period at start up, a short control pulse 1410 is applied to briefly turn on (and then turn off) and discharge the parasitic capacitance of the second low-side switching device Q4 of the power train. While the short control pulse 1410 is also applied to the first high-side switching device Q1, it is sufficiently short in duration to avoid any damage to the power converter. It should be noted that the short-circuit current from the input voltage  $V_{in}$  (as a result of the simultaneous conduction of the switching devices Q1, Q4) that may cause the damage may also be limited by an input filter choke to the power converter.. A second bias voltage boot-strap capacitor  $C_{B2}$  is also charged for the second high-side switching device Q2 (see, *e.g.*, FIGURE 6). With this procedure, discharge of parasitic capacitance of the first low-side switching device Q3 is performed through the transformer TR, which may produce a small, possibly inconsequential, magnetic flux unbalance thereof.

Additionally, a short control pulse 1420 is applied to briefly turn on (and then turn off) and discharge the parasitic capacitance of the fourth low-side switching device Q8 of the synchronous rectifier. The short control pulse 1420 is also applied to the third high-side switching device Q5. The short control pulse 1420 is sufficiently short in duration to prevent (via circuit inductance) a damaging current from flowing within the power converter. A bias voltage boot-strap capacitor  $C_{BS}$  is also charged for the fourth

high-side switching device Q6 (see, *e.g.*, FIGURE 13). Again, the duration of the short control pulses 1410, 1420 may be varied depending on the application.

Thereafter, the second high-side switching device Q2 and the first low-side switching device Q3 conduct delivering energy to and maintain a magnetic flux balance of the transformer TR for a period representing half a duty cycle  $D/2$ . The fourth high-side switching device Q6 and the third low-side switching device Q7 are also conducting during this time. Then, the first and second high-side switching devices Q1, Q2, and the first and second low-side switching devices Q3, Q4 are non-conducting, and a current in the output inductor L flows through the synchronous rectifier as the third and fourth high-side switching devices Q5, Q6 and the third and fourth low-side switching devices Q7, Q8 are conducting.

Entering a standard operating region, the first high-side switching device Q1 and the second low-side switching device Q4 conduct for a duty cycle D delivering energy to the transformer TR. The third high-side switching device Q5 and the fourth low-side switching device Q8 are also conducting during this time. During a freewheeling phase (from the duty cycle D to half the switching interval  $T/2$ ), the first and second high-side switching devices Q1, Q2, and the first and second low-side switching devices Q3, Q4 are non-conducting, and a current in the output inductor L flows through the synchronous rectifier (as the third and fourth high-side switching devices Q5, Q6 and the third and fourth low-side switching devices Q7, Q8 are conducting). During this period, a net magnetic flux in the transformer TR is zero (or about zero) as no energy is reflected back to the primary winding of the transformer TR.

For a period representing a duty cycle D (from half the switching interval  $T/2$  to half the switching interval plus the duty cycle  $T/2+D$ ), the second high-side switching device Q2 and the first low-side switching device Q3 conduct delivering energy to the transformer TR. The fourth high-side switching device Q6 and the third low-side switching device Q7 are also conducting during this time. During another freewheeling phase (from half the switching interval plus the duty cycle  $T/2+D$  to the end of the switching interval T), the first and second high-side switching devices Q1, Q2, and the first and second low-side switching devices Q3, Q4 are non-conducting, and a current in the output inductor L flows through the synchronous rectifier (as the third and fourth high-side switching devices Q5, Q6 and the third and fourth low-side switching devices Q7, Q8 are conducting). During this period, a net magnetic flux in the transformer TR is

zero (or about zero) as no energy is reflected back to the primary winding of the transformer TR.

As mentioned above, the application of full duty cycles to the transformer TR during a start-up of the power converter can produce saturation of the magnetic core thereof resulting in excessive currents. It is advantageous if both legs in the primary winding of the transformer TR transfer substantially the same amount of energy to keep the magnetic flux therein substantially balanced, thereby avoiding excessive currents in the power converter, particularly at start-up.

Turning now to FIGURE 15, illustrated are timing diagrams demonstrating an operation of the power converter of FIGURES 11 to 13. The timing diagrams represent the conduction intervals for the switching devices Q1, Q2, Q3, Q4, Q5, Q6, Q7, Q8 over a switching interval T as a function of time t (on the horizontal axis). In the illustrated embodiment, the first high-side switching device Q1 and the second low-side switching device Q4 are controlled with the same control signal, and the second high-side switching device Q2 and the first low-side switching device Q3 are controlled with the same control signal, thereby reducing the number of control signals per the switching interval T. Additionally, the third high-side switching device Q5 and the fourth low-side switching device Q8 are controlled with the same control signal, and the fourth high-side switching device Q6 and the third low-side switching device Q7 are controlled with the same control signal, thereby reducing the number of control signals for the synchronous rectifier per the switching interval T.

During an initialization period at start up, a short control pulse 1510 is applied to briefly turn on (and then turn off) and discharge the parasitic capacitance of the second low-side switching device Q4 of the power train. While the short control pulse 1510 is also applied to the first high-side switching device Q1, it is sufficiently short in duration to avoid any damage to the power converter. It should be noted that the short-circuit current from the input voltage  $V_{in}$  (as a result of the simultaneous conduction of the switching devices Q1, Q4) that may cause the damage may also be limited by an input filter choke to the power converter.. The second bias voltage boot-strap capacitor  $C_{B2}$  is also charged for the second high-side switching device Q2 (see, *e.g.*, FIGURE 6). With this procedure, discharge of parasitic capacitance of the first low-side switching device Q3 is performed through the transformer TR, which may produce a small, possibly inconsequential, magnetic flux unbalance thereof.

Additionally, a short control pulse 1520 is applied to briefly turn on (and then turn off) and discharge the parasitic capacitance of the fourth low-side switching device Q8 of the synchronous rectifier. The short control pulse 1520 is also applied to the third high-side switching device Q5. The short control pulse 1520 is sufficiently short in duration to prevent (via circuit inductance) a damaging current from flowing within the power converter. A bias voltage boot-strap capacitor  $C_{BS}$  is also charged for the fourth high-side switching device Q6 (see, *e.g.*, FIGURE 13).

A short control pulse 1530 is also applied to briefly turn on (and then turn off) and discharge the parasitic capacitance of the third low-side switching device Q7 of the synchronous rectifier. The short control pulse 1530 is also applied to the fourth high-side switching device Q6. The short control pulse 1530 is sufficiently short in duration to prevent (via circuit inductance) a damaging current from flowing within the power converter. A bias voltage boot-strap capacitor  $C_{BS}$  is also charged for the third high-side switching device Q5 (see, *e.g.*, FIGURE 12). Again, the duration of the short control pulses 1510, 1520, 1530 may be varied depending on the application. Thereafter, the timing diagrams of FIGURE 15 follow an analogous pattern as the timing diagrams of FIGURE 14.

Synchronous rectification was employed with operation of the power converter of FIGURES 14 and 15. As set forth below, alternative smooth synchronous rectifier ramp-in can be used to simplify pre-bias start-up. In such cases, the controller 1110 operates the power train at least in part in a discontinuous conduction mode (“DCM”).

Turning now to FIGURE 16, illustrated are timing diagrams demonstrating an operation of the power converter of FIGURES 11 to 13. The timing diagrams represent the conduction intervals for the switching devices Q1, Q2, Q3, Q4, Q5, Q6, Q7, Q8 over a switching interval T as a function of time t (on the horizontal axis). In the illustrated embodiment, the first high-side switching device Q1 and the second low-side switching device Q4 are controlled with the same control signal, and the second high-side switching device Q2 and the first low-side switching device Q3 are controlled with the same control signal, thereby reducing the number of control signals per the switching interval T. Additionally, the third high-side switching device Q5 and the fourth low-side switching device Q8 are controlled with the same control signal, and the fourth high-side switching device Q6 and the third low-side switching device Q7 are controlled with the same control signal, thereby reducing the number of control signals for the synchronous rectifier per the switching interval T.

During an initialization period at start up, a short control pulse 1610 is applied to briefly turn on (and then turn off) and discharge the parasitic capacitance of the second low-side switching device Q4 of the power train. While the short control pulse 1610 is also applied to the first high-side switching device Q1, it is sufficiently short in duration to avoid any damage to the power converter. It should be noted that the short-circuit current from the input voltage  $V_{in}$  (as a result of the simultaneous conduction of the switching devices Q1, Q4) that may cause the damage may also be limited by an input filter choke to the power converter. A second bias voltage boot-strap capacitor  $C_{B2}$  is also charged for the second high-side switching device Q2 (see, *e.g.*, FIGURE 6). With this procedure, discharge of parasitic capacitance of the first low-side switching device Q3 is performed through the transformer TR, which may produce a small, possibly inconsequential, magnetic flux unbalance thereof.

Additionally, a short control pulse 1620 is applied to briefly turn on (and then turn off) and discharge the parasitic capacitance of the fourth low-side switching device Q8 of the synchronous rectifier. The short control pulse 1620 is also applied to the third high-side switching device Q5. The short control pulse 1620 is sufficiently short in duration to prevent (via circuit inductance) a damaging current from flowing within the power converter. A bias voltage boot-strap capacitor  $C_{BS}$  is also charged for the fourth high-side switching device Q6 (see, *e.g.*, FIGURE 13). Again, the duration of the short control pulses 1610, 1620 may be varied depending on the application.

Thereafter, the second high-side switching device Q2 and the first low-side switching device Q3 conduct delivering energy to and maintain a magnetic flux balance of the transformer TR for a period representing half a duty cycle  $D/2$ . The fourth high-side switching device Q6 and the third low-side switching device Q7 are also conducting during this time. Then, the first and second high-side switching devices Q1, Q2, and the first and second low-side switching devices Q3, Q4 are non-conducting, and a current in the output inductor L flows through the synchronous rectifier through the body diodes of ones of the third and fourth high-side switching devices Q5, Q6 and the third and fourth low-side switching devices Q7, Q8.

Entering a standard operating region, the first high-side switching device Q1 and the second low-side switching device Q4 conduct for a duty cycle D delivering energy to the transformer TR. The third high-side switching device Q5 and the fourth low-side switching device Q8 are also conducting during this time. During a freewheeling phase (from the duty cycle D to half the switching interval  $T/2$ ), the first and second high-side

switching devices Q1, Q2, and the first and second low-side switching devices Q3, Q4 are non-conducting, and a current in the output inductor L flows through the synchronous rectifier (through the body diodes of ones of the third and fourth high-side switching devices Q5, Q6 and the third and fourth low-side switching devices Q7, Q8). During this period, a net magnetic flux in the transformer TR is zero (or about zero) as no energy is reflected back to the primary winding of the transformer TR.

For a period representing a duty cycle D (from half the switching interval  $T/2$  to half the switching interval plus the duty cycle  $T/2+D$ ), the second high-side switching device Q2 and the first low-side switching device Q3 conduct delivering energy to the transformer TR. The fourth high-side switching device Q6 and the third low-side switching device Q7 are also conducting during this time. During another freewheeling phase (from half the switching interval plus the duty cycle  $T/2+D$  to the end of the switching interval T), the first and second high-side switching devices Q1, Q2, and the first and second low-side switching devices Q3, Q4 are non-conducting, and a current in the output inductor L flows through the synchronous rectifier (through the body diodes of ones of the third and fourth high-side switching devices Q5, Q6 and the third and fourth low-side switching devices Q7, Q8). During this period, a net magnetic flux in the transformer TR is zero (or about zero) as no energy is reflected back to the primary winding of the transformer TR.

As mentioned above, the body diodes of ones of the third and fourth high-side switching devices Q5, Q6 and the third and fourth low-side switching devices Q7, Q8 are employed during the freewheeling phases of the operation of the power converter. This allows a smooth transition to synchronous rectification operation (see, *e.g.*, from time 0 to D). Dependent on the control loop bandwidth, the power converter may also transition DCM operation to continuous conduction mode (“CCM”) operation.

Turning now to FIGURE 17, illustrated is a flow diagram of an embodiment of a method of operating a power converter including a power train with a first high-side switching device coupled in series with a first low-side switching device at a first circuit node. The power converter also includes a first bias voltage boot-strap capacitor having a first terminal couplable to a first bias voltage source and a second terminal coupled to the first circuit node. The power train may also include a second high-side switching device coupled in series with a second low-side switching device at a second circuit node. The power converter may also include a second bias voltage boot-strap capacitor

having a first terminal couplable to the first bias voltage source and a second terminal coupled to the second circuit node.

The method begins at a start step or module 1700. At a step or module 1710, the method includes applying a short control pulse to and momentarily turn on the first low-side switching device to charge up the first bias voltage boot-strap capacitor via the first bias voltage source at a start-up of the power converter and/or the second low-side switching device to charge up the second bias voltage boot-strap capacitor via the first bias voltage source at the start-up of the power converter.

In a decisional step or module 1720, it is determined if the power converter includes a synchronous rectifier (“SR”) on a secondary side of a transformer. If the power converter includes the synchronous rectifier, the method continues to a step or module 1730. The synchronous rectifier includes a third high-side switching device coupled in series with a third low-side switching device at a third circuit node. The synchronous rectifier also includes a third bias voltage boot-strap capacitor having a first terminal couplable to a second bias voltage source and a second terminal coupled to the third circuit node. The synchronous rectifier may also include a fourth high-side switching device coupled in series with a fourth low-side switching device at a fourth circuit node. The synchronous rectifier may also include a fourth bias voltage boot-strap capacitor having a first terminal couplable to the second bias voltage source and a second terminal coupled to the fourth circuit node.

At the step or module 1730, the method includes applying a short control pulse to and momentarily turn on the third low-side switching device to charge up the third bias voltage boot-strap capacitor via the second bias voltage source at the start-up of the power converter and/or the fourth low-side switching device to charge up the fourth bias voltage boot-strap capacitor via the second bias voltage source at the start-up of the power converter. Then, the method includes causing at least one of the third high-side and low-side switching devices, and the fourth high-side and low-side switching devices to conduct for about half a duty cycle at a step or module 1740.

Thereafter, and if the power converter does not include a synchronous rectifier, the method includes causing at least one of the first high-side and low-side switching devices, and the second high-side and low-side switching devices to conduct for about half a duty cycle at a step or module 1750. At a step or module 1760, the method includes controlling the duty cycle of the second high-side and low-side switching devices in cooperation with controlling the first high-side and low-side switching devices

to regulate an output characteristic of the power converter thereafter. If the power converter includes a synchronous rectifier, the method also includes controlling the duty cycle of the third high-side and low-side switching devices and fourth high-side and low-side switching devices. To that end, the conduction period of ones of the third high-side and low-side switching devices, and fourth high-side and low-side switching devices may be extended beyond the duty cycle during periods of operation of the power converter. The method ends at an end step or module 1770.

Many modifications and variations can be made to the embodiments, without departing from the scope of the presently introduced solution. For example, generally, a circuit for a control process as introduced herein can be implemented using either analog or digital electronics, with no loss of performance. In a digital implementation of the circuit, the components of the circuit may be implemented as software components of that may form at least a part of a computer program, module, object or sequence of instructions executable by a programmable signal processing apparatus such as a processor, for example as shown in FIGURES 4 and 11.

As described herein, a controller (410, 1110) for use with a power converter, and method of operating the same has been introduced herein. In one embodiment, the power converter includes a power train including a first high-side switching device (Q1) coupled in series at a first circuit node (Va) with a first low-side switching device (Q3). The power converter also includes the controller (410, 1110), coupled to a first bias voltage boot-strap capacitor ( $C_{B1}$ ) having a first terminal couplable to a first bias voltage source ( $V_D$ ) and a second terminal coupled to the first circuit node (Va), configured to apply a short control pulse (710) to and momentarily turn on the first low-side switching device (Q3) to charge up the first bias voltage boot-strap capacitor ( $C_{B1}$ ) via the first bias voltage source ( $V_D$ ) at a start-up of the power converter. The duration (*e.g.*, less than five percent of a switching cycle (T) of the power train) of the short control pulse (710) is limited to substantially maintain a magnetic flux balance in a transformer (TR) while sufficient to charge the first bias voltage boot-strap capacitor ( $C_{B1}$ ). The power converter may also include a blocking diode ( $D_{B1}$ ) couplable between the first bias voltage source ( $V_D$ ) and coupled to the first terminal of the first bias voltage boot-strap capacitor ( $C_{B1}$ ).

The controller (410, 1110) is further configured to cause the first low-side switching device (Q3) to conduct for about half a duty cycle (D/2) following momentarily turning on the first low-side switching device (Q3), and control the duty cycle (D) of the first high-side switching device (Q1) and the first low-side switching

device (Q3) to regulate an output characteristic ( $V_{out}$ ) of the power converter thereafter. The controller (410, 1110) may also include a level shifter (LS) coupled to a first driver (510) configured to control a conductivity of the first high-side switching device (Q1), and a second driver (520) configured to control a conductivity of the first low-side switching device (Q3).

The power train may also include a second high-side switching device (Q2) coupled in series at a second circuit node (Vb) with a second low-side switching device (Q4). The controller (410, 1110), coupled to a second bias voltage boot-strap capacitor ( $C_{B2}$ ) having a first terminal couplable to the first bias voltage source ( $V_D$ ) and a second terminal coupled to the second circuit node (Vb), is further configured to apply a short control pulse (720) to and momentarily turn on the second low-side switching device (Q4) to charge up the second bias voltage boot-strap capacitor ( $C_{B2}$ ) via the first bias voltage source ( $V_D$ ) at the start-up of the power converter. The controller (410, 1110) is further configured to cause the second high-side switching device (Q2) to conduct for about half a duty cycle ( $D/2$ ) following momentarily turning on the second low-side switching device (Q4), and control the duty cycle (D) of the second high-side switching device (Q2) and the second low-side switching device (Q4) in cooperation with the first high-side switching device (Q1) and the first low-side switching device (Q3) to regulate an output characteristic ( $V_{out}$ ) of the power converter thereafter.

The power train may also include a transformer (TR) and a third high-side switching device (Q5) coupled in series at a third circuit node (Vc) with a third low-side switching device (Q7) on a secondary side of the power train. The controller (410, 1110), coupled to a third bias voltage boot-strap capacitor ( $C_{BS}$ ) having a first terminal couplable to a second bias voltage source ( $V_{DS}$ ) and a second terminal coupled to third circuit node (Vc), is further configured to apply a short control pulse (1530) to and momentarily turn on the third low-side switching device (Q7) to charge up the third bias voltage boot-strap capacitor ( $C_{BS}$ ) via the second bias voltage source ( $V_{DS}$ ) at the start-up of the power converter. The controller (410, 1110) is further configured to cause the third high-side switching device (Q5) to conduct for a period longer than a duty cycle (D) following momentarily turning on the third low-side switching device (Q7).

As described above, the exemplary embodiment provides both a method and corresponding apparatus consisting of various modules providing functionality for performing the steps of the method. The modules may be implemented as hardware (embodied in one or more chips including an integrated circuit such as an application

specific integrated circuit), or may be implemented as software or firmware for execution by a processor. In particular, in the case of firmware or software, the exemplary embodiment can be provided as a computer program product including a computer readable storage medium embodying computer program code (*i.e.*, software or firmware) thereon for execution by the computer processor. The computer readable storage medium may be non-transitory (*e.g.*, magnetic disks; optical disks; read only memory; flash memory devices; phase-change memory) or transitory (*e.g.*, electrical, optical, acoustical or other forms of propagated signals-such as carrier waves, infrared signals, digital signals, *etc.*). The coupling of a processor and other components is typically through one or more busses or bridges (also termed bus controllers). The storage device and signals carrying digital traffic respectively represent one or more non-transitory or transitory computer readable storage medium. Thus, the storage device of a given electronic device typically stores code and/or data for execution on the set of one or more processors of that electronic device such as a controller.

Although the embodiments and its advantages have been described in detail, it should be understood that various changes, substitutions, and alterations can be made herein without departing from the spirit and scope thereof as defined by the appended claims. For example, many of the features and functions discussed above can be implemented in software, hardware, or firmware, or a combination thereof. Also, many of the features, functions, and steps of operating the same may be reordered, omitted, added, *etc.*, and still fall within the broad scope of the various embodiments.

Moreover, the scope of the various embodiments is not intended to be limited to the particular embodiments of the process, machine, manufacture, composition of matter, means, methods and steps described in the specification. As one of ordinary skill in the art will readily appreciate from the disclosure, processes, machines, manufacture, compositions of matter, means, methods, or steps, presently existing or later to be developed, that perform substantially the same function or achieve substantially the same result as the corresponding embodiments described herein may be utilized as well. Accordingly, the appended claims are intended to include within their scope such processes, machines, manufacture, compositions of matter, means, methods, or steps.

## CLAIMS:

1. A controller (410, 1110) for use with a power converter including a power train having a first high-side switching device (Q1) coupled in series at a first circuit node (Va) with a first low-side switching device (Q3), said controller (410, 1110) coupled to a first bias voltage boot-strap capacitor ( $C_{B1}$ ) having a first terminal couplable to a first bias voltage source ( $V_D$ ) and a second terminal coupled to said first circuit node (Va), said controller (410, 1110), comprising:

a processor (420, 1120); and

a memory (430, 1130) including computer program code, wherein said processor (420, 1120), said memory (430, 1130), and said computer program code are collectively operable to apply a short control pulse (710) to and momentarily turn on said first low-side switching device (Q3) to charge up said first bias voltage boot-strap capacitor ( $C_{B1}$ ) via said first bias voltage source ( $V_D$ ) at a start-up of said power converter.

2. The controller (410, 1110) as recited in Claim 1 wherein said memory (430, 1130) and said computer program code are further configured to, with said processor (420, 1120) cause said controller (410, 1110) to:

cause said first low-side switching device (Q3) to conduct for about half a duty cycle ( $D/2$ ) following momentarily turning on said first low-side switching device (Q3); and

control said duty cycle (D) of said first high-side switching device (Q1) and said first low-side switching device (Q3) to regulate an output characteristic ( $V_{out}$ ) of said power converter thereafter.

3. The controller (410, 1110) as recited in Claim 1 wherein said power train comprises a second high-side switching device (Q2) coupled in series at a second circuit node (Vb) with a second low-side switching device (Q4), said controller (410, 1110) being coupled to a second bias voltage boot-strap capacitor ( $C_{B2}$ ) having a first terminal couplable to said first bias voltage source ( $V_D$ ) and a second terminal coupled to said second circuit node (Vb), said memory (430, 1130) and said computer program code being further configured to, with said processor (420, 1120) cause said controller (410, 1110) to apply a short control pulse (720) to and momentarily turn on said second low-side switching device (Q4) to charge up said second bias voltage boot-strap capacitor ( $C_{B2}$ ) via said first bias voltage source ( $V_D$ ) at said start-up of said power converter.

4. The controller (410, 1110) as recited in Claim 3 wherein said memory (430, 1130) and said computer program code are further configured to, with said processor (420, 1120) cause said controller (410, 1110) to:

cause said second high-side switching device (Q2) to conduct for about half a duty cycle ( $D/2$ ) following momentarily turning on said second low-side switching device (Q4); and

control said duty cycle ( $D$ ) of said second high-side switching device (Q2) and said second low-side switching device (Q4) in cooperation with said first high-side switching device (Q1) and said first low-side switching device (Q3) to regulate said output characteristic ( $V_{out}$ ) of said power converter thereafter.

5. The controller (410, 1110) as recited in Claim 1 wherein said power train comprises an transformer (TR) and a second high-side switching device (Q5) coupled in series at a second circuit node ( $V_c$ ) with a second low-side switching device (Q7) on a secondary side of said power train, said controller (410, 1110) being coupled to a second bias voltage boot-strap capacitor ( $C_{BS}$ ) having a first terminal couplable to a second bias voltage source ( $V_{DS}$ ) and a second terminal coupled to said second circuit node ( $V_c$ ), said memory (430, 1130) and said computer program code being further configured to, with said processor (420, 1120) cause said controller (410, 1110) to apply a short control pulse (1530) to and momentarily turn on said second low-side switching device (Q7) to charge up said second bias voltage boot-strap capacitor ( $C_{BS}$ ) via said second bias voltage source ( $V_{DS}$ ) at said start-up of said power converter.

6. The controller (410, 1110) as recited in Claim 5 wherein said memory (430, 1130) and said computer program code are further configured to, with said processor (420, 1120) cause said controller (410, 1110) to cause said second high-side switching device (Q5) to conduct for a period longer than a duty cycle ( $D$ ) following momentarily turning on said second low-side switching device (Q7).

7. A power converter, comprising:

a power train including a first high-side switching device (Q1) coupled in series at a first circuit node ( $V_a$ ) with a first low-side switching device (Q3); and

a controller (410, 1110), coupled to a first bias voltage boot-strap capacitor ( $C_{B1}$ ) having a first terminal couplable to a first bias voltage source ( $V_D$ ) and a second terminal coupled to said first circuit node ( $V_a$ ), configured to apply a short control pulse (710) to and momentarily turn on said first low-side switching device (Q3) to charge up said first

bias voltage boot-strap capacitor ( $C_{B1}$ ) via said first bias voltage source ( $V_D$ ) at a start-up of said power converter.

8. The power converter as recited in Claim 7 wherein said controller (410, 1110) is further configured to:

cause said first low-side switching device (Q3) to conduct for about half a duty cycle ( $D/2$ ) following momentarily turning on said first low-side switching device (Q3); and

control said duty cycle ( $D$ ) of said first high-side switching device (Q1) and said first low-side switching device (Q3) to regulate an output characteristic ( $V_{out}$ ) of said power converter thereafter.

9. The power converter as recited in Claim 7 wherein said power train comprises a second high-side switching device (Q2) coupled in series at a second circuit node ( $V_b$ ) with a second low-side switching device (Q4), said controller (410, 1110), coupled to a second bias voltage boot-strap capacitor ( $C_{B2}$ ) having a first terminal couplable to said first bias voltage source ( $V_D$ ) and a second terminal coupled to said second circuit node ( $V_b$ ), further configured to apply a short control pulse (720) to and momentarily turn on said second low-side switching device (Q4) to charge up said second bias voltage boot-strap capacitor ( $C_{B2}$ ) via said first bias voltage source ( $V_D$ ) at said start-up of said power converter.

10. The power converter as recited in Claim 9 wherein said controller (410, 1110) is further configured to:

cause said second high-side switching device (Q2) to conduct for about half a duty cycle ( $D/2$ ) following momentarily turning on said second low-side switching device (Q4); and

control said duty cycle ( $D$ ) of said second high-side switching device (Q2) and said second low-side switching device (Q4) in cooperation with said first high-side switching device (Q1) and said first low-side switching device (Q3) to regulate an output characteristic ( $V_{out}$ ) of said power converter thereafter.

11. The power converter as recited in Claim 7 wherein said power train comprises an transformer (TR) and a second high-side switching device (Q5) coupled in series at a second circuit node ( $V_c$ ) with a second low-side switching device (Q7) on a secondary side of said power train, said controller (410, 1110), coupled to a second bias voltage boot-strap capacitor ( $C_{BS}$ ) having a first terminal couplable to a second bias voltage source ( $V_{DS}$ ) and a second terminal coupled to said second circuit node ( $V_c$ ),

further configured to apply a short control pulse (1530) to and momentarily turn on said second low-side switching device (Q7) to charge up said second bias voltage boot-strap capacitor ( $C_{BS}$ ) via said second bias voltage source ( $V_{DS}$ ) at said start-up of said power converter.

12. The power converter as recited in Claim 11 wherein said controller (410, 1110) is further configured to cause said second high-side switching device (Q5) to conduct for a period longer than a duty cycle (D) following momentarily turning on said second low-side switching device (Q7).

13. The power converter as recited in Claim 7 wherein said power train includes an transformer (TR) coupled to said first circuit node (Va) and a duration of said short control pulse (710) is limited to substantially maintain a magnetic flux balance in said transformer (TR) while sufficient to charge said first bias voltage boot-strap capacitor ( $C_{B1}$ ).

14. The power converter as recited in Claim 7 wherein said short control pulse (710) is of a duration less than five percent of a switching cycle (T) of said power train.

15. The power converter as recited in Claim 7 further comprising a blocking diode ( $D_{B1}$ ) couplable between said first bias voltage source ( $V_D$ ) and coupled to said first terminal of said first bias voltage boot-strap capacitor ( $C_{B1}$ ).

16. The power converter as recited in Claim 1 wherein said controller (410, 1110) further comprises:

a level shifter (LS) coupled to a first driver (510) configured to control a conductivity of said first high-side switching device (Q1); and

a second driver (520) configured to control a conductivity of said first low-side switching device (Q3).

17. A method of operating a power converter including a power train including a first high-side switching device (Q1) coupled in series at a first circuit node (Va) with a first low-side switching device (Q3), said power converter including a first bias voltage boot-strap capacitor ( $C_{B1}$ ) having a first terminal couplable to a first bias voltage source ( $V_D$ ) and a second terminal coupled to said first circuit node (Va), the method, comprising:

applying (1710) a short control pulse (710) to and momentarily turning on said first low-side switching device (Q3) to charge up said first bias voltage boot-strap capacitor ( $C_{B1}$ ) via said first bias voltage source ( $V_D$ ) at a start-up of said power converter.

18. The method as recited in Claim 17, further comprising:

causing (1750) said low high-side switching device (Q3) to conduct for about half a duty cycle ( $D/2$ ) following momentarily turning on said first low-side switching device (Q3); and

controlling (1760) said duty cycle (D) of said first high-side switching device (Q1) and said first low-side switching device (Q3) to regulate an output characteristic ( $V_{out}$ ) of said power converter thereafter.

19. The method as recited in Claim 17 wherein said power train comprises a second high-side switching device (Q2) coupled in series at a second circuit node (Vb) with a second low-side switching device (Q4), and a second bias voltage boot-strap capacitor (CB2) having a first terminal couplable to said first bias voltage source ( $V_D$ ) and a second terminal coupled to said second circuit node (Vb), the method, further comprising

applying (1710) a short control pulse (720) to and momentarily turn on said second low-side switching device (Q4) to charge up said second bias voltage boot-strap capacitor ( $C_{B2}$ ) via said first bias voltage source ( $V_D$ ) at said start-up of said power converter;

causing (1750) said second high-side switching device (Q2) to conduct for about half a duty cycle ( $D/2$ ) following momentarily turning on said second low-side switching device (Q4); and

controlling (1760) said duty cycle (D) of said second high-side switching device (Q2) and said second low-side switching device (Q4) in cooperation with said first high-side switching device (Q1) and said first low-side switching device (Q3) to regulate an output characteristic ( $V_{out}$ ) of said power converter thereafter.

20. The method as recited in Claim 17 wherein said power train comprises an transformer (TR) and a second high-side switching device (Q5) coupled in series at a second circuit node (Vc) with a second low-side switching device (Q7) on a secondary side of said power train, said power converter including a second bias voltage boot-strap capacitor ( $C_{BS}$ ) having a first terminal coupled to a second bias voltage source ( $V_{DS}$ ) and a second terminal coupled to said second circuit node (Vc), the method, further comprising:

applying (1730) a short control pulse (1530) to and momentarily turn on said second low-side switching device (Q7) to charge up said second bias voltage boot-strap

capacitor ( $C_{BS}$ ) via said second bias voltage source ( $V_{DS}$ ) at said start-up of said power converter; and

causing (1740) said second high-side switching device (Q5) to conduct for a period longer than a duty cycle (D) following momentarily turning on said second low-side switching device (Q7).

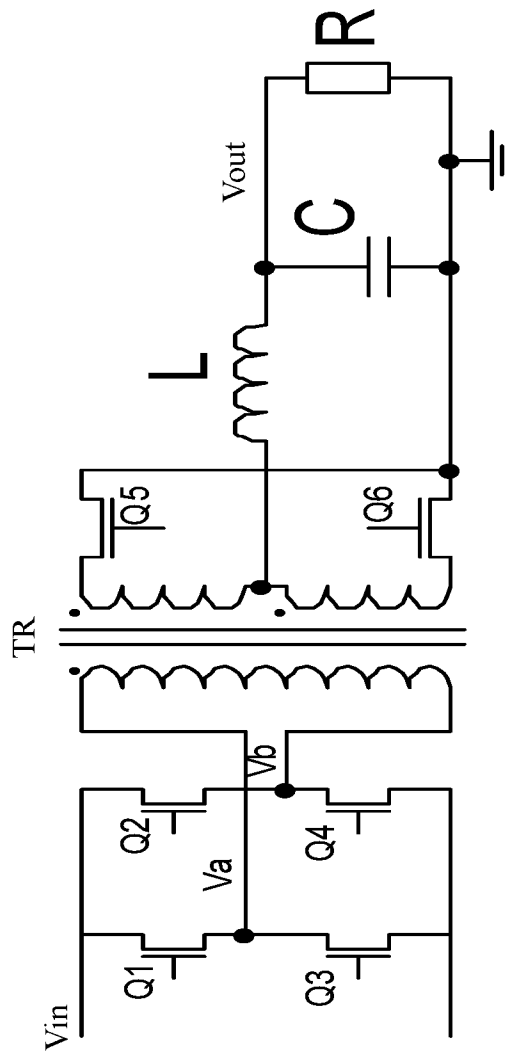


FIGURE 1

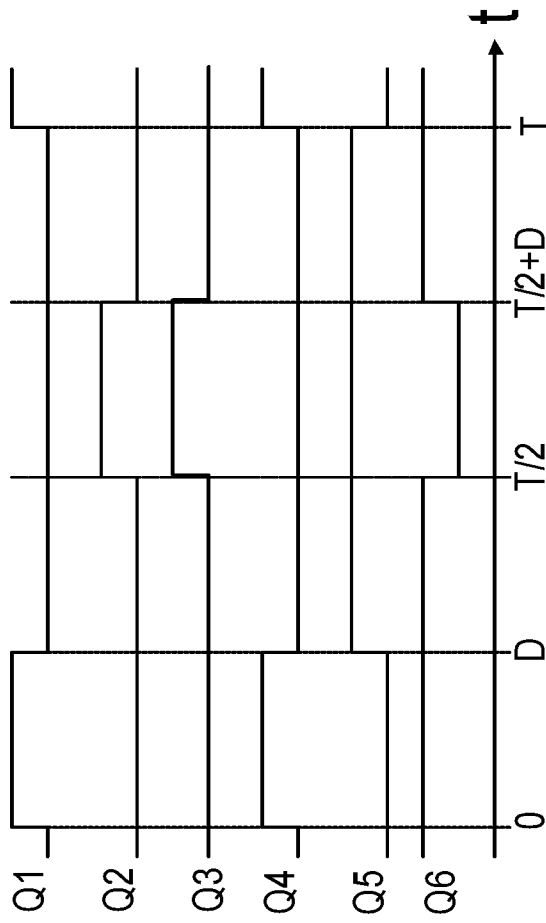


FIGURE 2

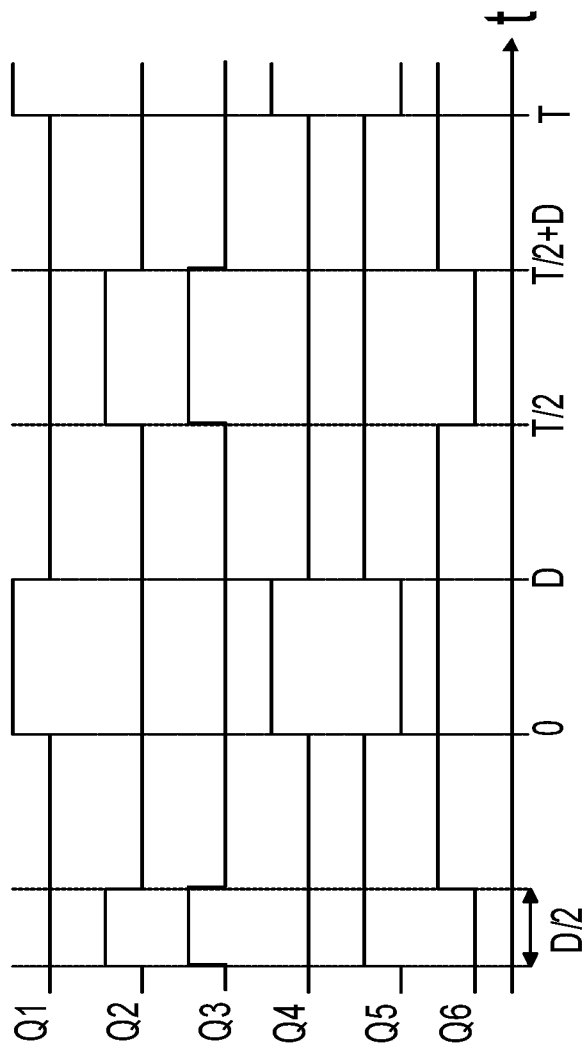


FIGURE 3

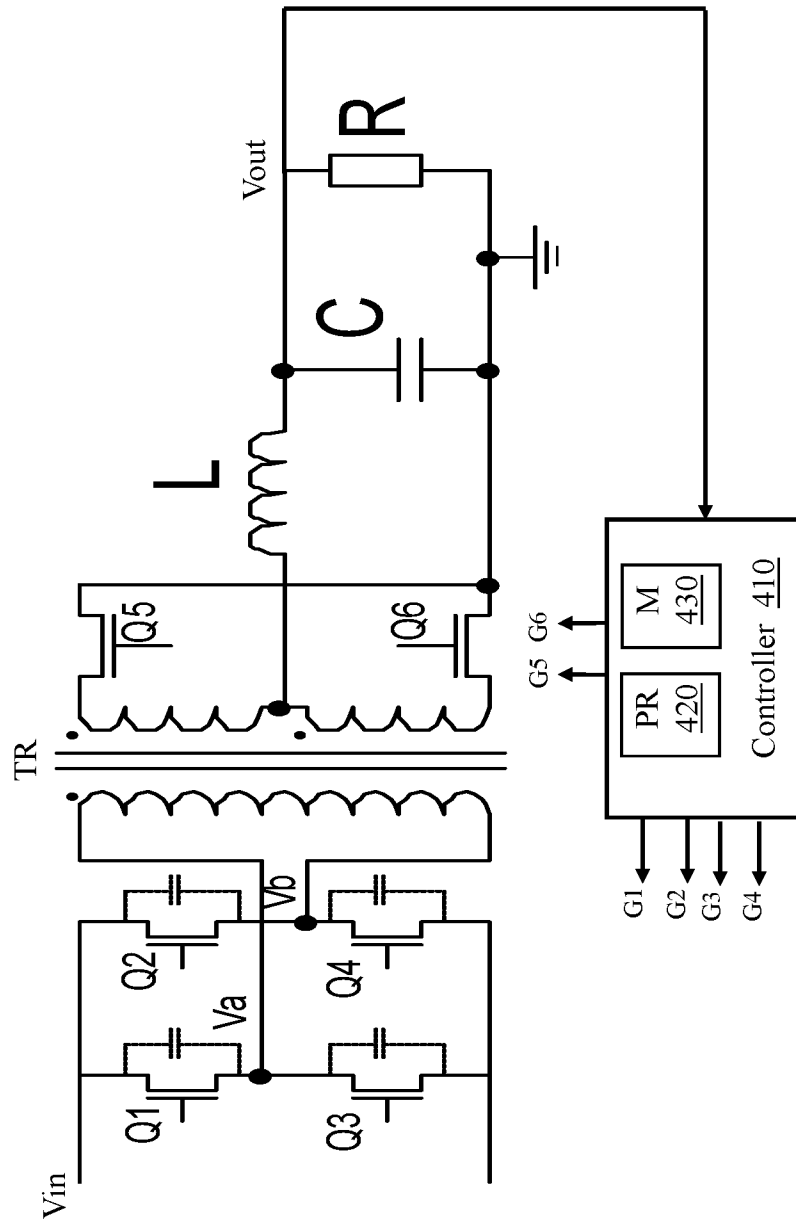


FIGURE 4

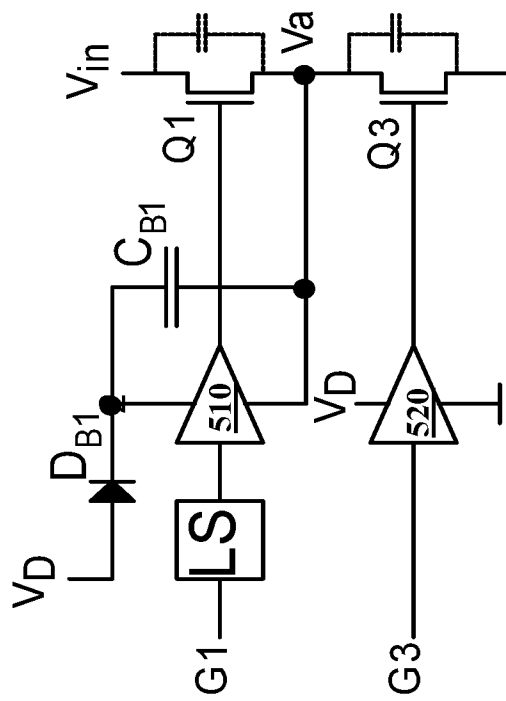


FIGURE 5

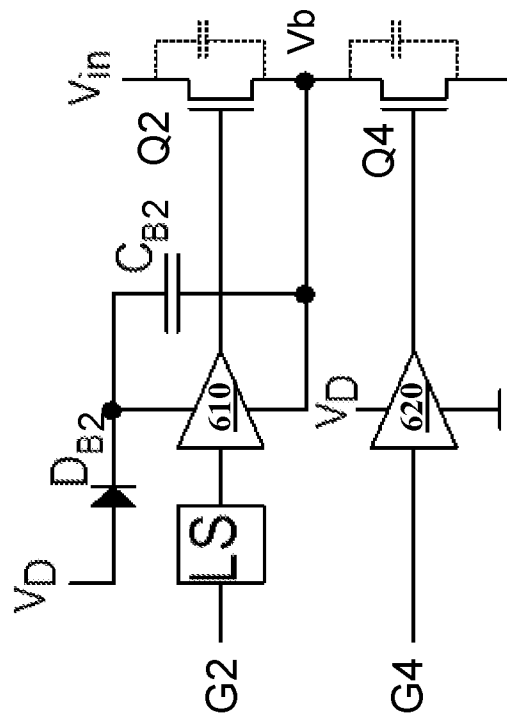


FIGURE 6

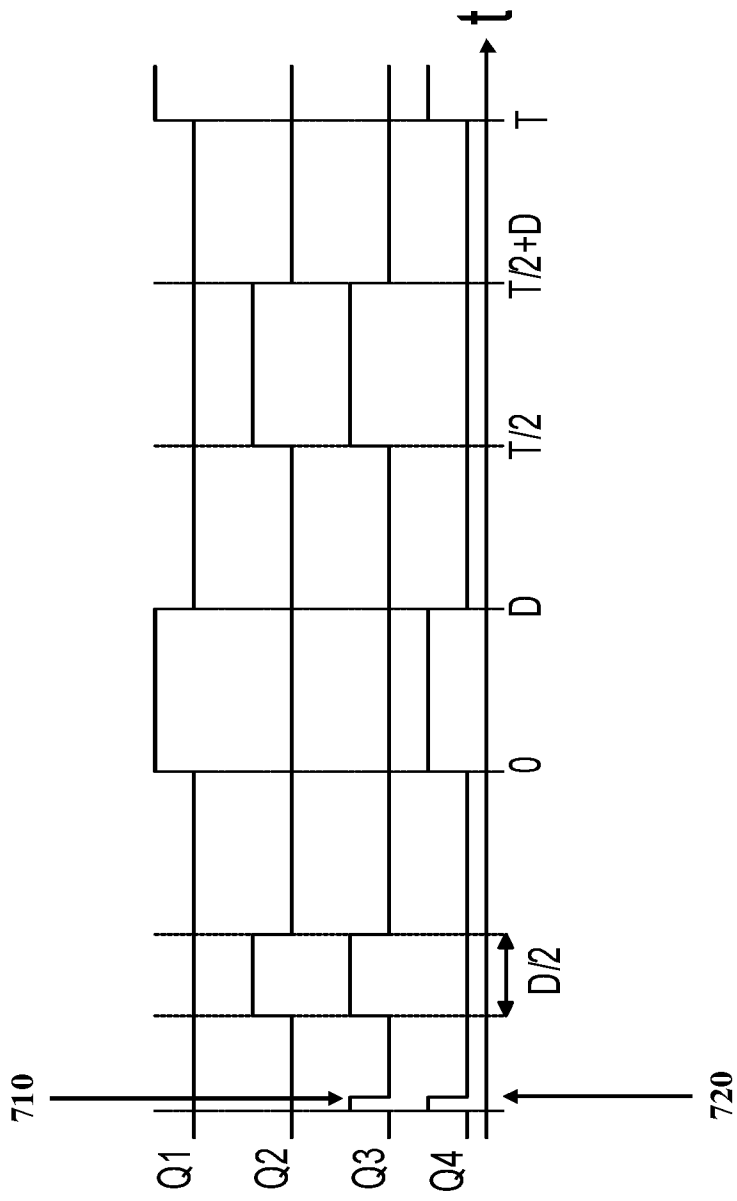


FIGURE 7

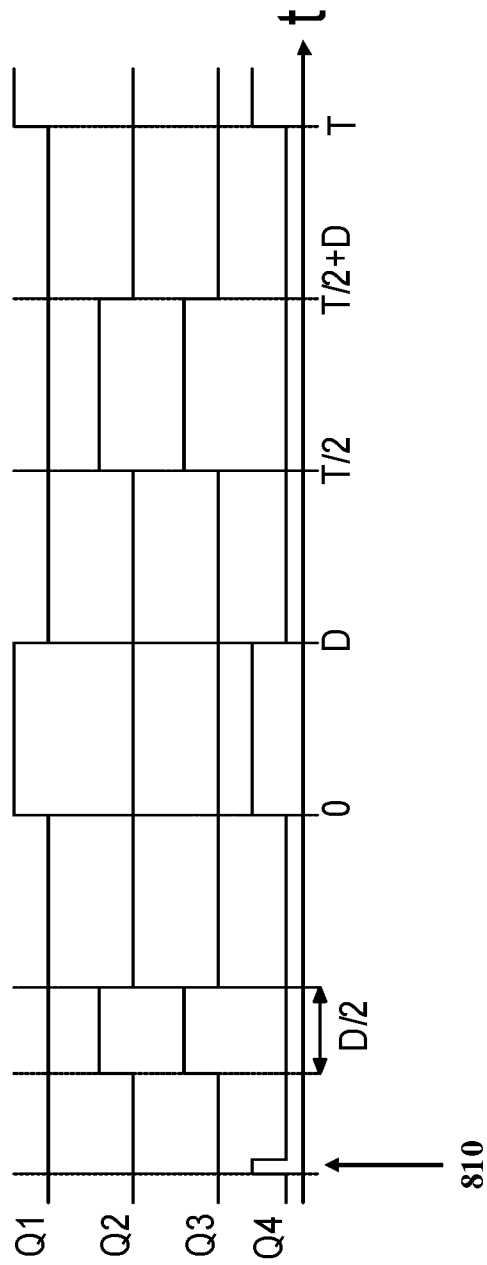


FIGURE 8

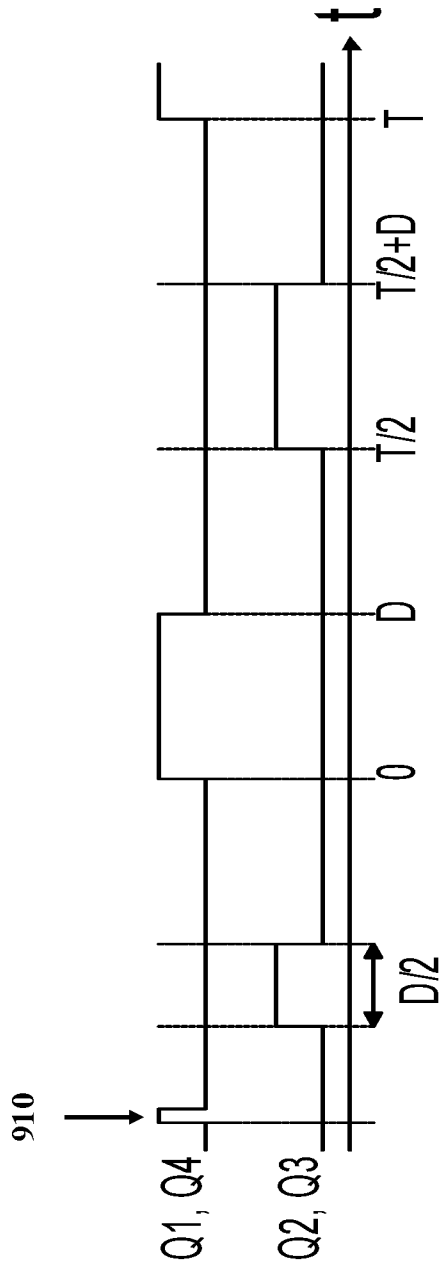


FIGURE 9

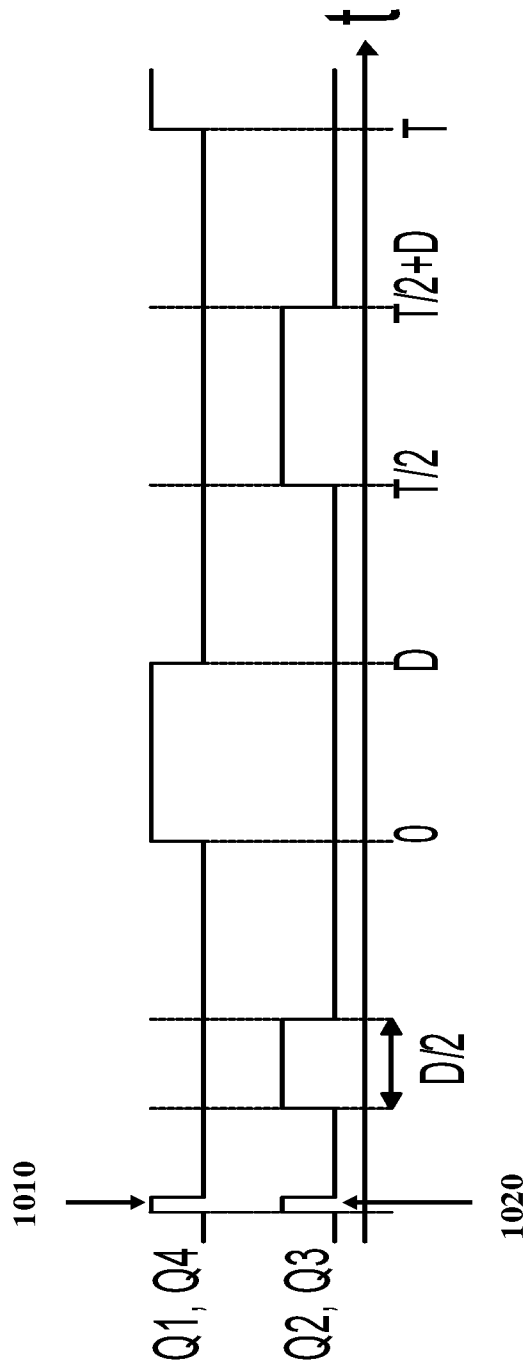


FIGURE 10

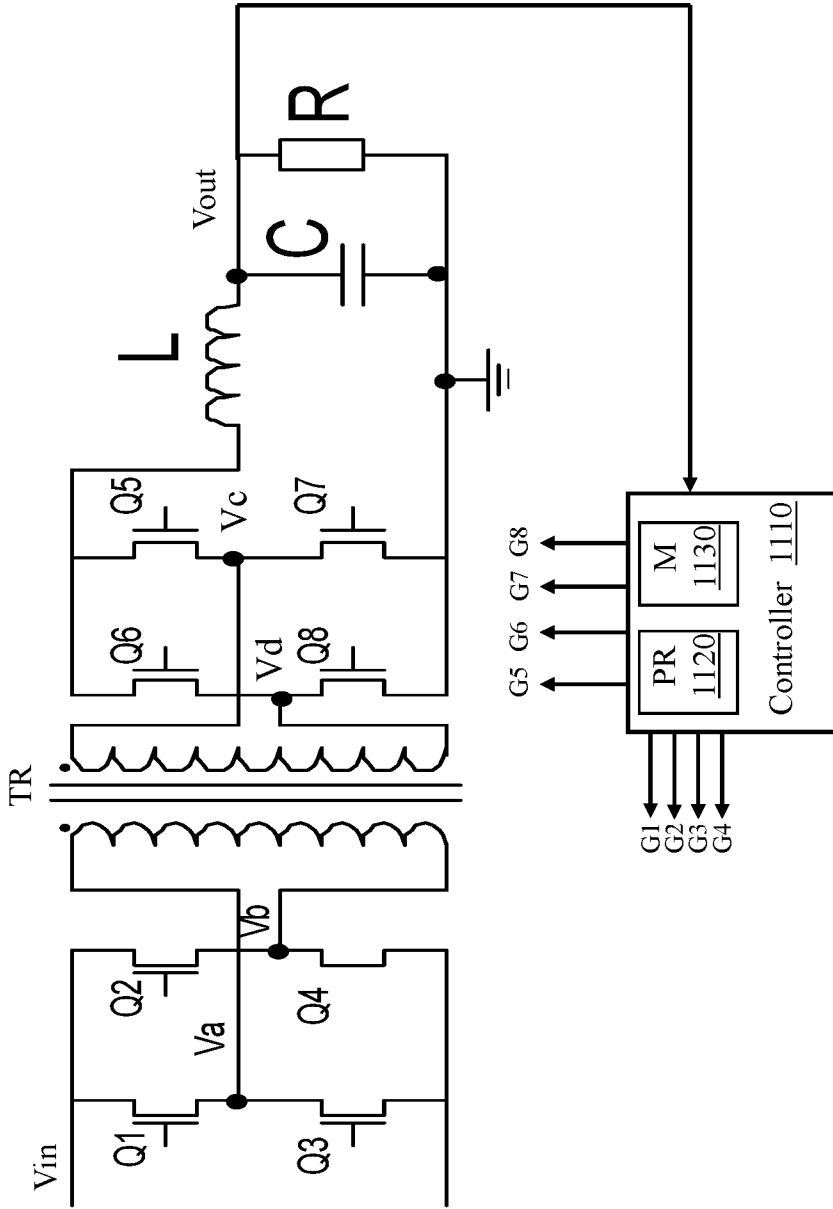


FIGURE 11

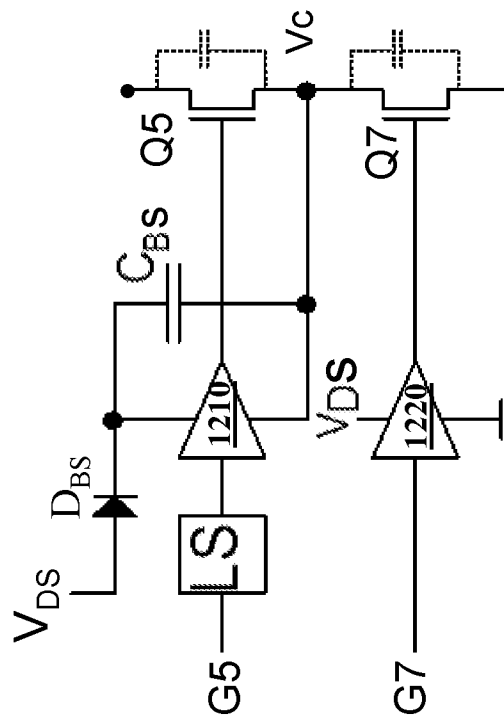


FIGURE 12

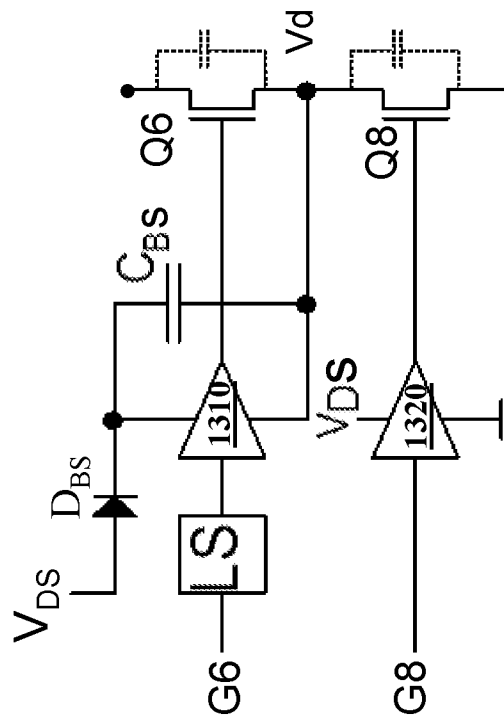


FIGURE 13

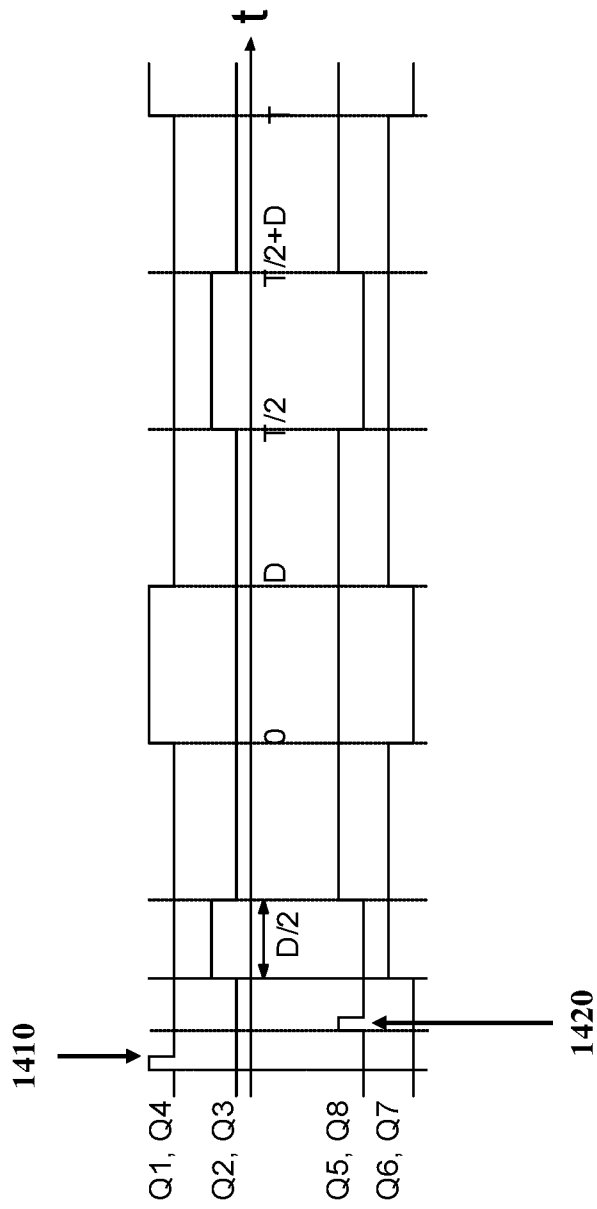


FIGURE 14

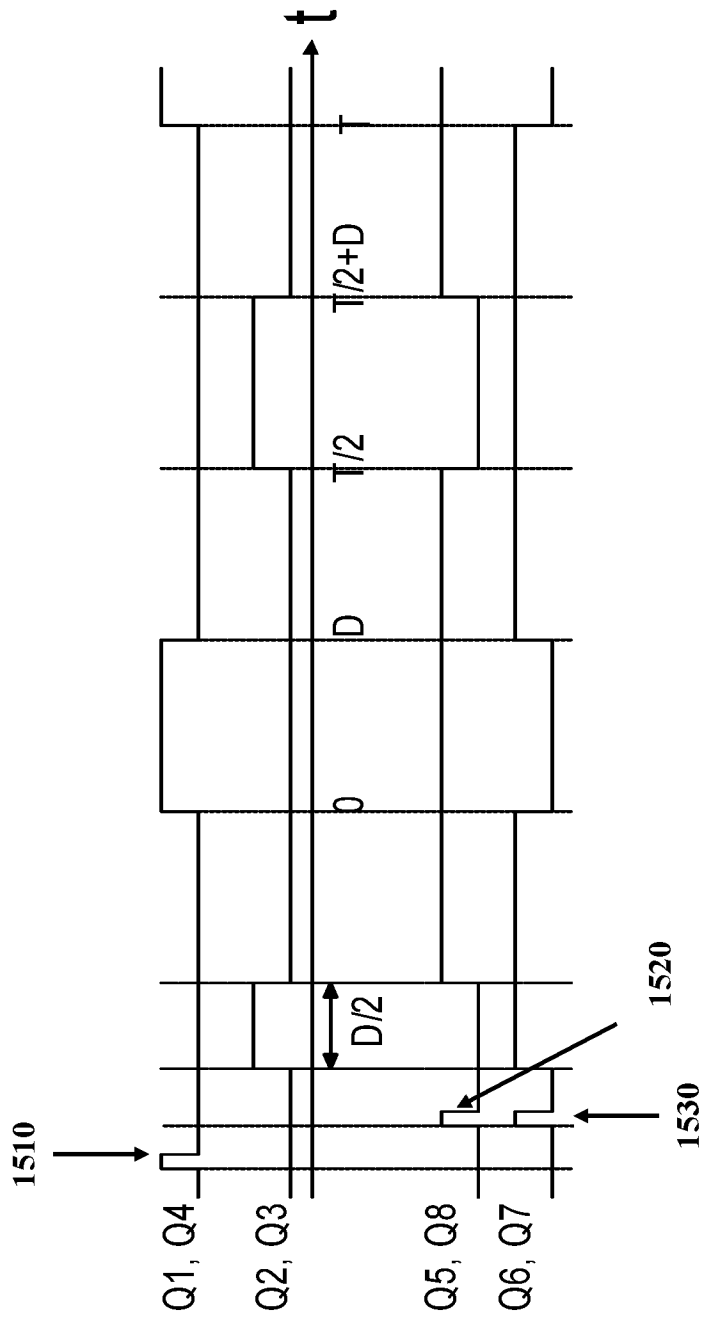


FIGURE 15

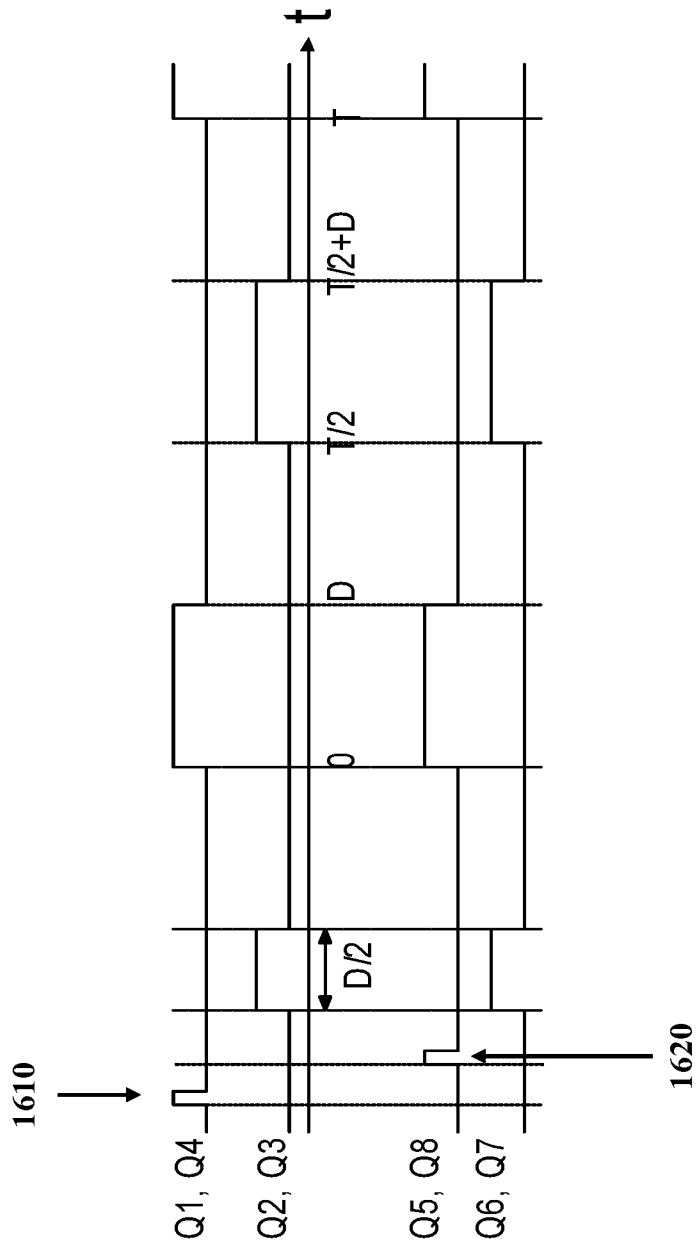


FIGURE 16

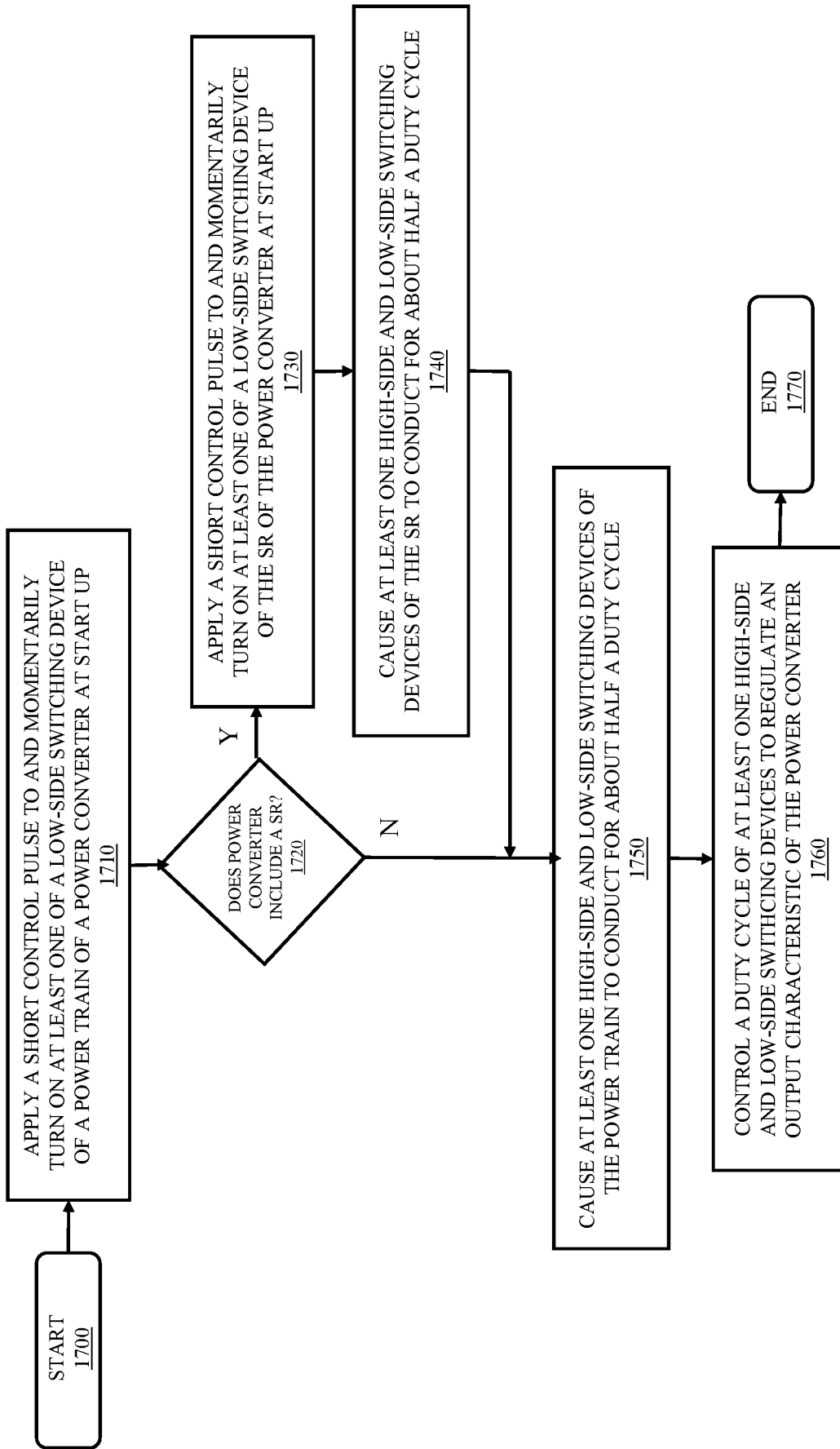


FIGURE 17

## INTERNATIONAL SEARCH REPORT

International application No

PCT/IB2016/053312

## A. CLASSIFICATION OF SUBJECT MATTER

INV. H02M1/40 H02M3/335 H02M1/36 H02M3/337  
 ADD. H02M1/08

According to International Patent Classification (IPC) or to both national classification and IPC

## B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)  
 H02M

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

EPO-Internal, WPI Data

## C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 8 456 867 B1 (KARLSSON MAGNUS [SE] ET AL) 4 June 2013 (2013-06-04) cited in the application the whole document	1-20
A	US 2015/365005 A1 (PANOV YURI [US] ET AL) 17 December 2015 (2015-12-17) the whole document	1-20
	----- -/--	

 Further documents are listed in the continuation of Box C. See patent family annex.

\* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&amp;" document member of the same patent family

Date of the actual completion of the international search

29 November 2016

Date of mailing of the international search report

08/12/2016

Name and mailing address of the ISA/

European Patent Office, P.B. 5818 Patentlaan 2  
 NL - 2280 HV Rijswijk  
 Tel. (+31-70) 340-2040,  
 Fax: (+31-70) 340-3016

Authorized officer

Van der Meer, Paul

## INTERNATIONAL SEARCH REPORT

International application No

PCT/IB2016/053312

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT		
Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	<p>ORTIZ G ET AL: "Magnetic Ear-based balancing of magnetic flux in high power medium frequency dual active bridge converter transformer cores", POWER ELECTRONICS AND ECCE ASIA (ICPE&amp;ECCE), 2011 IEEE 8TH INTERNATIONAL CONFERENCE ON, IEEE, 30 May 2011 (2011-05-30), pages 1307-1314, XP031955973, DOI: 10.1109/ICPE.2011.5944377 ISBN: 978-1-61284-958-4 the whole document</p> <p style="text-align: center;">-----</p>	1-20
A	<p>ORTIZ GABRIEL ET AL: "Flux Balancing of Isolation Transformers and Application of The Magnetic Ear for Closed-Loop Volt-Second", IEEE TRANSACTIONS ON POWER ELECTRONICS, INSTITUTE OF ELECTRICAL AND ELECTRONICS ENGINEERS, USA, vol. 29, no. 8, 1 August 2014 (2014-08-01), pages 4078-4090, XP011544087, ISSN: 0885-8993, DOI: 10.1109/TPEL.2013.2294551 [retrieved on 2014-03-26] the whole document</p> <p style="text-align: center;">-----</p>	1-20

# INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No

PCT/IB2016/053312

Patent document cited in search report	Publication date	Patent family member(s)	Publication date	
US 8456867	B1	04-06-2013	CN 103959626 A	30-07-2014
			EP 2786476 A1	08-10-2014
			US 8456867 B1	04-06-2013
			WO 2013079111 A1	06-06-2013
-----				
US 2015365005	A1	17-12-2015	NONE	
-----				