

(19) AUSTRALIAN PATENT OFFICE

(54) Title
Interface System

(51)⁶ International Patent Classification(s)
G08C 013/02 **G06F 159/00**
H03K 005/22

(21) Application No: **2003204497** (22) Application Date: **2003.06.02**

(30) Priority Data

(31) Number (32) Date (33) Country
60385285 **2002.06.04** **US**
7

(43) Publication Date : **2003.12.18**

(43) Publication Journal Date : **2003.12.18**

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INTERFACE SYSTEM

ABSTRACT

An interface system (30) is disclosed that delivers an output signal having a first signal characteristic in response to first and second input signals having the first signal characteristic and a second, different signal characteristic. The interface system (30) includes a signal input (10, 12) for receiving a first signal having a first signal characteristic and a second signal having a second signal characteristic which is different from the first signal characteristic, a detector circuit (32, 70) for detecting whether the signal at the input (10, 12) is the first signal or the second signal, and a translator circuit (52) for translating either of the first signal or the second signal into the output signal.

AUSTRALIA

PATENTS ACT 1990

COMPLETE SPECIFICATION

FOR A STANDARD PATENT

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Invention Title:	Interface System

The following statement is a full description of this invention, including the best method of performing it known to me/us:-

INTERFACE SYSTEM

FIELD OF THE INVENTION

This invention is directed generally to an improvement in a monitoring system, 5 and more particularly, to a novel interface device for interconnecting two or more different monitoring devices with a processor, such as a personal computer (PC), laptop, hand-held system or the like.

BACKGROUND OF THE INVENTION

10 While the invention may find other uses, the ensuing description refers specifically to its use with blood glucose monitoring systems.

Those who have irregular blood glucose concentration levels are medically required to regularly self-monitor their blood glucose concentration level. An irregular blood glucose level can be brought on by a variety of reasons including illness such as 15 diabetes. The purpose of monitoring the blood glucose concentration level is to determine the blood glucose concentration level and then to take corrective action, if needed, based upon whether the level is too high or too low, to bring the level back within a normal range. The failure to take corrective action can have serious implications. When blood glucose levels drop too low - a condition known as 20 hypoglycemia - a person can become nervous, shaky and confused. That person's judgment may become impaired and that person may eventually pass out. A person can also become very ill if their blood glucose level becomes too high - a condition known as hyperglycemia.

One method of monitoring a person's blood glucose level is with a portable, 25 hand-held blood glucose testing device. The portable nature of these devices enables the users to conveniently test their blood glucose levels wherever the user may be. The glucose testing device includes a biosensor to harvest the blood for analysis. One type of biosensor is the electrochemical biosensor. The electrochemical biosensor includes a reagent designed to react with glucose in the blood to create an oxidation current at 30 electrodes disposed within the electrochemical biosensor which is directly proportional to the user's blood glucose concentration. Such a biosensor is described in U.S. Patent

Nos. 5,120,420, 5,660,791, 5,759,364 and 5,798,031. Another type of sensor is an optical biosensor, which incorporates a reagent designed to produce a calorimetric reaction indicative of a user's blood glucose concentration level. The calorimetric reaction is then read by a spectrometer incorporated into the testing device. Such an 5 optical biosensor is described in U.S. Patent No. 5,194,393.

In order to check a person's blood glucose level, a drop of blood is obtained from the person's fingertip using a lancing device, and the blood is harvested using the biosensor. The biosensor, which is inserted into a testing unit or "meter" is brought into contact with the blood drop. The biosensor draws the blood, via capillary action, inside 10 the biosensor and the ensuing electrochemical reaction is measured by the test unit which then determines the concentration of glucose in the blood. Once the results of the test are displayed on a display of the test unit, the biosensor is discarded. Each new test requires 15 a new biosensor.

The invention concerns an adapter which permits different types of monitoring 15 devices to exchange signals with a processor, such as a personal computer (PC) or the like. This involves electronically differentiating between and automatically adapting to an open-collector signaling convention or an RS-232 (EIA-232) compatible signaling 20 convention.

One existing blood glucose meter has an RS-232 (EIA-232) compatible output 20 port with a custom connector. A redesign of this meter's electronics has been undertaken to reduce cost. However, the connector is molded into the case and a mold change is beyond the project scope. Therefore, the redesigned meter must use the same connector 25 as the earlier meter. Component and cost savings would, however, accrue if the RS-232 (EIA-232) compatible interface were replaced by an open-collector (OC) interface; however, the existing I/O cable, used for coupling the meter to a PC, would not be 30 compatible with this change. To simplify meter-to-computer interfacing for professionals that will be seeing both meter types (i.e., OC and RS-232 (EIA-232)), it would be advantageous to develop a single cable that would automatically work with either meter. The invention provides an electronic circuit, to be implemented in a modified cable, for accomplishing the above. If a stereo plug is wired in parallel with the 35 plug, compatibility can be extended to other existing "open collector" output meters.

Existing cables are not compatible with both signaling conventions. The one prior interface device, "Basic Cradle™" can handle both signaling conventions, but not automatically through a shared connector. This is true in part because of the incompatible plug/connector design of some other OC type meters.

5 The proposed invention will handle both signaling conventions automatically through a shared plug. It identifies the signal convention by monitoring for a negative marking voltage that is unique to the RS-232 (EIA-232) compatible interface of the existing meter. It uses the detected interface type to automatically correct signal polarity and adjust the signal detection level for the serial data stream. The level-shifted and
10 polarity-corrected data stream is then fed to another level translator to produce an RS-232 (EIA-232) compatible signal for the host computer. Like at least one existing cable, the interface is powered via signal pins of the host computer interface.

OBJECTS OF THE INVENTION

15 Accordingly, it is a general object of the invention to provide an adapter which permits different types of monitoring devices to exchange signals with a processor, such as a personal computer (PC) or the like.

SUMMARY OF THE INVENTION

20 Briefly, in accordance with the foregoing, an interface system for delivering an output signal having a said signal characteristic in response to first and second input signals having said first signal characteristic and a second different signal characteristic, comprises a signal input for receiving a first signal having a first signal characteristic and a second signal having a second signal characteristic which is different from said first
25 signal characteristic, a detector circuit for detecting whether the signal at said input is said first signal or said second signal, and a translator circuit for translating either of said first signal or said second signal into said output signal.

In accordance with another aspect of the invention, an interface method for delivering an output signal having a given signal characteristic in response to first and
30 second input signals having said first signal characteristic and a second, different signal characteristic, comprises receiving a first signal having a first signal characteristic and a

second signal having a second signal characteristic which is different from said first signal characteristic, detecting whether the signal at said input is said first signal or said second signal, and translating either of said first signal or said second signal into said output signal.

5 In accordance with another aspect of the invention, an interface system for delivering an output signal having a given signal characteristic in response to first and second input signals having said first signal characteristic and a second, different signal characteristic, comprises means for receiving a first signal having a first signal characteristic and a second signal having a second signal characteristic which is different
10 from said first signal characteristic, means for detecting whether the signal at said input is said first signal or said second signal, and means for translating either of said first signal or said second signal into said output signal.

BRIEF DESCRIPTION OF THE DRAWINGS

15 In the drawings:
FIG. 1 is a block diagram of a prior art cable device;
FIG. 2 is a somewhat more detailed schematic of the device of FIG. 1;
FIG. 3 is a simplified schematic of an interface in accordance with the invention;
FIG. 4 is a second schematic, similar to FIG. 3, showing a meter interface of the
20 invention;
FIG. 5 is a detailed schematic of the interface of FIGS. 3 and 4; and
FIG. 6 shows a cable interface according to one embodiment of the present invention.

DETAILED DESCRIPTION OF THE ILLUSTRATED EMBODIMENT

The present "DexTM" meter (a blood glucose monitoring device) has an I/O port
25 with a custom connector and uses RS-232 (EIA-232)-compatible signals. To save costs in a new meter design, called "Dex CURETM", it is necessary to use the same connector, but would be desirable to use an open collector (OC) interface built into a previously designed data acquisition ASIC, used in the prior "EliteTM" meter. The "OC" meter output is an open collector transistor with series resistor. The transistor's emitter is referenced to signal ground. The polarities of the two meter outputs (OC and RS-232 (EIA-232)) are also reversed. Accordingly, the present I/O cable is unsuitable for use
30

with this new meter interface. It would be useful to have a common I/O cable or "interface" for use with both the Dex™ and Dex CURE™ meters that would automatically adapt to the interface type (OC or RS-232 (EIA-232)) of the meter to which it is connected.

5 The (prior art) Basic Cradle™ electronics had the ability to interface with either the RS-232 (EIA-232)-compatible interface of a Dex™ meter or the open-collector logic level interface of an Elite™ meter. Different connectors 10, 12 were required for the two meters. After appropriate signal level translation and inversion of the Dex™ meter's output (at connector 10), the signals from the two connections were wire-ANDED 14.

10 The composite signal was then used to drive a signal level translator 16 feeding the host computer's input 20. The Basic Cradle™ circuit schematic is shown in FIGS. 1 and 2.

The interface 30 of the invention (see FIGS. 3-5) buffers the meter output and performs the necessary signal level translation to drive exclusive OR logic that the invention uses to feed a level translator used to drive a host computer's EIA-232D interface. The buffer input also has a pull-up to support an open-collector (OC) output meter style interface. Because the OC meter interface contains series resistance of up to 10 KΩ, the buffer input voltage swing is never fully to ground and is influenced by the strength of the pull-up. The pull-up should be strong enough to overcome anticipated leakage currents, but should be weak enough to allow adequate signal swing. In the 15 block diagrams (FIGS. 3 and 4), a comparator 32 referenced to a voltage negatively offset from the pull-up voltage is used as a voltage level translator to detect OC signal transitions and perform a voltage level translation. In practice, the comparator and reference functions might be implemented with a PNP transistor 70 (see FIG. 5).

The existing RS-232 (EIA-232) meter output is driven high in the spacing state. 25 Under low battery conditions, the magnitude of the spacing output may be only 3V to 4V. The transition level for the buffer should be less than the minimum spacing voltage in order to detect the transition. As illustrated in the block diagrams (FIGS. 3 and 4), this might be accomplished by regulating the pull-up voltage just below the 3V to 4V range of the minimum spacing voltage. An alternative, not diagrammed, is to use the output of 30 the comparator 48 to modify the input threshold when an RS-232 (EIA-232) type or "Dex™" meter is detected. The interface buffer should withstand RS-232 (EIA-232)

signal levels (± 15 V maximum) without damage. The computer interface software should be tolerant of any break characters or chatter that may occur when connecting or disconnecting a "DexTM" meter.

Like the "Basic CradleTM," power for the interface of the invention is derived 5 from the host computer's DTR and TxD signals. Maximum loading of these pins should be consistent with the drive capabilities of an EIA-232 interface. Ideally, current required to operate the interface should be less than 1 mA.

Although not shown, ESD (electrostatic discharge) protection is recommended for all exposed interface signals.

10 If an EliteTM meter compatible stereo plug 12 (not shown in FIG. 4) is connected in parallel to the DexTM plug 10 (see also FIG. 6), the interface cable 80 can also be used for Bayer Corporation EliteTM and CatalystTM meters.

For the proposed cable interface 80 (see FIG. 6), a single DexTM compatible connector 10 must be shared for both (OC and RS-232 (EIA-232)) signaling conventions.

15 As in the Basic CradleTM design, the host computer's TxD output 40 (FIGS. 3-5) can directly drive the shared RxD/DATA_IN meter input 42. The shared TxD/DATA_OUT meter output connection requires unique handling for each interface type.

A distinguishing signal characteristic that the proposed interface can use to identify the type of meter interface connected is the marking voltage level. In the 20 marking state, the DexTM style interface voltage goes negative, typically by 5V to 15V. The open-collector interface is never driven to a negative voltage. If the meter's signal output is appropriately rectified and used to charge a small capacitor 44, the capacitor voltage should go negative when the DexTM meter (RS-232 (EIA-232) output) is connected. A large value bleed resistor 46 (see FIG. 5) shunting the capacitor 44 will 25 discharge the capacitor 44 if the DexTM meter is disconnected. The capacitor should be sized so as to not excessively load and distort the meter output. The RC time constant should be optimized so that the capacitor voltage stays below a negative threshold during the normal spacing bits of DexTM data transmissions. The maximum discharge time should be limited so that the interface can recognize the switch from a DexTM to EliteTM 30 style meter within a reasonable time period (several seconds). The capacitor 44 is monitored by a comparator 48 referenced to an appropriate threshold voltage (negative

relative to that of the input driven by capacitor 44 when the meter's output is maintained at a voltage greater than or equal to signal ground, as would be characteristic of the OC meter output). The comparator output will reflect the interface type. It can be used to control exclusive-OR logic 50 to appropriately invert the polarity of the meter output.

5 In operation, the rectified meter output signal is used to negatively charge the capacitor 44 whenever an RS-232 (EIA-232) compatible signal is present. The resistor 46 paralleling the capacitor is used to discharge it whenever the RS-232 (EIA-232) compatible signal is removed. The comparator 48 is used to compare the capacitor voltage with a negative threshold voltage. The RC time constant is optimized to
10 minimize distortion of the data signal, to maintain the capacitor voltage more negative than the threshold voltage during spacing bits of an RS-232 (EIA-232) data stream, and to allow the capacitor to discharge above the threshold voltage if an RS-232 (EIA-232) marking voltage is not present for more than a few seconds.

15 The meter output is also fed to a voltage level translator 32 (70) to produce a common voltage swing for either type of meter output. A pull-up is used at the input to this level translator to handle the open-collector output of the Elite™ style interface. In FIG. 5, a voltage regulator 60 assures that the transition level for the level translator is within the signal swing for both the open-collector with pull-up and the RS-232 (EIA-232) signal swings. Alternatively, the output of the interface type detection comparator
20 48 can be used to adaptively adjust the transition level to match the presently connected interface type. The series resistance of the Elite™ style interface requires a transition voltage that is set close to, but below, the pull-up voltage of the interface. In a non-adaptive interface, this voltage must be less than the maximum 3V to 4V positive swing of a Dex™ meter under low battery conditions or RS-232 (EIA-232) transitions will not
25 be recognized. In an adaptive system, the threshold voltage for an RS-232 (EIA-232) signal can be lowered closer to signal ground. The outputs of the level translator 32 and of the interface type detection comparator 48 are fed to the exclusive-OR logic 50. This logic corrects for the signal polarity inversion inherent in the two interface types. The polarity-corrected signal then drives a level translator 52 that produces an RS-232 (EIA-
30 232) compatible signal for the host computer.

Regarding the circuitry feeding comparator 48 in FIG. 5, in FIGS. 3 and 4, it was assumed that the comparator inputs could swing both positive and negative relative to ground. This would have required a comparator needing both positive and negative supplies. The implementation of FIG. 5 uses a low voltage comparator that can operate off of only the 3V regulator used to power the level translator. For a single supply comparator to work, both inputs must be biased positive relative to ground. Rather than a negative reference voltage, the reference input ("+") of comparator 48 is supplied a voltage slightly above ground by a resistive divider. This divider is supplied by a 3V regulator 60. A second resistive divider is also supplied by the 3V regulator and creates a positive bias from the capacitor 44 voltage for the other comparator 48 input (-). This divider also provides the equivalent function of the bleed resistor 46 of FIGS. 3 and 4. Instead of bleeding capacitor 44 to ground, the bleed is to +3V. When the negative Dex marking voltage is present, capacitor 44 is driven negative through a MMBD914LT1 diode 54. As the lower leg of the divider goes negative, the comparator 48 input driven by its center tap goes more negative than the reference input and the comparator state changes. A BAS40LT1 diode 56 clamps the comparator input near ground when the capacitor voltage goes negative so that the comparator is not damaged by negative voltage swings (marking voltage can go as low as -15V, which the comparator would not survive without the diode). This diode will not bleed the capacitor of positive voltages. Other than the positive biasing tricks to allow a single supply comparator to be used, the functionality is completely consistent with the other FIGS. 3 and 4.

The invention recognizes that the negative marking voltage produced by the RS-232 (EIA-232) compatible interface of the existing Dex™ meter is a distinguishing signal characteristic that can be used reliably to distinguish between interface types. It also recognizes that a rectifier and capacitor combination provide a simple method for detection that rejects the spacing bits of an RS-232 (EIA-232) data stream and that this "filtered" signal can be used to control polarity correction and threshold setting for the input buffer.

While particular embodiments and applications of the present invention have been illustrated and described, it is to be understood that the invention is not limited to the precise construction and compositions disclosed herein and that various

modifications, changes, and variations may be apparent from the foregoing descriptions without departing from the spirit and scope of the invention as defined in the appended claims.

The claims defining the invention are as follows:

2 1. An interface system for delivering an output signal having a given signal
characteristic in response to first and second input signals having said first signal
4 characteristic and a second signal characteristic different from said first signal
characteristic, said interface system comprising:
6 a signal input for receiving a first signal having a first signal characteristic and a
second signal having a second signal characteristic which is different from said first
8 signal characteristic;
10 a detector circuit for detecting whether the signal at said input is said first signal
or said second signal; and
12 a translator circuit for translating either of said first signal or said second signal
into said output signal.

14 2. The system of claim 1 wherein said first and second signals comprise
output signals of a metering device and wherein said output signals comprises a signal
16 compatible with an input of a digital signal processor.

18 3. The system of claim 1 wherein said detector circuit is capable of
recognizing a marking voltage characteristic of each of said first signal and said second
20 signal.

22 4. The system of claim 3 wherein said detector circuit comprises a rectifier-
capacitor circuit or a resistor-capacitor circuit.

24 5. The system of claim 1 wherein said translator includes a polarity setting
26 circuit and a level setting circuit.

28 6. The system of claim 1 wherein said detector circuit includes a signal
characteristic type detector circuit and a voltage level translator.

7. The system of claim 1 wherein said first signal is an RS-232 (EIA-232)
2 output signal and said second signal is an open-collector output signal.

8. An interface method for delivering an output signal having a given signal
4 characteristic in response to first and second input signals having said first signal
characteristic and a second, signal characteristic different from said first signal
6 characteristic, said method comprising:

receiving a first signal having a first signal characteristic and a second signal
8 having a second signal characteristic which is different from said first signal
characteristic;

10 detecting whether the signal at said input is said first signal or said second signal;
and

12 translating either of said first signal or said second signal into said output signal.

14 9. The method of claim 8 wherein said first and second signals comprise
output signals of a metering device and wherein said output signals comprises a signal
16 compatible with an input of a digital signal processor.

18 10. The method of claim 8 wherein said detecting includes recognizing a
marking voltage characteristic of each of said first signal and said second signal.

20
22 11. The method of claim 10 wherein said detecting uses a rectifier-capacitor
circuit or a resistor-capacitor circuit.

24
26 12. The method of claim 8 wherein said translating includes polarity setting
and level setting.

28 13. The method of claim 8 wherein said detecting includes detecting said
signal characteristics and translating a voltage level of at least one of said first and
second signals.

14. The method of claim 8 wherein said first signal is an RS-232 (EIA-232)
2 output signal and said second signal is an open-collector output signal.

4 15. An interface system for delivering an output signal having a given signal
5 characteristic in response to first and second input signals having said first signal
6 characteristic and a second signal characteristic different from said first signal
7 characteristic, said system comprising:
8 means for receiving a first signal having a first signal characteristic and a second
9 signal having a second signal characteristic which is different from said first signal
10 characteristic;

11 means for detecting whether the signal at said input is said first signal or said
12 second signal; and

13 means for translating either of said first signal or said second signal into said
14 output signal.

16 16. The interface system of claim 8 wherein said first and second signals
17 comprise output signals of a metering device and wherein said output signals comprise a
18 signal compatible with an input of a digital signal processor.

20 17. The interface system of claim 8 wherein said means for detecting includes
21 means for recognizing a marking voltage characteristic of each of said first signal and
22 said second signal.

24 18. The interface system of claim 10 wherein said means for detecting uses a
25 rectifier-capacitor circuit or a resistor-capacitor circuit.

26 19. The interface system of claim 8 wherein said means for translating
27 includes means for polarity setting and means for level setting.

20. The interface system of claim 8 wherein said means for detecting includes means for detecting said signal characteristics and means for translating a voltage level of at least one of said first and second signals.

5 21. The interface system of claim 8 wherein said first signal is an RS-232 (EIA-232) output signal and said second signal is an open-collector output signal.

10 22. An interface system for delivering an output signal having a given signal characteristic in response to first and second input signals having said first signal characteristic and a second signal characteristic different from said first signal characteristic, said interface system being substantially as described herein with reference to Figs. 3 to 6 of the accompanying drawings.

15 23. An interface method for delivering an output signal having a given signal characteristic in response to first and second input signals having said first signal characteristic and a second signal characteristic different from said first signal characteristic, said method being substantially as described herein with reference to Figs. 3 to 6 of the accompanying drawings.

20 DATED this Twenty-first Day of May, 2003

Bayer Corporation
Patent Attorneys for the Applicant
SPRUSON & FERGUSON

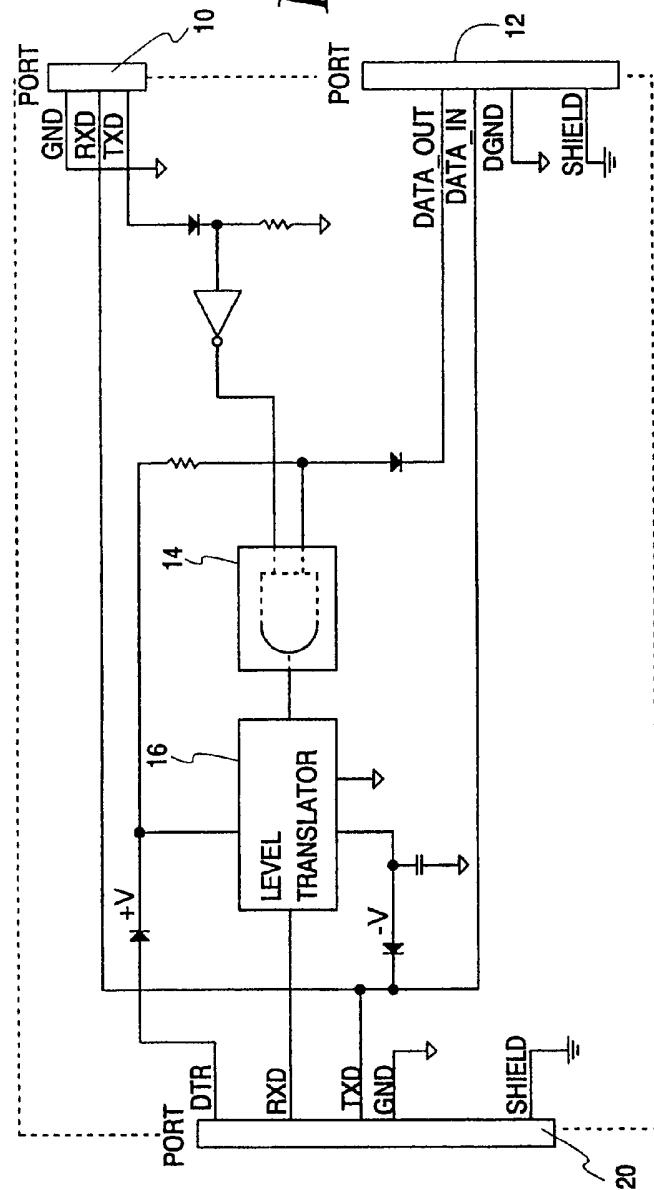
Fig. 1
Prior Art

Fig. 6

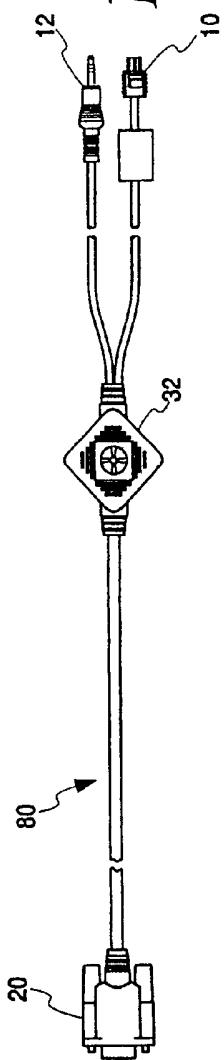
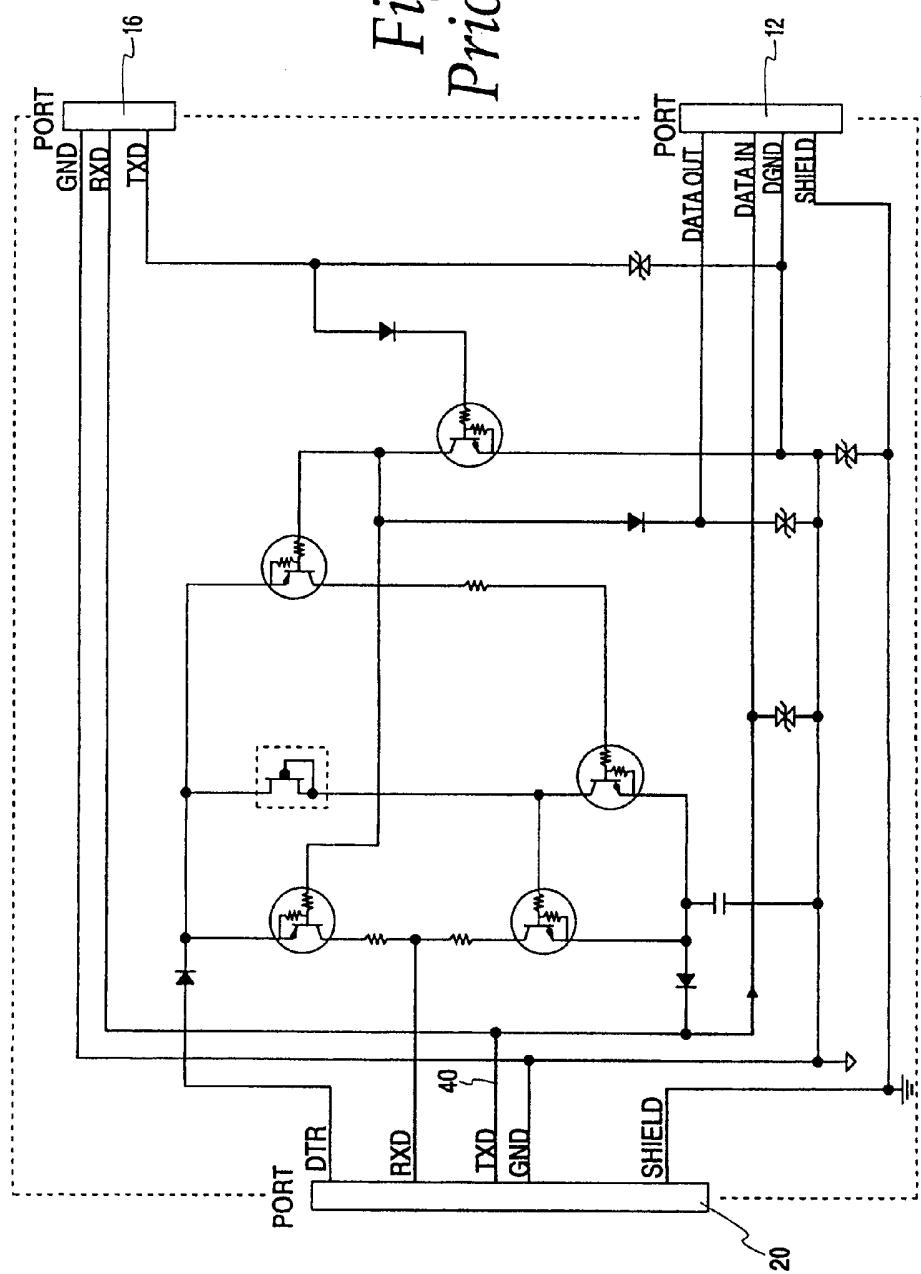


Fig. 2
Prior Art

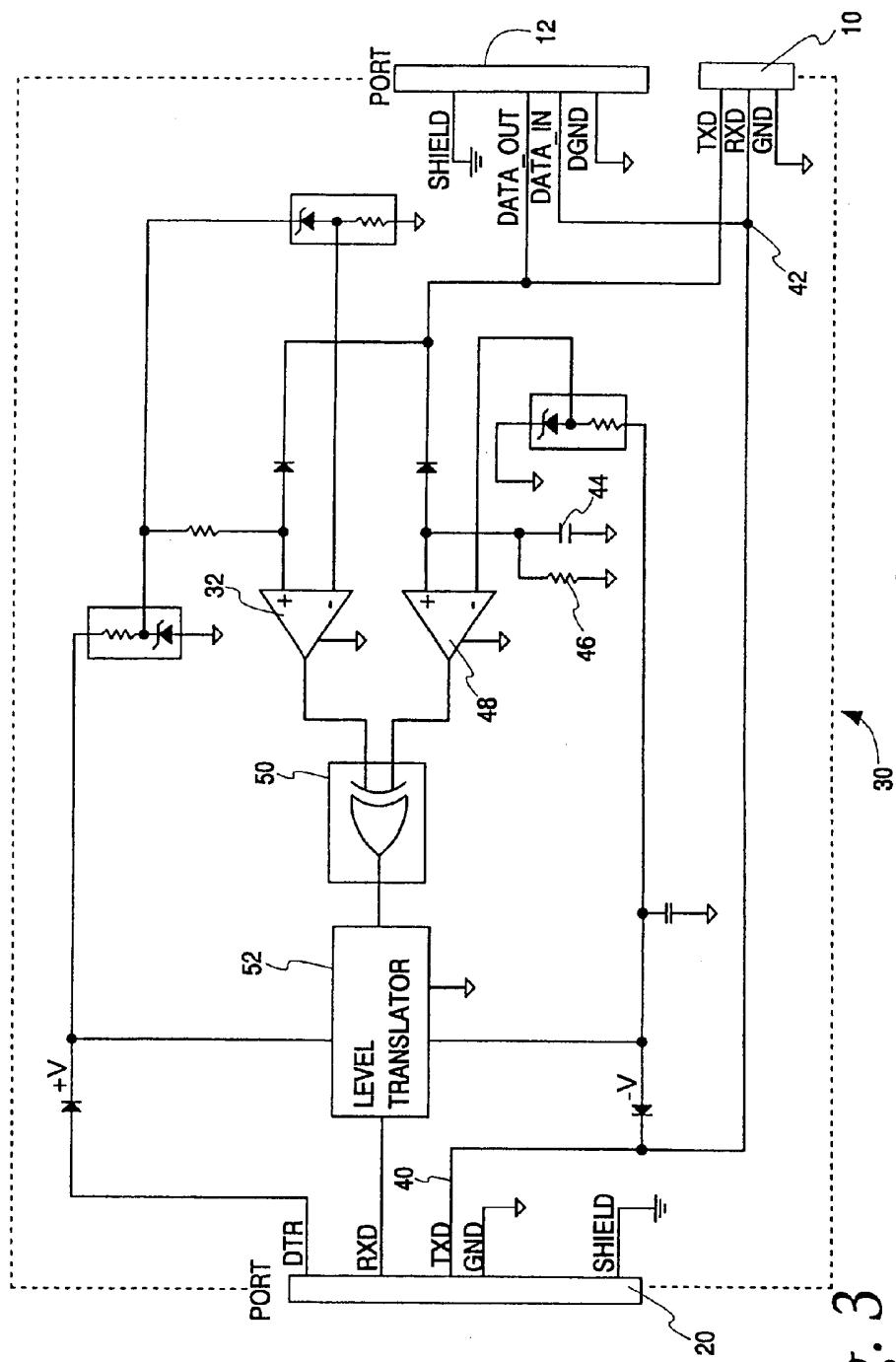


Fig. 3

Fig. 4

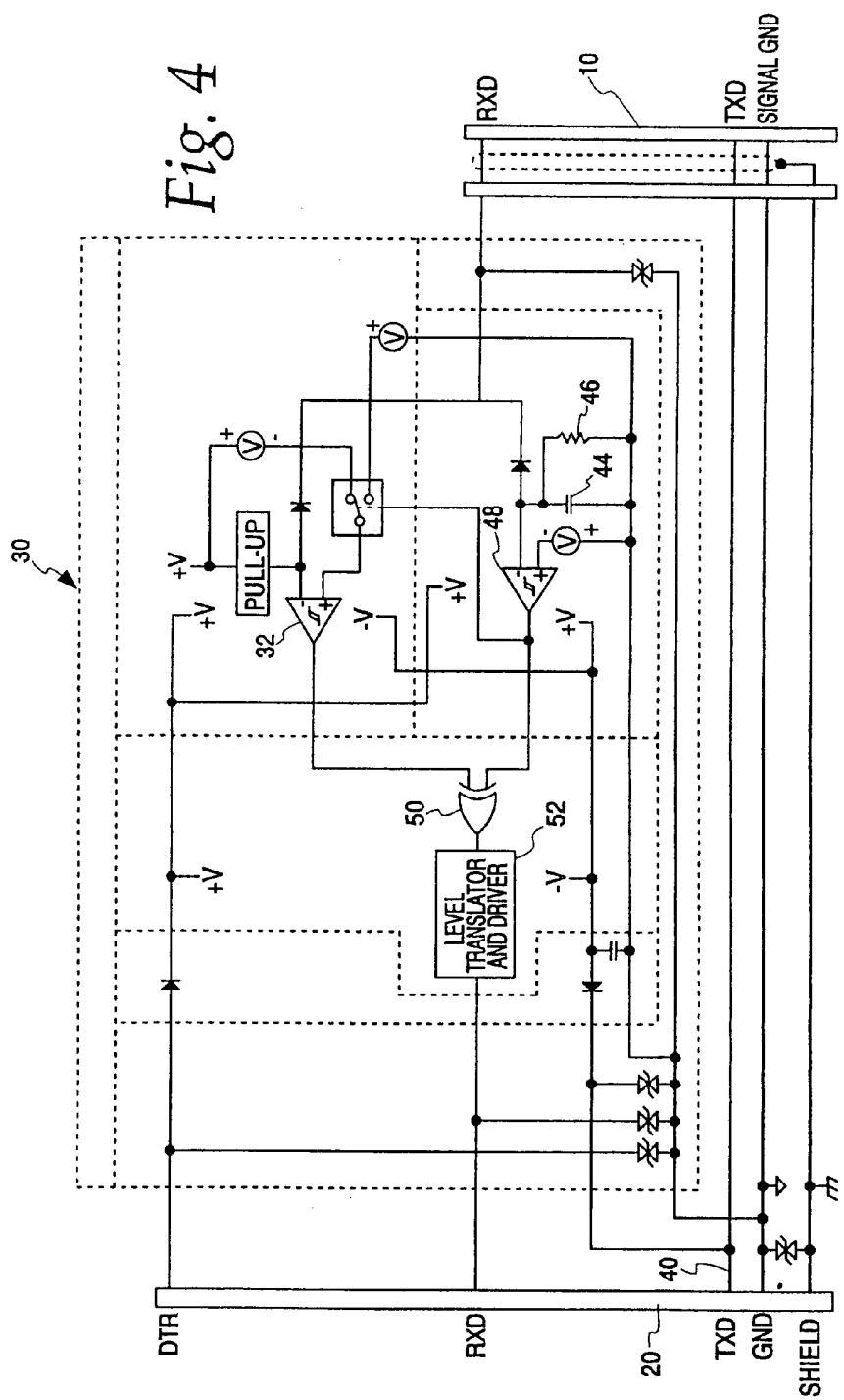


Fig. 5

