United States Patent

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[72] Inventor **Fred Karwacki**
Hopkins, Minn.

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[73] Assignee **Honeywell Inc.**
Minneapolis, Minn.
a corporation of Delaware

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[54] **CONTROL APPARATUS**
7 Claims, 2 Drawing Figs.

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[51] **Int. Cl.** **H03k 17/00**
[50] **Field of Search** 307/239, 246, 243, 244, 288, 255, 253

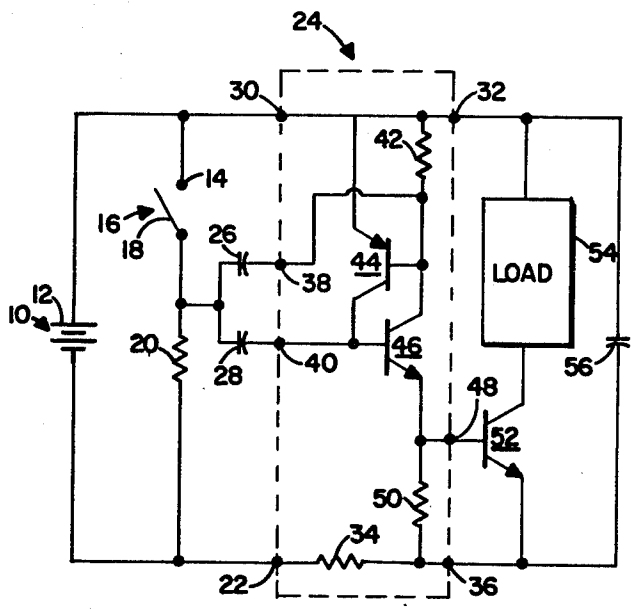
[56] **References Cited**
UNITED STATES PATENTS

3,160,766	12/1964	Reymond	307/255
2,890,353	6/1959	Overbeek et al	307/288X
3,023,323	2/1962	Kojalowicz	307/288X
3,139,539	6/1964	Hewett	307/288X
3,381,146	4/1968	Egan	307/252UX

Primary Examiner—Donald D. Forrer
Assistant Examiner—B. P. Davis
Attorneys—Roger W. Jensen, Charles J. Ungemach and Bruce C. Lutz

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ABSTRACT: A circuit for providing a positive output pulse upon either the opening or closing of a switch which provides either positive or negative going input signals to the circuit.



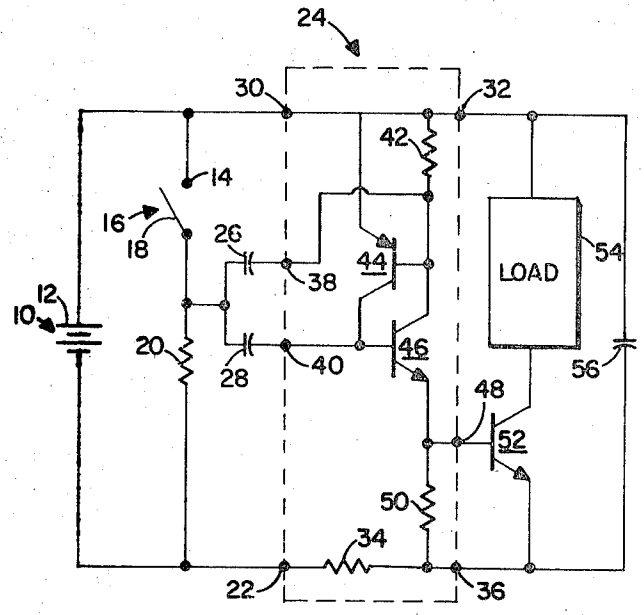


FIG. 1

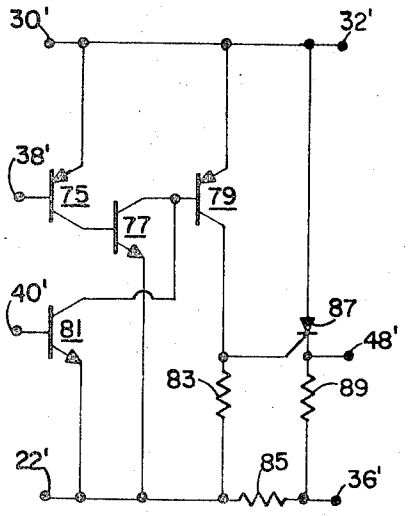


FIG. 2

INVENTOR.
FRED KARWACKI
BY Bruce C Lutz
ATTORNEY

CONTROL APPARATUS

THE INVENTION

This application generally relates to electronic circuitry and more specifically to circuitry for providing an output pulse of a given polarity direction in response to input pulses of either polarity direction.

Other switches for accomplishing the same general function as outlined above have been presented in the past but it is believed that the present invention accomplishes the desired result better and more efficiently than previously designed switches.

It is therefore a general object of this invention to provide improved switching apparatus.

Further objects and advantages of the present invention will be apparent from a reading of the specification and appended claims in conjunction with the drawings wherein:

FIG. 1 is a circuit diagram of the invention; and

FIG. 2 is a partial circuit schematic which may be used in place of a portion of FIG. 1. In FIG. 1, a battery generally designated as 10 has a positive terminal 12 which is connected to one stationary contact 14 of a switch generally designated as 16 having a movable contact 18. The negative terminal of battery 12 is connected to one end of a resistor 20 and to a terminal 22 of a dashed line box generally designated as 24. The other end of resistor 20 is connected to movable contact 18 and also to one end of each of two energy storage means or capacitive means 26 and 28. The movable contact 18 of switch 16 can be altered between open and closed positions. Contact 14 is also connected to a terminal means 30 on the edge of dashed line box 24 and is common with another terminal 32 on the opposite side of box 24. A resistance means 34 is connected between terminal 22 on one side of dashed line box 24 and a terminal 36 on the other side thereof. The unconnected electrodes of capacitors 26 and 28 are connected respectively to terminal means 38 and 40 on the side of box 24. A resistive means 42 is connected between terminals 30 and 38. A PNP transistor generally designated as 44 has an emitter connected to terminal 30 while a collector is connected to terminal 40 and a base thereof is connected to terminal 38. An NPN transistor generally designated as 46 has its base connected to terminal 40 while its collector is connected to terminal 38 and its emitter is connected to a final output terminal 48 on block 24. A resistor 50 is connected between terminals 48 and 36.

The transistors 44 and 46 constitute a four-layer semiconductor device which in some instances is referred to as a PNPN semiconductor. When the two transistors are commonly connected within one container the device is also known as a silicon controlled switch. This configuration is also substantially the same a that used for a silicon controlled rectifier (SCR) except that a SCR only uses one of the two base terminals. While a PNPN device is shown, for the opposite polarity signals and voltage supplied potentials, a NPNP four layer device could equally well be used.

A transistor or switch 52 has its base connected to terminal 48 while its emitter is connected to terminal 36. A load 54 is connected between terminal 32 and a collector of transistor 52. A capacitive means 56 is connected between terminals 32 and 36.

The circuit shown in FIG. 2 can be used to replace the block 24 of FIG. 1 and the corresponding terminals are numbered exactly the same in FIG. 2 and are placed in similar positions. However, each of these corresponding numbers is designated with a prime so as to differentiate FIG. 2 from FIG. 1. A PNP transistor generally designated as 75 has its emitter connected to terminal 30' while its base is connected to terminal 38'. A collector of transistor 75 is connected to a base of an NPN transistor 77 which has its emitter connected to terminal 22' and its collector connected to a base of a PNP transistor generally designated as 79 and also to a collector of an NPN transistor generally designated as 81. Transistor 79 has its emitter connected to terminal 30' while its collector is connected through a resistor 83 to terminal 22'. A resistor 85 which corresponds in function to resistor 34 is connected between terminals 22' and 36'. The transistor 81 has its base connected to terminal 40' while its emitter is connected to terminal 22'. An SCR or four-layer semicondctor means 87 has its anode connected to terminal 30' while its gate is connected to the collector of transistor 79. The cathode of SCR 87 is connected to terminal 48'. A resistor 89 is connected between terminals 48' and 36' and corresponds to resistor 50 of FIG. 1.

OPERATION

In operation, the capacitor 56 charges to the potential of supply 10 through resistor 34. It will be assumed that the switch utilizing transistors 44 and 46 is OFF initially. The switch 16 is then operated to its closed condition and this suddenly raises the potential of contact 18 in an upward or positive polarity direction. This will quickly raise the potential at the bases of the two transistors 44 and 46 through capacitors 26 and 28 respectively. However, a positive pulse at the base of transistor 44 will be disregarded. The positive pulse at the base of transistor 46, however, will actuate this transistor and turn the transistor to an ON condition. By feedback through the two transistor devices, the lowering of the collector of transistor 46 will actuate transistor 44 to keep the combination in an ON condition. The turn-on of transistor 46 will provide a positive going pulse at terminal 48 so as to actuate transistor 52. When transistor 52 turns ON, there is a short circuit produced between the load 54 and the capacitor 56 so that capacitor may discharge its energy into load 54. When capacitor 56 is sufficiently discharged, the voltage thereacross and thus the voltage across the combination of transistors 44 and 46 is so low that the combination switch is starved to an OFF condition. By definition in this specification, a positive going or unidirectional output pulse is meant to define the leading edge of the pulse. In other words, the voltage at junction point 48 is normally at ground potential and when transistor 46 turns ON, the voltage at junction point or terminal 48 suddenly rises in potential although it will fall to ground potential again as soon as capacitor 56 discharges. Also, by definition, the input signals from switch 16 are bidirectional in that sometimes the leading edge is positive going and sometimes it is negative going.

One example where the leading edge of the signal from switch 16 would be negative going would be in a condition opposite that considered above. In this instance, the switch including transistors 44 and 56 is OFF while capacitor 56 is charged and switch 16 is changed from the previously mentioned closed condition to an open condition. The potential at contact 18 will suddenly be lowered in potential so as to provide negative pulses through capacitors 26 and 28 to the bases of transistors 44 and 46. A negative going pulse will not actuate transistor 46 but it will actuate transistor 44. When transistor 44 turns ON, its collector will rise in potential and actuate transistor 46 thereby producing a positive going pulse at terminal 48 with respect to terminal 36. Again, transistor 52 will turn ON allowing capacitor 56 to discharge and thereby turn OFF the four-layer semiconductor switch.

Referring now to FIG. 2 it will be noted that while the circuit is somewhat similar to the circuit shown within block 24 of FIG. 1, the circuit utilizes an SCR as the four-layer semiconductor means and replaces one resistor with another resistor and four transistors. The circuit as shown in FIG. 2 is simpler to produce in integrated circuit form and is another embodiment of of the basic invention. If negative going pulses are applied at terminals 38' and 40', only transistor 75 will be actuated. The actuation of transistor 75 will actuate transistor 77 which in turn actuates transistor 79 and thus produces a positive pulse to turn SCR 87 to an ON condition and thereby produce a positive going output pulse at terminal 48' with respect to terminal 36'.

If two positive going pulses are applied at terminals 38' and 40', transistor 81 will be actuated thereby actuating transistor 79 and again actuating SCR 87.

As will be realized by those skilled in the art, resistors **34** and **85** are of such a value that capacitor **56** can normally charge to the full potential of the load **10** between repositioning of switch **16** or between the occurrence of positive and negative going pulses to the circuit in the event that a device other than switch **16** is used to produce the pulses. However, the impedance of these two resistors is large enough that the SCR or PNPN switch is starved to an OFF condition by the rapid discharge of capacitor **56** through the load **54** upon each occurrence of discharge of this capacitor.

While I have shown two embodiments of my invention I do not wish to be limited to the embodiments shown but only by the scope of the appended claims which describe the use of a two-energy storage means network for receiving either positive or negative going pulses to actuate a four-layer semiconductor means.

I claim:

1. A circuit for providing a unidirectional output pulse in response to bidirectional sudden changes in input voltage comprising, in combination:

input means for providing bidirectional rapidly changing input signals;

four-layer semiconductor means including signal input means;

impedance means connected in series combination with said four-layer semiconductor means;

power supplying means connected for supplying power across said series combination;

first and second capacitance means for supplying positive and negative pulses, connected between said input means and said semiconductor means for actuating said semiconductor means to an ON condition for each rapid change in input potential; and

output means connected to supply unidirectional output pulses from said semiconductor means.

2. Apparatus as claimed in claim **1** wherein said impedance means has an intermediate terminal means and the output means is connected between said semiconductor means and said terminal means.

3. Apparatus as claimed in claim **2** comprising in addition:

load means; and

switch means connected in series combination with said load means and connected to said output means for receiving therefrom unidirectional actuating signals.

4. Apparatus as claimed in claim **3** comprising in addition capacitive means connected in parallel with the series combination of said load means and switch means for discharging trough the load means when said switch means is actuated and also lowering the potential across said four-layer semiconductor means to deactivate said semiconductor means upon discharge of said capacitive means.

5. Apparatus as claimed in claim **4** wherein said semiconductor means is a PNPN semiconductor switch and the unidirectional output pulses are positive.

6. Apparatus for providing an output for each opening and closing of a monitored switch having at least first and second contacts and means or closing and opening an electrical path therebetween, said apparatus comprising:

first and second terminals for connection respectively to said first and second contacts of said monitored switch;

power supply means having a first polarity end connected to said first terminal and having a second polarity end connected through an impedance to said second terminal;

controlled switch means connected across said power supply means for opening and closing a series current path between said power supply and a load, said controlled switch means having first and second controlled inputs for receiving positive and negative pulses respectively, said controlled switch means being operable to close said series current path between said power supply means and said load upon application of a positive pulse to said first controlled input and also upon application of a negative pulse to said second controlled input; and

first and second capacitor means connecting said second terminal respectively to said first and said second controlled inputs of said controlled switch means, whereby upon opening of said monitored switch a pulse of a first polarity is presented to said first and second controlled inputs of said controlled switch means and upon closing of said monitored switch a pulse of a second polarity is presented to said first and second controlled inputs of said controlled switch means.

7. Apparatus as claimed in claim **6** comprising, in addition energy storage means connected across said controlled switch means, for discharging though said load upon closing of said series current path between said power supply means and said load, to deactivate said controlled switch means.