(54) Title: GATE DRIVER FOR ENHANCEMENT-MODE AND DEPLETION-MODE WIDE BANDGAP SEMICONDUCTOR JFETS
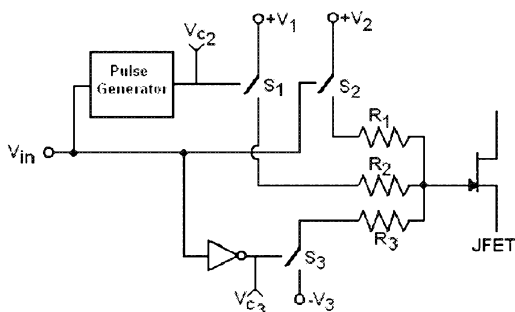
FIG. 3

(57) Abstract: A DC-coupled two-stage gate driver circuit for driving a junction field effect transistor (JFET) is provided. The
JFET can be a wide bandgap junction field effect transistor (JFET) such as a SiC JFET. The driver includes a first turn-on circuit,
a second turn-on circuit and a pull-down circuit. The driver is configured to accept an input pulse-width modulation (PWM) con-
trol signal and generate an output driver signal for driving the gate of the JFET.

GATE DRIVER FOR ENHANCEMENT-MODE AND DEPLETION-MODE WIDE BANDGAP SEMICONDUCTOR JFETS

[0001] This application claims the benefit of Provisional U.S. Patent Application Serial

No. 61/177,014, filed May 11, 2009, which is incorporated by reference herein in its

entirety.

[0002] TECHNICAL FIELD

[0003] The present invention relates generally to gate drivers and integrated circuits

including the same, and more particularly, to an n-channel junction field effect transistor

(JFET) based gate driver for enhancement-mode and depletion-mode wide bandgap

semiconductor JFETs.

[0004] BACKGROUND OF THE TECHNOLOGY

[0005] One application for wide bandgap junction field effect transistors (JFETs) is in

high voltage, high frequency power electronics. The exceptional device properties of

wide bandgap JFETs make these devices capable of replacing high voltage insulated gate

bipolar transistors (IGBTs) in a number of applications. Switching energy losses are one

of the main characteristics of power semiconductor switches that are compared when

selecting a device for new design. The transition speed is ultimately limited by the device.

However, the performance of the gate driver can impact this speed considerably.

[0006] The main function of the gate driver is to deliver/remove the necessary gate

charge required the by internal gate-source and Miller capacitance of the device in order

for the device to transition between states. The faster the gate driver can perform this task,

the faster the device will transition from off-state to the on-state, and from the on-state to

the off-state. Therefore it is important to use a properly designed gate driver circuit for maximum performance of the device within a practical system application.

[0007] The gate structure of the JFET poses two distinct requirements in order to drive the device into conduction. These requirements are similar to a combination of a metal oxide semiconductor field effect transistor (MOSFET) and a bipolar junction transistor (BJT). First a high peak transient current is recommended for quickly charging the gate capacitance, like that of a MOSFET. Second a small DC gate current is required to maintain conduction, similar to a BJT.

[0008] An AC coupled, BJT-like RC driver can be used for wide bandgap JFETs in most applications. A driver of this type is depicted in FIG. 1. This driver solution has proven to provide exceptional switching performance, but experiences duty factor and switching frequency limitations. The RC driver is composed of a paralleled resistor and bypass capacitor connected between the gate/base of a semiconductor switch and the output of a Pulse Width Modulated (PWM) IC or other pulse generating circuit.

[0009] The RC driver is capable of level shifting, setting a DC current limit, as well as providing the high peak transient current required by most power semiconductors for a fast turn-on. To consistently maintain maximum switching speeds, the bypass capacitor of the RC driver must be full discharged prior to the next switching event. The time to discharge is depended on the RC time constant of the RC driver. Therefore the maximum switching frequency and duty factor of the application is limited by the RC time constant of the RC driver.

[0010] Accordingly, there still exists a need for improved gate drivers for wide bandgap JFETs and, in particular, an active, DC coupled driver that can overcome the limitations of the RC driver.

[0011] SUMMARY

[0012] A two-stage gate driver circuit for driving a junction field effect transistor (JFET) having a gate, a source and a drain is provided which comprises:

an input for supplying a control pulse signal V_{in};

three resistors, R_1, R_2 and R_3, each having first and second terminals and being electrically coupled to the gate of the JFET by the second terminal;

a first turn-on circuit electrically coupled between the input and the first terminal of the resistor R_2;

a second turn-on circuit electrically coupled between the input and the first terminal of the resistor R_1; and

a pull-down circuit electrically coupled between the input and the first terminal of the resistor R_3.

[0013] A two-stage gate driver circuit for driving a junction field effect transistor (JFET) having a gate, a source and a drain is also provided which comprises:

an input for supplying a control pulse signal V_{in};

a first turn-on circuit;

a second turn-on circuit; and

a pull-down circuit,

wherein the first turn-on circuit, the second turn-on circuit and the pull-down circuit are electrically coupled between the input and the gate of the JFET in parallel.

[0014] These and other features of the present teachings are set forth herein.

[0015] BRIEF DESCRIPTION OF THE DRAWINGS

[0016] The accompanying drawings illustrate one or more embodiments of the invention and, together with the written description, serve to explain the principles of the invention.

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Wherever possible, the same reference numbers are used throughout the drawings to refer to the same or like elements of an embodiment.

[0017] FIG. 1 is a circuit diagram of an AC coupled RC gate driver.

[0018] FIG. 2 is a schematic representation of a VJFET modeled as a capacitance in parallel with a pn diode.

[0019] FIG. 3 is a circuit diagram of a DC-coupled two stage gate driver for wide-bandgap JFETs.

[0020] FIG. 4 is a circuit diagram of a DC-coupled two stage gate driver for wide-bandgap JFETs with feedback to a pulse generator circuit.

[0021] FIG. 5 is a circuit diagram of a DC-coupled two stage gate driver for wide-bandgap JFETs according to a further embodiment.

[0022] FIG. 6 is a circuit diagram of a DC-coupled two stage gate driver for wide-bandgap JFETs with feedback to a pulse generator circuit according to a further embodiment.

[0023] FIG. 7 is a circuit diagram showing a portion of the gate driver in operation during period t_1.

[0024] FIG. 8 is a circuit diagram showing a portion of the gate driver in operation during period t_2.

[0025] FIG. 9 is a circuit diagram showing a portion of the gate driver in operation during period t_3.

[0026] FIG. 10A-10F show operating waveforms for a two-stage JFET gate driver.

[0027] FIG. 11A is a circuit diagram of a dual driver IC being used to drive an enhancement-mode (EM) SiC JFET.

[0028] FIG. 11B are waveforms for the device of FIG. 11A.

[0029] FIG. 12A is a circuit diagram of a switching energy test circuit for single device testing.

[0030] FIG. 12B is a circuit diagram of a switching energy test circuit for bridge configuration testing.

[0031] FIG. 13 shows operating waveforms for AC-coupled drive in a single switch test circuit of FIG. 12A.

[0032] FIGS. 14A and 14B show switching energy measurements for a SiC JEFT (SJEP120R125) tested in a full phase leg using the test circuit of FIG. 12B.

[0033] FIGS. 15A and 15B are graphs showing switching energy versus load current at junction temperatures of 25° C and 150° C for two SiC JFETs (SJEP120R125 and SJEP120R063).

[0034] FIG. 16A is a schematic of an embodiment wherein dual driver circuits are used to drive an enhancement-mode (EM) SiC JFET.

[0035] FIGS. 16B-16E illustrate experimental results for the embodiment depicted in FIG. 16A.

[0036] FIG. 17A is a schematic of an embodiment wherein an IC driver and a transistor driver are used to drive an enhancement-mode (EM) SiC JFET.

[0037] FIGS. 17B-17E illustrate experimental results for the embodiment depicted in FIG. 17A.

[0038] FIG. 18A is a schematic of an alternative embodiment wherein an IC driver and a transistor driver are used to drive an enhancement-mode (EM) SiC JFET.

[0039] FIGS. 18B-18C illustrate experimental results for the embodiment depicted in FIG. 18A.

[0040] **<u>DETAILED DESCRIPTION</u>**

[0041] Various embodiments of the invention are now described in detail. Referring to the drawings, like numbers indicate like components throughout the views. As used in the description herein and throughout the claims that follow, the meaning of "a", "an", and "the" includes plural reference unless the context clearly dictates otherwise. Also, as used in the description herein and throughout the claims that follow, the meaning of "in" includes "in" and "on" unless the context clearly dictates otherwise.

[0042] The description will be made as to the embodiments of the present invention in conjunction with the accompanying drawings.

[0043] The transition speed of a JFET is ultimately limited by the device. However, the performance of the gate driver can impact this speed significantly. As set forth above, two main requirements must be satisfied by the gate driver: delivery/removal of dynamic gate charge; and sustainability of DC gate voltage and resulting gate-source current during conduction. The ability of the gate driver to quickly deliver/remove the necessary gate charge required by the internal gate-source and Miler capacitance of the device is the main factor that affects the time it takes for the device to transition between states. The gate drive should also be designed to efficiently maintain the steady state DC gate voltage and gate current required to maintain minimum $R_{DS(ON)}$ during conduction.

[0044] The AC (capacitor) coupled gate driver circuit interfaces the gate of the JFET to the output of a standard COTS MOSFET/IGBT gate driver ICs with a simple RC network to allow for a drop-in replacement of MOSFETs or IGBTs with a normally-off SiC JFET in a range of applications. While the AC coupled driver has proven to be an effective

means of driving an enhancement-mode (EM) SiC JFET, it can experience duty factor and switching frequency limitations.

[0045] FIG. 1 provides a schematic diagram of the AC-coupled drive. This particular gate driver uses a current limiting resistor R_{CL} to set the DC operating point in the "on" state by dropping the potential difference between the high level output of the gate driver IC and the required gate-source voltage of the SiC JFET at a specified I_{GFWD}. The bypass capacitor is used to rapidly deliver/remove the dynamic gate charge for a fast turn-on and turn-off. In a sense, the capacitor appears to overdrive the gate of the JFET, visible by the overshoot of the gate-source voltage as measured at the terminals. Overdriving the gate for a duration of < 200 ns with a maximum driver IC voltage of +15V connected to the gate through a low ohm resistor is acceptable and recommended for fast turn on. As the device is transitioning between a blocking state and conduction state, high peak currents from the gate drive are delivering the charge required by the input capacitance and not flowing through the gate-source diode. Once the input capacitance is fully charged steady state conditions will be regulated by the current limiting resistor. An additional low ohm resistor (typically 1-5 ohms) can be included in series with the bypass capacitor to dampen any observed gate ringing.

[0046] This type of driver can be used with unipolar or bipolar drive voltages. If used with a unipolar drive voltage, the bypass capacitor will provide some negative gate bias at turn-off to aid in reduced turn-off times and provide a degree of noise immunity for a limited duration of time. As MOSFETs and IGBTs are typically interfaced to a driver IC through a gate resistor, a simple change in resistor value and the addition of a bypass capacitor is all that is necessary to convert a standard MOSFET/IGBT drive to a SiC JFET drive in most power switching topologies.

[0047] The appropriate C_{BP} value is selected based on Q_g of the SiC JFET and its independent PWM/driver IC supply rail voltages. Parasitic circuit effects can influence the selection of C_{BP}, so one particular value is C_{BP} is not necessarily appropriate for all applications. Rather a range of C_{BP} values to be evaluated empirically is suggested to the user as a starting point and defined by the following expression:

$$\frac{2*Q_g}{V_{DD} - V_{GS}} \leq C_{BP} \leq \frac{4*Q_g}{V_{DD} - V_{GS}}$$

RCL is used to limit the continuous current flowing from the PWM/driver IC through the gate-source diode of the SiC JFET, thus setting the gate-source voltage. To avoid overdriving the gate of the JFET during steady state conduction, it is recommended that a positive gate-source bias of no more than +3.0 V be applied. The selection of R_{CL} requires the following information:

    a. V_O = Positive output voltage of the PWM/driver IC

    b. V_{GS} = Desired JFET gate-source voltage

    c. I_{GFWD} = Gate-source diode current at the desired gate-source voltage. I_{GFWD} can be estimated from Figure X of the datasheet.

The following expression is then used to calculate R_{CL}:

$$R_{CL} = \frac{V_O - V_{gs}}{I_{GFWD \, (@ \, Vgs)}} \, .$$

[0048] To consistently obtain the fastest switching performance possible, it is necessary for the bypass capacitor of the RC network to be fully discharged prior to the next switching event. The size of this capacitor depends on the specifics of the application and the driver IC. Any particular value may need more time to discharge than that available for certain combinations of switching frequency and duty factor. While no operational problems will result from not fully discharging this capacitor; slower turn-on transitions

will result as there is less voltage differential between the output of the driver IC and the capacitor voltage at the next turn-on event. Therefore additional DC-coupled gate driver designs that can operate over a wider range of switching frequencies and duty factors are necessary.

[0049] This gate-source and gate drain structure of the JFET device can be modeled as a capacitance in parallel with a pn diode as shown in FIG. 2. This device equivalent model is unique, and represents some characteristics of a MOSFET, and some characteristics of a BJT. The power JFET presents two main requirements for the gate driver: fast delivery/removal of dynamic charge for charging/discharging the total gate capacitance; and sustainability of the required steady state voltage/current requirements of the gate-source diode through the duration of the conduction state.

[0050] High frequency applications need a driver that is not dependent on an RC time constant for best performance. A two-stage, DC-coupled driver design has been developed specifically for the JFET. A two-stage, DC-coupled driver according to one embodiment is shown in FIG. 3. Other embodiments of the two-stage gate driver are depicted in FIGS. 4, 5 and 6. The driver can apply a high peak current pulse for supplying the required dynamic charge as quickly as possible for a fast turn-on and also maintain the steady state DC gate voltage/current to sustain conduction. The driver can be used to overdrive the gate during the turn-on transient. The two-stage driver developed allows for precise control of the overdrive conditions as well as the steady state condition.

[0051] The circuit shown in FIG. 3 accepts a single PWM control signal and generates a second pulse-width modulation (PWM) signal that is synchronized with the original control signal. The generated pulse drives the first turn-on stage which provides a high peak current source for quickly charging the device's gate and Miller (or gate to drain)

capacitance. The pulse width of this second control pulse lasts until the Miller

capacitance of the device is fully charged and the drain-source voltage is fully collapsed.

This second control pulse can be generated by an open or closed loop circuit.

[0052] The second PWM signal that is synchronized with the original control signal has a

much shorter pulse width. The generated pulse drives a first turn-on stage which controls

delivery of dynamic gate charge. Switch S_1 of the first stage connects a high peak current

source for quickly charging the device's gate and miller capacitance at turn-on. The

original control pulse is applied to the second turn-on stage, where switch S_2 supplies the

necessary steady state DC gate current required to maintain conduction. Current limiting

resistor R_1 is properly sized to set the forward gate current I_{GFWD} while stepping down the

voltage from the positive rail voltage to that required by the gate of the JFET. R_1 is sized

with the same approach used for the current limiting resistor in the AC-coupled RC drive

circuit. The complement of the user supplied PWM pulse controls the turn-off stage

which pulls the JFET gate low through a low ohm pull-down resistor R_3. This driver

approach can be realized in many ways; using discrete transistors, multiple driver ICs, or

a single dual driver IC. The method chosen will depend upon the required driver voltages,

transition times, and desired peak current supply.

[0053] The original control pulse is applied to the second turn-on stage which supplies

the necessary steady state DC gate current required to maintain conduction. A current

limiting resistor is properly sized to set the forward gate current while stepping down the

voltage from the positive rail voltage to that required by the gate of the JFET. When the

user input PWM signal transitions to the logic state indicating the desired t_{off} duration of

the JFET, a pull-down circuit pulls the gate to either the switch common or a negative

voltage through a small pull-down resistor.

[0054] Depending upon the transistor technology used (i.e., FET or bipolar) the inverting circuit may not be necessary to drive the pull-down circuit. FIG. 4 shows a DC-coupled two stage gate driver for wide bandgap JFETs with feedback to a pulse generator circuit. FIG. 5 is a circuit diagram of a DC-coupled two stage gate driver for wide-bandgap JFETs according to a further embodiment. FIG. 6 is a circuit diagram of a DC-coupled two stage gate driver for wide-bandgap JFETs with feedback to a pulse generator circuit according to a further embodiment. As shown in FIGS. 4-6, the two-stage gate driver is divided into three sections.

[0055] FIGS. 10A-10F provide corresponding waveforms describing the complete gate driver operation. During the period t_1 the first turn-on circuit is active. A user input, V_{in}, shown in FIG. 10A, is accepted and the pulse generator circuit derives a second control pulse, Vc_2, which is shown in FIG. 10B. Vc_2 drives a switch that connects the gate of the JFET to a high peak current source through a small damping resistor R_2. The waveform for the gate current (I_G), which is shown in FIG. 1F, illustrates that for the duration of t_1 the gate current is high, $\leq 1A$. After the drain-source voltage, V_{DS}, which is shown in FIG. 10E, collapses the first turn-on circuit is turned off.

[0056] The duration of time t_1 can be manually adjusted in the case of the preferred embodiment or automatically adjusted based on feedback from the JFET. The second turn-on circuit is also turned on at the start of t_1. However, the small current contribution of this stage of the driver is minimal compared to that of the first turn-on stage. After the first turn-on circuit is deactivated the second turn-on circuit regulates the DC gate current, ($\leq 1A$) for the remainder of the conduction period. From FIG. 10F, it can be seen that I_G is reduced to a much lower value at the start of t_2. The end of the t_2 period is determined by the user input voltage. The gate pull-down circuit is activated at the end of t_2 starting period t_3. During this period the JFET is to transition to a blocking state and remain

blocking until the next input pulse is received. During t_3 the pull-down circuit holds the gate of the device at either switch common or a negative voltage for the duration of the blocking state.

[0057] FIG. 7 is a circuit diagram showing a portion of the gate driver in operation during period t_1. FIG. 8 is a circuit diagram showing a portion of the gate driver in operation during period t_2. FIG. 9 is a circuit diagram showing a portion of the gate driver in operation during period t_3.

[0058] <u>Exemplary Embodiments</u>

[0059] A circuit is provided which comprises:

    a wide bandgap junction field effect transistor (JFET); and

    a DC-coupled, two-stage driver, wherein the driver comprises:

        a first turn-on circuit;

        a second turn-on circuit; and

        a pull-down circuit;

    wherein the driver is configured to accept an input pulse-width modulation (PWM) control signal and generate an output driver signal for driving the gate of the wide bandgap JFET.

[0060] The period of the user input control pulse can be equal to the sum of the pulse duration, t_{on} that indicates the time in which the JFET is to be in conduction and the pulse duration, t_{off} that indicates the time in which the JFET is to be blocking.

[0061] The first turn-on circuit can comprise a pulse generator circuit and a high peak current source. The pulse generator circuit can accept the user input PWM control signal and generate a second control pulse. The output can be in sync with the user input pulse but with ≤ 15% of the pulse width of the user input pulse. The first turn-on circuit can be

connected to a positive rail voltage $+V_1$. The pulse width can be adjustable. For example, the pulse width can be manually adjusted or automatically adjusted based on feedback from the JFET.

[0062] The first turn-on circuit can connect the gate of the wide-bandgap JFET to a high peak current source through a low value (e.g., < 10 Ohms) damping resistor.

[0063] The first turn-on circuit can be active for ≤ 15% of the t_{on} duration of the user input control pulse as determined by the pulse generator circuit.

[0064] The second turn-on circuit can connect the gate of the transistor to a positive voltage rail, $+V_2$, by a current limiting resistor (e.g., < 2 kOhms). The second turn-on circuit can be active for the full t_{on} duration of the user input control pulse.

[0065] The pull-down circuit can connect the gate of the transistor to a circuit common or negative voltage, $-V_3$, rail through a low damping resistor (e.g., < 100 Ohms). The pull-down circuit can include an inverting circuit. The pull-down circuit can be active for the t_{off} duration of the user input voltage.

[0066] The positive rail voltages $+V_1$ and $+V_2$ can be separate positive voltages or connected to the same positive voltage rail.

[0067] **Experimental**

[0068] A dual driver IC was used to drive an enhancement-mode (EM) SiC JFET. This approach is depicted in FIG. 11A. In this circuit, *driver A* controls the dynamic charging conditions while *driver B* controls the steady state gate conditions. The pulse width of the input to *drive A* can be limited to ≤ 200 ns. Since the purpose of *driver A* is to deliver a high peak current for charged the devices input capacitance, its pulse width should not exceed the turn-on time of the device by more than 100 ns. Again, high peak current supplied during the turn-on transient is internally distributed so that it delivers charge to

the input capacitance and is not simply flowing through the gate-source diode. This results in an overshoot of the gate voltage greater than +3 V for a precisely limited time. However, once the input capacitance is fully charged and the drain voltage fully collapses the gate voltage will continue to rise, allowing high current to flow to the gate-source diode until *driver A* is turned off. It is recommended that the time difference between the end of the transition period and the time at which *driver A* is turned off be minimized as much as possible. For any duration of time that *driver A* remains active during the conduction period, excessive power loss will be dissipated by the gate and could result in damage to the gate if this duration lasts longer than 100 ns.

[0069] FIG. 11B presents some experimental results for driving a SiC JFET using the dual drive circuit depicted in FIG. 11A. The SiC JFET used was SJEP120R125, manufactured by SemiSouth Laboratories, Inc. Gate drive voltages of +15 V and -10 V were supplied and resistors sized accordingly (i.e., $R_1 = R_3 = 5$ ohms and $R_2 = 135$ ohms). *Driver A* pulse width was set to 100 ns.

[0070] FIG. 11B shows $I_{GS(PK)} = 2A$ at $V_{GS} = +6V$ during the turn-on transition. Once *driver A* turns off and *driver B* takes control, the steady state conditions were measured at $V_{GS} = +3V$ and $I_{GS} = 100mA$.

[0071] Switching energy loss is one of the major performance factors used in comparing different semiconductor transistors for new designs. Minimizing this number is a priority for high switching frequency applications as this type of loss can become a significant portion of the total device losses. The normally-off SiC JFET is measured according to the same standard as MOSFET/IGBTs. A standard, double-pulse, clamped inductive load test circuit is used to observe the energy loss during both turn-on and turn-off. These measurements have also been conducted based on different drive voltage recommendations (i.e. unipolar or bipolar drive) as well as switch configurations (i.e.

single device or bridge configuration). Measurements have also been conducted at elevated temperature and show that there is very little change in switching energy as junction temperature increases.

[0072] For single device applications, boost and buck converters for example, a unipolar drive voltage is typically sufficient for driving an EM SiC JFET. In these types of circuits current is commutated between the main power transistor and a free-wheeling diode. While each application/design can present a different set of conditions, experimental results have thus far proven that the use of a negative rail is not usually needed in single switch applications. The use of the AC-coupled, RC driver has also proven to be sufficient for most single switch applications with the bypass capacitor providing some negative bias at turn-off (duration of negative bias based on RC time constant) to aid in a fast turn-off and provide some degree of noise immunity for a limited amount of time. The switching losses for a SiC JFET (i.e., SJEP120R125) have been observed under a variety of conditions. A +15V unipolar driver IC as well as a +15V/-10V bipolar driver in combination with the AC-coupled, RC driver interface was evaluated using the test circuit shown in FIG. 12A. The duty factor was adjusted to observe the difference in switching losses when the bypass capacitor was allowed to fully discharge and partially discharge. Table 1 lists the resulting turn-on losses for each case. As expected, the turn-on energy loss can be up to 2x greater when the bypass cap is not allowed to fully discharge prior to the next switching event. These results may or may not be sufficient based on the needs of a specific application and may require the use of the two-stage driver with a modest negative rail to achieve higher switching frequencies or higher duty factors.

[0073] The test circuit for monitoring the switching energy based on the conditions was modified to reflect the conditions experienced in applications using a bridge configuration

as shown in FIG. 12B. For these applications, shoot through can be a real problem and thus noise immunity must be evaluated. A negative drive voltage is recommended for turn-off to aid in noise immunity and prevent shoot thru caused by the "Miller effect". Similar to MOSFETs and IGBTs there are three common approaches for preventing a positive spike on the gate voltage from reaching the device's threshold voltage:

     a. negative drive voltage on gate during turn-off;

     b. capacitive clamp connected closely at gate-source terminals;

     c. limit the dV/dt during switching.

[0074] If the lowest possible switching losses are required, increasing the voltage differential between the turn-off voltage and the threshold voltage by adding or increasing the amount of negative voltage is recommended as a first approach. This is an easy solution and the only solution that does not impact the switching performance of either the high-or low-side device. However, as with all field-controlled power devices there is a limit to the amount of negative voltage that can be applied to the gate of the SiC JFET. If a positive gate spike is still evident after the maximum negative voltage is applied then another approach must be taken. A capacitive clamp connected tightly across the gate-source terminals of each device will provide a secondary source to pull necessary displacement current. This will reduce the positive spike at the gate; however, this method will require the gate driver to deliver more gate charge during each turn-on switching event. A modest increase in gate drive power and possibly a slightly slower turn-on speed will be observed. The last option is a downward adjustment of the dV/dt by adjusting a series gate resistance of the gate drive. This will reduce the peak current through the Miller capacitance of both switches and reduce the probability of shoot-through through the blocking switch. This third option will obviously result in slower

switching than the maximum possible; therefore the designer must way the trade-offs for each specific application.

[0075] FIGS. 14A and 14B show switching energy measurements for a SiC JEFT (SJEP120R125) tested in a full phase leg using the test circuit of FIG. 12B.

[0076] Table 1 includes the switching losses observed using the test set up described by FIG. 12B using the DC-coupled gate driver.

Table 1: Switching Energy Losses for SJEP120R125 (Conditions: V_{DS} = 600V, I_D = 12A)

Device Configuration	Test Circuit	Gate Driver	CBP Discharge	E_{ON} (us)	E_{OFF} (us)
Single Switch	FIG. 12A	Unipolar +15V; AC-coupled drive	100%	75	38
Single Switch	FIG. 12A	Unipolar +15V; AC-coupled drive	75%	82	38
Single Switch	FIG. 12A	Unipolar +15V; AC-coupled drive	58%	105	38
Single Switch	FIG. 12A	Unipolar +15V; AC-coupled drive	30%	149	38
Single Switch	FIG. 12A	Bipolar +15V / -10V ; AC-coupled drive	100%	57	35
Single Switch	FIG. 12A	Bipolar +15V / -10V; DC-coupled drive	N/A	52	45
Bridge	FIG. 12B	Bipolar +15V / -10V; 10nF capacitive clamp; DC-coupled drive	N/A	121	59

[0077] FIGS. 15A and 15B presents measured switching energy losses for two SiC JFETS (i.e., SJEP120R125 and SJEP120R063, both manufactured by SemiSouth Laboratories, Inc.) as a function of load current and junction temperature. As shown, there is approximately a 10% increase in total switching energy between 25 °C and 150 °C junction temperature.

[0078] Even though the enhancement-mode SiC JFET is a new device technology, many of the same design and layout tips valid for other types of high frequency power transistors are still applicable for SiC JFET designs. Care must always be taken when

creating PCB layouts for power converters such that additional coupling capacitances are not introduced, the device is not mounted to close to switching IC and magnetic components, symmetrical layouts are used when paralleling devices, and adequate cooling/heat sinking is obtained.

[0079] Gate ringing can be caused by feedback of high frequency noise through the Miller capacitance of the device or ground bounce cause by improper separate of signal and power grounds. Layouts should designed to properly separate power grounds from signal ground with a common connection between the two made at a single point. Also the proper use of ground planes can help shield the gate from the drain as well as other high frequency circuit connections. Ferrite beads connected as close as possible to the gate terminal of the SiC JFET may also be used to reduce voltage spikes at the gate. A small, low ohm external gate resistor may also be sufficient, as used in the design examples presented in this document. The use of a series R-C snubber connected directly across the main DC voltage bus has proven to reduce the amount of high frequency noise feedback through the miller capacitance. Lastly, gate drivers and gate turn-off components should always be connected as close as possible to the gate terminal of the device to reduce all of the aforementioned contributors of gate noise.

[0080] The specifics of the application can be evaluated to determine the best gate driver approach. The use of a dual driver IC is the simplest approach. However, two separate driver ICs can be used to achieve a desired peak current rating. Derivation of the overdrive pulse should be precise and closely match the turn-on speed of the transistor to minimize unnecessary gate power dissipation.

[0081] As with any low threshold device, noise immunity is an important concern. A negative turn-off voltage is recommended when using EM SiC JFETs in a bridge or series configuration. As with MOSFET/IGBTs the JFET can also experiences false triggering

due to the "miller effect". However, by increasing the voltage difference between the turn-off voltage and the gate threshold voltage this adverse effect can be minimized. If positive gate voltage spikes are still a problem then adding a small capacitive clamp across the gate-source terminals is recommended to limit the effect of high dV/dt on the gate of the opposing JFET.

[0082] **Additional Embodiments**

[0083] A circuit is also provided which comprises: a wide bandgap junction field effect transistor (JFET) and a DC-coupled, two-stage driver. The driver comprises: an upper turn-on driver (U9) circuit; a lower turn-on driver (U11) circuit; and a logic gate U12 for receiving a signal from its input and generating a brief "turn-on" pulse for the upper turn-on driver (U9). The upper and lower drivers are configured to accept an input pulse-width modulation (PWM) control signal and generate an output driver signal VG for driving the gate of the wide bandgap JFET.

[0084] According to this embodiment, the upper turn-on driver comprises a turn-on driver U9, a first resistor (5) and a first diode D1, with the output of the turn-on driver U9 coupled to the first terminal of the first resistor, the second terminal of the first resistor coupled to the anode terminal of the first diode D1, and the cathode of the first diode D1 forming the output of the upper driver circuit. The lower turn-on driver comprises a turn-on driver U11, a second resistor (100) having a first terminal and a second terminal, a second diode D2 having an anode and a cathode, and a third resistor having a first terminal and a second terminal. The output of the turn-on driver U11 is coupled to the first terminal of the second resistor and the cathode of the second diode D2. The anode of the second diode D2 is coupled to the first terminal of the third resistor. The second terminal of the third resistor is coupled to the second terminal of the third resistor to form the output of the lower driver circuit. The output of the upper driver circuit and the

output of the lower driver circuit are connected together to form the input to the wide bandgap junction field effect transistor (JFET).

[0085] Dual driver circuits were used to drive an enhancement-mode (EM) SiC JFET. This approach is depicted in FIG. 16A. In this circuit, the output of the logic gate U12 is connected to the input of the upper turn-on driver U9 and the input of the lower turn-on driver U11.

[0086] FIG. 16B shows the Dead Time of the input VA of the logic gate U12 and the output VB of the logic gate U12. The waveforms of the output of the upper turn-on driver U9 is shown in FIG. 16C as V1 and the waveforms of the output of the lower turn-on driver U11 is shown in FIG. 16C as V2.

[0087] FIG. 16C shows the upper turn-on driver U9 causes an extra time delay compared to the output of the lower turn-on driver U11. This delay is too far behind a "maintain ON" pulse from the lower turn-on driver U11. One effective approach which can be employed to reduce the time delay comprises adding a 1.5 K resistor and a 120 pF capacitor RC delay circuit at the input to the lower turn-on driver U11 to align the V1 and V2 as shown in FIG. 16D. The value of the resistor and capacitor of the RC delay circuit can be chosen such that the output of the upper turn-on driver U9 and the output of the lower turn-on driver U11 will go high simultaneously.

[0088] In FIG. 16D, the output of the upper turn-on driver U9 and the output of the lower turn-on driver U11 are shown going high simultaneously. When the third resistor (6.8 ohm shown) and the second diode D2 were not used as depicted in FIG. 16D, a slow turn-off is observed. In order to speed up the turn-off, the third resistor (6.8 ohm shown) and the second diode D2 were used to create a faster turn-off. The effect of adding the speed up circuit is shown in FIG. 16E.

[0089] A circuit is also provided which comprises: a wide bandgap junction field effect transistor (JFET) and a DC-coupled, two-stage driver. According to this embodiment, the driver comprises: a logic circuit for receiving a pulse-width modulation (PWM) control signal and generating an enabling signal and an inverse PWM signal; an IC driver (509) circuit having the PWM input signal and the enabling signal input from the logic circuit (LOGIC) and a transistor driver circuit having an input of the inverse PWM signal. The IC driver (509) circuit and the transistor driver circuit are configured to accept the input pulse-width modulation (PWM) control signal and generate an output driver signal VG for driving the gate of the wide bandgap JFET.

[0090] The logic circuit (LOGIC) according to this embodiment comprises: a first NOR gate, a second NOR gate, a first capacitor having a first terminal and a second terminal, a second diode (1N914) having an anode and a cathode, a fourth resistor 500 having a first terminal and a second terminal, a third NOR gate, and a fourth NOR gate. Each of the first, second, third and fourth NOR gate has a first input, a second input and an output. The detailed circuit layout is depicted in the FIG. 17A.

[0091] The IC driver (509) circuit comprises a 509 Driver IC and a first resistor 1. The 509 Driver IC has a positive power supply, a negative power supply, an input terminal receiving the PWM control signal, an input for receiving enabling signal and an output. The input for receiving enabling signal receives the enabling signal from the output of the logic circuit (LOGIC). The input terminal receives the PWM control signal. The output of the 509 Driver IC is coupled to the first terminal of the first resistor and the second terminal of the first resistor is coupled to the gate terminal of the JFET.

[0092] The transistor driver circuit comprises a zener diode D1 having an anode and a cathode, a second resistor 100 having a first terminal and a second terminal, a transistor (2N3906) having a base terminal, an emitter terminal and a collector terminal, and a third

resistor 15 having a first terminal and a second terminal. The anode of the zener diode

D1 forms the input of the transistor driver circuit. The cathode of the zener diode D1 is

connected to the first terminal of the second resistor 100. The second terminal of the

second resistor 100 is connected to the base terminal of the transistor. The emitter

terminal of the transistor is connected to the positive power supply of the transistor driver

circuit. The collector terminal of the transistor is connected to the first terminal of the

third resistor. The second terminal of the third resistor is connected to the output of the

IC driver (509) circuit and the gate terminal of the JFET.

[0093] The output of the IC driver (509) circuit and the output of the transistor driver

circuit are connected together to form the input to the wide bandgap junction field effect

transistor (JFET).

[0094] A driver arrangement as set forth above was used to drive an enhancement-mode

(EM) SiC JFET. This approach is depicted in FIG. 17A. In this circuit, the output of the

logic circuit (LOGIC) is connected to the enabling signal input of the IC driver circuit and

the inverse of PWM signal output of the logic circuit (LOGIC) is connected to the input

of the transistor driver circuit. FIG. 17B shows double pulse waveforms of the voltage

between the gate terminal and the source terminal of the JFET, and the current flowing

into the gate of the JFET. FIG. 17C shows the turn-on voltage between the gate and

source terminals of the JFET and the turn-on pulse current flow into the gate of the JFET,

showing that the current peaked at 5.5A. Therefore, at least one high current driver, such

as the IC driver, should be included for both turn-on and turn-off. When viewed on an

enlarged time scale, a ripple effect is shown at the turn-on and turn-off edges. FIG. 17D

shows the double pulse current flow into the gate of the JFET. It shows the turn-on and

turn-off edges are swift and clean. The "stay-on" current can be provided by a lower

current transistor powered from a lower power supply. Such an arrangement is used to

economize on components and reduce the losses in the associated gate resistor. FIG. 17E shows the turn-on voltage between the gate and source terminals of the JFET, and the turn-on pulse current flow into the gate of the JFET. When viewed on an enlarged time scale, a ripple effect is shown at the turn-on and turn-off edges.

[0095] Another similar two stage driver circuit is shown in FIG. 18A. Only the components around the JFET were further added and modified. FIG. 18B shows the turn-on voltage between the gate and source terminal of the JFET and the turn-off current flowing into the gate terminal of the JFET. FIG. 18C shows the turn-off voltage between the gate and source terminal of the JFET and the turn-off current flowing into the gate terminal of the JFET. The turn-off waveforms show significant ripple. While not wishing to be bound by theory, it is believed that the reason for such ripple may be associated with high dV/dT false triggering of the logic circuit due to its "sky-wiring".

[0096] The foregoing description of the exemplary embodiments of the invention has been presented only for the purposes of illustration and description and is not intended to be exhaustive or to limit the invention to the precise forms disclosed. Many modifications and variations are possible in light of the above teachings.

[0097] The embodiments were chosen and described in order to explain the principles of the invention and their practical application so as to enable others skilled in the art to utilize the invention and various embodiments and with various modifications as are suited to the particular use contemplated. Alternative embodiments will become apparent to those skilled in the art to which the present invention pertains without departing from its spirit and scope. Accordingly, the scope of the present invention is defined by the appended claims rather than the foregoing description and the exemplary embodiments described therein.

REFERENCES

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[2] G. Schmitt, R. Kennel, and J. Holtz, " Voltage Gradient Limitation of IGBTs by Optimized Gate-Current Profiles," Power Electronics Specialists Conference, 2008. PESC 2008, pp. 3592 – 3596 (June 15-19, 2008).

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WHAT IS CLAIMED IS:

1. A two-stage gate driver circuit for driving a junction field effect transistor (JFET) having a gate, a source and a drain, comprising:

an input for supplying a control pulse signal V_{in};

three resistors, R_1, R_2 and R_3, each having first and second terminals and being electrically coupled to the gate of the JFET by the second terminal;

a first turn-on circuit electrically coupled between the input and the first terminal of the resistor R_2;

a second turn-on circuit electrically coupled between the input and the first terminal of the resistor R_1; and

a pull-down circuit electrically coupled between the input and the first terminal of the resistor R_3.

2. The two-stage gate driver circuit of Claim 1, wherein the control pulse signal V_{in} is configured to have a pulse duration, t_{on}, and a pulse-off duration, t_{off}, such that in the pulse duration t_{on}, the JFET is in a conduction state, while the JFET is in a blocking state in a pulse-off duration t_{off}.

3. The two-stage gate driver circuit of Claim 2, wherein the first turn-on circuit comprises:

a switch S1 having a gate, a source electrically coupled to the first terminal of the resistor R2 and a drain electrically coupled to a first current source for providing a positive voltage $+V_1$; and

a pulse generator electrically coupled between the input and the gate of the switch S1.

4. The two-stage gate driver circuit of Claim 3, wherein the second turn-on circuit

comprises a switch S2 having a gate electrically coupled to the input, a source electrically coupled to the first terminal of the resistor R1 and a drain electrically coupled to a second current source for providing a positive voltage $+V_2$.

5. The two-stage gate driver circuit of Claim 4, wherein the first and second current sources are corresponding to a single current source or two different current sources.

6. The two-stage gate driver circuit of Claim 4, wherein the pull-down circuit comprises a switch S3 having a gate electrically coupled to the input, a source electrically coupled to a third current source for providing a negative voltage $-V_3$ and a drain electrically coupled to the first terminal of the resistor R3.

7. The two-stage gate driver circuit of Claim 6, wherein the pull-down circuit further comprises an inverter electrically coupled between the input and the gate of the switch S3.

8. The two-stage gate driver circuit of Claim 7, wherein when the control pulse signal V_{in} is supplied:

the pulse generator responsively generates a corresponding control pulse signal, V_{c2}, having a pulse duration, t1, that turns on the switch S1 for the pulse duration t1;

the control pulse signal V_{in} turns on the switch S2 for the pulse duration t_{on} and turns off the switch S2 for the pulse duration t_{off}, respectively; and

the control pulse signal V_{in} turns off the switch S3 for the pulse duration t_{on} and turns on the switch S3 for the pulse duration t_{on}, respectively.

9. The two-stage gate driver circuit of Claim 8, wherein the generated control pulse signal V_{c2} is in synchronization with the control pulse signal and wherein the pulse duration, t_1 of the generated control pulse signal V_{c2} is equal to or less than 15% of the

pulse duration t_{on} of the control pulse signal V_{in}.

10. The two-stage gate driver circuit of Claim 9, wherein the pulse duration t_1 of the generated control pulse signal V_{c2} is adjustable manually.

11. The two-stage gate driver circuit of Claim 9, wherein, the pulse duration t_1 of the generated control pulse signal V_{c2} is adjustable automatically in accordance with a feedback signal, V_{FB}, from the JFET.

12. A two-stage gate driver circuit for driving a junction field effect transistor (JFET) having a gate, a source and a drain, comprising:

an input for supplying a control pulse signal V_{in};

a first turn-on circuit;

a second turn-on circuit; and

a pull-down circuit,

wherein the first turn-on circuit, the second turn-on circuit and the pull-down circuit are electrically coupled between the input and the gate of the JFET in parallel.

13. The two-stage gate driver circuit of Claim 12, wherein the control pulse signal V_{in} is configured to have a pulse duration, t_{on}, and a pulse-off duration, t_{off}, such that the JFET is in a conduction state in the pulse duration t_{on}, while the JFET is in a blocking state in the pulse-off duration t_{off}.

14. The two-stage gate driver circuit of Claim 13, wherein the first turn-on circuit comprises:

a switch S1 having a gate, a source electrically coupled to the gate of the JFET through a resistor R2 and a drain electrically coupled to a first current source for providing a positive voltage $+V_1$; and

a pulse generator electrically coupled between the input and the gate of the switch

S1.

15. The two-stage gate driver circuit of Claim 14, wherein the pulse generator is configured such that when the control pulse signal V_{in} is supplied, the pulse generator responsively generates a corresponding control pulse signal, V_{c2}, that is in synchronization with the control pulse signal V_{in}.

16. The two-stage gate driver circuit of Claim 15, wherein the generated control pulse signal V_{c2} has a pulse duration, t_1, that is equal to or less than 15% of the pulse duration t_{on} of the control pulse signal V_{in}.

17. The two-stage gate driver circuit of Claim 16, wherein the pulse duration t_1 of the generated control pulse signal V_{c2} is adjustable manually.

18. The two-stage gate driver circuit of Claim 16, wherein, the pulse duration t_1 of the generated control pulse signal V_{c2} is adjustable automatically in accordance with a feedback signal, V_{FB}, from the JFET.

19. The two-stage gate driver circuit of Claim 14, wherein the second turn-on circuit comprises a switch S2 having a gate electrically coupled to the input, a source electrically coupled to the gate of the JFET through a resistor R1 and a drain electrically coupled to a second current source for providing a positive voltage $+V_2$.

20. The two-stage gate driver circuit of Claim 19, wherein the pull-down circuit comprises:

a switch S3 having a gate, a source electrically coupled to a third current source for providing a negative voltage $-V_3$ and a drain electrically coupled to the gate of the JFET through a resistor R3; and

an inverter electrically coupled between the input and the gate of the switch S3.

21. The two-stage gate driver circuit of Claim 13, wherein the first turn-on circuit is electrically coupled between a first current source and the gate of the JFET through a resistor R2, wherein the first current source is adapted for providing a positive voltage, $+V_1$.

22. The two-stage gate driver circuit of Claim 21, wherein in operation, when the control pulse signal V_{in} is in the pulse duration t_{on}, the first turn-on circuit is turned on for a duration, t_1, that is equal to or less than 15% of the pulse duration t_{on} of the control pulse signal V_{in}, while the first turn-on circuit is turned off for the pulse-off duration t_{off} when the control pulse signal V_{in} is in the pulse-off duration t_{off}.

23. The two-stage gate driver circuit of Claim 22, wherein the second turn-on circuit is electrically coupled between a second current source and the gate of the JFET through a resistor R1, wherein R1 > R1, and wherein the second current source is adapted for providing a positive voltage, $+V_2$.

24. The two-stage gate driver circuit of Claim 23, wherein the first and second current sources are corresponding to a single current source or two different current sources.

25. The two-stage gate driver circuit of Claim 23, wherein in operation, when the control pulse signal V_{in} is in the pulse duration t_{on}, the second turn-on circuit is turned on for the pulse duration t_{on}, while the second turn-on circuit is turned off for the pulse-off duration t_{off} when the control pulse signal V_{in} is in the pulse-off duration t_{off}.

26. The two-stage gate driver circuit of Claim 23, wherein the pull-down circuit is electrically coupled between a third current source and the gate of the JFET through a resistor R3, wherein the third current source is adapted for providing a negative voltage $-V_3$.

27. The two-stage gate driver circuit of Claim 26, wherein the pull-down circuit comprises an inverter electrically coupled between the input and the resistor R3.

28. The two-stage gate driver circuit of Claim 27, wherein the pull-down circuit is turned off for the pulse duration t_{on} when the control pulse signal V_{in} is in the pulse duration t_{on} and wherein the pull-down circuit is turned on for the pulse duration t_{off} when the control pulse signal V_{in} is in the pulse-off duration t_{off}.

29. The two-stage gate driver circuit of Claim 1, wherein the JFET is a wide bandgap JFET or a SiC JFET.

30. The two-stage gate driver circuit of Claim 12, wherein the JFET is a wide bandgap JFET or a SiC JFET.
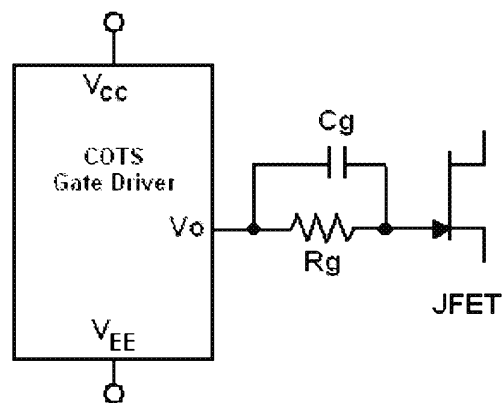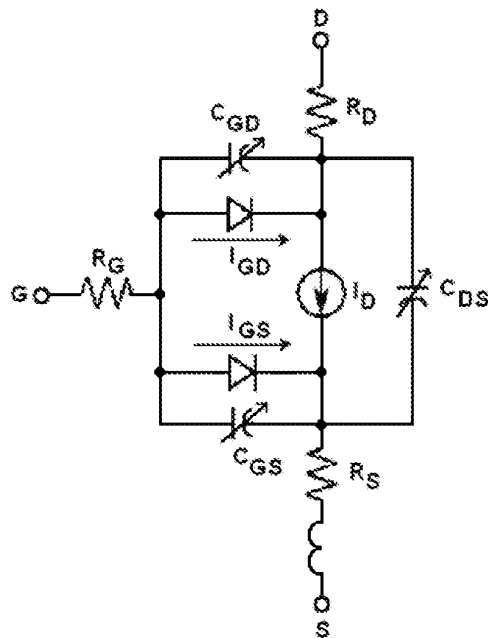
FIG. 1

FIG. 2

FIG. 3

FIG. 4

FIG. 5

FIG. 6

FIG. 7

FIG. 8

FIG. 9

FIG. 10

FIG. 11A

FIG. 11B

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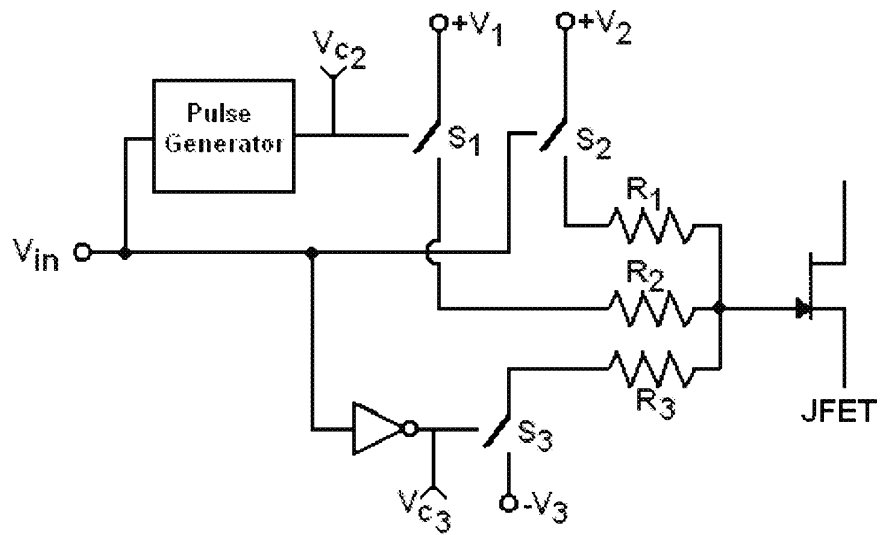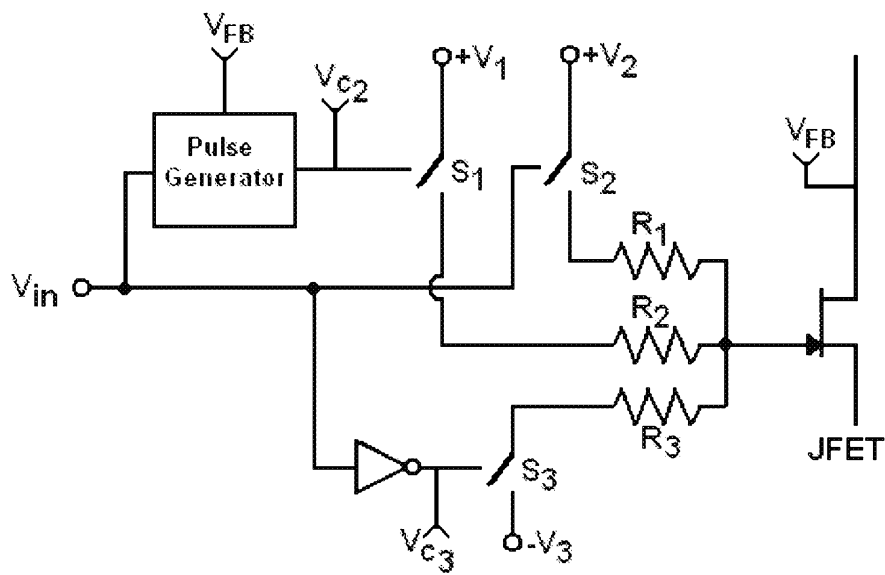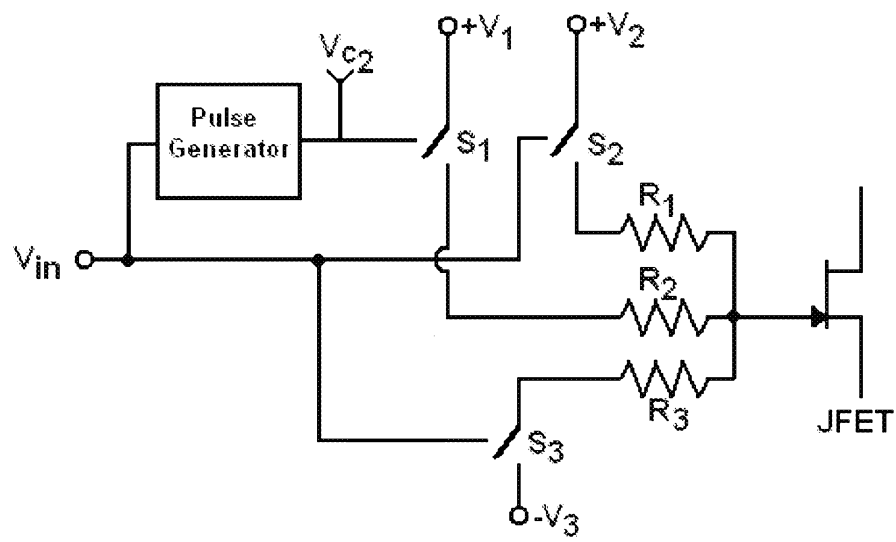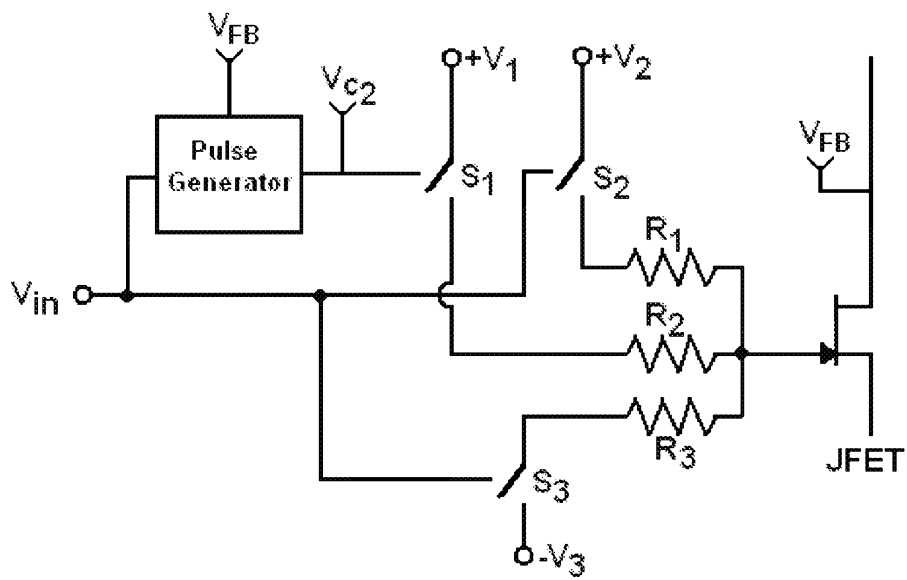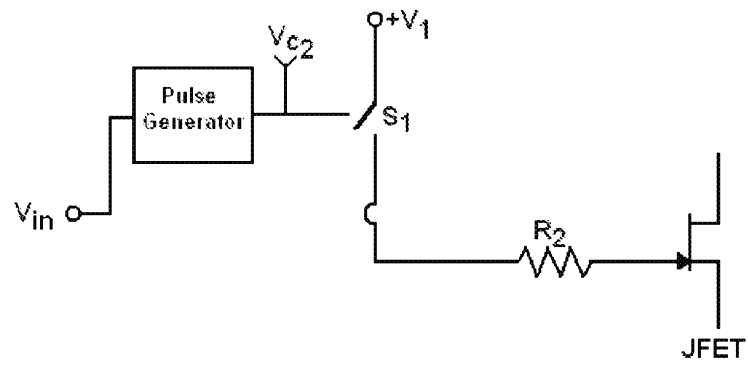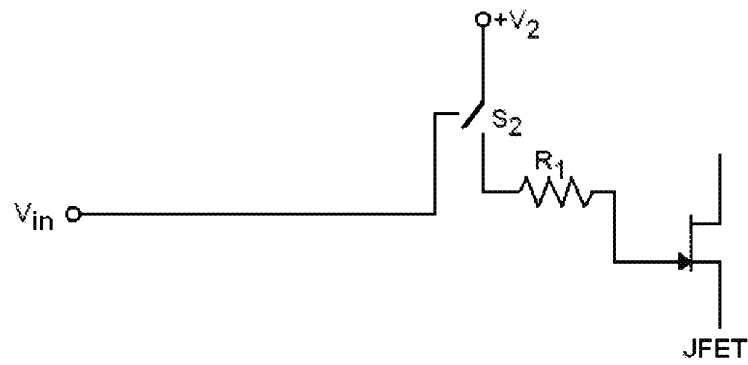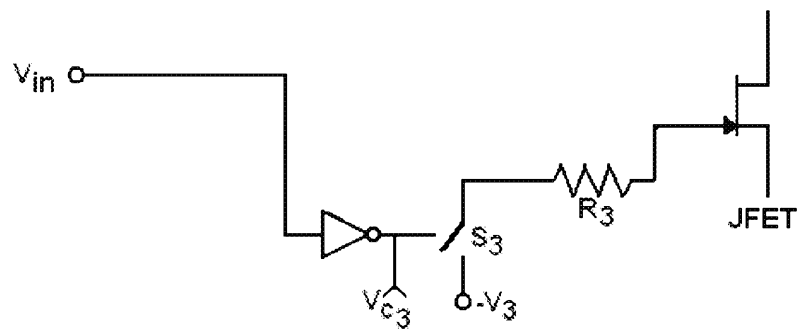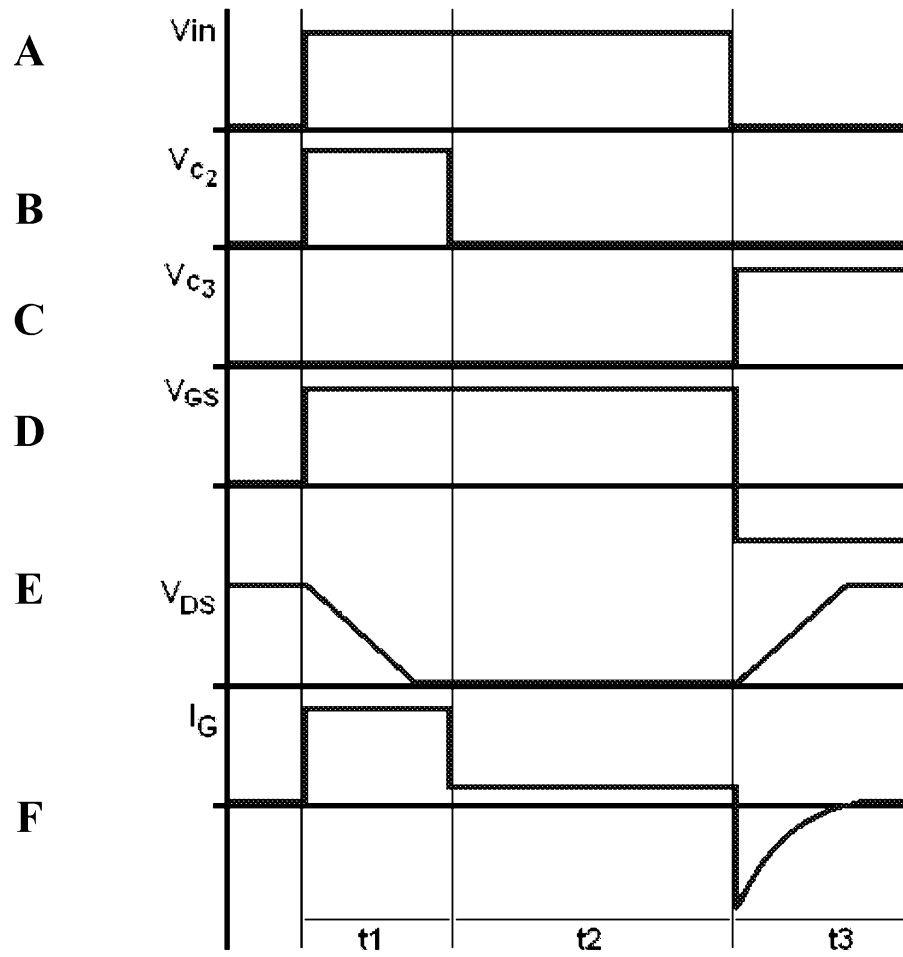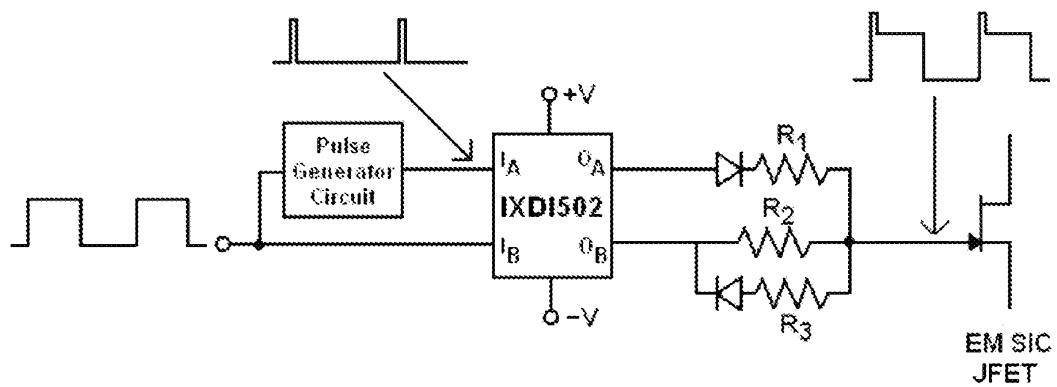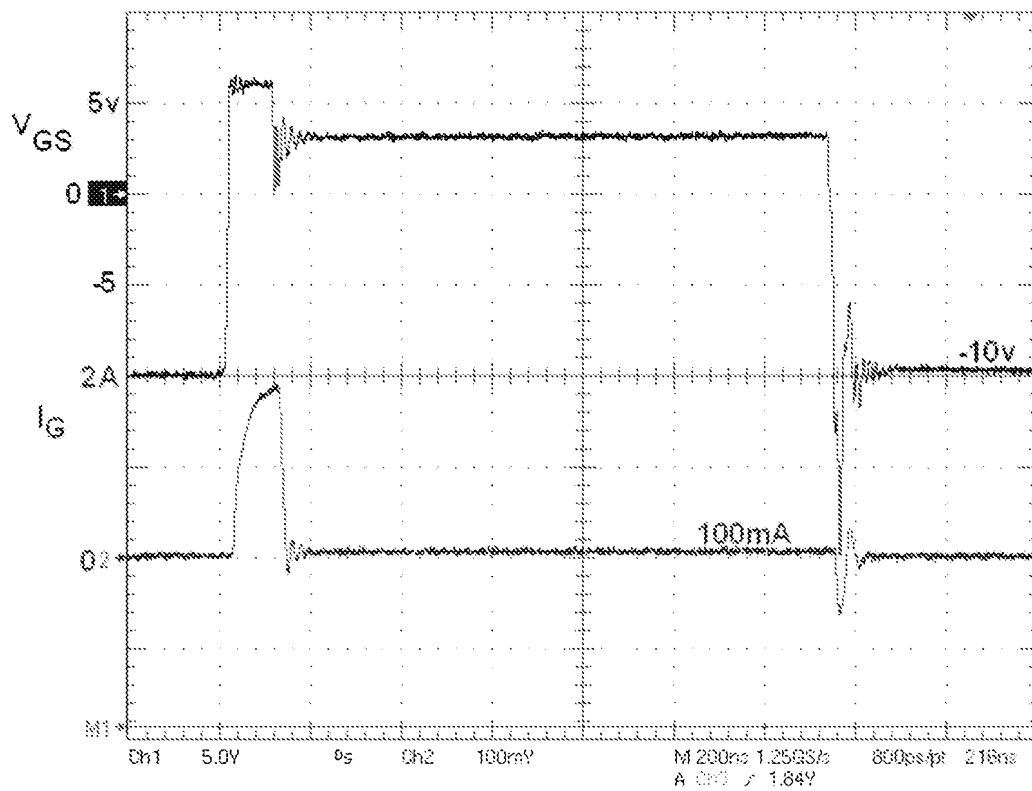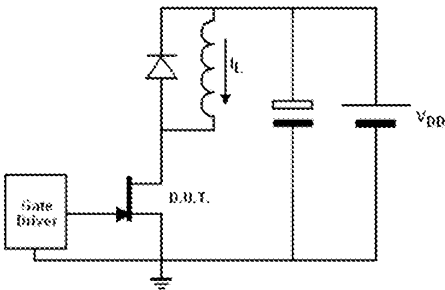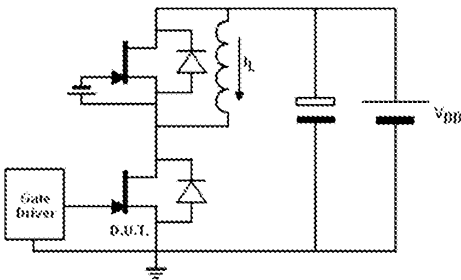
FIG. 12A
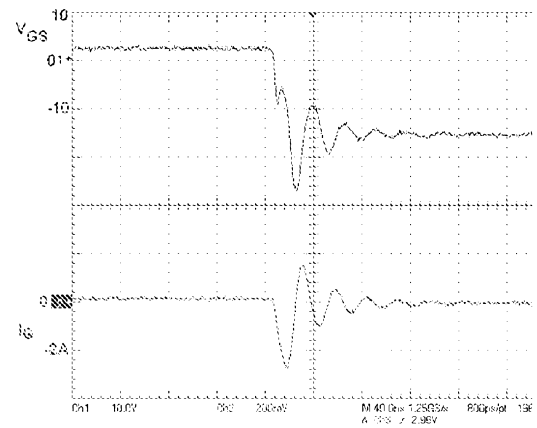

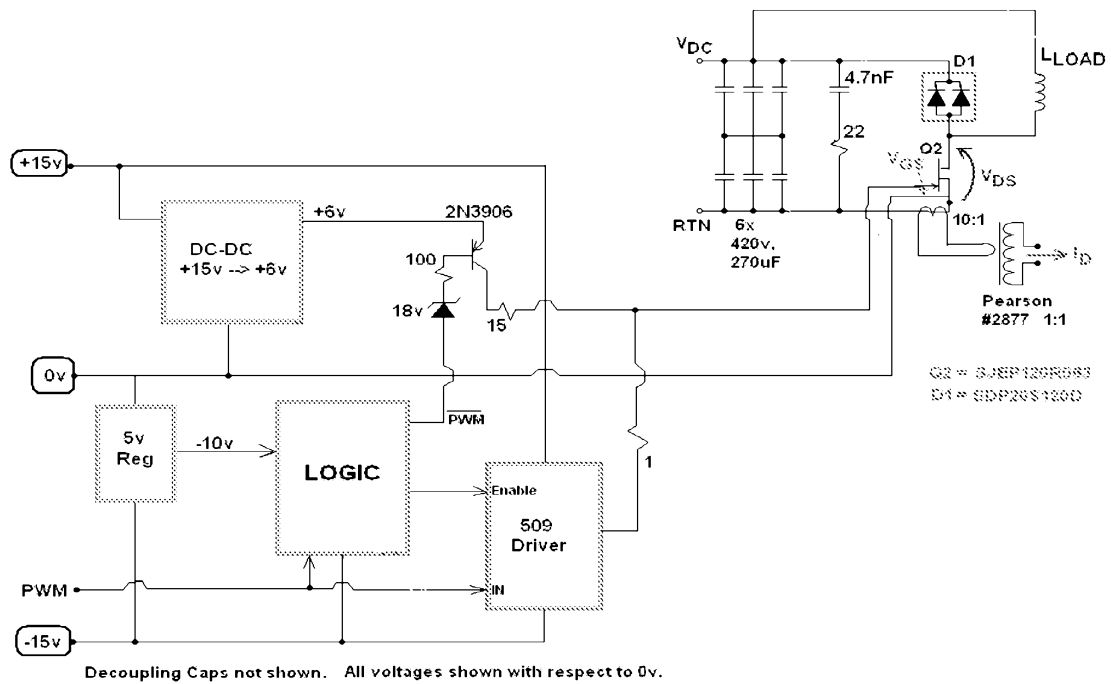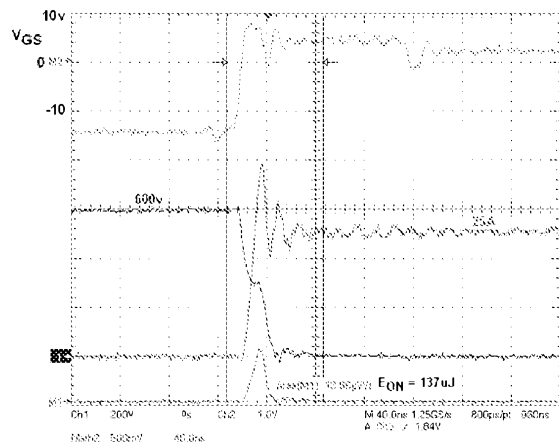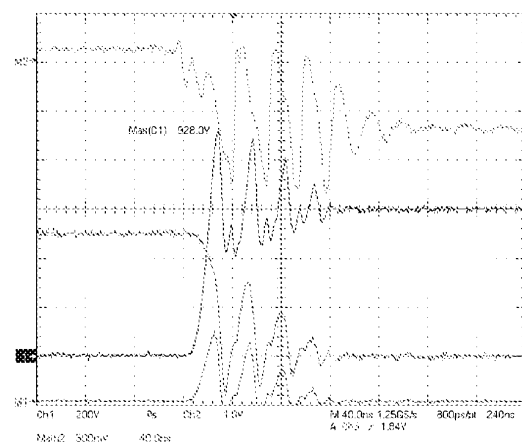**FIG. 12B**
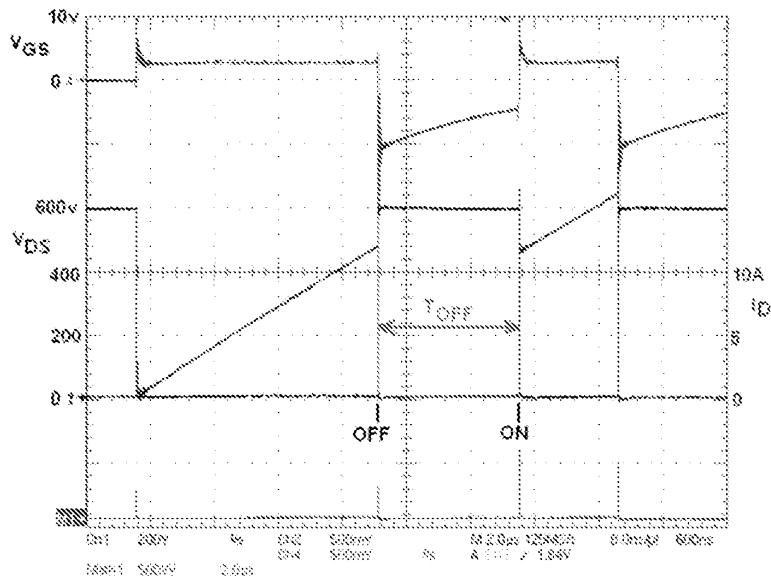
FIG. 13
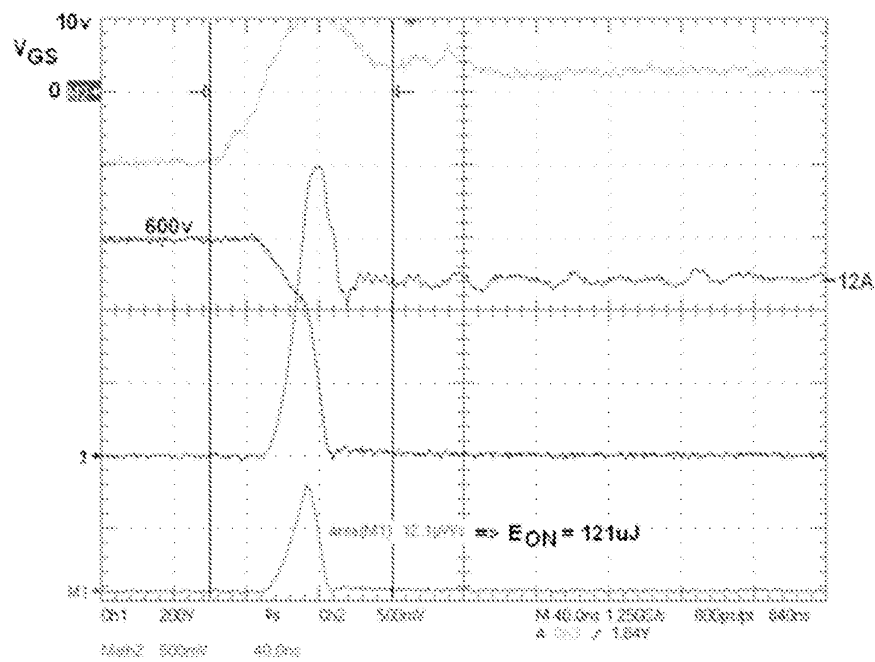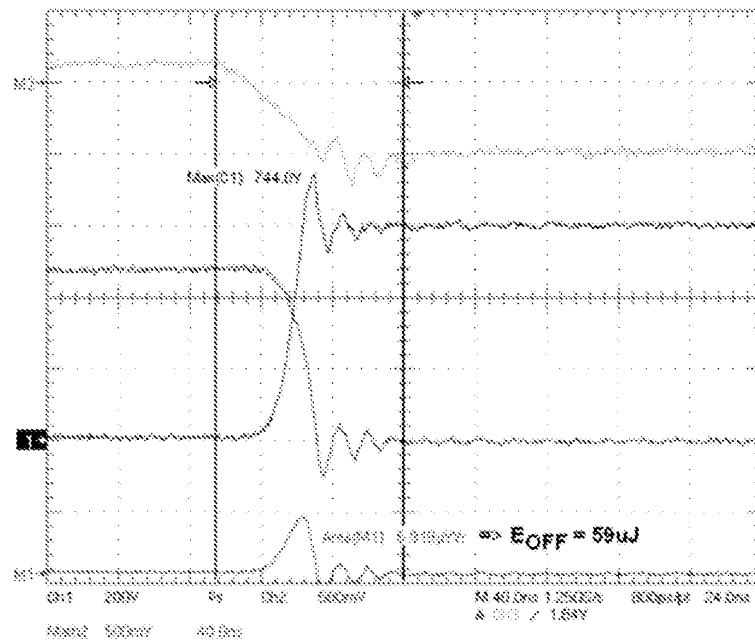
FIG. 14A

FIG. 14B
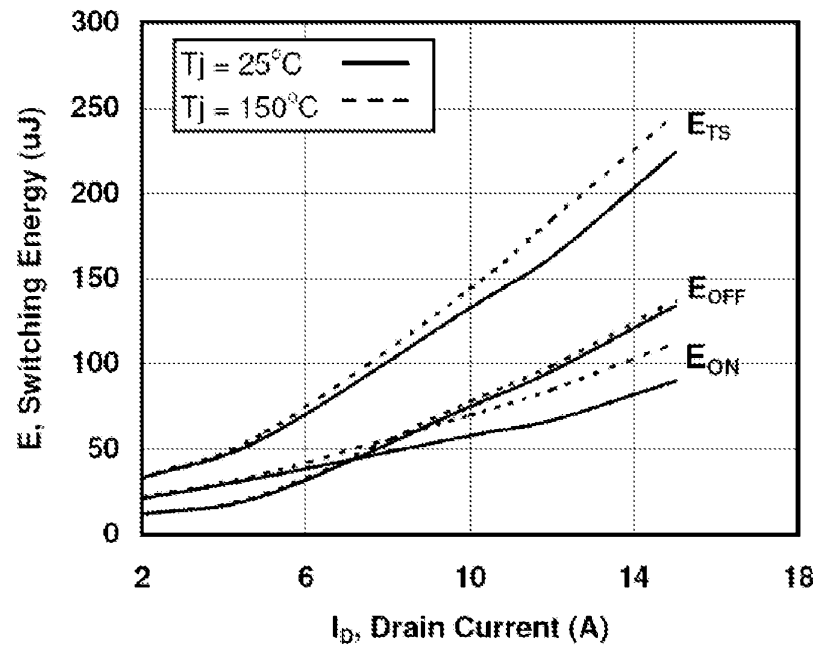
FIG. 15A
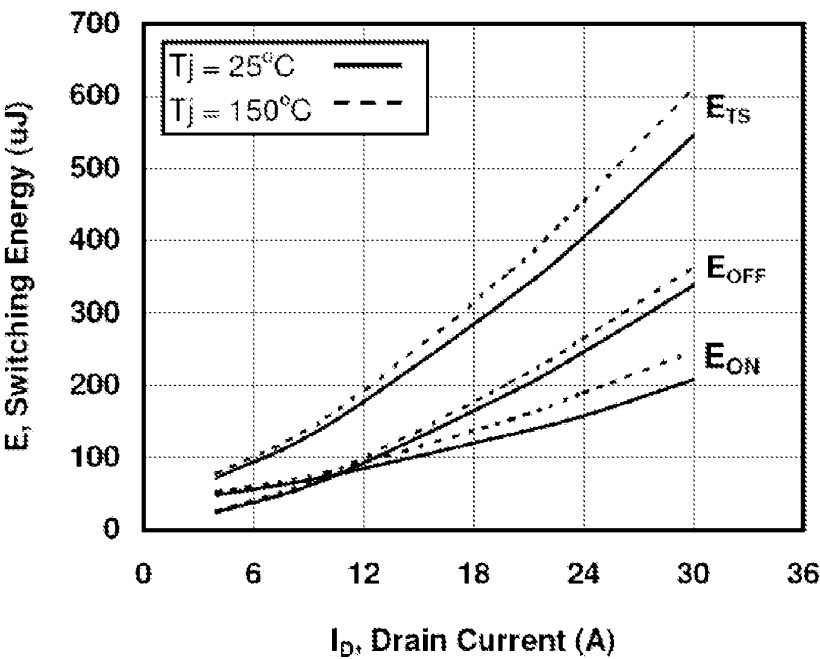
FIG. 15B

FIG. 16A

FIG. 16B

FIG. 16C

FIG. 16D

FIG. 16E

Decoupling Caps not shown.   All voltages shown with respect to 0v.
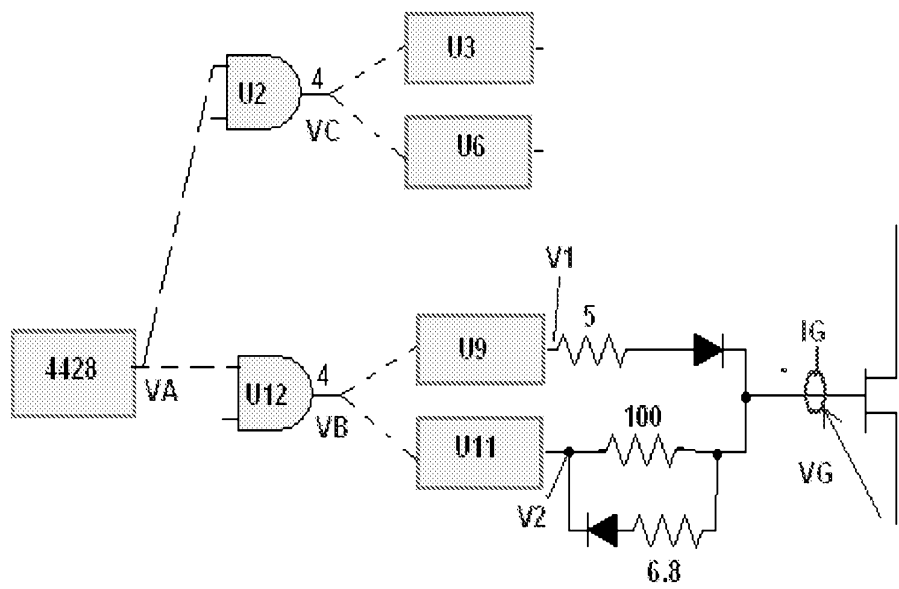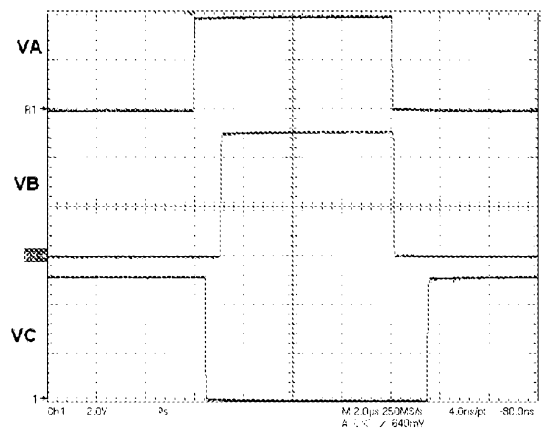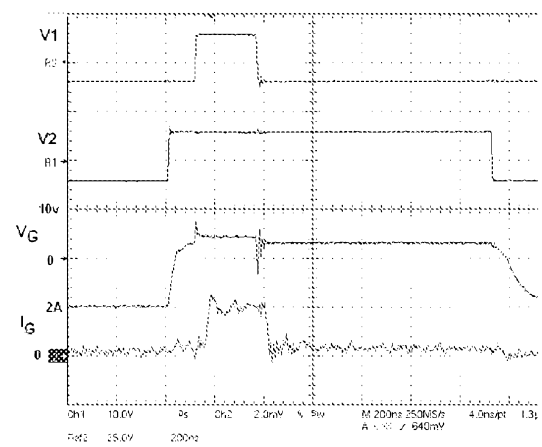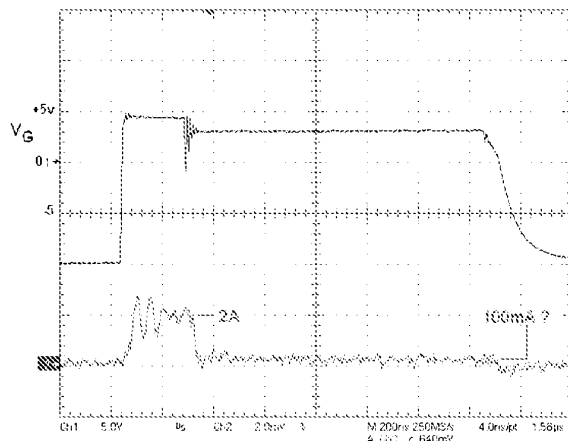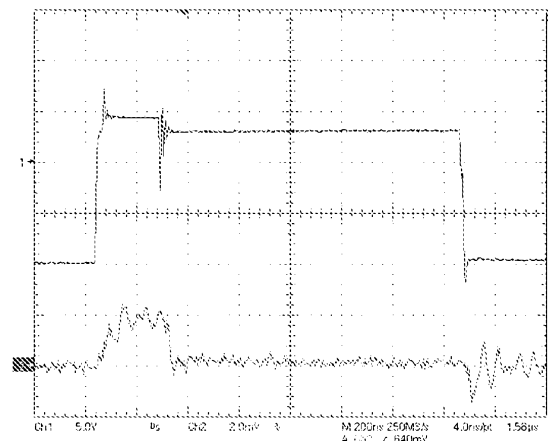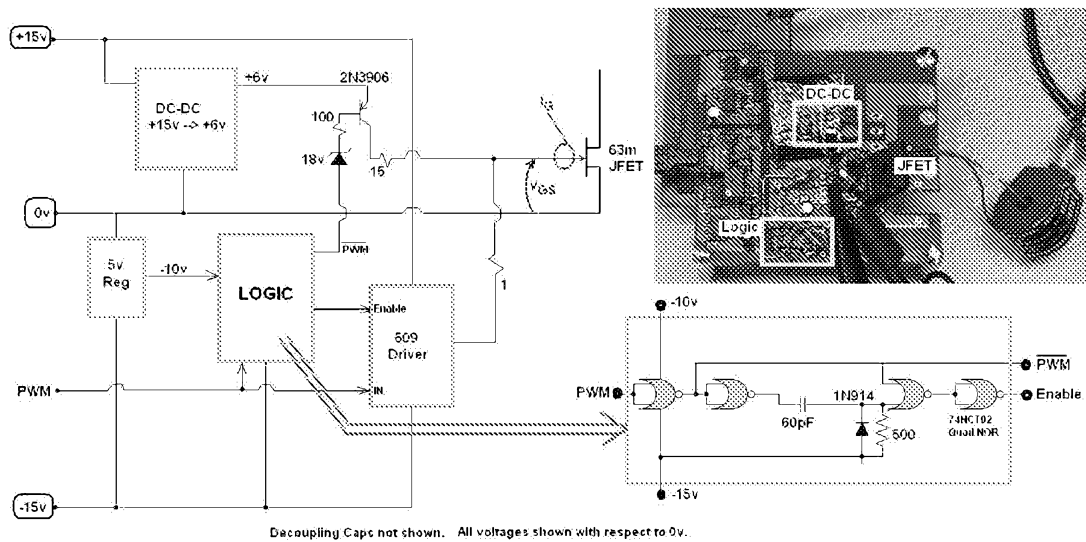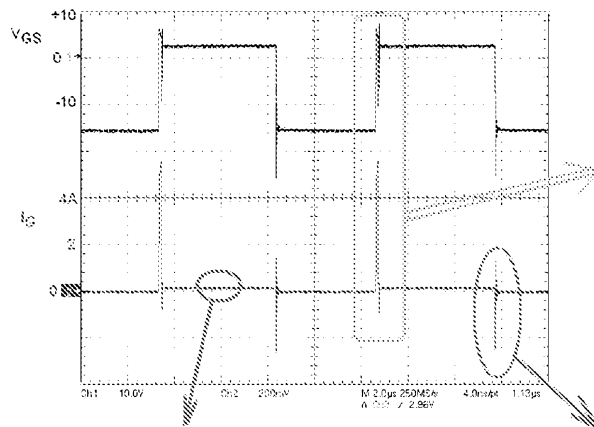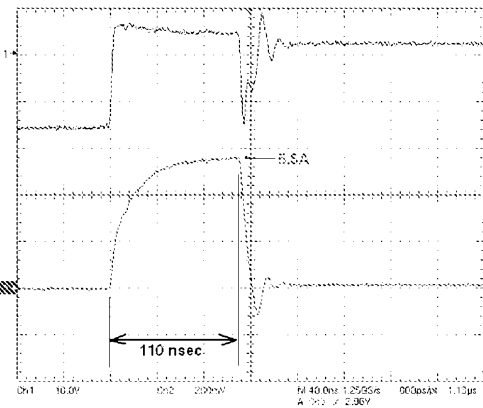
FIG. 17A

FIG. 17B

FIG. 17C

FIG. 17D

FIG. 17E

FIG. 18A

Decoupling Caps not shown.   All voltages shown with respect to 0v.

FIG. 18B

FIG. 18C