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PUSH-PULL PARALLEL OPERATING CIRCUIT FOR
POWER TRANSMISSION DEVICES
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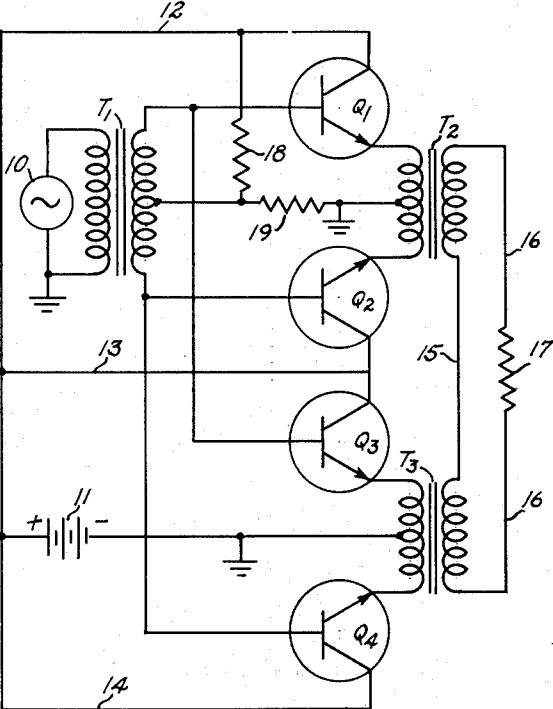


FIG. 1

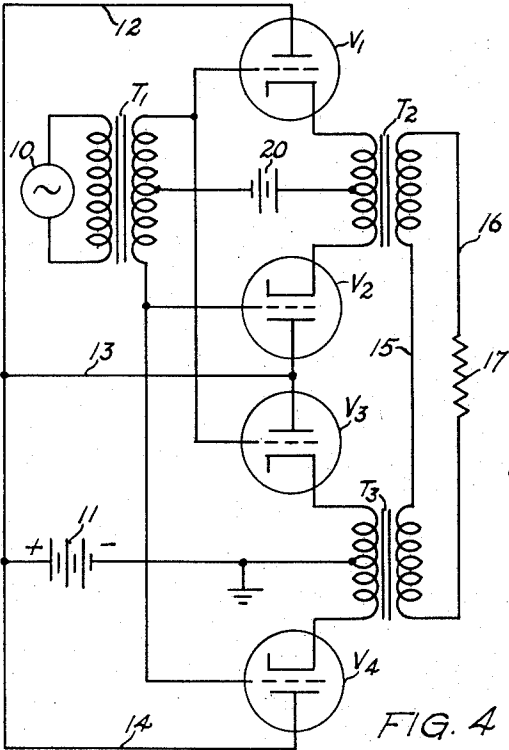


FIG. 4

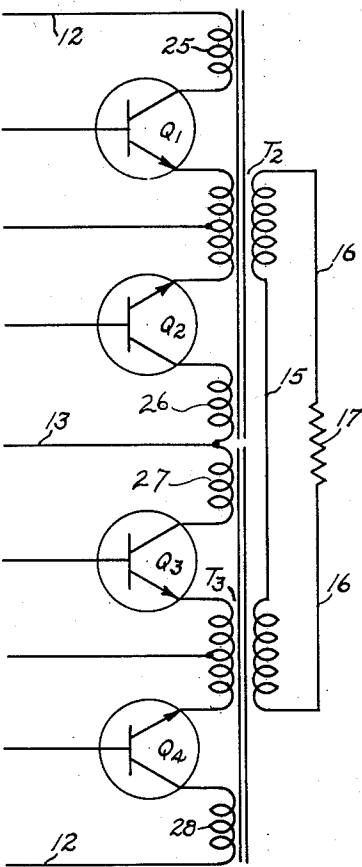


FIG. 3

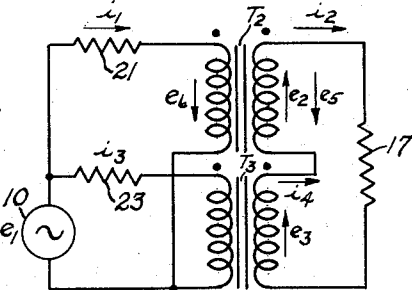


FIG. 2

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1

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PUSH-PULL PARALLEL OPERATING CIRCUIT FOR POWER TRANSMISSION DEVICES

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6 Claims. (Cl. 330—14)

(Granted under Title 35, U.S. Code (1952), sec. 266)

This invention described herein may be manufactured and used by or for the Government of the United States of America for governmental purposes without the payment of any royalties thereon or therefor.

This invention relates to electrical power transmitting devices and more particularly to circuit means coupled and arranged for transmission of alternating current power by parallel operation of electron emitting devices through power amplifiers, or the like, without the loss of power by power dissipation elements therein.

In known devices for transmitting electrical power through amplifiers or the like, separate resistors have been employed in the power transmitting devices, such as in the emitter circuits of transistors or the cathode circuits of vacuum tubes, arranged in parallel to equalize the load on the power transmission elements. The degeneration of power dissipation, which results from the presence of these resistors, tends to equalize the currents through the transistors or tubes and thus equalize their power dissipation. These circuits using resistors in the emitter or cathode circuits of the transistor or vacuum tube power transmitting means do not provide perfect equalization of the output currents unless the resistors are infinitely large. In addition, the presence of these resistors limits the available output power.

In the present invention electron power transmitting devices, such as transistors or vacuum tubes, are used in parallel or in push-pull parallel stages, the outputs of which are coupled through primary windings of a pair of output transformers. The two secondary windings of the output transformers are coupled in serial relation to insure equalization of currents therein and in the output transformer primaries. The currents in the two secondary windings of the two output transformers will equalize the currents in the primary windings and these primary windings will equalize the currents in the electron emitting power transmitting devices, whether the electron emitting devices are paired in a single ended manner or paired in push-pull stages. It is therefore a general object of this invention to produce parallel operating electron emission devices to transmit alternating current power from a single source to a load with the currents equalized in the power transmitting electron emission devices.

These and other objects and the attendant advantages, features, and uses may become more apparent to those skilled in the art as the description proceeds when taken in consideration with the accompanying drawing, in which:

FIGURE 1 illustrates a transistor circuit arranged with two push-pull stages;

FIGURE 2 is a circuit schematic representing a single ended power equalizing circuit equivalent to one-half of the push-pull stage shown in FIGURE 1;

FIGURE 3 illustrates a modification of FIGURE 1 in which both the emitter and collector circuits are through related primary windings of the output transformers; and

FIGURE 4 illustrates a further modification of FIGURE 1 in which the transistors are replaced by vacuum tubes.

Referring more particularly to FIGURE 1, an alternating current source 10 supplies alternating current to the primary winding of a transformer T₁ which transforms the alternating current to the center tapped secondary wind-

2

ing. The upper half of the secondary winding of transformer T₁ is coupled to the base electrodes of a transistor Q₁ and of a transistor Q₃, and the lower half of the secondary winding of transformer T₁ is coupled to the base electrodes of a transistor Q₂ and of a transistor Q₄. The collector electrodes of all four transistors Q₁ through Q₄ are coupled to a B+ potential such as a battery 11 through the conductor means 12, 13, and 14. The emitters of transistors Q₁ and Q₂ are coupled through the primary winding of an output transformer T₂ which primary winding is center tapped to a fixed potential such as ground. The emitters of transistors Q₃ and Q₄ are coupled through the primary winding of a transformer T₃ which primary winding is center tapped to ground in like manner as transformer T₂. The secondary windings of transformers T₂ and T₃ are connected in series by way of the conductor means 15 and 16 through a load represented by the reference character 17 and shown herein as a resistance. A base bias voltage is applied to all the transistors Q₁ through Q₄ by a voltage divider consisting of resistors 18 and 19 serially connected between the B+ lead 12 and ground. The center tap of the secondary winding of the transformer T₁ is coupled to the junction of the voltage divider resistors 18 and 19 to place a bias voltage on the base electrodes of the transistors of sufficient magnitude to overcome the threshold conduction voltage of the transistors. The parallel coupling to the base electrodes of transistors Q₁ and Q₃, as well as the parallel coupling to the base electrodes of transistors Q₂ and Q₄ with the emitters of transistors Q₁ and Q₂ coupled to the primary winding of transformer T₂ and with the emitter coupling of transistors Q₃ and Q₄ through the primary winding of transformer T₃, provide two push-pull stages constituting that of transistors Q₁ and Q₂ for one stage and transistors Q₃ and Q₄ for the other stage. The push-pull operation of transistors Q₁ and Q₂ on the primary winding of transformer T₂ induces currents in the secondary winding of transformer T₂ to the output load 17 which is duplicated for the transformer T₃ in the push-pull stage incorporating the transistors Q₃ and Q₄. The load 17 on the output of the secondary windings of transformers T₂ and T₃ may be of any variable type utilizing an alternating current.

In the operation of the device illustrated in FIGURE 1, reference will occasionally be made to FIGURE 2 which illustrates one-half of each output transformer by virtue of illustrating only one-half of the primary winding in each output transformer, or one-half of each push-pull stage of FIGURE 1. In referring to FIGURE 2, let it be understood that the resistances 21 and 23 merely illustrate the impedance of each electron emission device such as the transistors Q₁ and Q₃, respectively, of FIGURE 1. Assuming that the primary windings coupling the emitters of transistors Q₁ and Q₃, respectively, are equal, the voltage source 10 will supply a voltage e₁ to the base electrodes of transistors Q₁ and Q₃ producing conduction through the base and emitter electrodes to ground source. The currents produced by the voltage e₁ are represented in FIGURE 2 by the reference characters i₁ and i₃ through the impedances 21 and 23, respectively. This will produce the voltages e₂ and e₃, respectively, across each of the secondaries of transformers T₂ and T₃. Voltages e₂ and e₃ will be produced in equal magnitude in the secondary windings of transformers T₂ and T₃ to produce equal currents in the conductors 15 and 16 coupled in series to the load 17. The transformers T₂ and T₃ are polarized such that the induced voltages e₂ and e₃ will tend to cause currents i₂ and i₄ to flow from the top side of their respective windings. Let it be assumed, for the purpose of example, that the impedances of transistors Q₁ and Q₃ are different as is exemplified in FIGURE 2 by a difference of impedance in the resistors 21 and 23 whereupon currents in the secondary windings of transformer T₂ and T₃ tend

to flow unequally. Let it further be assumed, for the purpose of example, that i_2 is less than i_4 . This would attempt to cause a difference current of i_4 minus i_2 to flow into the bottom of transformer T_2 secondary. This attempted difference current would induce a voltage e_5 in the secondary of transformer T_2 which would be opposite in polarity of the voltage e_2 . Voltage e_5 in turn would induce a voltage e_6 in the primary of transformer T_2 . The two voltages e_1 and e_6 are in series in the primary of transformer T_2 and thus would tend to cause an increase in current i_1 for this hypothetical example. The current i_2 in the secondary of transformer T_2 would then increase to a point where the difference current i_4 minus i_2 vanishes. The secondary currents i_2 and i_4 are forced to be equal by virtue of their series circuit through the secondaries to the load which likewise produces equalized primary currents i_1 and i_3 to equalize the loads in the electron emission devices such as the transistors shown in FIGURE 1. With equal primary winding current flow in the output transformers T_2 and T_3 , the power dissipation of the electron emitting devices, such as transistors or vacuum tubes, are equalized without expending power in equalizing resistors and without limiting the output power. By this operation it may be seen that in FIGURE 1 the power dissipation in each of the transistor Q_1 through Q_4 will be equalized with a minimized loss of power through the output transformers T_2 and T_3 .

Referring more particularly to FIGURE 3 wherein a modification is shown of FIGURE 1, and in which like parts are identified by like reference characters, the transistors Q_1 through Q_4 are each coupled to the B+ voltage supply through additional or auxiliary primary windings such as 25, 26, 27, and 28, respectively. Such a coupling results in increased stage gain at the expense of less efficient current and power dissipation equalization. The transistors Q_1 through Q_4 are coupled to the alternating current voltage source through the transformer T_1 and the collector circuits are connected to the B+ voltage supply 11 in the same manner as shown and described for FIGURE 1. The operation of the modified form of FIGURE 1, as shown in FIGURE 3, would be substantially the same as that described for FIGURE 1 with the exception of the increase in gain and the loss in efficiency of power dissipation as set forth above.

Referring more particularly to FIGURE 4, the circuit arrangement is substantially the same as that of FIGURE 1 except that vacuum tubes V_1 , V_2 , V_3 , and V_4 are used in place of the corresponding transistors Q_1 through Q_4 with the base, emitter, and collector couplings being made respectively to the control grid, cathode, and anode of the tubes. The remaining elements and components corresponding to FIGURE 1 will therefore have like reference characters. Grid bias for the tubes V_1 through V_4 is provided by a voltage source 20 in accordance with the operating characteristic demands of these tubes. The operation of the vacuum tube circuit shown in FIGURE 4 is substantially the same as that described for FIGURE 1 and accordingly, will not be further described herein.

It is to be understood that many modifications and changes may be made in the circuits illustrated herein in further carrying out the spirit and scope of this invention such as making a single ended transistor or tube circuit in the manner illustrated by FIGURE 2, or by the addition of push-pull stages to those illustrated without departing from the spirit and scope of this invention. It is also to be understood that it is within the skill of one practicing the invention to use N-P-N and P-N-P transistors in any combination within the teaching herein disclosed. Although many modifications may become apparent from the teaching herein set forth, I desire to be limited in the definition of my invention only by the scope of the appended claims.

I claim:

1. Parallel operation of power electron emission means comprising:

at least two pairs of electron emission devices, each electron emission device having a pair of conduction electrodes and a control electrode for controlling current conduction in the conduction electrodes; an alternating current input of two phases, one phase input being coupled to the control electrode of a first electron emission device of each pair and the other phase input being coupled to the control electrode of a second electron emission device of each pair; and a pair of output transformers, one of said conduction electrodes of both of said electron emission devices in each pair of electron emission devices being coupled in series through one primary winding of each pair of output transformers, the other of said conduction electrodes of both of said electron emission device pairs being coupled to one terminal of a voltage supply, said primary windings each being center tapped and said center tap being coupled to the other terminal of said voltage supply providing parallel couplings for said two pairs of electron emission devices, and the secondary windings of said pair of output transformers being coupled in series to an output circuit whereby parallel operation of said electron emission devices accomplishes a minimum of power loss and equalization of currents in the electron emission devices.

2. Parallel operation of power electron emission means as set forth in claim 1 wherein

said electron emission devices are semiconductors.

3. Parallel operation of power electron emission means as set forth in claim 1 wherein

said electron emission devices are vacuum tubes.

4. Parallel operation of power electron emission means as set forth in claim 1 wherein

said electron emission devices are transistors, said control electrodes are base electrodes, and said conduction electrodes are emitter and collector electrodes, the conduction electrodes coupled in series through said primary winding being said emitter electrodes and said other electrodes coupled to said one terminal of a voltage supply being said collector electrodes.

5. A circuit of parallel operative power transistors comprising:

first and second pairs of transistors, each transistor having an emitter electrode, a collector electrode, and a base electrode;

an input phase inverting transformer having a secondary output of one phase coupling one base electrode of one transistor of each of said first and second pairs of transistors, and a secondary output of the other phase coupling one base electrode of the other transistors of said first and second pairs of transistors; and

a pair of output transformers, each having a primary winding one primary winding of which is coupled in series with the emitter electrodes of the first pair of transistors and the other primary winding of which is coupled in series with the emitter electrode of the second pair of transistors, the collector electrodes of all said transistors being coupled to one terminal of a direct current voltage supply source, said primary windings each being center tapped and said center tap being coupled to the other terminal of said direct current supply source, and the secondaries of said output transformers are coupled in series to a load circuit whereby equalized current loads occur through said transistors by equalization of current through the secondaries and primaries of said pair of output transformers.

6. A circuit as set forth in claim 5 wherein

said coupling of said collector electrodes to said one terminal of direct current voltage supply each being through an auxiliary primary winding in flux aiding

5

relation with the primary winding of the associated emitter electrodes.

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