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(54) INCREASED PWM DEPTH IN DIGITAL DRIVING OF ACTIVE MATRIX DISPLAYS

ERHÖHTE PWM-TIEFE BEI DER DIGITALEN ANSTEUERUNG VON AKTIVMATRIX-DISPLAYS
PROFONDEUR PWM ACCRUE DANS LA COMMANDE NUMÉRIQUE DES ÉCRANS À MATRICE ACTIVE

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(56) References cited:
US-A1- 2010 188 393 US-A1- 2012 320 005
US-A1- 2015 302 795

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Description**Field of the invention**

5 **[0001]** The present invention relates to the field of digital driving of displays. More specifically it relates to methods for digitally driving active matrix displays, for instance AMOLED (Active Matrix Organic Light Emitting Diode) displays, so as to obtain high color accuracy, and to digital driving circuitry for active matrix displays, for instance AMOLED displays, providing high color accuracy.

Background of the invention

10 **[0002]** Prior art backplanes for AMOLED displays use a pixel driver circuit for each OLED, each pixel driver circuit driving a predetermined current through the corresponding OLED. Multiple pixel driver circuit schematics are being implemented, which all comprise a drive transistor (such as M1 in FIG. 1) driving the predetermined current through the OLED.

15 **[0003]** In an analog driving method an amplitude modulation approach is used, wherein each OLED emits light during a full frame period with an intensity corresponding to the required gray level. The current through the OLED is determined in accordance with an analog data voltage on the floating gate of the drive transistor M1. As this transistor M1 preferably operates in saturation for accurate current control, the current through the OLED (and thus the OLED luminance) varies with the square of the M1 gate voltage. This introduces non-linearity in the display response, limits accuracy and makes the display sensitive to noise. An overall display architecture as schematically shown in FIG. 2 is currently used for analog driven displays. At one edge of the display, a select line driver integrated circuit is provided. The select lines are digitally driven, for instance by a running one, cycling at a rate corresponding to the frame rate. At another edge of the display, data line driver circuitry is provided for driving the data lines. The data lines are driven by an analog voltage, keeping the pixels at a constant luminance during an entire image frame.

20 **[0004]** In a digital driving method a Pulse Width Modulation approach can be used, wherein each OLED emits light during a portion of a frame period, at a single luminance. In this approach the portion of the frame period during which an OLED emits light has a duration corresponding to the required gray level. A pulse current having a duty ratio in accordance with the data voltage is supplied to each OLED. In such known approach, a frame is divided into n sub-frames, wherein n is the number of bits used for digitally representing the image data. These n sub-frames may have a different duration, there being a ratio 1:2:4:8:.....:2ⁿ⁻¹ between the different sub-frame durations. In each sub-frame a pixel (OLED) is either ON or OFF. In this way 2ⁿ different gray levels can be created. A display architecture is used wherein select lines (for instance rows) are digitally driven by dedicated timing control circuitry and wherein data lines (for instance columns) are driven by a digital voltage, as schematically illustrated in FIG. 3.

25 **[0005]** FIG. 4 shows a comparison between a typical analog pixel driving method (dashed lines) and a digital pixel driving method (full lines). In an analog driven pixel, the pixel luminance is constant during each image frame period and it can be different from frame to frame. The pixel luminance can have 2ⁿ different levels. In a digital driven pixel, a pixel is at full luminance(ON) during part of a frame period and at zero luminance (OFF) during the remaining part of the frame period. FIG. 4 is only a schematic representation, not showing a division in sub-frames for the digital driving approach.

30 **[0006]** WO 2014/068017 describes a method and digital driving circuitry for digital driving of an active matrix display with a predetermined frame rate, by means of pulse width modulation (PWM). To obtain high color accuracy, both under low-light intensity and under high-light intensity; the width of the pulses needs to be controlled very accurately. The described method includes representing each of the plurality of pixels of an image to be displayed within a frame by an n-bit digital code. The image frame is divided into sub-frames, which may be of substantially equal duration. Within each sub-frame, the method includes sequentially selecting at least one of the plurality of rows twice. Upon a first selection, a first digital code is written to the selected row, and upon a second selection, a second digital code is written to the selected row. This alternation of driving between both lines causes that the line driven first is typically half a time unit longer active than the other line. One way to avoid this half time unit difference is to swap the sequence of both lines during the next image frame, such that on average they have equal length. However, this implementation is not preferred, because it again gives a variation at half the frame refresh rate, which leads to possible subharmonics (e.g. a 30 Hz signal component in a display driven at 60 Hz), which may lead to causing flickering and hence should be avoided.

35 **[0007]** Documents US 2010/188393 and US 2012/320005 are directed to driver circuits and methods that make use of erase circuitry for a sub-frame controlled shortening of the light emission period.

Summary of the invention

40 **[0008]** It is an object of embodiments of the present invention to provide good methods for digital driving of active

matrix displays, such as for instance, but not limited thereto, AMOLED displays, based on Pulse Width Modulation, so as to obtain high color accuracy.

[0009] The above objective is accomplished by a method and device set out in the appended set of claims.

[0010] Particular objects and advantages of various aspects have been described herein above. Of course, it is to be understood that not necessarily all such objects or advantages may be achieved in accordance with any particular embodiment of the disclosure. Thus, for example, those skilled in the art will recognize that the disclosure may be embodied or carried out in a manner that achieves or optimizes one advantage or group of advantages as taught herein without necessarily achieving other objects or advantages as may be taught or suggested herein. Further, it is understood that this summary recites merely some examples and is not intended to limit the scope of the disclosure. The disclosure, both as to organization and method of operation, together with features and advantages thereof, may best be understood by reference to the following detailed description when read in conjunction with the accompanying drawings.

Brief description of the drawings

[0011]

FIG. 1 schematically shows an example of a prior art AMOLED pixel driver circuit, wherein an analog voltage on the gate of the drive transistor M1 determines the OLED luminance.

FIG. 2 schematically shows a prior art AMOLED display architecture using an analog driving method.

FIG. 3 schematically shows a prior art AMOLED display architecture using a digital driving method.

FIG. 4 shows a comparison in OLED current output between an analog pixel driving method as in FIG. 2 (dashed lines) and a digital driving method as in FIG. 3 (full lines).

FIG. 5 schematically shows a digitally driven AMOLED display architecture as an example of an active matrix display architecture in accordance with embodiments of the present invention.

FIG. 6 is a schematic representation of a time delay determination circuit of a select line driving circuit that can be used in embodiments of the present invention.

FIG. 7 is a schematic representation of a time delay determination circuit of a select line driving circuit comprising Output Enable circuitry.

FIG. 8 illustrates a hardware implementation of a bit counter which may be used in a 12-bit coding table optimisation algorithm in accordance with embodiments of the present invention.

FIG. 9 illustrates a hardware implementation of an adder which may be used in a 12-bit coding table optimisation algorithm in accordance with embodiments of the present invention.

FIG. 10 illustrates a hardware implementation of a look-up table which may be used in a 12-bit coding table optimisation algorithm in accordance with embodiments of the present invention.

FIG. 11, FIG. 12 and FIG. 13 illustrate a hardware implementation of a bit counter, an adder and a look-up table, respectively, which may be used in a 9-bit coding table optimisation algorithm in accordance with embodiments of the present invention.

FIG. 14, FIG. 15 and FIG. 16 illustrate a hardware implementation of a bit counter, an adder and a look-up table, respectively, which may be used in a 13-bit coding table optimisation algorithm in accordance with embodiments of the present invention.

FIG. 17, FIG. 18 and FIG. 19a and 19b illustrate a hardware implementation of a bit counter, an adder and a look-up table, respectively, which may be used in a 14-bit coding table optimisation algorithm in accordance with embodiments of the present invention.

FIG. 20, FIG. 21 and FIG. 22a and 22b illustrate a hardware implementation of a bit counter, an adder and a look-up table, respectively, which may be used in a 15-bit coding table optimisation algorithm in accordance with embodiments of the present invention.

FIG. 23, FIG. 24 and FIG. 25a and 25b illustrate a hardware implementation of a bit counter, an adder and a look-up table, respectively, which may be used in a 16-bit coding table optimisation algorithm in accordance with embodiments of the present invention.

[0012] The drawings are only schematic and are non-limiting. In the drawings, the size of some of the elements may be exaggerated and not drawn on scale for illustrative purposes.

[0013] Any reference signs in the claims shall not be construed as limiting the scope.

[0014] In the different drawings, the same reference signs refer to the same or analogous elements.

Detailed Description of illustrative embodiments

[0015] In the following detailed description, numerous specific details are set forth in order to provide a thorough

understanding of the present invention and how it may be practiced in particular embodiments. However, it will be understood that embodiments of the present invention may be practiced without necessarily having all these specific details. In other instances, well-known methods, procedures and techniques have not been described in detail, so as not to obscure the disclosure. While the present invention will be described with respect to particular embodiments and with reference to certain drawings, the invention is not limited hereto. The drawings included and described herein are schematic and are not limiting the scope of the disclosure.

[0016] It is to be noticed that the term "comprising" should not be interpreted as being restricted to the means listed thereafter; it does not exclude other elements or steps. It is thus to be interpreted as specifying the presence of the stated features, integers, steps or components as referred to, but does not preclude the presence or addition of one or more other features, integers, steps or components, or groups thereof. Thus, the scope of the expression "a device comprising means A and B" should not be limited to devices consisting only of components A and B.

[0017] OLED displays are displays comprising an array of light-emitting diodes in which the emissive electroluminescent layer is a film of organic compound which emits light in response to an electric current. OLED displays can either use passive-matrix (PMOLED) or active-matrix (AMOLED) addressing schemes. In case of OLED displays, the present invention relates to AMOLED displays. The corresponding addressing scheme makes use of a thin-film transistor back-plane to switch each individual OLED pixel on or off. AMOLED displays allow for higher resolution and larger display sizes than PMOLED displays.

[0018] The present invention, however, is not limited to AMOLED displays, but in a broader concept relates to active matrix displays. Any type of active matrix displays may use the concepts of embodiments of the present invention, although AMOLED displays are particularly advantageous in view of the current switching speeds of their pixel elements. It is advantageous if the pixel elements of the active matrix displays can switch faster, as this allows to obtain higher frame rates, hence less flickering images.

[0019] An active matrix display, e.g. an AMOLED display, according to embodiments of the present invention comprises a plurality of pixels, each comprising a pixel element, e.g. an OLED element. The pixel elements are arranged in an array, and are logically organised in rows and columns. Throughout the description of the present invention, the terms "horizontal" and "vertical" (related to the terms "row" of "line" and "column", respectively) are used to provide a co-ordinate system and for ease of explanation only. They do not need to, but may, refer to an actual physical direction of the device. Furthermore, the terms "column" and "row" or "line" are used to describe sets of array elements which are linked together. The linking can be in the form of a Cartesian array of lines and columns; however, the present invention is not limited thereto. As will be understood by those skilled in the art, columns and lines can be easily interchanged and it is intended in this disclosure that these terms be interchangeable. Also, non-Cartesian arrays may be constructed and are included within the scope of the invention. Accordingly the terms "row" or "line" and "column" should be interpreted widely. To facilitate in this wide interpretation, the claims refer to logically organised in rows and columns. By this is meant that sets of pixel elements are linked together in a topologically linear intersecting manner; however, that the physical or topographical arrangement need not be so. For example, the rows may be circles and the columns radii of these circles and the circles and radii are described in this invention as "logically organised" rows and columns. Also, specific names of the various lines, e.g. select line and data line, are intended to be generic names used to facilitate the explanation and to refer to a particular function and this specific choice of words is not intended to in any way limit the invention. It should be understood that all these terms are used only to facilitate a better understanding of the specific structure being described, and are in no way intended to limit the invention.

[0020] Where in embodiments of the present invention reference is made to "selection" in "first selection" and "second selection", reference is made to an action in the circuit that enables data to be introduced. This could be, for example, multiplying a bit from a data code by one in a logical implementation. Alternatively, it may be seen as running a one in a select line of a circuit, changing the state of a transistor to introduce data from a data line. Hence, a first selection followed by a second selection may comprise introducing data a first time, followed by introducing data a second time.

[0021] In the context of the present invention, a frame is a single picture or single image that is shown as part of a sequence of pictures. For example, many single images or frames can be provided in succession to produce a video or a movie. The frame rate or frame frequency is the rate or frequency at which consecutive images (frames) are formed and displayed. The frame period (fp) is a time interval equal to the reciprocal of the frame frequency. It corresponds to the display period of a single frame or image.

[0022] A frame can be divided into sub-frames. In the analog way of display driving, each pixel is addressed once each frame. When the display is driven digitally using pulse width modulation, different pulse with different lengths are needed to obtain the different grey scales. The different timing moments to drive a pixel are grouped into sub-frames. The sub-frames which together form a frame, each have a subframe duration which lasts for only part of the total frame period; the sum of these parts of all sub-frames together forming a frame being equal to one frame period. Pixels in the frame which are very bright, may give a lot of intensity in all sub-frames, while pixels which are less bright may give more intensity in some sub-frames, and less intensity in other sub-frames, and pixels which are very dark may give little intensity in all sub-frames. In embodiments of the present invention, the duration of each of the sub-frames of a frame

may be, but does not have to be, substantially equal. In those embodiments in which each sub-frame duration is substantially equal, each frame, which has a duration of one frame period f_p , may be divided in N sub-frames with a duration of f_p/N . Nonetheless, the present invention is not limited by equal duration of the sub-frames.

[0023] In some embodiments, N may be an arbitrary number. In certain embodiments, N may be equal to the number of bits used per image colour for representing the image data ($N = n$, n bit gray scale). For instance, exemplary embodiments are described wherein the number of sub-frames N is equal to the number of bits n , which in the example described is 8. In this example, 8 bits are used for representing each colour, e.g. for use in a 24 bit RGB (Red Green Blue) display. However, the present invention is not limited thereto, and the number of sub-frames can be different, e.g. larger or smaller than 8.

[0024] In those cases in which the number of bits n is not a power of two (i.e., n is not 4, 8, 16, etc), then N may be chosen as the number of bits n , so $N = n$ as before; alternatively, N may be chosen equal to the power of two higher than, but closest to, n . In this case, for instance, if $n = 5, 6$ or 7 , then $N = 8$, and if $n = 11, 12, 14$, then $N = 16$.

[0025] In one aspect, the present invention relates to methods for digital driving of pixels of active matrix displays, for instance AMOLED displays, with a predetermined frame rate. The display comprises a plurality of pixels logically organized in a plurality of rows and columns.

[0026] The method comprises representing each of the plurality of pixels of an image to be displayed within a frame by an n -bit digital image code, and dividing the image into a natural number $N (>1)$ of sub-frames. Each sub-frame is further divided into time slots, and a number of time slots are assigned to each bit of the n -bit image code according to each bit's significance in the code.

[0027] The method further comprises selecting each of the plurality of rows one first time per sub-frame, and subsequently for at least one sub-frame, a second time. This implies that at least one sub-frame will be sequentially selected twice. Data code corresponding to pixel data of image pixels to be represented and, in some embodiments, dummy data or reset data (a zero) is introduced with each selection. In preferred embodiments of the present selection, this sequence of first selection and second selection takes place in at least 35% of the sub-frames, or in at least half of the sub-frames. In certain embodiments, at least 75%, 80% or even more than 90% of sub-frames are selected twice.

[0028] The first selection and the second selection are performed sequentially for at least one and preferably more of the sub-frames. This means that there is a time delay between the first selection and the second selection, and this time delay may be different for each sub-frame.

[0029] In embodiments where the number of sub-frames N equals the number of bits ($N = n$), the time delay in at least one of the sub-frames, e.g. the x^{th} sub-frame, may equal 1 more or 1 less than $1/2^{N-x}$ of the sub-frame duration. The data introduced in each sub-frame is the bits in order from the least significant bit LSB to the most significant bit MSB.

[0030] In the prior art method as disclosed in WO 2014/068017, for driving n bits, a frame is divided into 2^n time slots, from which only $2^n - 1$ time slots are used for effective driving. There remains one time slot that is unused. The present invention will use that one unused time slot for improving the driving scheme.

[0031] This is now illustrated by means of an example first illustrating the method of WO 2014/068017.

[0032] In case the number of bits of the digital image code $n = 5$ bits, and the number of subframes $N = 8$, it is possible to drive the data to the pixel during a first and second selection in each sub-frame, for a number of time slots according to the significance of each data bit. Firstly, each sub-frame may be considered with the same duration. Each sub-frame is divided in time slots, which may also have the same duration. The number of time slots can be $2^n/N = 2^5/8 = 4$ time slots per sub-frame (or 32 time slots for the whole frame). Now, each bit is assigned to a number of time slots according to their position, so the m^{th} bit ($1 \leq m \leq n$), the first bit being the LSB and the n -th bit being the MSB, will be assigned to 2^{m-1} time slots. In a data code with 5 bits, B4 B3 B2 B1 B0, the MSB bit B4 will be assigned to $2^4 = 16$ time slots. Bit B3 will be assigned to 8 time slots, B2 will be assigned to 4, B1 will receive 2 time slots and B0 will be introduced in the pixel during $2^0 = 1$ time slot. The introduction of the data is performed twice per sub-frame, for instance according to Table 1. Each of the first three sub-frames are run with two selections. The first sub-frame is run with a zero for one time slot, the rest of the sub-frame is run with data bit B4. The second sub-frame is run with two selections, one time slot for bit B0, and the remaining three time slots for B4. The third sub-frame is selected twice, the first 2 time slots for driving bit B1, the second 2 time slots for driving B4. The remainder of the sub-frames are selected only once, for the bits B2, B3 and B4, the second selection not being needed. This way, all bits are represented longer according to their significance in the data code, and this in a homogeneous way, and utilizing most of the time slots (most of the frame) for driving data in the pixel.

Table 1

Sub-Frame number (length code a, code b)	code driven after running one a	code driven after running one b
1 (1,3)	0	B4
2 (1,3)	B0	B4

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(continued)

Sub-Frame number (length code a, code b)	code driven after running one a	code driven after running one b
3 (2,2)	B1	B4
4 (4,/)	B2	/
5 (4,/)	B3	/
6 (4,/)	B3	/
7 (4,/)	B4	/
8 (4,/)	B4	/

[0033] A similar example can be given for an 11-bit image code ($n=11$) and the number of subframes $N = 16$ (power of two higher than, but closest to, n). It is possible to drive the data to the pixel during a first and second selection in each sub-frame, for a number of time slots according to the significance of each data bit. Firstly, each sub-frame may be considered with the same duration. Each sub-frame is divided in time slots, which may also have the same duration. The number of time slots can be $2^n/N = 2^{11}/16 = 128$ time slots per sub-frame (or 2048 time slots for the whole frame). Now, each bit is assigned to a number of time slots according to their position, so the m^{th} bit ($1 \leq m \leq n$), the first bit being the LSB and the n -th bit being the MSB, will be assigned to 2^{m-1} time slots. In a data code with 11 bits, B10 B9 B8 B7 B6 B5 B4 B3 B2 B1 B0, the MSB bit B10 will be assigned to $2^{10} = 1024$ time slots, bit B9 will be assigned 512 time slots, B8 will be assigned 256 time slots, B7 will be assigned 128 time slots, B6 will be assigned 64 time slots, B5 will be assigned 32 time slots, B4 will be assigned 16 time slots, B3 will be assigned to 8 time slots, B2 will be assigned to 4, B1 will receive 2 and B0 will be introduced in the pixel during $2^0 = 1$ time slot. The introduction of the data is performed twice per sub-frame, for instance according to Table 2.

Table 2

Sub-Frame number (length code a, code b)	code driven after running one a	code driven after running one b
1 (1,127)	0	B10
2 (1,127)	B0	B10
3 (2,126)	B1	B10
4 (128,/)	B9	/
5 (8,120)	B3	B10
6 (16,112)	B4	B10
7 (32,96)	B5	B10
8 (64,64)	B6	B10
9 (128,/)	B7	/
10 (128,/)	B8	/
11 (128,/)	B8	/
12 (4,124)	B2	B10
13 (128,/)	B9	/
14 (128,/)	B9	/
15 (128,/)	B9	/
16 (128,/)	B10	/

[0034] The minimal driving speed required for 60 Hz frames, 16 subframes per frame, 128 time slots per frame, and 2 lines selected per time slot, would be $f_{\text{data}} = 60 * 16 * 128 * 2 = 246$ kHz.

[0035] Of course it is desired to have the image data encoded with as many bits as possible. However, compared to the above example, if the image data is coded by $n = 12$ bits and the number of subframes is still $N = 16$ (power of two equal or higher than, but closest to, n), the required data rate increases severely. Again, each sub-frame may be

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considered with the same duration. Each sub-frame is divided in time slots, which may also have the same duration. The number of time slots can be $2^n/N = 2^{12}/16 = 256$ time slots per sub-frame (or 4096 time slots for the whole frame). Again, each bit is assigned to a number of time slots according to their position, so the m^{th} bit ($1 \leq m \leq n$), the first bit being the LSB and the n -th bit being the MSB, will be assigned to 2^{m-1} time slots. A data code with 12 bits may be represented as B11 B10 B9 B8 B7 B6 B5 B4 B3 B2 B1 B0, the MSB bit B11 and LSB B0. The introduction of the data is performed twice per sub-frame, for instance according to Table 3.

Table 3

Sub-Frame number (length code a, code b)	code driven after running one a	code driven after running one b
1 (1,255)	0	B11
2 (1,255)	B0	B11
3 (2,254)	B1	B11
4 (4,252)	B2	B11
5 (8,248)	B3	B11
6 (16,240)	B4	B11
7 (32,224)	B5	B11
8 (64,192)	B6	B11
9 (128,128)	B7	B11
10 (256,/)	B8	/
11 (256,/)	B9	/
12 (256,/)	B9	/
13 (256,/)	B10	/
14 (256,/)	B10	/
15 (256,/)	B10	/
16 (256,/)	B10	/

[0036] The minimal driving speed required for 60 Hz frames, 16 subframes per frame, 256 time slots per frame, and 2 lines selected per time slot, would be $f_{\text{data}} = 60 * 16 * 256 * 2 = 492$ kHz.

[0037] In summary, for the above type of driving method as disclosed in WO 2014/068017, in case the number of sub-frames N equals the power of 2 closest and not smaller than the number of bits n, and the sub-frames have substantially the same duration, for n-bit image code and each sub-frame divided in $2^n/N$ time slots, then 2^{m-1} time slots may be assigned to the m^{th} bit of the n-bit image code. Then, the MSB would be assigned with 2^{n-1} time slots, the second MSB with 2^{n-2} , and so on until the LSB is assigned with 2^0 time slots (one time slot). The introduction of data is performed with two selections per sub-frame.

[0038] It can be seen from the above that, according to WO 2014/068/017, for driving n bits, a frame is divided into 2^n (in the example given $2^5 = 32$) time slots, from which only 2^n-1 ($16+8+4+2+1 = 31$ for the case of $n = 5$) time slots are used for effective driving. There always remains one time slot that is unused. This can also be seen from the values 0 shown in Table 2 and Table 3, at the first time slot of subframe 1.

[0039] The inventors of the present invention have now found that exactly this one unused time slot can advantageously be used for improving the driving scheme, by recoding the bits. This has the advantage that an additional bit of color depth may be obtained, without having to increase the data rate.

[0040] In the further description, the coding method according to embodiments of the present invention is explained in more detail. In such coding method, the remaining unused time slot is used as an additional minimal length block (length 1). This block is indicated CX in Table 4 below.

[0041] To build a given coding table, in accordance with embodiments of the present invention, again each of the bits will be assigned to a number of time slots according to their position, with bits closer to the LSB bit having less time slots assigned than bits closer to the MSB. A difference compared to the method described in WO 2014/068017, however, is that the number of time slots assigned to a bit value now no longer is a power of 2, but deviates therefrom. In this embodiment, the most significant bits are implemented as in the prior art, with the number of time slots assigned being a power of 2 of the value of the position of that bit in the image code. The first least significant bit is assigned 1 time slot.

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The further least significant bits are assigned a number of time slots which is larger than the number of time slots (larger than 2^{m-1} for the m^{th} bit) which would be assigned if a power of 2 of the value of the position of that bit in the image code would be taken, and the middle significant bits are assigned a number of time slots which is smaller than the number of time slots (smaller than 2^{m-1} for the m^{th} bit) which would be assigned if a power of 2 of the value of the position of that bit in the image code would be taken.

[0042] For a 12-bit input code B11 B10 B9 B8 B7 B6 B5 B4 B3 B2 B1 B0, for instance, with 16 subframes being used, each subframe comprises maximal (any multiple of) 128 lines. Each image comprises in this approach typically 128 lines. If the image consists of more than 128 lines, the lines are grouped in blocks. e.g. a display of 1000 lines will be driven with this code as 128 blocks of 8 lines.

[0043] Driving each subframe comprises driving maximum 2 pulses of in total 256 timeslots.

Time slots acc to prior art	1	2	4	8	16	32	64	128	256	512	1024	2048
Bit number	B0	B1	B2	B3	B4	B5	B6	B7	B8	B9	B10	B11

The number of time slots assigned to each bit value can be as follows:

Time slots acc to invention	1	3	5	11	15	31	63	127	255	512	1024	2048	1
Bit number	C0	C1	C2	C3	C4	C5	C6	C7	C8	C9	C10	C11	CX

[0044] This shows that, in this embodiment, the least significant bit B0 is assigned 1 time slot (indicated by C0), the second least significant bit B1 (indicated by C1) is assigned 3 time slots, where in the prior art it would have been $2^{m-1}=2$, m being the position of the bit in the code, bit B2 (indicated by C2) is assigned 5 time slots, and bit B3 (indicated by C3) is assigned 11 time slots. In the example illustrated, bits C1 to C3 are the ones being assigned more time slots than would have been the case in the prior art. In accordance with embodiments of the present invention, the number of time slots assigned to the least significant bits should always be uneven.

[0045] Correspondingly, the middle significant bits B4 to B8 each are assigned less time slots, for instance one time slot less, than would have been the case in the prior art. In accordance with embodiments of the present invention, the number of time slots assigned to the middle significant bits can be uneven.

[0046] The most significant bits B9 to B11 are implemented just at their actual value according to their position in the code, if a power of 2 is taken. The MSB bit B11 will be assigned $2^{11} = 2048$ time slots (indicated by C11), B10 will be assigned to $2^{10} = 1024$ time slots (indicated by C10), bit B9 will be assigned 512 time slots (indicated by C9).

[0047] The assigning of the number of time slots to each of the bit values (e.g. more than 2^{m-1} for at least one of the least significant bits, less than 2^{m-1} for at least one of the middle significant bits, and exactly 2^{m-1} for the most significant bits, m being the position of the corresponding bit in the image code) must be such that all intensity values can be covered. In accordance with embodiments of the present invention, this can be done by assigning a value 1 to the otherwise unused time slot CX.

[0048] The coding table may be implemented as illustrated in FIG. 8 to FIG. 10. The driving bits which code the same amount of time slots as if they would have been coded in a prior art power of 2 coding or less, i.e. in this embodiment C11, C10, C9, ..., C5, C4 are directly connected to the input bits B11, B10, B9, ..., B5, B4. The driving bits C8, C7, C6, C5, C4 are each one time slot short compared to the time slots that would be assigned in the prior art. Hence 5 time slots need to be compensated for in the least significant bits. As illustrated in FIG. 8, the active bits in this range having 1 time slot short are counted, B3 B2 B1 B0 (input) covers [0 ... 15]. The needed range to be covered for compensating for the 5 time slots which are short in the middle significant bits is the sum of both, as illustrated in FIG.9, hence [0 ... 20]. C3 C2 C1 C0, including the extra CX covers [0 ... 21]. Depending on the outcome of the addition, CX has a value 1 or 0, to be able to compensate for the lacking time slots, as illustrated in FIG. 10.

[0049] One implementation of a coding table for this example may be as illustrated in Table 4. In this table, the first column gives the definition in old time slots, corresponding to the shifting of the line. The last two columns give the definition in terms of new time slots, taking into account the additional delay between driving the 1st line and the second line. The second and the third column give the value of the code driven in each of the blocks, respectively.

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Table 4

	Sub-Frame number (length code a, code b)	code driven after running one a	code driven after running one b		
5	0 (128,/)	C10	/	2k=256	
	1 (0,128)	C0	C11	2k+1=1	2k-1=255
	2 (1,127)	C1	C11	2k+1=3	2k-1=253
10	3 (128,/)	C9	/	2k=256	
	4 (5,123)	C3	C11	2k+1=11	2k-1=245
	5 (112,16)	C11	C5	2k+1=225	2k-1=31
	6 (128,/)	C10	/	2k=256	
15	7 (31,97)	C6	C11	2k+1=63	2k-1=193
	8 (64,64)	C11	C7	2k+1=129	2k-1=127
	9 (128,/)	C10	/	2k=256	
20	10 (7,121)	C4	C11	2k+1=15	2k-1=241
	11 (128,/)	C9	/	2k=256	
	12 (2,126)	C2	C11	2k+1=5	2k-1=251
	13 (128,/)	C10	/	2k=256	
25	14 (127,1)	C8	CX	2k+1=255	2k-1=1
	15 (128,/)	C11	/	2k=256	

[0050] This table (Table 4) is assigned values as if the image code were 11 bits, hence 1 bit less than the actual input data, meaning that there would be $2^0/N = 2^{11}/16 = 128$ time slots per sub-frame. The recoding of the bits in accordance with the present invention, however, takes into account the amended number of time slots assigned. If, during the first selection, running a data bit during k=128 time slots is proposed, in the actual implementation 256 (2k) time slots are used for running that data bit. In such case, no second selection takes place. If, during the first selection, another value k is proposed for running the data bit, in the actual implementation 2k+1 time slots are used. During the subsequent second selection another value k is proposed for running another data bit, and in the actual implementation 2k-1 time slots are used.

[0051] For instance, in the example of Table 4, the proposed value for the first subframe is 128. This means that the bit C10 is run for 256 time slots upon the first selection, and that no second selection is required. In the second subframe, the proposed values are 0 for the first selection and 128 for the second selection. This means that the bit C0 is run for 1 time slot upon the first selection, and the bit C11 is run for 255 time slots upon the second selection.

[0052] It can be seen that the length of the pulses becomes 2k or 2k+1 for pulses in the first selection, and 2k-1 for pulses in the second selection, with k being the number of time slots proposed if the image code would consist of n=11 bits.

[0053] When implementing the above example of Table 4, the minimal driving speed required for 60 Hz frames, 16 subframes per frame, 128 time slots per frame, and 2 lines selected per time slot, would be $f_{data} = 60 * 16 * 128 * 2 = 246$ kHz. It can thus be seen that advantageously an additional bit of color depth may be obtained, without having to increase the data rate. Or alternatively worded: the demanded driver speed is only half the prior art implementation for an equal color depth.

[0054] Similarly, other examples can be given.

[0055] For instance, a 9-bit input string may be coded as if it were an 8-bit input string. 8 subframes are used. Each subframe comprises maximal (any multiple of) 32 lines. Each image comprises in this approach typically 32 lines. If the image consists of more than 32 lines, the lines are grouped in blocks. e.g. a display of 1000 lines will be driven with this code as 32 blocks of 32 lines, whereas the last 24 lines are virtual lines. Driving each subframe comprises driving maximum 2 pulses of in total 64 timeslots.

[0056] The 9-bit input code may have a binary representation B8 B7 B6 B5 B4 B3 B2 B1 B0.

Time slots acc to prior art	1	2	4	8	16	32	64	128	256
Bit number	B0	B1	B2	B3	B4	B5	B6	B7	B8

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the number of time slots assigned to each bit value can be as follows:

Time slots acc to invention	1	3	5	11	15	31	64	126	255	1
Bit number	C0	C1	C2	C3	C4	C5	C6	C7	C8	CX

[0057] This shows that the least significant bit B0 is assigned 1 time slot (indicated by C0), the second least significant bit B1 (indicated by C1) is assigned 3 time slots, where in the prior art it would have been $2^{m-1}=2$, m being the position of the bit in the code, bit B2 (indicated by C2) is assigned 5 time slots, and bit B3 (indicated by C3) is assigned 11 time slots. In the example illustrated, bits C1 to C3 are being assigned more time slots than would have been the case in the prior art. In accordance with embodiments of the present invention, the number of time slots assigned to the least significant bits is uneven.

[0058] Correspondingly, other bits, the middle significant bits B4, B5 and the most significant bits B7, B8 each are assigned less time slots, for instance one time slot less for B4, B5 and B8 (indicated C4, C5 and C8), and 2 time slots less for B7 (indicated C7), than would have been the case in the prior art.

[0059] An intermediate significant bit between the middle significant bits and the most significant bit, B6 is implemented just at its actual value according to its position in the code, if a power of 2 is taken. The intermediate bit 6 will be assigned $2^6 = 64$ time slots (indicated by C6).

[0060] The assigning of the number of time slots to each of the bit values (e.g. more than 2^{m-1} for at least one of the least significant bits, in this embodiment is less than 2^{m-1} for at least one of the middle significant bits and for at least one of the most significant bits, and exactly 2^{m-1} for an intermediate significant bits, m being the position of the corresponding bit in the image code) must be such that all intensity values can be covered. In accordance with embodiments of the present invention, this can be done by assigning a value 1 to the otherwise unused time slot CX.

[0061] The coding table may be implemented as illustrated in FIG. 11 to FIG. 13. The driving bits which code the same amount of time slots as if they would have been coded in a prior art power of 2 coding or less, i.e. in this embodiment C8, C7, C6, C5, C4 are directly connected to the input bits B8, B7, B6, B5, B4. The driving bits C8, C5, C4 are each one time slot short compared to the time slots that would be assigned in the prior art, and C7 is two time slots short. Hence 5 time slots need to be compensated for in the least significant bits. As illustrated in FIG. 12, the active bits in this range having time slots short are counted, B3 B2 B1 B0 (input) covers [0 ... 15]. The needed range to be covered for compensating for the 5 time slots which are short in the middle significant bits is the sum of both, as illustrated in FIG.9, hence [0 ... 20]. C3 C2 C1 C0, including the extra CX covers [0 ... 21]. Depending on the outcome of the addition, CX has a value 1 or 0, to be able to compensate for the lacking time slots, as illustrated in FIG. 12.

[0062] One implementation of a coding table for this example may be as illustrated in Table 5. In this table, the first column gives the definition in old time slots, corresponding to the shifting of the line. The last two columns give the definition in terms of new time slots, taking into account the additional delay between driving the 1st line and the second line. The second and the third column give the value of the code driven in each of the blocks, respectively.

Table 5

Sub-Frame number (length code a, code b)	code driven after running one a	code driven after running one b		
0 (0,32)	C0	C7	$2k+1=1$	$2k-1=63$
1 (1,31)	C1	C8	$2k+1=3$	$2k-1=61$
2 (2,30)	C2	C8	$2k+1=5$	$2k-1=59$
3 (5,27)	C3	C8	$2k+1=11$	$2k-1=53$
4 (7,25)	C4	C8	$2k+1=15$	$2k-1=49$
5 (16,16)	C8	C5	$2k+1=33$	$2k-1=31$
6 (31,1)	C7	CX	$2k+1=63$	$2k-1=1$
7 (32,1)	C6	/	$2k=64$	

[0063] This table (Table 5) is assigned values as if the image code were 8 bits, hence 1 bit less than the actual input data, meaning that there would be $2^n/N = 2^8/8 = 32$ time slots per sub-frame. The recoding of the bits in accordance with the present invention, however, takes into account the amended number of time slots assigned. If, during the first selection, running a data bit during $k=32$ time slots is proposed, in the actual implementation $64 (2k)$ time slots are used

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for running that data bit, In such case, no second selection takes place. If, during the first selection, another value k is proposed for running the data bit, in the actual implementation 2k+1 time slots are used. During the subsequent second selection another value k is proposed for running another data bit, and in the actual implementation 2k-1 time slots are used.

5 [0064] For instance, in the example of Table 5, the proposed values for the first subframe are 0 for the first selection and 32 for the second selection. This means that the bit C0 is run for 1 time slot upon the first selection, and that during a second selection the bit C7 is run for 63 time slots. In the second subframe, the proposed values are 1 for the first selection and 31 for the second selection. This means that the bit C1 is run for 3 time slots upon the first selection, and the bit C8 is run for 61 time slots upon the second selection.

10 [0065] It can be seen that the length of the pulses becomes 2k or 2k+1 for pulses in the first selection, and 2k-1 for pulses in the second selection, with k being the number of time slots proposed if the image code would consist of n=8 bits. Or in other words: if the separation between the driven lines corresponds to k lines, the block is driven 2k+1 or 2k-1 time slots.

15 [0066] When implementing the above example of Table 5, the minimal driving speed required for 60 Hz frames, 8 subframes per frame, 32 time slots per frame, and 2 lines selected per time slot, would be $f_{data} = 60 * 8 * 32 * 2 = 31$ kHz. It can thus be seen that advantageously an additional bit of color depth may be obtained, without having to increase the data rate. Or alternatively worded: the demanded driver speed is only half the prior art implementation for an equal color depth.

20 [0067] For a 13-bit input code B12 B11 B10 B9 B8 B7 B6 B5 B4 B3 B2 B1 B0, for instance, 16 subframes may be used. Each subframe comprises maximal (any multiple of) 256 lines. Each image comprises in this approach typically 256 lines. If there are less lines in the display, virtual lines are added up to 256 lines. In the timing they are considered to be present, but they are not actually driven. If the image consists of more than 256 lines, the lines are grouped in blocks. e.g. a display of 1000 lines will be driven with this code as 256 blocks of 4 lines. Driving each subframe comprises driving maximum 2 pulses of in total 512 timeslots.

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Time slots acc to prior art	1	2	4	8	16	32	64	128	256	512	1024	2048	4096
Bit number	B0	B1	B2	B3	B4	B5	B6	B7	B8	B9	B10	B11	B12

30 The number of time slots assigned to each bit value can be as follows:

35

Time slots acc to invention	1	3	5	11	15	31	63	127	255	512	1024	2048	4096	1
Bit number	C0	C1	C2	C3	C4	C5	C6	C7	C8	C9	C10	C11	C12	CX

40 [0068] This shows that the least significant bit B0 is assigned 1 time slot (indicated by C0), the second least significant bit B1 (indicated by C1) is assigned 3 time slots, where in the prior art it would have been $2^{m-1}=2$, m being the position of the bit in the code, bit B2 (indicated by C2) is assigned 5 time slots, and bit B3 (indicated by C3) is assigned 11 time slots. In the example illustrated, bits C1 to C3 are the ones being assigned more time slots than would have been the case in the prior art. In accordance with this embodiment of the present invention, the number of time slots assigned to the least significant bits should always be uneven.

45 [0069] Correspondingly, the middle significant bits B4 to B8 each are assigned less time slots, for instance one time slot less, than would have been the case in the prior art. In accordance with embodiments of the present invention, the number of time slots assigned to the middle significant bits in this embodiment can be uneven.

50 [0070] The most significant bits B9 to B12 are implemented just at their actual value according to their position in the code, if a power of 2 is taken. The MSB bit B12 will be assigned $2^{12} = 4096$ time slots (indicated C12), B11 will be assigned $2^{11} = 2048$ time slots (indicated by C11), B10 will be assigned to $2^{10} = 1024$ time slots (indicated by C10), bit B9 will be assigned 512 time slots (indicated by C9).

55 [0071] The assigning of the number of time slots to each of the bit values (e.g. more than 2^{m-1} for at least one of the least significant bits, less than 2^{m-1} for at least one of the middle significant bits, and exactly 2^{m-1} for the most significant bits, m being the position of the corresponding bit in the image code) must be such that all intensity values can be covered. In accordance with embodiments of the present invention, this can be done by assigning a value 1 to the otherwise unused time slot CX.

[0072] The coding table may be implemented as illustrated in FIG. 14 to FIG. 16. The driving bits which code the same amount of time slots as if they would have been coded in a prior art power of 2 coding or less, i.e. in this embodiment

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C12, C11, C10, C9, ..., C5, C4 are directly connected to the input bits B12, B11, B10, B9, ..., B5, B4. The driving bits C8, C7, C6, C5, C4 are each one time slot short compared to the time slots that would be assigned in the prior art. Hence 5 time slots need to be compensated for in the least significant bits. As illustrated in FIG. 14, the active bits in this range having 1 time slot short are counted, B3 B2 B1 B0 (input) covers [0 ... 15]. The needed range to be covered for compensating for the 5 time slots which are short in the middle significant bits is the sum of both, as illustrated in FIG.15, hence [0 ... 20]. C3 C2 C1 C0, including the extra CX covers [0 ... 21]. Depending on the outcome of the addition, CX has a value 1 or 0, to be able to compensate for the lacking time slots, as illustrated in FIG. 16.

[0073] One implementation of a coding table for this example may be as illustrated in Table 6. In this table, the first column gives the definition in old time slots, corresponding to the shifting of the line. The last two columns give the definition in terms of new time slots, taking into account the additional delay between driving the 1st line and the second line. The second and the third column give the value of the code driven in each of the blocks, respectively.

Table 6

Sub-Frame number (length code a, code b)	code driven after running one a	code driven after running one b		
0 (0,256)	CX	C12	$2k+1=1$	$2k-1=511$
1 (0,256)	C0	C12	$2k+1=1$	$2k-1=511$
2 (1,255)	C1	C12	$2k+1=3$	$2k-1=509$
3 (2,254)	C2	C12	$2k+1=5$	$2k-1=507$
4 (5,251)	C3	C11	$2k+1=11$	$2k-1=501$
5 (7,249)	C4	C11	$2k+1=15$	$2k-1=497$
6 (13,243)	C11	C12	$2k+1=27$	$2k-1=485$
7 (256,/)	C10	/	$2k=512$	
8 (15,241)	C5	C12	$2k+1=31$	$2k-1=481$
9 (31,225)	C6	C12	$2k+1=63$	$2k-1=449$
10 (63,193)	C7	C12	$2k+1=127$	$2k-1=385$
11 (127,129)	C8	C12	$2k+1=255$	$2k-1=257$
12 (255,1)	C11	C12	$2k+1=511$	$2k-1=1$
13 (256,/)	C9	/	$2k=512$	
14 (256,/)	C11	/	$2k=512$	
15 (256,/)	C10	/	$2k=512$	

[0074] This table (Table 6) is assigned values as if the image code were 12 bits, hence 1 bit less than the actual input data, meaning that there would be $2^N/N = 2^{12}/16 = 256$ time slots per sub-frame. The recoding of the bits in accordance with the present invention, however, takes into account the amended number of time slots assigned. If, during the first selection, running a data bit during $k=256$ time slots is proposed, in the actual implementation 512 ($2k$) time slots are used for running that data bit, In such case, no second selection takes place. If, during the first selection, another value k is proposed for running the data bit, in the actual implementation $2k+1$ time slots are used. During the subsequent second selection another value k is proposed for running another data bit, and in the actual implementation $2k-1$ time slots are used.

[0075] For instance, in the example of Table 6, the proposed values for the first subframe are 0 for the first selection and 256 for the second selection. This means that the bit CX is run for 1 time slot upon the first selection, and that during a second selection the bit C12 is run for 511 time slots. In the second subframe, the proposed values are again 0 for the first selection and 256 for the second selection. This means that the bit C0 is run for 1 time slot upon the first selection, and the bit C12 is run for 511 time slots upon the second selection. The proposed values for the third subframe are 1 for the first selection and 255 for the second selection. This means that the bit C1 is run for 3 time slots upon the first selection, and the bit C12 is run for 509 time slots upon the second selection.

[0076] It can be seen that the length of the pulses becomes $2k$ or $2k+1$ for pulses in the first selection, and $2k-1$ for pulses in the second selection, with k being the number of time slots proposed if the image code would consist of $n=12$ bits (although it actually consists of 13 bits).

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[0077] When implementing the above example of Table 6, the minimal driving speed required for 60 Hz frames, 16 subframes per frame, 512 time slots per frame, and 2 lines selected per time slot, would be $f_{data} = 60 * 16 * 512 * 2 = 983$ kHz. Advantageously an additional bit of color depth may be obtained, without having to increase the data rate. Or alternatively worded: the demanded driver speed is only half the prior art implementation for an equal color depth.

[0078] Similarly, but explained in less detail, for a 14-bit input code B13 B12 B11 B10 B9 B8 B7 B6 B5 B4 B3 B2 B1 B0, for instance, 16 subframes may be used. Each subframe comprises maximal (any multiple of) 512 lines. Each image comprises in this approach typically 512 lines. If there are less lines in the display, virtual lines are added up to 512 lines. In the timing they are considered to be present, but they are not actually driven. If the image consists of more than 512 lines, the lines are grouped in blocks. e.g. a display of 1000 lines will be driven with this code as 512 blocks of 2 lines, whereas the last 24 lines are virtual lines. Driving each subframe comprises driving maximum 2 pulses of in total 1024 timeslots.

Time slots acc to prior art	1	2	4	8	16	32	64	128	256	512	1024	2048	4096	8192
Bit number	B0	B1	B2	B3	B4	B5	B6	B7	B8	B9	B10	B11	B12	B13

The number of time slots assigned to each bit value can be as follows:

Time slots acc to invention	1	3	5	11	17	31	63	127	255	511	
Bit number	C0	C1	C2	C3	C4	C5	C6	C7	C8	C9	
Time slots acc to invention							1024	2048	4096	8191	1
Bit number							C10	C11	C12	C13	CX

[0079] This shows that the least significant bit B0 is assigned 1 time slot (indicated by C0). The bits B1, B2, B3, B4 are assigned 3, 5, 11, 17 time slots, respectively (indicated by C1, C2, C3, C4). In the example illustrated, bits C1 to C4 are the ones being assigned more time slots than would have been the case in the prior art. In accordance with this embodiment of the present invention, the number of time slots assigned to the least significant bits is uneven.

[0080] Correspondingly, the middle significant bits B5 to B9 and the most significant bit B13 each are assigned less time slots, for instance one time slot less, than would have been the case in the prior art. In accordance with embodiments of the present invention, the number of time slots assigned to the middle significant bits and to the most significant bit in this embodiment is uneven.

[0081] The most significant bits B10 to B12 are implemented just at their actual value according to their position in the code, if a power of 2 is taken. The MSB bit B12 will be assigned $2^{12} = 4096$ time slots (indicated C12), B11 will be assigned $2^{11} = 2048$ time slots (indicated by C11), and B10 will be assigned to $2^{10} = 1024$ time slots (indicated by C10).

[0082] The assigning of the number of time slots to each of the bit values (e.g. more than 2^{m-1} for some of the bits, less than 2^{m-1} for at least one of other bits, and exactly 2^{m-1} for yet at least one other bit, m being the position of the corresponding bit in the image code) must be such that all intensity values can be covered. In accordance with embodiments of the present invention, this can be done by assigning a value 1 to the otherwise unused time slot CX.

[0083] The coding table may be implemented as illustrated in FIG. 17, FIG. 18, FIG. 19a and FIG. 19b. The driving bits which code the same amount of time slots as if they would have been coded in a prior art power of 2 coding or less, i.e. in this embodiment C13, C12, C11, C10, C9, ..., C5 are directly connected to the input bits B13, B12, B11, B10, B9, ..., B5. The driving bits C13, C9, C8, C7, C6, C5 are each one time slot short compared to the time slots that would be assigned in the prior art. Hence 6 time slots need to be compensated for in the least significant bits. As illustrated in FIG. 17, the active bits in this range having 1 time slot short are counted. B4 B3 B2 B1 B0 (input) covers [0 ... 31]. The needed range to be covered for compensating for the 6 time slots which are short in the middle significant bits is the sum of both, as illustrated in FIG. 18, hence [0 ... 37]. C4 C3 C2 C1 C0, including the extra CX covers [0 ... 38]. Depending on the outcome of the addition, CX has a value 1 or 0, to be able to compensate for the lacking time slots, as illustrated in FIG. 19a and FIG. 19b.

[0084] One implementation of a coding table for this example may be as illustrated in Table 7. In this table, the first column gives the definition in old time slots, corresponding to the shifting of the line. The last two columns give the definition in terms of new time slots, taking into account the additional delay between driving the 1st line and the second line. The second and the third column give the value of the code driven in each of the blocks, respectively.

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Table 7

	Sub-Frame number (length code a, code b)	code driven after running one a	code driven after running one b		
5	0 (0,512)	CX	C13	$2k+1=1$	$2k-1=1023$
	1 (0,512)	C0	C13	$2k+1=1$	$2k-1=1023$
10	2 (1,511)	C1	C13	$2k+1=3$	$2k-1=1021$
	3 (2,510)	C2	C13	$2k+1=5$	$2k-1=1019$
15	4 (5,507)	C3	C13	$2k+1=11$	$2k-1=1013$
	5 (8,504)	C4	C13	$2k+1=17$	$2k-1=1007$
20	6 (15,497)	C5	C13	$2k+1=31$	$2k-1=993$
	7 (31,481)	C6	C13	$2k+1=63$	$2k-1=961$
	8 (63,449)	C7	C12	$2k+1=127$	$2k-1=897$
25	9 (66,446)	C12	C12	$2k+1=133$	$2k-1=891$
	10 (127,385)	C8	C12	$2k+1=255$	$2k-1=769$
	11 (255,257)	C9	C12	$2k+1=511$	$2k-1=513$
	12 (446,66)	C12	C13	$2k+1=893$	$2k-1=131$
30	13 (512,/)	C11	/	$2k=1024$	
	14 (512,/)	C11	/	$2k=1024$	
	15 (512,/)	C10	/	$2k=1024$	

35 **[0085]** This table (Table 7) is assigned values as if the image code were 13 bits, hence 1 bit less than the actual input data, meaning that there would be $2^N/N = 2^{13}/16 = 512$ time slots per sub-frame. The recoding of the bits in accordance with the present invention, however, takes into account the amended number of time slots assigned. If, during the first selection, running a data bit during $k=512$ time slots is proposed, in the actual implementation 1024 ($2k$) time slots are used for running that data bit. In such case, no second selection takes place. If, during the first selection, another value

40 k is proposed for running the data bit, in the actual implementation $2k+1$ time slots are used. During the subsequent second selection another value k is proposed for running another data bit, and in the actual implementation $2k-1$ time slots are used.

the length of the pulses becomes $2k$ or $2k+1$ for pulses in the first selection, and $2k-1$ for pulses in the second selection, with k being the number of time slots proposed if the image code would consist of $n=13$ bits (although it actually consists of 14 bits).

45 **[0086]** As a further example, for a 15-bit input code B14 B13 B12 B11 B10 B9 B8 B7 B6 B5 B4 B3 B2 B1 B0, for instance, 16 subframes may be used. Each subframe comprises maximal (any multiple of) 1024 lines. Each image comprises in this approach typically 1024 lines. If there are less lines in the display, virtual lines are added up to 1024 lines. In the timing they are considered to be present, but they are not actually driven. If the image consists of more than

50 1024 lines, the lines are grouped in blocks. e.g. a display of 4000 lines will be driven with this code as 1024 blocks of 4 lines, whereas the last 96 lines are virtual lines. Driving each subframe comprises driving maximum 2 pulses of in total 2048 timeslots.

55	Time slots acc to prior art	1	2	4	8	16	32	64	128	256	512	1024
	Bit number	B0	B1	B2	B3	B4	B5	B6	B7	B8	B9	B10
	Time slots acc to prior art								2048	4096	8192	16384

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(continued)

Bit number		B11	B12	B13	B14
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5 **[0087]** The number of time slots assigned to each bit value can be as follows:

Time slots acc to invention	1	3	5	11	19	31	63	127	255	511	1023
Bit number	C0	C1	C2	C3	C4	C5	C6	C7	C8	C9	C10
Time slots acc to invention							2048	4096	8191	16383	1
Bit number							C11	C12	C13	C14	CX

15 **[0088]** This shows that the least significant bit B0 is assigned 1 time slot (indicated by C0). The bits B1, B2, B3, B4 are assigned 3, 5, 11, 19 time slots, respectively (indicated by C1, C2, C3, C4). In the example illustrated, bits C1 to C4 are the ones being assigned more time slots than would have been the case in the prior art. In accordance with this embodiment of the present invention, the number of time slots assigned to the least significant bits is uneven.

20 **[0089]** The middle significant bits B5 to B10 and the most significant bits B13 and B14 each are assigned less time slots, for instance one time slot less, than would have been the case in the prior art. In accordance with embodiments of the present invention, the number of time slots assigned to the middle significant bits and to the most significant bits in this embodiment is uneven.

25 **[0090]** The intermediate significant bits B11 and B12 between the middle significant bits and the most significant bits are implemented just at their actual value according to their position in the code, if a power of 2 is taken. The intermediate significant bit B12 will be assigned $2^{12} = 4096$ time slots (indicated C12), and B11 will be assigned $2^{11} = 2048$ time slots (indicated by C11).

30 **[0091]** The assigning of the number of time slots to each of the bit values (e.g. more than 2^{m-1} for some of the bits, less than 2^{m-1} for at least one of other bits, and exactly 2^{m-1} for yet at least one other bit, m being the position of the corresponding bit in the image code) must be such that all intensity values can be covered. In accordance with embodiments of the present invention, this can be done by assigning a value 1 to the otherwise unused time slot CX.

35 **[0092]** The coding table may be implemented as illustrated in FIG. 20, FIG. 21, FIG. 22a and FIG. 22b. The driving bits which code the same amount of time slots as if they would have been coded in a prior art power of 2 coding or less, i.e. in this embodiment C14, C13, C10, C9, ..., C5 are directly connected to the input bits B14, B13, B10, B9, ..., B5. The driving bits C14, C13, C10, C9, C8, C7, C6, C5 are each one time slot short compared to the time slots that would be assigned in the prior art. Hence 8 time slots need to be compensated for in the least significant bits. As illustrated in FIG. 20, the active bits in this range having 1 time slot short are counted. B4 B3 B2 B1 B0 (input) covers [0 ... 31]. The needed range to be covered for compensating for the 8 time slots which are short in the middle significant bits is the sum of both, as illustrated in FIG.21, hence [0 ... 39]. C4 C3 C2 C1 C0, including the extra CX covers [0 ... 40]. Depending on the outcome of the addition, CX has a value 1 or 0, to be able to compensate for the lacking time slots, as illustrated in FIG. 21a and FIG. 21b.

40 **[0093]** One implementation of a coding table for this example may be as illustrated in Table 8. In this table, the first column gives the definition in old time slots, corresponding to the shifting of the line. The last two columns give the definition in terms of new time slots, taking into account the additional delay between driving the 1st line and the second line. The second and the third column give the value of the code driven in each of the blocks, respectively.

45 Table 8

Sub-Frame number (length code a, code b)	code driven after running one a	code driven after running one b		
0 (0,1024)	CX	C14	$2k+1=1$	$2k-1=2047$
1 (0,1024)	C0	C14	$2k+1=1$	$2k-1=2047$
2 (1,1023)	C1	C14	$2k+1=3$	$2k-1=2045$
3 (2,1022)	C2	C14	$2k+1=5$	$2k-1=2043$

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(continued)

	Sub-Frame number (length code a, code b)	code driven after running one a	code driven after running one b		
5	4 (5,1019)	C3	C14	2k+1=11	2k-1=2037
	5 (9,1015)	C4	C14	2k+1=19	2k-1=2029
10	6 (15,1009)	C5	C14	2k+1=31	2k-1=2017
	7 (31,993)	C6	C14	2k+1=63	2k-1=1985
15	8 (63,961)	C7	C13	2k+1=127	2k-1=1921
	9 (66,958)	C12	C13	2k+1=133	2k-1=1915
20	10 (127,897)	C8	C13	2k+1=255	2k-1=1793
	11 (255,769)	C9	C13	2k+1=511	2k-1=1537
25	12 (511,513)	C10	C13	2k+1=1023	2k-1=1025
	13 (957,67)	C12	C14	2k+1=1915	2k-1=133
	14 (1024,/))	C12	/	2k=2048	
30	15 (1024,/))	C11	/	2k=2048	

[0094] This table (Table 8) is assigned values as if the image code were 14 bits, hence 1 bit less than the actual input data, meaning that there would be $2^n/N = 2^{14}/16 = 1024$ time slots per sub-frame. The recoding of the bits in accordance with the present invention, however, takes into account the amended number of time slots assigned. If, during the first selection, running a data bit during k=1024 time slots is proposed, in the actual implementation 2048 (2k) time slots are used for running that data bit. In such case, no second selection takes place. If, during the first selection, another value k is proposed for running the data bit, in the actual implementation 2k+1 time slots are used. During the subsequent second selection another value k is proposed for running another data bit, and in the actual implementation 2k-1 time slots are used.

[0095] The length of the pulses thus becomes 2k or 2k+1 for pulses in the first selection, and 2k-1 for pulses in the second selection, with k being the number of time slots proposed if the image code would consist of n=14 bits (although it actually consists of 15 bits).

[0096] As a last example, for a 16-bit input code B15 B14 B13 B12 B11 B10 B9 B8 B7 B6 B5 B4 B3 B2 B1 B0, for instance, 16 subframes may be used. Each subframe comprises maximal (any multiple of) 2048 lines. Each image comprises in this approach typically 2048 lines. If there are less lines in the display, virtual lines are added up to 2048 lines. In the timing they are considered to be present, but they are not actually driven. If the image consists of more than 2048 lines, the lines are grouped in blocks. e.g. a display of 4000 lines will be driven with this code as 2048 blocks of 2 lines, whereas the last 96 lines are virtual lines. Driving each subframe comprises driving maximum 2 pulses of in total 4096 timeslots.

Time slots acc to prior art	1	2	4	8	16	32	64	128	256	512	1024	2048
Bit number	B0	B1	B2	B3	B4	B5	B6	B7	B8	B9	B10	B11
Time slots acc to prior art									4096	8192	16384	32768

(continued)

Bit number		B12	B13	B14	B15
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5 **[0097]** The number of time slots assigned to each bit value can be as follows:

Time slots acc to invention	1	3	5	11	21	31	63	127	255	511	1023	2047
Bit number	C0	C1	C2	C3	C4	C5	C6	C7	C8	C9	C10	C11
Time slots acc to invention								4096	8191	16383	32767	1
Bit number								C12	C13	C14	C15	CX

15 **[0098]** This shows that the least significant bit B0 is assigned 1 time slot (indicated by C0). The bits B1, B2, B3, B4 are assigned 3, 5, 11, 21 time slots, respectively (indicated by C1, C2, C3, C4). In the example illustrated, bits C1 to C4 are the ones being assigned more time slots than would have been the case in the prior art. In accordance with this embodiment of the present invention, the number of time slots assigned to the least significant bits is uneven.

20 **[0099]** The middle significant bits B5 to B11 and the most significant bits B13 to B15 each are assigned less time slots, for instance each one time slot less, than would have been the case in the prior art. In accordance with embodiments of the present invention, the number of time slots assigned to the middle significant bits and to the most significant bits in this embodiment is uneven.

25 **[0100]** The intermediate significant bit B12 between the middle significant bits and the most significant bits is implemented just at its actual value according to its position in the code, if a power of 2 is taken. The intermediate significant bit B12 will be assigned $2^{12} = 4096$ time slots (indicated C12).

30 **[0101]** The assigning of the number of time slots to each of the bit values (e.g. more than 2^{m-1} for some of the bits, less than 2^{m-1} for at least one of other bits, and exactly 2^{m-1} for yet at least one other bit, m being the position of the corresponding bit in the image code) must be such that all intensity values can be covered. In accordance with embodiments of the present invention, this can be done by assigning a value 1 to the otherwise unused time slot CX.

35 **[0102]** The coding table may be implemented as illustrated in FIG. 23, FIG. 24, FIG. 25a and FIG. 25b. The driving bits which code the same amount of time slots as if they would have been coded in a prior art power of 2 coding or less, i.e. in this embodiment C15, C14, C13, C10, C9, ..., C5 are directly connected to the input bits B15, B14, B13, B10, B9, ..., B5. The driving bits C15, C14, C13, C10, C9, C8, C7, C6, C5 are each one time slot short compared to the time slots that would be assigned in the prior art. Hence 10 time slots need to be compensated for in the least significant bits. As illustrated in FIG. 23, the active bits in this range having 1 time slot short are counted. B4 B3 B2 B1 B0 (input) covers [0 ... 31]. The needed range to be covered for compensating for the 10 time slots which are short in the middle significant bits and most significant bits is the sum of both, as illustrated in FIG.24, hence [0 ... 41]. C4 C3 C2 C1 C0, including the extra CX covers [0 ... 42]. Depending on the outcome of the addition, CX has a value 1 or 0, to be able to compensate for the lacking time slots, as illustrated in FIG. 25a and FIG. 25b.

40 **[0103]** One implementation of a coding table for this example may be as illustrated in Table 9. In this table, the first column gives the definition in old time slots, corresponding to the shifting of the line. The last two columns give the definition in terms of new time slots, taking into account the additional delay between driving the 1st line and the second line. The second and the third column give the value of the code driven in each of the blocks, respectively.

Table 9

Sub-Frame number (length code a, code b)	code driven after running one a	code driven after running one b		
0 (0,2048)	CX	C14	$2^{k+1}=1$	$2^{k-1}=4095$
1 (0,2048)	C0	C14	$2^{k+1}=1$	$2^{k-1}=4095$
2 (1,2047)	C1	C14	$2^{k+1}=3$	$2^{k-1}=4093$

(continued)

	Sub-Frame number (length code a, code b)	code driven after running one a	code driven after running one b		
5	3 (2,2046)	C2	C14	$2k+1=5$	$2k-1=4091$
	4 (4,2044)	C14	C15	$2k+1=9$	$2k-1=4087$
10	5 (5,2043)	C3	C15	$2k+1=11$	$2k-1=4085$
	6 (10,2038)	C4	C15	$2k+1=21$	$2k-1=4075$
15	7 (15,2033)	C5	C15	$2k+1=31$	$2k-1=4065$
	8 (31,2017)	C6	C15	$2k+1=63$	$2k-1=4033$
20	9 (63,1985)	C7	C15	$2k+1=127$	$2k-1=3969$
	10 (127,1921)	C8	C15	$2k+1=255$	$2k-1=3841$
25	11 (255,1793)	C9	C15	$2k+1=511$	$2k-1=3585$
	12 (511,1537)	C10	C13	$2k+1=1023$	$2k-1=3073$
30	13 (513,1535)	C15	C13	$2k+1=1027$	$2k-1=3069$
	14 (1023,1025)	C11	C13	$2k+1=2047$	$2k-1=2049$
35	15 (2048,/)	C12	/	$2k=4096$	

[0104] This table (Table 9) is assigned values as if the image code were 15 bits, hence 1 bit less than the actual input data, meaning that there would be $2^n/N = 2^{15}/16 = 2048$ time slots per sub-frame. The recoding of the bits in accordance with the present invention, however, takes into account the amended number of time slots assigned. If, during the first selection, running a data bit during $k=2048$ time slots is proposed, in the actual implementation 4096 ($2k$) time slots are used for running that data bit. In such case, no second selection takes place. If, during the first selection, another value k is proposed for running the data bit, in the actual implementation $2k+1$ time slots are used. During the subsequent second selection another value k is proposed for running another data bit, and in the actual implementation $2k-1$ time slots are used.

[0105] The length of the pulses thus becomes $2k$ or $2k+1$ for pulses in the first selection, and $2k-1$ for pulses in the second selection, with k being the number of time slots proposed if the image code would consist of $n=15$ bits (although it actually consists of 16 bits).

[0106] FIG. 5 schematically shows a digital driven AMOLED display architecture 50, as a particular type of active matrix display, in accordance with an aspect of the present invention. This architecture 50 comprises an AMOLED display 55 comprising an array of OLED pixel elements (not illustrated in detail in FIG. 5) logically organised in rows and columns. The driving circuitry for driving these OLED pixel elements is based on digital select line (row) driving circuitry 51 using two select signals for at least one of the rows, for instance implemented by running ones, and digital data line (column) driving circuitry 52. Digital driving can be done for instance using Pulse Density Modulation methods, for instance Pulse Width Modulation. It is an advantage of this architecture as compared to existing digital driving architectures that switching of the transistors in the backplane of the display can be slower and that the driving circuitry can be less complex and less space consuming.

[0107] In a method for digital pixel driving according to an aspect of the present invention, the select line driving circuitry 51 provides two select signals, for instance two running ones, providing a first selection and a second selection, thereby

sequentially selecting at least one, and preferably at least 35% of the plurality of rows, twice within each sub-frame. Within the sub-frames which are selected twice, the second select signal, for instance the second running one, has a fixed predetermined delay with respect to the first running one. This predetermined delay can be different for each sub-frame, thus enabling different digital output combinations, as further explained.

5 **[0108]** The method first and second selection of rows is as described in WO 2014/068017, The only difference is the number of time slots assigned to the bit values, as explained above.

[0109] In the example shown in Table 4, in the first sub-frame, the fixed delay between the first running one and the second running one corresponds to the duration of 256 time slots. This means that no second selection will be made. In the 256 time slots of the first sub-frame, the pixel is driven by one of the most significant bits (C10). If C10 is a logical 1, the pixel is ON during these 256 time slots; if C10 is a logical 0, the pixel is OFF. In the second sub-frame the fixed delay between the first running one and the second running one corresponds to the duration of 1 time slot (i.e., $2k+1$). In the first time slot of the second sub-frame the pixel has bit value C0 and in the remaining 255 time slots of the second sub-frame the most significant bit (C11) drives the pixel. If the most significant bit is a logical 1, the pixel is ON during these 255 time slots; if the most significant bit is a logical 0, the pixel is OFF. In the third sub-frame the fixed delay between the first running one and the second running one corresponds to the duration of 3 time slots (i.e., $2k+1$). In the first three time slots of the third sub-frame one of the least significant bits (C1) drives the pixel, and in the remaining 253 time slots of the third sub-frame again the most significant bit (C11) drives the pixel. This continues similarly for the other subframes.

20 **[0110]** In another aspect, the present invention relates to digital driving circuitry for driving an active matrix display such as, but not limited thereto, an AMOLED display arranged with pixels, the display comprising, for instance, LED pixel elements or OLED pixel elements such as fluorescent OLEDs, phosphorescent OLEDs, or light-emitting polymers, or Quantum dot LEDs (QLEDs). The pixels can be logically arranged in rows and columns, so the display forms a matrix capable of displaying images in consecutive frames of a certain duration.

25 **[0111]** The digital driving circuitry may comprise digital select line driving circuitry 51 for sequentially selecting the plurality of rows and digital data line driving circuitry 52 for writing the digital image code, represented by an n-bit image code, to corresponding pixels in a selected row. The digital select line driving circuitry 51 is adapted for sequentially selecting, within one sub-frame, at least one of the plurality of rows twice, so as to, upon a first selection, write a first digital code to the selected row and, upon a second selection, write a second digital code to the selected row, there being a predetermined time delay between the second selection and the first selection.

30 **[0112]** FIG. 6 shows an exemplary select line driving circuit 90 that can be used for generating a first and a second select signal under the form of a first running one and a second running one. In the select line driving circuit 90 shown in FIG. 6, the first running one and the second running one are each generated using a linear array 91, 92 of D-flip-flops, each array 91, 92 comprising maximum a single logical one, which advances through the array of flip-flops 91, 92 by one position each clock pulse. The first running one advances row by row through the lines of the display 55, progressing one row at each clock pulse. The second running one also advances row by row through the lines of the display 55, progressing one row at each clock pulse, but with a delay corresponding to a predetermined number of clock pulses with respect to the first running one. The invention is not restricted to D-flip-flops; any other suitable implementation of a dynamic or static shift register can be used. An even more compact implementation of the time delay determination circuit is a transparent latch with, for instance, two or three clocks.

40 **[0113]** As can be seen from FIG. 6, in order not to provide the first and the second select signal to the same row at the same time, a number of selectors, e.g. multiplexers 93_i , are provided, having as input both the first and the second select signal, and as output any of the first or second select signal, depending on a control signal for controlling the selectors 93_i , which control signal may be emanating from a controller and may be generated taking into account the number of time slots the code needs to be applied.

45 **[0114]** Consider, for instance, a first and a second running one are cycling through the arrays 91, 92 of D flip-flops, the first running one for instance residing in flip-flop 91_2 and the second running one residing in flip-flop 92_1 , there thus being a delay of 1 clock cycle between both. The control signal to the selectors 93_i may be such that during a first time period, equal to a first predetermined number of time slots, the first running one is applied to the rows, and during a second time period, equal to a second predetermined number of time slots, the second running one is applied to the rows. During the first time period, the first running one will be applied to the row corresponding and connected to selector 93_2 , and image data present on and provided by the data line driving circuitry 52 will be put on this corresponding row. During the second time period, the second running one will be applied to the row corresponding and connected to selector 93_1 , and image data present on and provided by the data line driving circuitry 52 will be put on this corresponding row. This way, data cannot be written to two rows simultaneously, despite the two select signals, e.g. two running ones, being present in the digital select line driving circuitry 51.

55 **[0115]** Alternatively to the embodiment illustrated in FIG. 6, a select line driving circuit 100 as illustrated in FIG. 7 can be used, in which the multiplexers 93_i have been substituted by output enable circuitry 101, grouped in blocks according to the minimum delay between selections. An odd number of clocks may be provided for driving the output enable

circuitry 101.

Claims

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1. A method for digital driving of an active matrix display (55) comprising a plurality of pixels logically organized in a plurality of rows and a plurality of columns, the display (55) being driven with a predetermined frame rate and row time, the method comprising:

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- representing n-bit wide pixel data for each of the plurality of pixels of an image frame to be displayed by a corresponding binary codeword of bit length n+1, wherein a first one (CX) of the bits composing the codeword forms a first block and the remaining n bits (C0, ..., Cn-1) of the codeword form a second block;

- dividing the image frame into a natural number N of sub-frames, each sub-frame being further divided into time slots, each time slot having a duration equal to one half of said row time during said digital driving;

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- assigning a number of said time slots to each bit of the codeword;

- within at least one sub-frame, sequentially selecting at least one of the plurality of rows twice, wherein upon a first selection a first bit of the codewords representative of pixels of the selected row is written to the pixels of the selected row and upon a second selection a second bit of the codewords representative of pixels of the selected row, different from the written first bit, is written to the pixels of the selected row, there being a predetermined time delay between the second selection and the first selection;

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characterized in that

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said step of assigning further includes assigning one time slot to the bit (CX) of the first block of the codeword and assigning one or more time slots to each bit (C0, ..., Cn-1) of the second block of the codeword in accordance with the bit position in the second block, wherein the number of time slots assigned to most significant bits of the second block are natural powers of two and the number of time slots assigned to least significant bits of the second block are odd positive integers; and

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the time delay between the second selection and the first selection in at least one of the sub-frames, expressed in a number of time slots, deviates from a natural power of two.

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2. A method according to claim 1, wherein the time delay between the second selection and the first selection in the at least one sub-frame is one time slot longer than the delay 2^k needed for sequentially selecting k rows k being a non-negative integer.

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3. A method according to claim 2, wherein upon the second selection in that at least one sub-frame, the second bit of the codewords is written to the respective pixels of the selected row during a number of time slots equal to one less than the delay 2^k needed for sequentially selecting said k rows.

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4. A method according to any of the previous claims, wherein dividing the image frame comprises dividing the image frame into sub-frames of substantially equal duration.

5. A method according to any of claims 1 to 4, n not being a natural power of two, wherein dividing the image frame into sub-frames comprises dividing the image frame into N sub-frames, wherein N is the power of 2 superior and closest to n.

6. A method according to claim 5, wherein each sub-frame is further divided into $2^n/N$ time slots.

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7. A method according to claim 6, further assigning more than 2^{m-1} time slots, $m \geq 0$, to the m^{th} bit of the second block of the codeword, if the m^{th} bit belongs to the least significant bits of the second block.

8. A method according to any of claims 6 or 7, further assigning less than 2^{m-1} time slots, $m \geq 0$, to the m^{th} bit of the second block of the codeword, if the m^{th} bit belongs to the middle significant bits of the second block.

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9. A method according to any of claims 6 to 8, further assigning 2^{m-1} time slots, $m \geq 0$, to the m^{th} bit of the second block of the codeword, if the m^{th} bit belongs to the most significant bits of the second block.

10. A method according to any of the previous claims, wherein writing the first bit of the codeword and writing the second

bit of the codeword comprises using pulse-width modulation.

- 5 11. Digital driving circuitry for driving, with a predetermined frame rate and row time, an active matrix display (55) comprising a plurality of pixels logically organized in a plurality of rows and a plurality of columns, so as to display subsequent sub-frames of an image frame to be displayed, the digital driving circuitry comprising:

10 - bit recoding hardware adapted for converting n-bit wide pixel data (B_0, \dots, B_{n-1}) of the image frame to be displayed into a corresponding binary codeword of bit length $n+1$, wherein a first one (CX) of the bits composing each codeword forms a first block and the remaining n bits (C_0, \dots, C_{n-1}) of each codeword form a second block,
 - digital select line driving circuitry (51) for sequentially selecting the plurality of rows at intervals corresponding to one row time, said row time being subdivided into two time slots of equal duration,
 the digital select line driving circuitry (51) being adapted for sequentially selecting, within one sub-frame, at least one of the plurality of rows twice, so as to, upon a first selection, write a first bit of the codeword to the selected row and, upon a second selection, write a second bit of the codeword, different than the first written bit, to the selected row, there being a predetermined time delay between the second selection and the first selection,
 15 - digital data line driving circuitry (52) for writing the codewords to corresponding pixels in a selected row,

20 **characterized in that**

one time slot is associated with the bit (CX) of the first block of the codeword and one or more time slots are associated with each bit (C_0, \dots, C_{n-1}) of the second block of the codeword in accordance with the bit position in the second block, wherein an odd integer number of time slots is associated with each one of the least significant bits in the second block and 2^m time slots are associated with each one of the most significant bits of the second block, where m denotes the bit position in the second block,
 25 the time delay between the second selection and the first selection in at least one of the sub-frames, expressed in a number of time slots, deviates from a natural power of two,
 the bit recoding hardware is configured to relay most significant bits of the n-bit wide pixel data from respective input connectors of the bit recoding hardware to corresponding output connectors of the bit recoding hardware,
 30 the bit recoding hardware comprises a bit counting circuit configured to determine active bits within the range of middle significant bits of the n-bit wide pixel data and count the differences in time slots between the 2^m time slots represented by the position m of each active bit in the pixel data and the number of time slots associated with the middle significant bit of the second block corresponding to the active bit,
 the bit recoding hardware comprises an adder configured to add the counted differences in time slots to the binary number represented by the least significant bits of the n-bit wide pixel data, and
 35 the bit recoding hardware comprises a look-up-table storing a corresponding codeword portion for each possible output from the adder, said codeword portion comprising the bit of the first block and the middle and least significant bits of the second block.

- 40 12. Digital driving circuitry according to claim 11, wherein the digital select line driving circuitry (51) comprises a time delay implementation circuit for implementing the predetermined time delay between the second selection and the first selection.
- 45 13. Active matrix display (55) comprising an array of light emitting elements arranged for being driven by a digital driving circuitry according to any of claims 11 or 12.
14. Active matrix display (55) according to claim 13, wherein the active matrix display is an AMLED display, an AMOLED display or an AMQLED display.
- 50 15. Active matrix display (55) according to claim 14, wherein the light emitting elements are any of crystalline semiconducting LEDs, fluorescent OLEDs, phosphorescent OLEDs, light emitting polymers, Quantum dot QLEDs.

55 **Patentansprüche**

1. Ein Verfahren zur digitalen Ansteuerung einer Aktivmatrixanzeige (55), die eine Vielzahl von Pixeln umfasst, die logisch in einer Vielzahl von Reihen und einer Vielzahl von Spalten organisiert sind, wobei die Anzeige (55) mit einer vorbestimmten Bildrate und Reihenzeit angesteuert wird, wobei das Verfahren umfasst:

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- Darstellen von n-Bit breiten Pixeldaten für jedes der Vielzahl von Pixeln eines anzuzeigenden Einzelbildes durch ein entsprechendes binäres Codewort der Bitlänge n+1, wobei ein erstes (CX) der das Codewort bildenden Bits einen ersten Block bildet und die verbleibenden n Bits (C0, ..., Cn-1) des Codewortes einen zweiten Block bilden;

- Unterteilung des Einzelbildes in eine natürliche Anzahl N von Teilbildern, wobei jedes Teilbild weiter in Zeitschlitze unterteilt wird, wobei jeder Zeitschlitz eine Dauer aufweist, die gleich einer Hälfte der Reihenzeit während der digitalen Ansteuerung ist;

- Zuordnen einer Anzahl der genannten Zeitschlitze zu jedem Bit des Codeworts;

- innerhalb mindestens eines Teilbildes, sequentielles Auswählen mindestens einer der Vielzahl von Reihen zweimal, wobei bei einer ersten Auswahl ein erstes Bit der Codewörter, die für Pixel der ausgewählten Reihe repräsentativ sind, in die Pixel der ausgewählten Reihe geschrieben wird, und bei einer zweiten Auswahl ein zweites Bit der Codewörter, die für Pixel der ausgewählten Reihe repräsentativ sind, das sich von dem geschriebenen ersten Bit unterscheidet, in die Pixel der ausgewählten Reihe geschrieben wird, wobei zwischen der zweiten Auswahl und der ersten Auswahl eine vorbestimmte Zeitverzögerung besteht;

dadurch gekennzeichnet, dass

der Schritt des Zuordnens ferner das Zuordnen eines Zeitschlitzes zu dem Bit (CX) des ersten Blocks des Codeworts und das Zuordnen eines oder mehrerer Zeitschlitze zu jedem Bit (C0, ..., Cn-1) des zweiten Blocks des Codeworts in Übereinstimmung mit der Bitposition in dem zweiten Block umfasst, wobei die Anzahl der Zeitschlitze, die den höchstwertigen Bits des zweiten Blocks zugeordnet sind, natürliche Potenzen von zwei sind und die Anzahl der Zeitschlitze, die den niedrigstwertigen Bits des zweiten Blocks zugeordnet sind, ungerade positive ganze Zahlen sind; und

die Zeitverzögerung zwischen der zweiten Auswahl und der ersten Auswahl in mindestens einem der Teilbilder, ausgedrückt in einer Anzahl von Zeitschlitzen, von einer natürlichen Potenz von zwei abweicht.

2. Ein Verfahren nach Anspruch 1, wobei die Zeitverzögerung zwischen der zweiten Auswahl und der ersten Auswahl in dem mindestens einen Teilbild um einen Zeitschlitz länger ist als die Verzögerung $2k$, die für die sequentielle Auswahl von k Reihen benötigt wird, wobei k eine nicht negative ganze Zahl ist.
3. Ein Verfahren nach Anspruch 2, wobei bei der zweiten Auswahl in diesem mindestens einen Teilbild das zweite Bit der Codewörter in die jeweiligen Pixel der ausgewählten Reihe während einer Anzahl von Zeitschlitzen geschrieben wird, die um eins geringer ist als die Verzögerung $2k$, die für die sequentielle Auswahl der k Reihen benötigt wird.
4. Ein Verfahren nach einem der vorstehenden Ansprüche, wobei die Aufteilung des Einzelbildes die Aufteilung des Einzelbildes in Teilbilder von im Wesentlichen gleicher Dauer umfasst.
5. Ein Verfahren nach einem der Ansprüche 1 bis 4, wobei n keine natürliche Potenz von zwei ist, wobei das Aufteilen des Einzelbildes in Teilbilder das Aufteilen des Einzelbildes in N Teilbilder umfasst, wobei N die Potenz von 2 ist, die größer und am nächsten zu n ist.
6. Ein Verfahren nach Anspruch 5, wobei jedes Teilbild weiter in $2^{n/N}$ Zeitschlitze unterteilt ist.
7. Ein Verfahren nach Anspruch 6, wobei ferner dem m-ten Bit des zweiten Blocks des Codeworts mehr als 2^{m-1} Zeitschlitze, $m \geq 0$, zugeordnet werden, wenn das m-te Bit zu den niederwertigsten Bits des zweiten Blocks gehört.
8. Ein Verfahren nach einem der Ansprüche 6 oder 7, wobei ferner dem m-ten Bit des zweiten Blocks des Codeworts weniger als 2^{m-1} Zeitschlitze, $m \geq 0$, zugeordnet werden, wenn das m-te Bit zu den mittelwertigen Bits des zweiten Blocks gehört.
9. Ein Verfahren nach einem der Ansprüche 6 bis 8, wobei ferner dem m-ten Bit des zweiten Blocks des Codeworts 2^{m-1} Zeitschlitze, $m \geq 0$, zugeordnet werden, wenn das m-te Bit zu den höchstwertigen Bits des zweiten Blocks gehört.
10. Ein Verfahren nach einem der vorstehenden Ansprüche, wobei das Schreiben des ersten Bits des Codeworts und das Schreiben des zweiten Bits des Codeworts die Verwendung von Pulsbreitenmodulation umfasst.
11. Digitale Ansteuerungsschaltung zum Ansteuern einer Aktivmatrixanzeige (55) mit einer Vielzahl von Pixeln, die logisch in einer Vielzahl von Reihen und einer Vielzahl von Spalten organisiert sind, mit einer vorbestimmten Bildrate

und Reihenzeit, um aufeinanderfolgende Teilbilder eines anzuzeigenden Einzelbildes anzuzeigen, wobei die digitale Ansteuerungsschaltung umfasst:

- Bitumkodierungshardware, die dazu ausgelegt ist, n-Bit breite Pixeldaten (B_0, \dots, B_{n-1}) des anzuzeigenden Einzelbildes in ein entsprechendes binäres Codewort der Bitlänge $n+1$ umzuwandeln, wobei ein erstes (CX) der Bits, aus denen jedes Codewort besteht, einen ersten Block bildet und die restlichen n Bits (C_0, \dots, C_{n-1}) jedes Codeworts einen zweiten Block bilden,
- digitale Auswahlleitungs-Treiberschaltung (51) zum sequentiellen Auswählen der Vielzahl von Reihen in Intervallen, die einer Reihenzeit entsprechen, wobei die Reihenzeit in zwei Zeitschlitze gleicher Dauer unterteilt ist, wobei die digitale Auswahlleitungs-Treiberschaltung (51) dazu ausgelegt ist, innerhalb eines Teilbildes mindestens eine der Vielzahl von Reihen zweimal sequentiell auszuwählen, um bei einer ersten Auswahl ein erstes Bit des Codeworts in die ausgewählte Reihe zu schreiben und bei einer zweiten Auswahl ein zweites Bit des Codeworts, das sich von dem ersten geschriebenen Bit unterscheidet, in die ausgewählte Reihe zu schreiben, wobei zwischen der zweiten Auswahl und der ersten Auswahl eine vorbestimmte Zeitverzögerung besteht,
- digitale Datenleitungs-Treiberschaltung (52) zum Schreiben der Codewörter in entsprechende Pixel in einer ausgewählten Reihe,

dadurch gekennzeichnet, dass

ein Zeitschlitz dem Bit (CX) des ersten Blocks des Codeworts zugeordnet ist und ein oder mehrere Zeitschlitze jedem Bit (C_0, \dots, C_{n-1}) des zweiten Blocks des Codeworts in Übereinstimmung mit der Bitposition im zweiten Block zugeordnet sind, wobei eine ungerade ganze Zahl von Zeitschlitzen jedem der niederwertigsten Bits im zweiten Block zugeordnet ist und 2^m Zeitschlitze jedem der höchstwertigen Bits des zweiten Blocks zugeordnet sind, wobei m die Bitposition im zweiten Block bezeichnet, die Zeitverzögerung zwischen der zweiten Auswahl und der ersten Auswahl in mindestens einem der Teilbilder, ausgedrückt in einer Anzahl von Zeitschlitzen, von einer natürlichen Potenz von zwei abweicht, die Bitumkodierungshardware so konfiguriert ist, dass sie die höchstwertigen Bits der n-Bit breiten Pixeldaten von entsprechenden Eingangsanschlüssen der Bitumkodierungshardware an entsprechende Ausgangsanschlüsse der Bitumkodierungshardware weiterleitet, die Bitumkodierungshardware eine Bitzählschaltung umfasst, die so konfiguriert ist, dass sie aktive Bits innerhalb des Bereichs der mittelwertigen Bits der n-Bit breiten Pixeldaten bestimmt und die Differenzen in Zeitschlitzen zwischen den 2^m Zeitschlitzen, die durch die Position m jedes aktiven Bits in den Pixeldaten dargestellt werden, und der Anzahl der Zeitschlitze zählt, die dem mittelwertigen Bit des zweiten Blocks, der dem aktiven Bit entspricht, zugeordnet sind, die Bitumkodierungshardware einen Addierer umfasst, der so konfiguriert ist, dass er die gezählten Differenzen in Zeitschlitzen zu der Binärzahl addiert, die durch die niedrigstwertigen Bits der n-Bit breiten Pixeldaten dargestellt wird, und die Bitumkodierungshardware eine Nachschlagetabelle umfasst, die einen entsprechenden Codewortteil für jeden möglichen Ausgang des Addierers speichert, wobei der Codewortteil das Bit des ersten Blocks und das mittlere und das niedrigstwertige Bit des zweiten Blocks umfasst.

12. Digitale Treiberschaltung nach Anspruch 11, wobei die digitale Auswahlleitungs-Treiberschaltung (51) eine Zeitverzögerungs-Implementierungsschaltung zur Implementierung der vorbestimmten Zeitverzögerung zwischen der zweiten Auswahl und der ersten Auswahl umfasst.
13. Aktivmatrixanzeige (55), umfassend eine Anordnung von lichtemittierenden Elementen, die so angeordnet sind, dass sie von einer digitalen Ansteuerungsschaltung nach einem der Ansprüche 11 oder 12 angesteuert werden.
14. Aktivmatrixanzeige (55) nach Anspruch 13, wobei die Aktivmatrixanzeige eine AMLED-Anzeige, eine AMOLED-Anzeige oder eine AMQLED-Anzeige ist.
15. Aktivmatrixanzeige (55) nach Anspruch 14, wobei die lichtemittierenden Elemente kristalline halbleitende LEDs, fluoreszierende OLEDs, phosphoreszierende OLEDs, lichtemittierende Polymere und Quantenpunkt-QLEDs sind.

Revendications

1. Un procédé pour la commande numérique d'un affichage à matrice active (55) comprenant une pluralité de pixels logiquement organisés en une pluralité de rangées et une pluralité de colonnes, l'affichage (55) étant commandé avec une fréquence d'image prédéterminée et un temps de rangée, le procédé comprenant :

- Représenter des données de pixel de largeur n bits pour chacun des pixels de la pluralité d'une trame d'image à afficher par un mot de code binaire correspondant de longueur de bits $n+1$, dans lequel un premier bit (CX) des bits composant le mot de code forme un premier bloc et les n bits restants (C_0, \dots, C_{n-1}) du mot de code forment un second bloc ;

- Diviser la trame d'image en un nombre naturel N de sous-trames, chaque sous-trame étant en outre divisée en créneaux temporels, chaque créneau temporel ayant une durée égale à la moitié dudit temps de rangée pendant ladite commande numérique ;

- Attribuer un nombre de ces créneaux temporels à chaque bit du mot de code ;

- Dans au moins une sous-trame, sélectionner séquentiellement au moins une des pluralités de rangées deux fois, dans lequel lors d'une première sélection un premier bit des mots de code représentatifs des pixels de la rangée sélectionnée est écrit sur les pixels de la rangée sélectionnée et lors d'une seconde sélection un second bit des mots de code représentatifs des pixels de la rangée sélectionnée, différent du premier bit écrit, est écrit sur les pixels de la rangée sélectionnée, un délai prédéterminé existant entre la seconde sélection et la première sélection ;

Caractérisé en ce que

ladite étape d'attribution comprend en outre l'attribution d'un créneau temporel au bit (CX) du premier bloc du mot de code et l'attribution d'un ou plusieurs créneaux temporels à chaque bit (C_0, \dots, C_{n-1}) du second bloc du mot de code conformément à la position du bit dans le second bloc, dans lequel le nombre de créneaux temporels attribués aux bits les plus significatifs du second bloc sont des puissances naturelles de deux et le nombre de créneaux temporels attribués aux bits les moins significatifs du second bloc sont des entiers positifs impairs ; et le délai entre la seconde sélection et la première sélection dans au moins une des sous-trames, exprimé en nombre de créneaux temporels, s'écarte d'une puissance naturelle de deux.

2. Un procédé selon la revendication 1, dans lequel le délai entre la seconde sélection et la première sélection dans ladite au moins une sous-trame est d'un créneau temporel plus long que le délai $2k$ nécessaire pour sélectionner séquentiellement k rangées, k étant un entier non négatif.
3. Un procédé selon la revendication 2, dans lequel lors de la seconde sélection dans ladite au moins une sous-trame, le second bit des mots de code est écrit sur les pixels respectifs de la rangée sélectionnée pendant un nombre de créneaux temporels égal à un de moins que le délai $2k$ nécessaire pour sélectionner séquentiellement lesdites k rangées.
4. Un procédé selon l'une quelconque des revendications précédentes, dans lequel diviser la trame d'image comprend diviser la trame d'image en sous-trames de durée sensiblement égale.
5. Un procédé selon l'une quelconque des revendications 1 à 4, n n'étant pas une puissance naturelle de deux, dans lequel diviser la trame d'image en sous-trames comprend diviser la trame d'image en N sous-trames, dans lequel N est la puissance de 2 supérieure et la plus proche de n .
6. Un procédé selon la revendication 5, dans lequel chaque sous-trame est en outre divisée en $2^n/N$ créneaux temporels.
7. Un procédé selon la revendication 6, attribuant en outre plus de 2^{m-1} créneaux temporels, $m \geq 0$, au m -ième bit du second bloc du mot de code, si le m -ième bit appartient aux bits les moins significatifs du second bloc.
8. Un procédé selon l'une quelconque des revendications 6 ou 7, attribuant en outre moins de 2^{m-1} créneaux temporels, $m \geq 0$, au m -ième bit du second bloc du mot de code, si le m -ième bit appartient aux bits moyennement significatifs du second bloc.
9. Un procédé selon l'une quelconque des revendications 6 à 8, attribuant en outre 2^{m-1} créneaux temporels, $m \geq 0$, au m -ième bit du second bloc du mot de code, si le m -ième bit appartient aux bits les plus significatifs du second bloc.

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10. Un procédé selon l'une quelconque des revendications précédentes, dans lequel écrire le premier bit du mot de code et écrire le second bit du mot de code comprend l'utilisation de la modulation par largeur d'impulsion.
- 5 11. Circuit de commande numérique pour commander, avec une fréquence d'image prédéterminée et un temps de rangée, un affichage à matrice active (55) comprenant une pluralité de pixels logiquement organisés en une pluralité de rangées et une pluralité de colonnes, de manière à afficher des sous-trames subséquentes d'une trame d'image à afficher, le circuit de commande numérique comprenant :
- 10 - Un matériel de recodage de bits adapté pour convertir des données de pixel de largeur n bits (B_0, \dots, B_{n-1}) de la trame d'image à afficher en un mot de code binaire correspondant de longueur de bits $n+1$, dans lequel un premier bit (CX) des bits composant chaque mot de code forme un premier bloc et les n bits restants (C_0, \dots, C_{n-1}) de chaque mot de code forment un second bloc ;
- 15 - Un circuit de commande de ligne de sélection numérique (51) pour sélectionner séquentiellement la pluralité de rangées à des intervalles correspondant à un temps de rangée, ledit temps de rangée étant subdivisé en deux créneaux temporels de durée égale, le circuit de commande de ligne de sélection numérique (51) étant adapté pour sélectionner séquentiellement, dans une sous-trame, au moins une des pluralités de rangées deux fois, de manière à, lors d'une première sélection, écrire un premier bit du mot de code sur la rangée sélectionnée et, lors d'une seconde sélection, écrire un second bit du mot de code, différent du premier bit écrit, sur la rangée sélectionnée, un délai prédéterminé existant entre la seconde sélection et la première sélection ;
- 20 - Un circuit de commande de ligne de données numérique (52) pour écrire les mots de code sur les pixels correspondants dans une rangée sélectionnée, **caractérisé en ce que** un créneau temporel est associé au bit (CX) du premier bloc du mot de code et un ou plusieurs créneaux temporels sont associés à chaque bit (C_0, C_{n-1}) du second bloc du mot de code conformément à la position du bit dans le second bloc, dans lequel un nombre impair de créneaux temporels est associé à chacun des bits les moins significatifs dans le second bloc et 2^m créneaux temporels sont associés à chacun des bits les plus significatifs du second bloc, où m désigne la position du bit dans le second bloc, le délai entre la seconde sélection et la première sélection dans au moins une des sous-trames, exprimé en nombre de créneaux temporels, s'écarte d'une puissance naturelle de deux ;
- 25 Le matériel de recodage de bits est configuré pour relayer les bits les plus significatifs des données de pixel de largeur n bits depuis des connecteurs d'entrée respectifs du matériel de recodage de bits vers des connecteurs de sortie correspondants du matériel de recodage de bits,
- 30 le matériel de recodage de bits comprend un circuit de comptage de bits configuré pour déterminer les bits actifs dans la plage des bits moyennement significatifs des données de pixel de largeur n bits et compter les différences en créneaux temporels entre les 2^m créneaux temporels représentés par la position m de chaque bit actif dans les données de pixel et le nombre de créneaux temporels associés au bit moyennement significatif du second bloc correspondant au bit actif,
- 35 le matériel de recodage de bits comprend un additionneur configuré pour ajouter les différences comptées en créneaux temporels au nombre binaire représenté par les bits les moins significatifs des données de pixel de largeur n bits, et
- 40 le matériel de recodage de bits comprend une table de consultation stockant une portion de mot de code correspondante pour chaque sortie possible de l'additionneur, ladite portion de mot de code comprenant le bit du premier bloc et les bits moyennement et les moins significatifs du second bloc.
- 45 12. Circuit de commande numérique selon la revendication 11, dans lequel le circuit de commande de ligne de sélection numérique (51) comprend un circuit de mise en œuvre de délai pour mettre en œuvre le délai prédéterminé entre la seconde sélection et la première sélection.
- 50 13. Affichage à matrice active (55) comprenant un réseau d'éléments émetteurs de lumière agencés pour être commandés par un circuit de commande numérique selon l'une quelconque des revendications 11 ou 12.
- 55 14. Affichage à matrice active (55) selon la revendication 13, dans lequel l'affichage à matrice active est un affichage AMLED, un affichage AMOLED ou un affichage AMQLED.
15. Affichage à matrice active (55) selon la revendication 14, dans lequel les éléments émetteurs de lumière sont l'un quelconque parmi des LED à semiconducteurs cristallins, des OLED fluorescentes, des OLED phosphorescentes, des polymères émetteurs de lumière, des QLED à points quantiques.

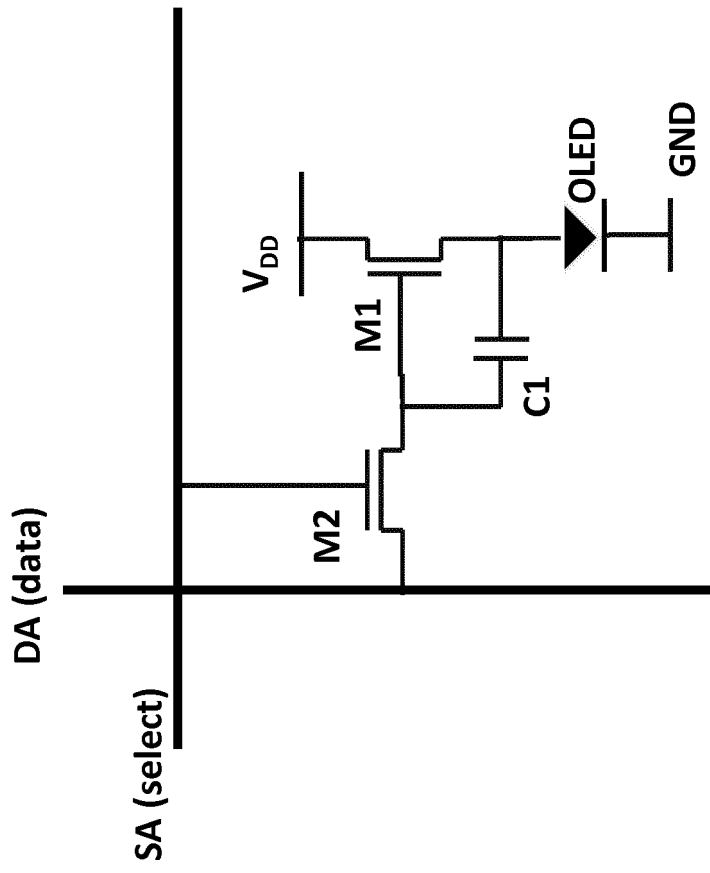


FIG. 1 (prior art)

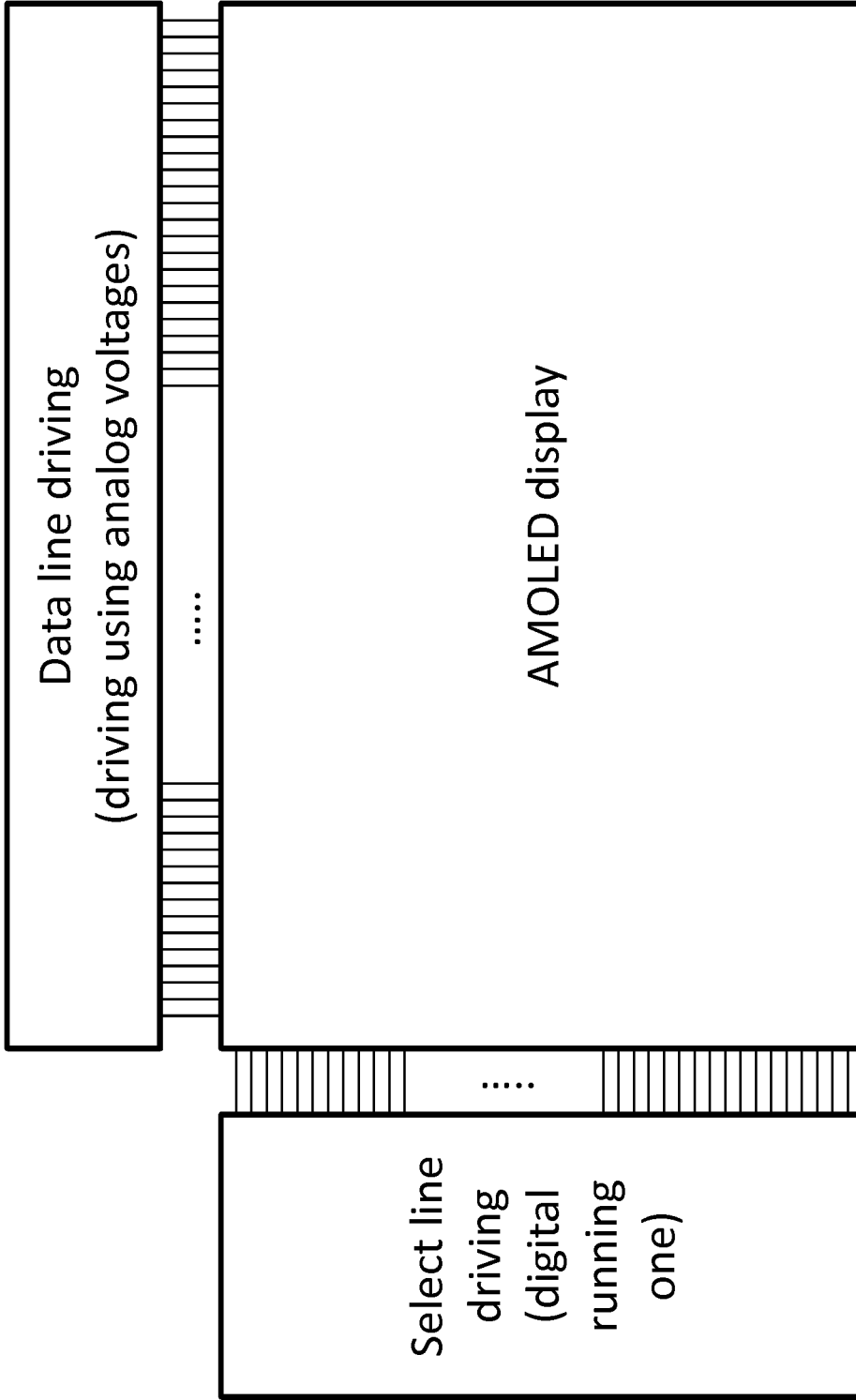


FIG. 2 (prior art)

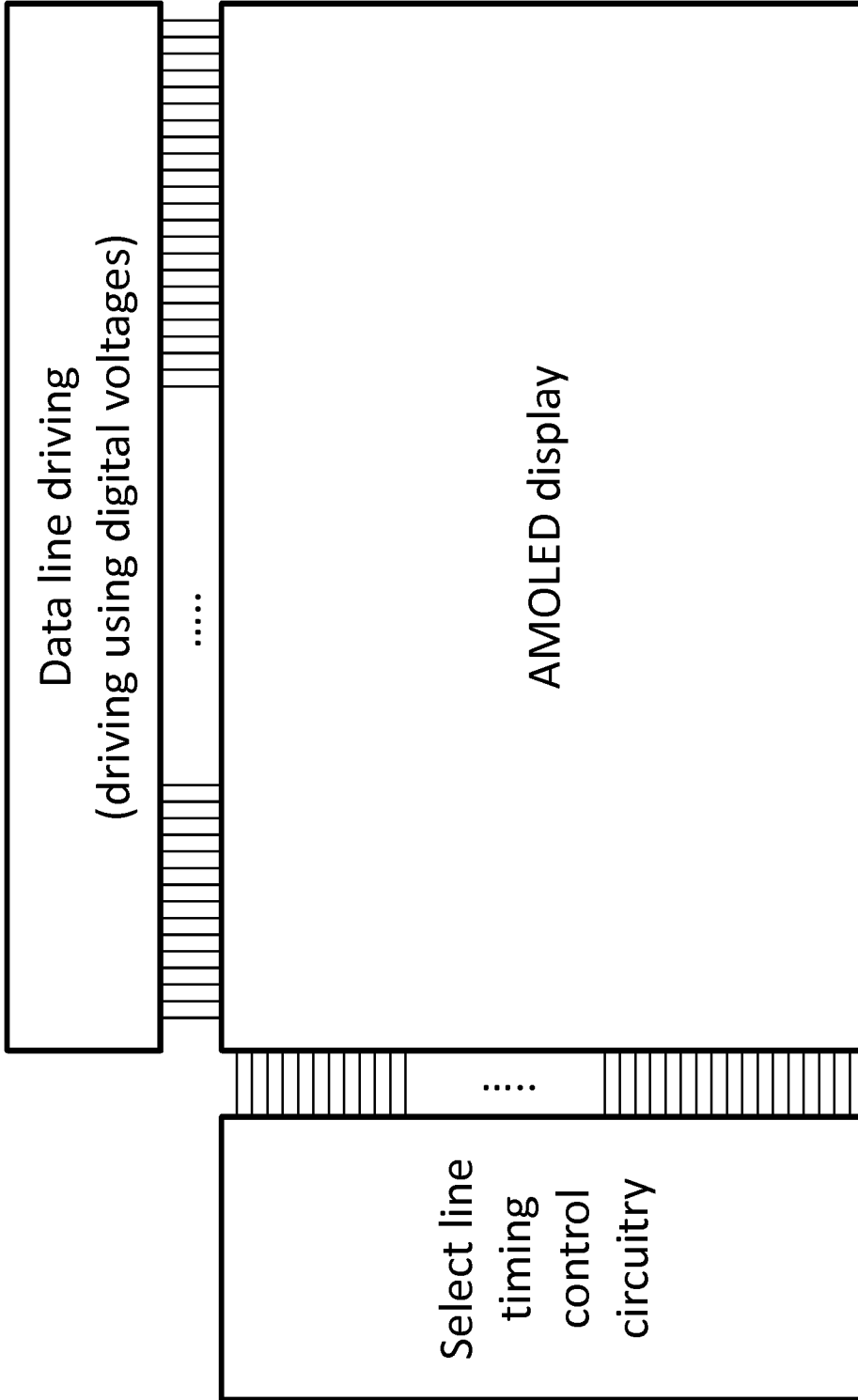


FIG. 3 (prior art)

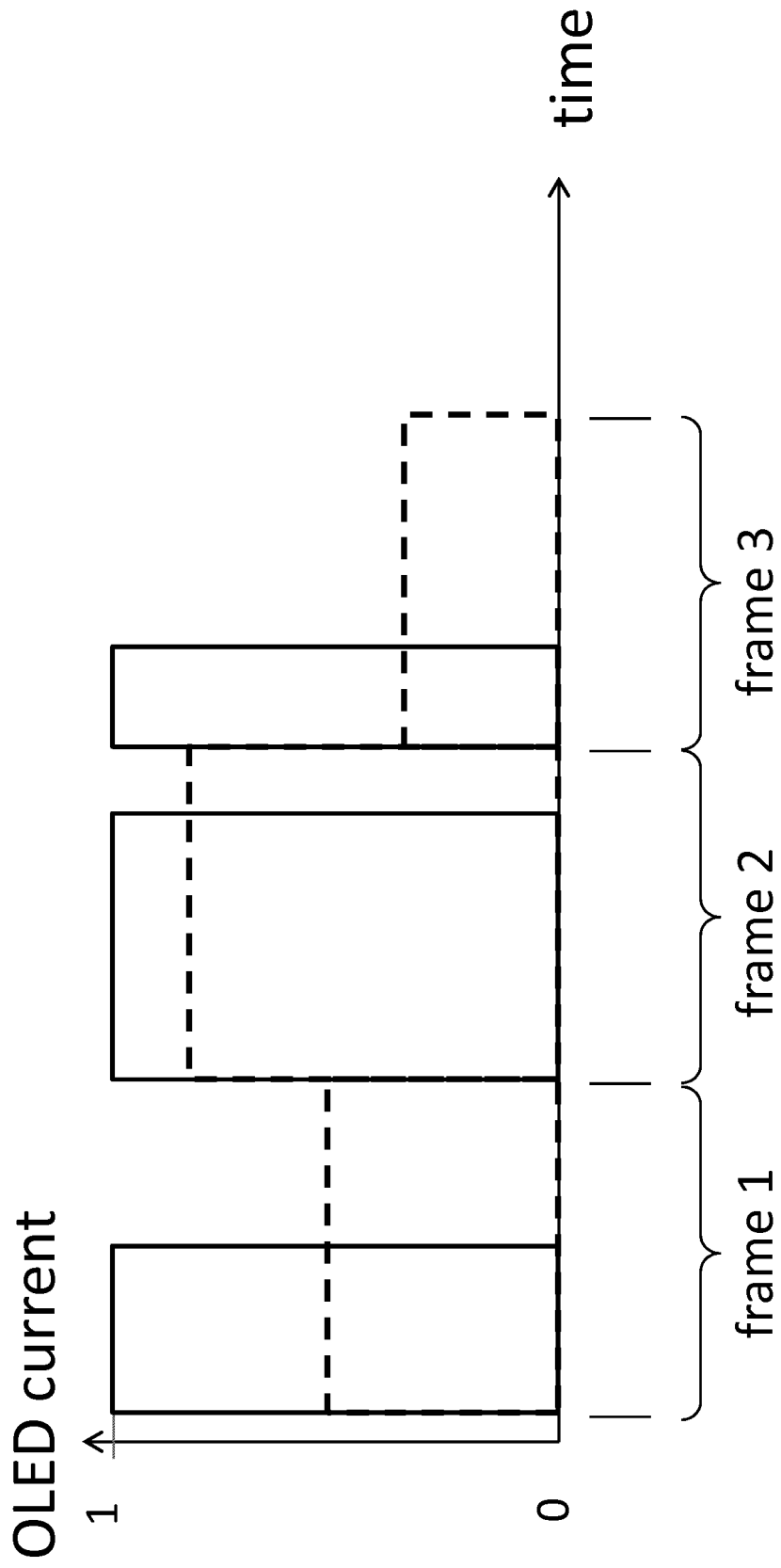


FIG. 4

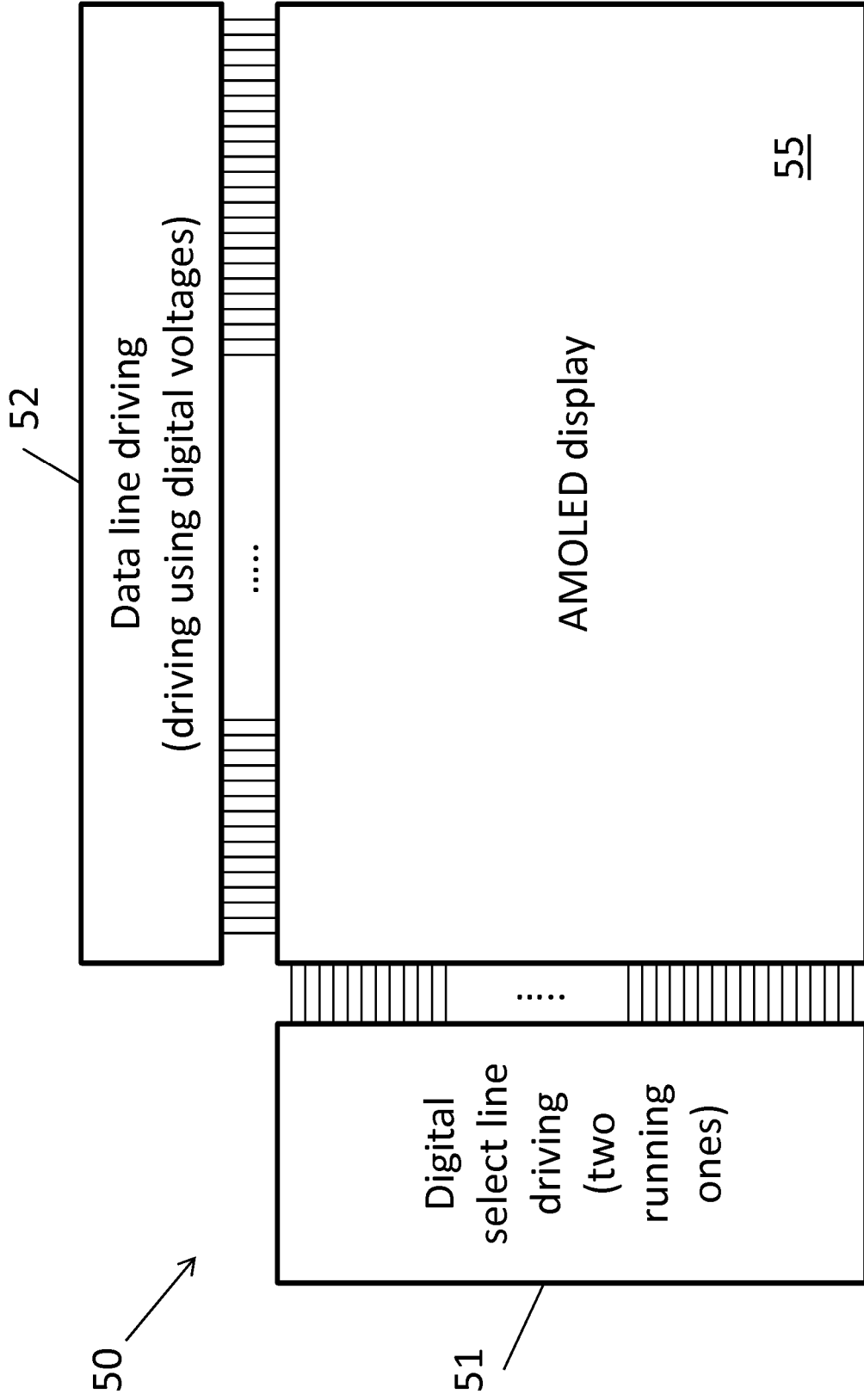


FIG. 5

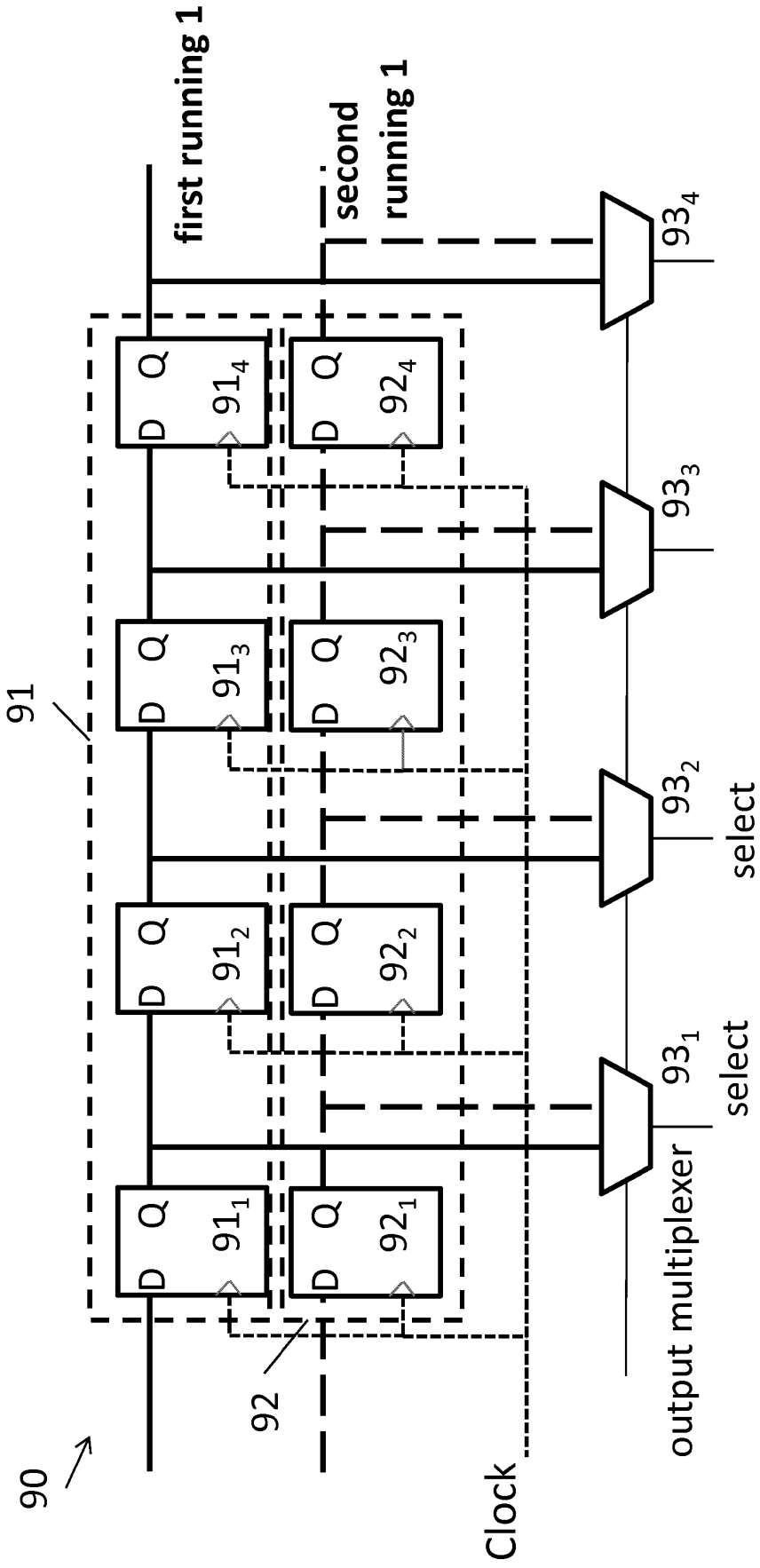


FIG. 6

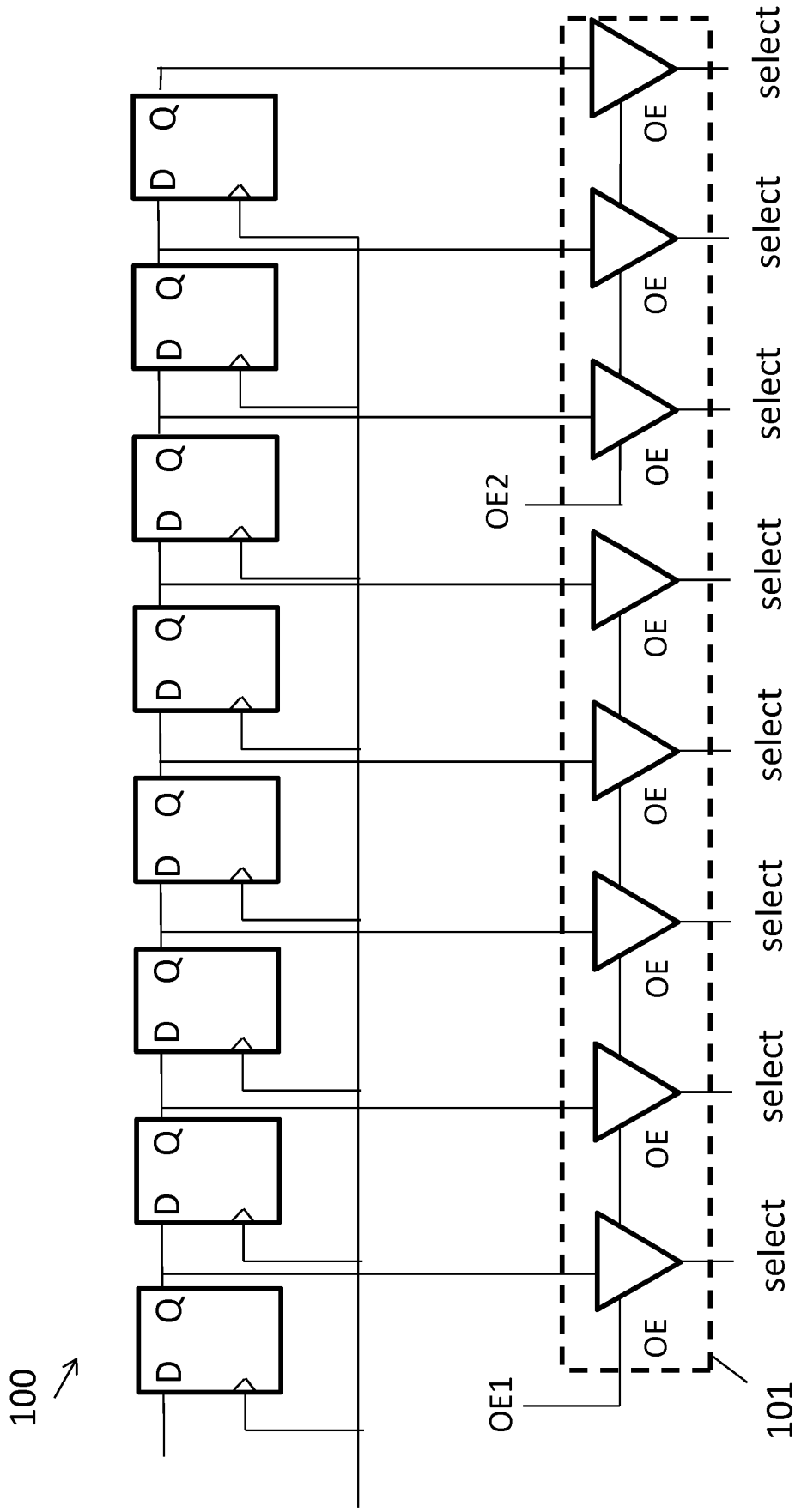


FIG. 7

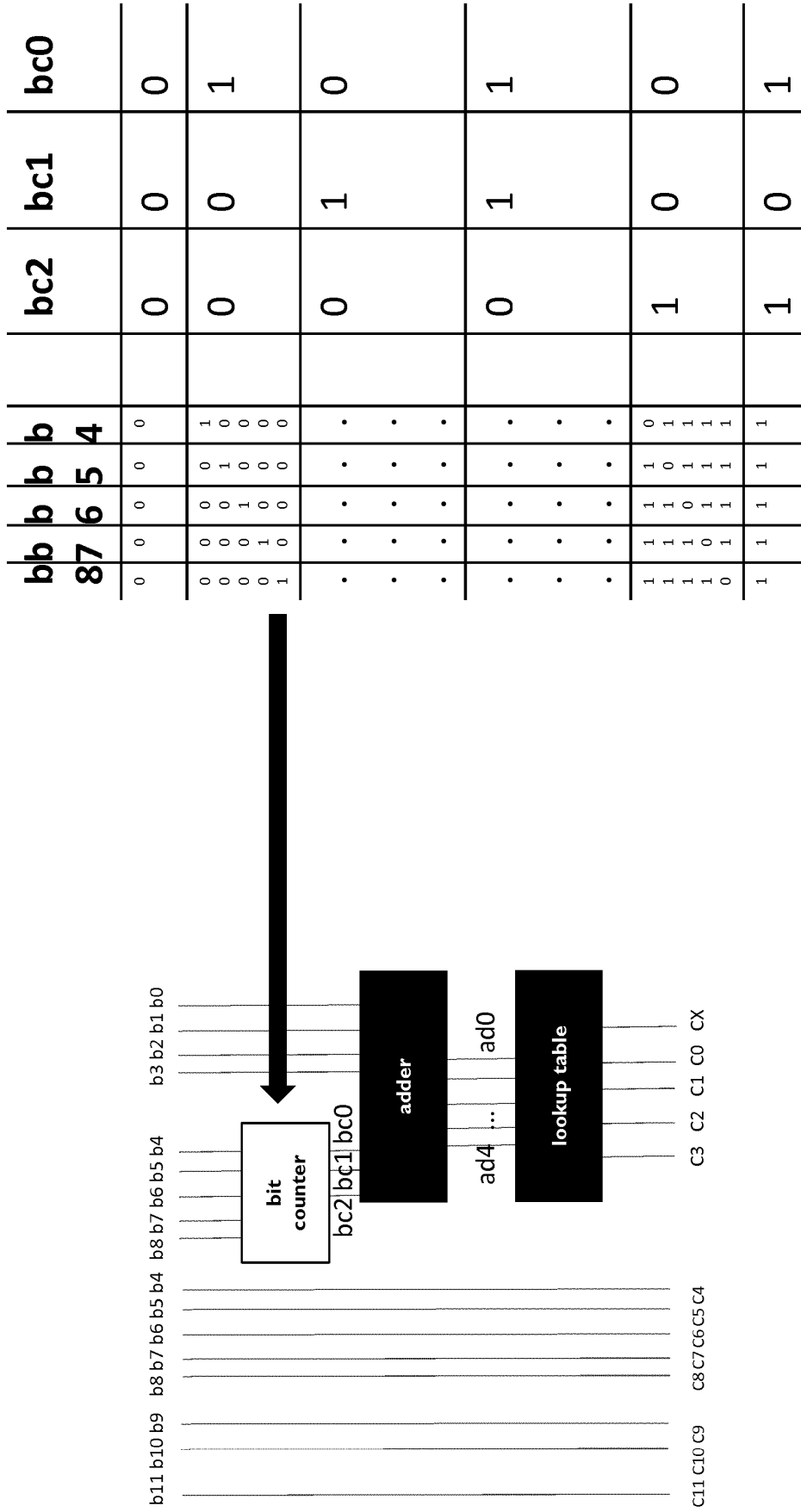


FIG. 8

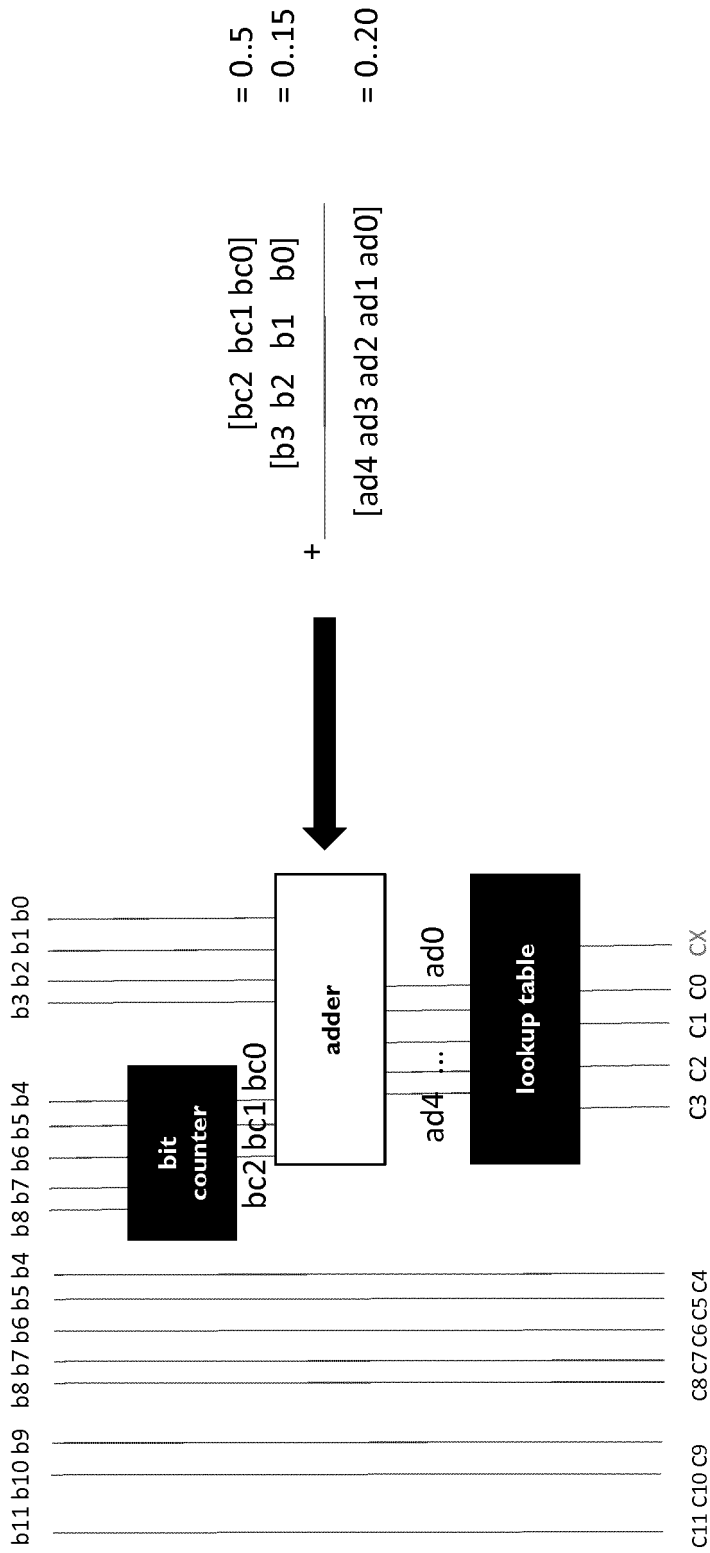


FIG. 9

ad	C3	C2	C1	C0	CX
[]	11	5	3	1	1
0	0	0	0	0	0
1	0	0	0	1	0
2	0	0	0	1	1
3	0	0	1	0	0
4	0	0	1	1	0
5	0	1	0	0	0
6	0	1	0	1	0
7	0	1	0	1	1
8	0	1	1	0	0
9	0	1	1	1	0
10	0	1	1	1	1
11	1	0	0	0	0
12	1	0	0	1	0
13	1	0	0	1	1
14	1	0	1	0	0
15	1	0	1	1	0
16	1	1	0	0	0
17	1	1	0	1	0
18	1	1	0	1	1
19	1	1	1	0	0
20	1	1	1	1	0

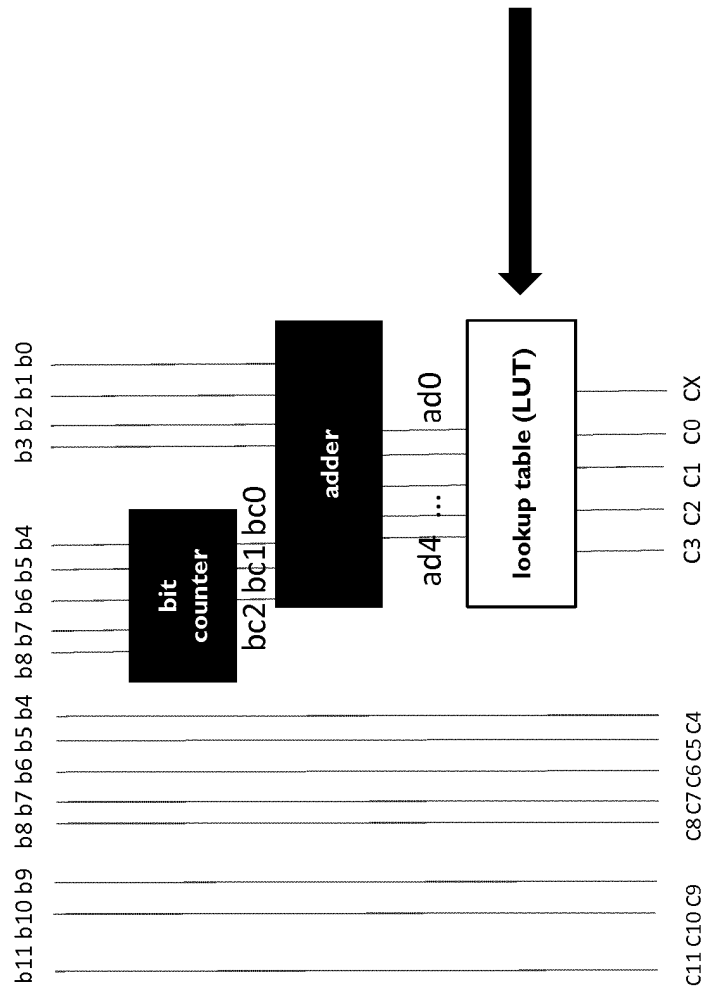


FIG. 10

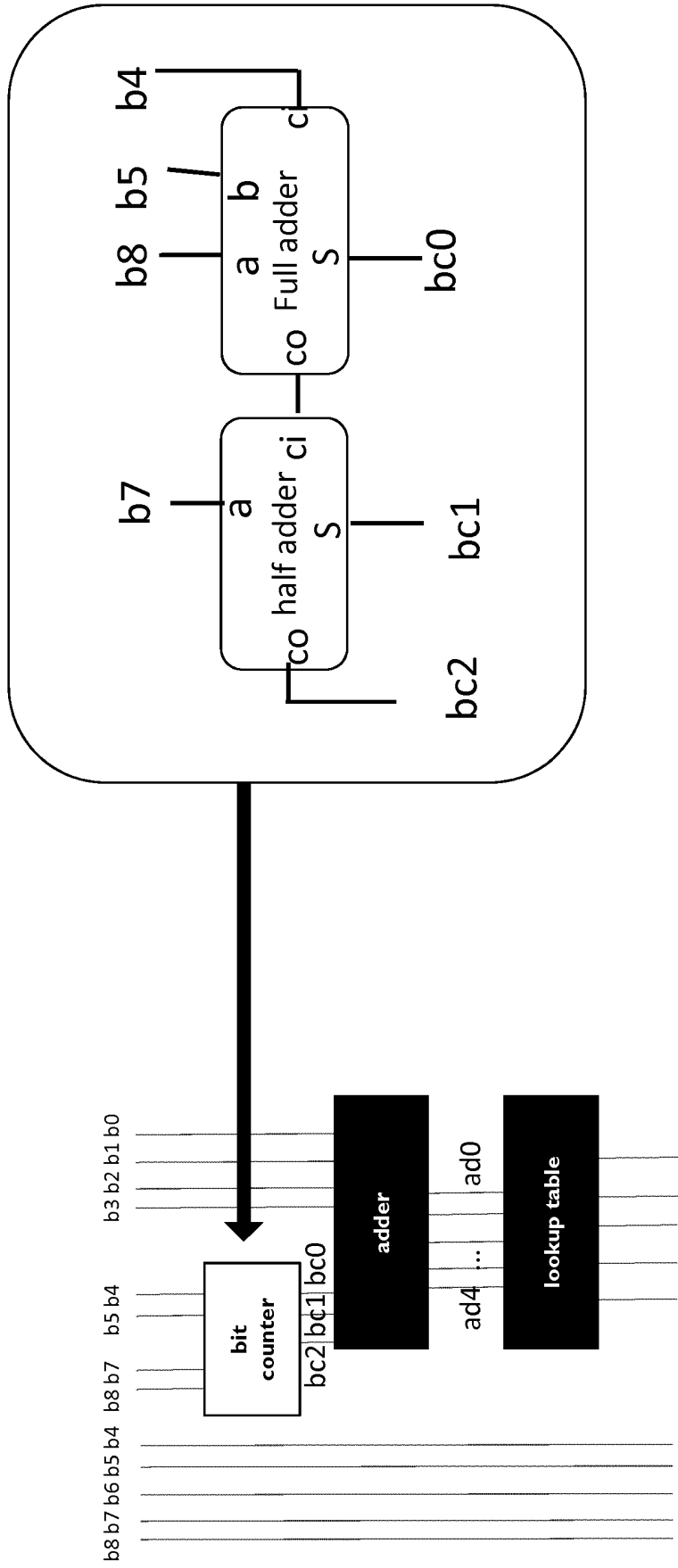


FIG. 11

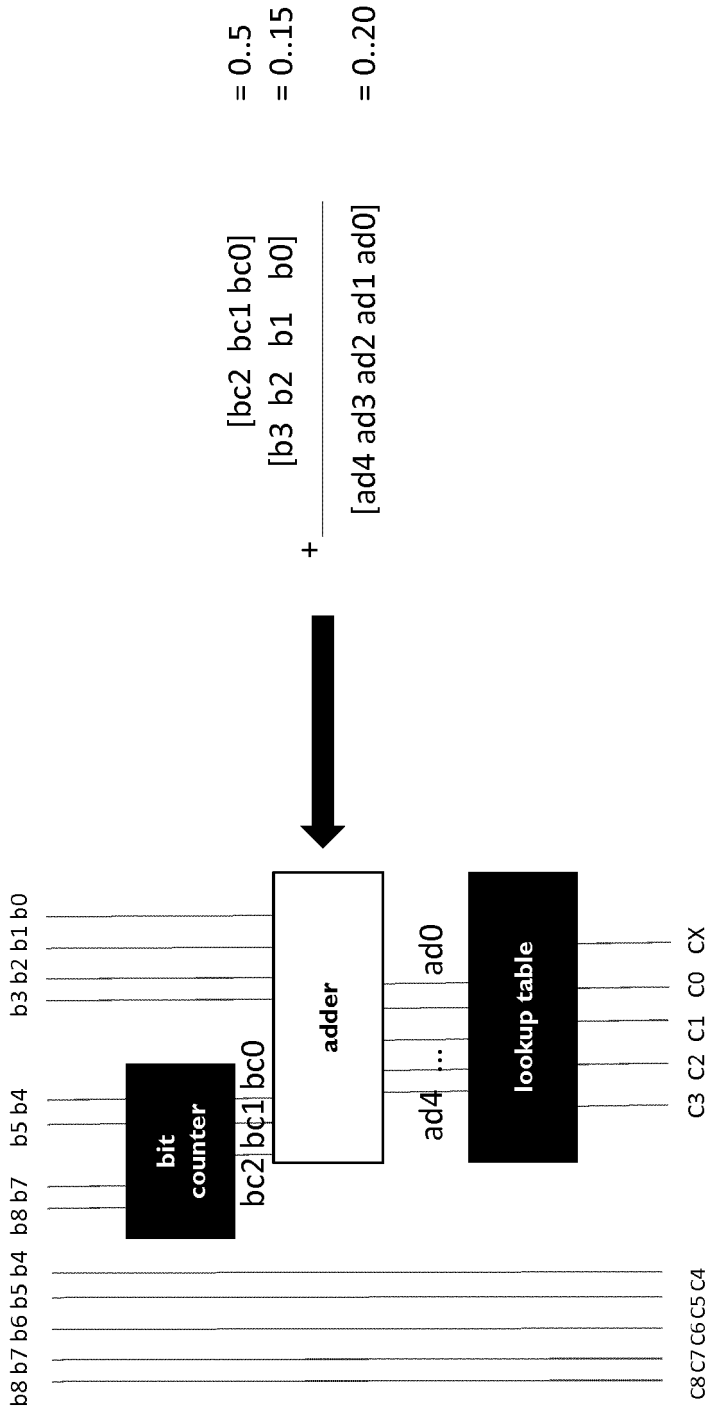


FIG. 12

ad	C3	C2	C1	C0	CX
[]	11	5	3	1	1
0	0	0	0	0	0
1	0	0	0	1	0
2	0	0	0	1	1
3	0	0	1	0	0
4	0	0	1	1	0
5	0	1	0	0	0
6	0	1	0	1	0
7	0	1	0	1	1
8	0	1	1	0	0
9	0	1	1	1	0
10	0	1	1	1	1
11	1	0	0	0	0
12	1	0	0	1	0
13	1	0	0	1	1
14	1	0	1	0	0
15	1	0	1	1	0
16	1	1	0	0	0
17	1	1	0	1	0
18	1	1	0	1	1
19	1	1	1	0	0
20	1	1	1	1	0

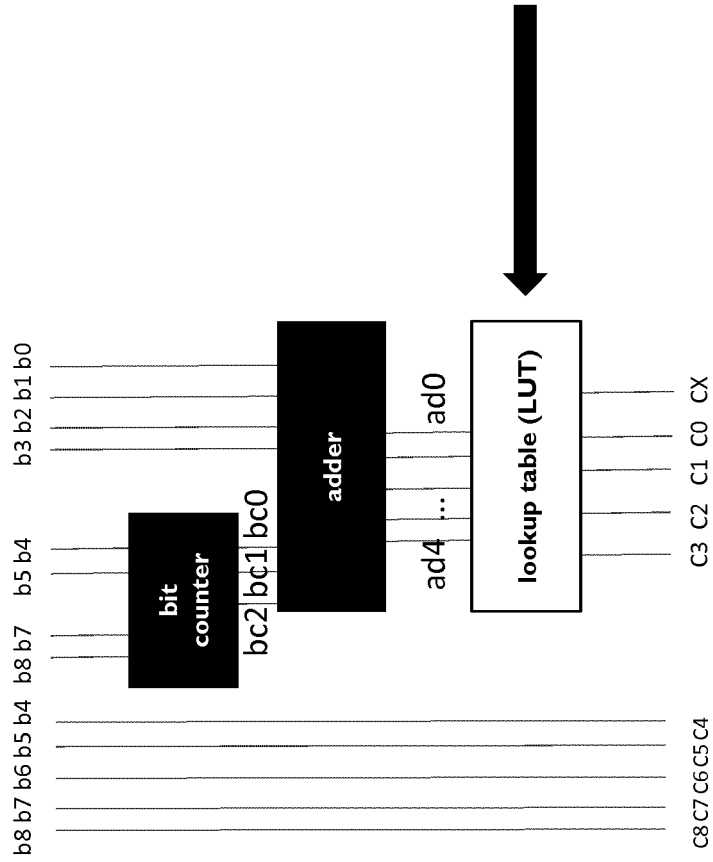


FIG. 13

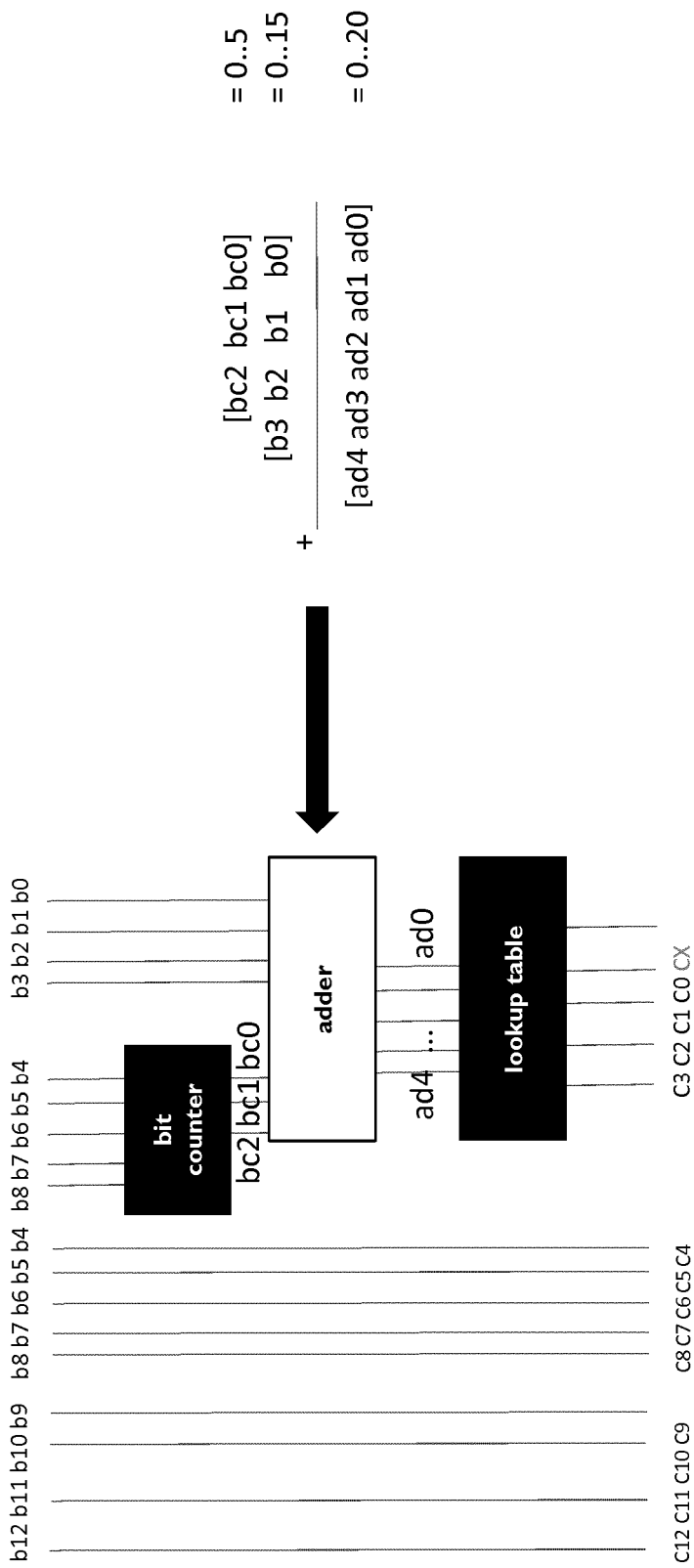


FIG.15

ad	C3	C2	C1	C0	CX
[]	11	5	3	1	1
0	0	0	0	0	0
1	0	0	0	1	0
2	0	0	0	1	1
3	0	0	1	0	0
4	0	0	1	1	0
5	0	1	0	0	0
6	0	1	0	1	0
7	0	1	0	1	1
8	0	1	1	0	0
9	0	1	1	1	0
10	0	1	1	1	1
11	1	0	0	0	0
12	1	0	0	1	0
13	1	0	0	1	1
14	1	0	1	0	0
15	1	0	1	1	0
16	1	1	0	0	0
17	1	1	0	1	0
18	1	1	0	1	1
19	1	1	1	0	0
20	1	1	1	1	0

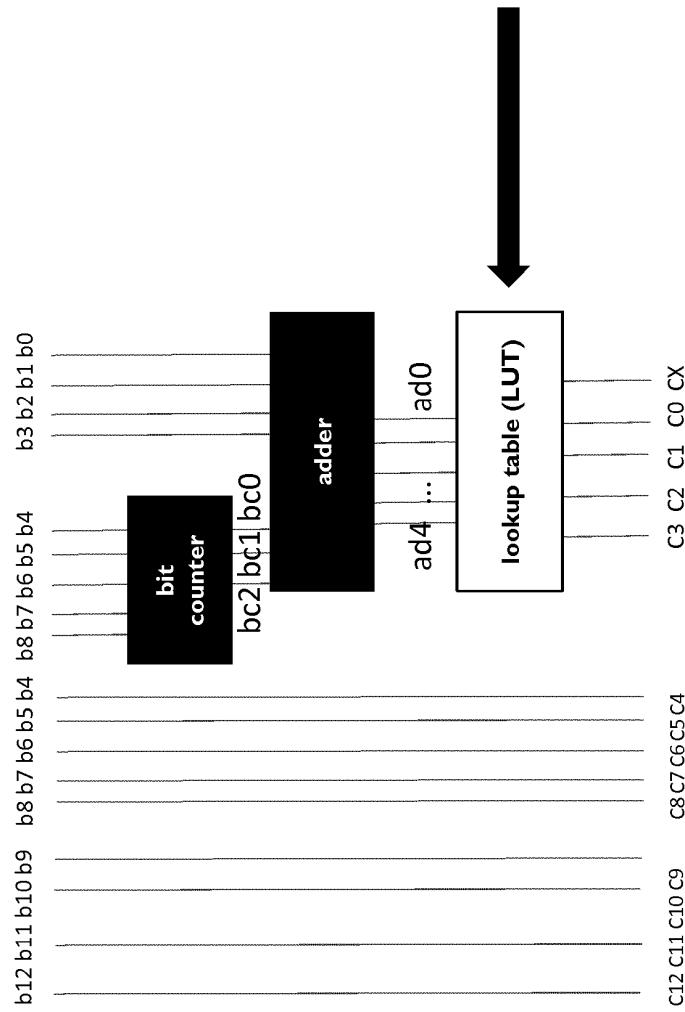


FIG. 16

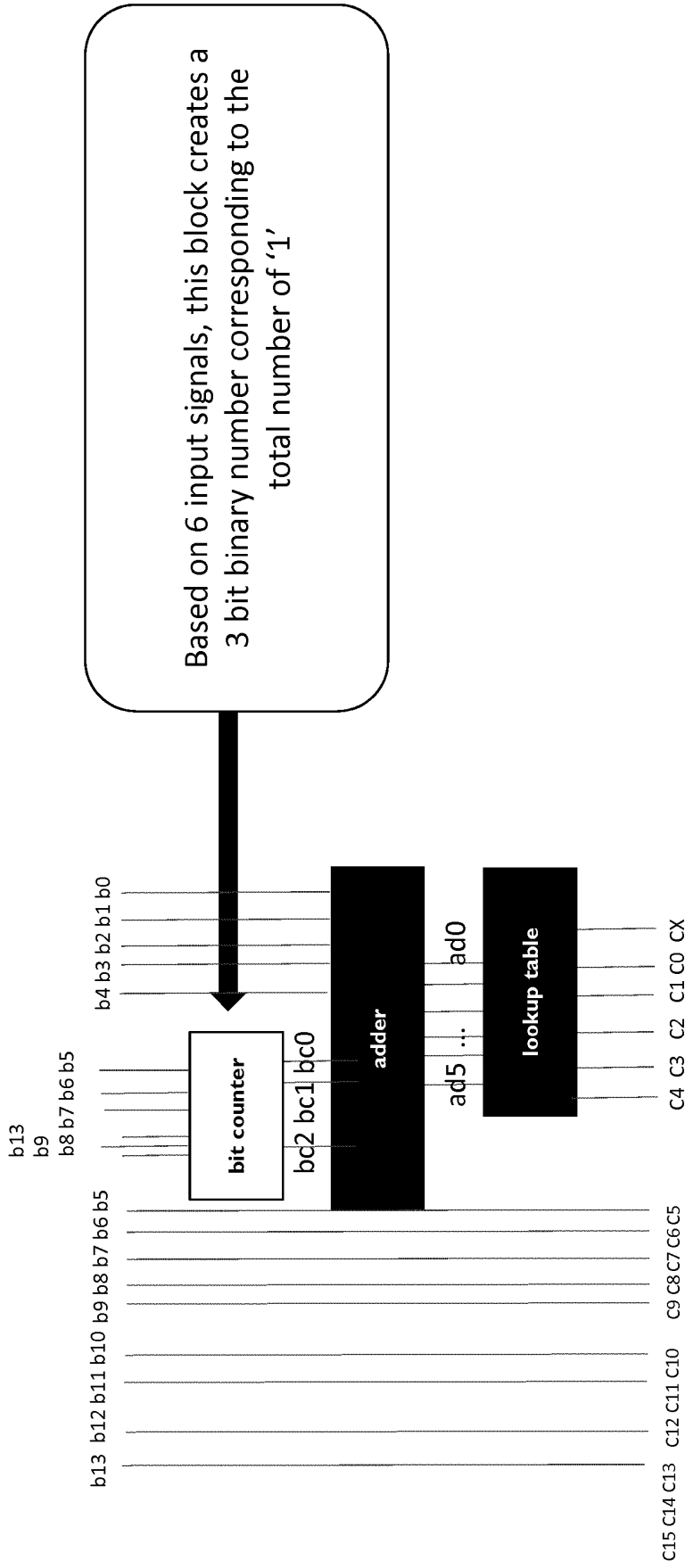


FIG. 17

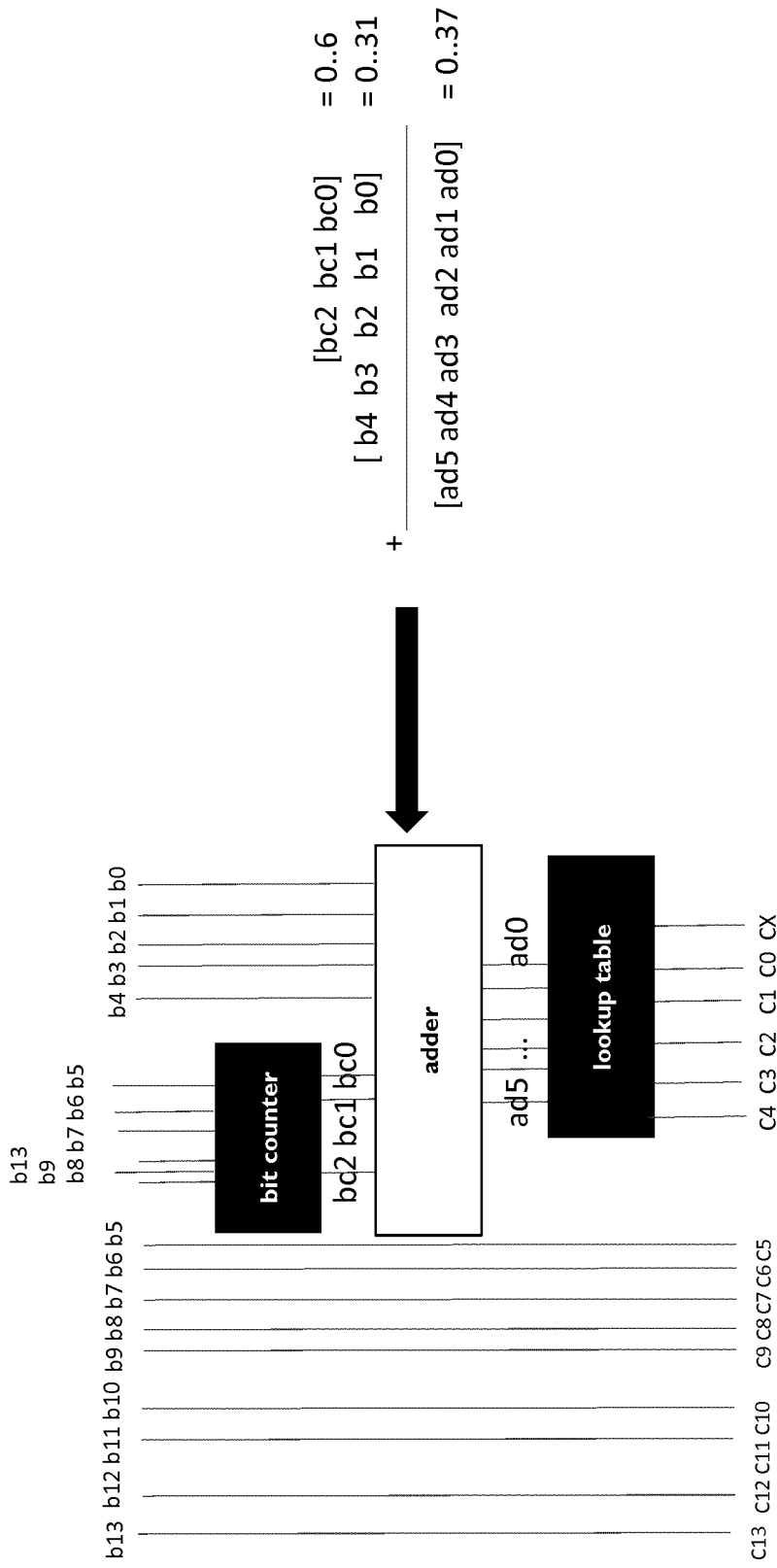


FIG. 18

ad	C4	C3	C2	C1	C0	CX
[]	17	11	5	3	1	1
0	0	0	0	0	0	0
1	0	0	0	0	1	0
2	0	0	0	0	1	1
3	0	0	0	1	0	0
4	0	0	0	1	1	0
5	0	0	1	0	0	0
6	0	0	1	0	1	0
7	0	0	1	0	1	1
8	0	0	1	1	0	0
9	0	0	1	1	1	0
10	0	0	1	1	1	1
11	0	1	0	0	0	0
12	0	1	0	0	1	0
13	0	1	0	0	1	1
14	0	1	0	1	0	0
15	0	1	0	1	1	0
16	0	1	1	0	0	0

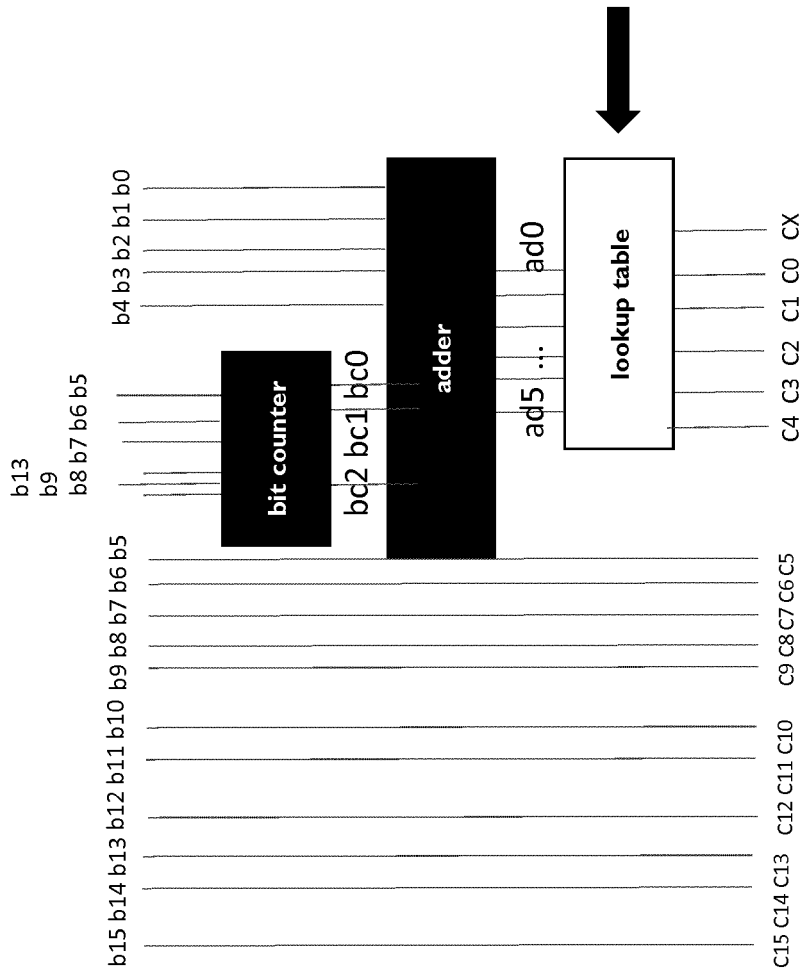


FIG. 19a

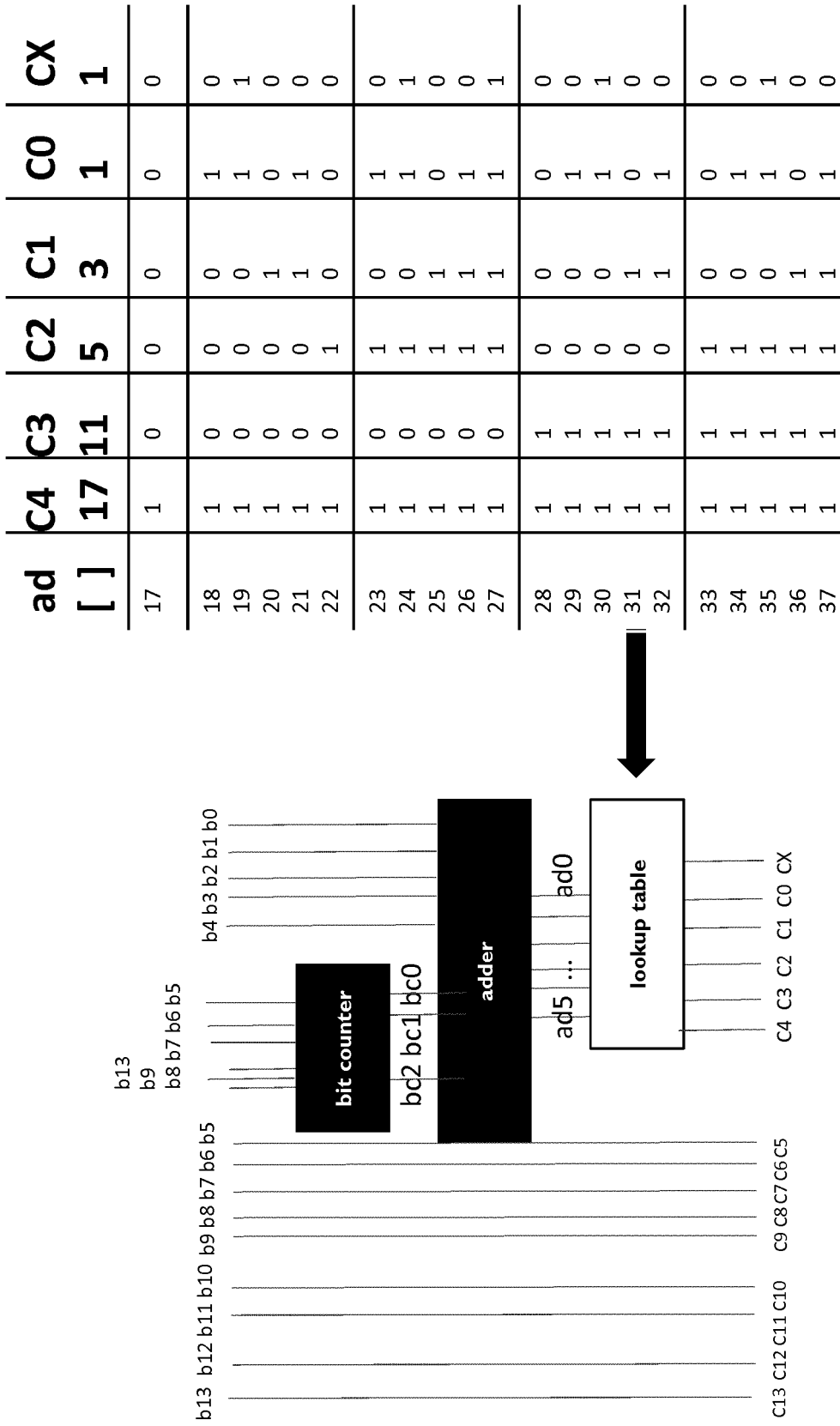


FIG.19b

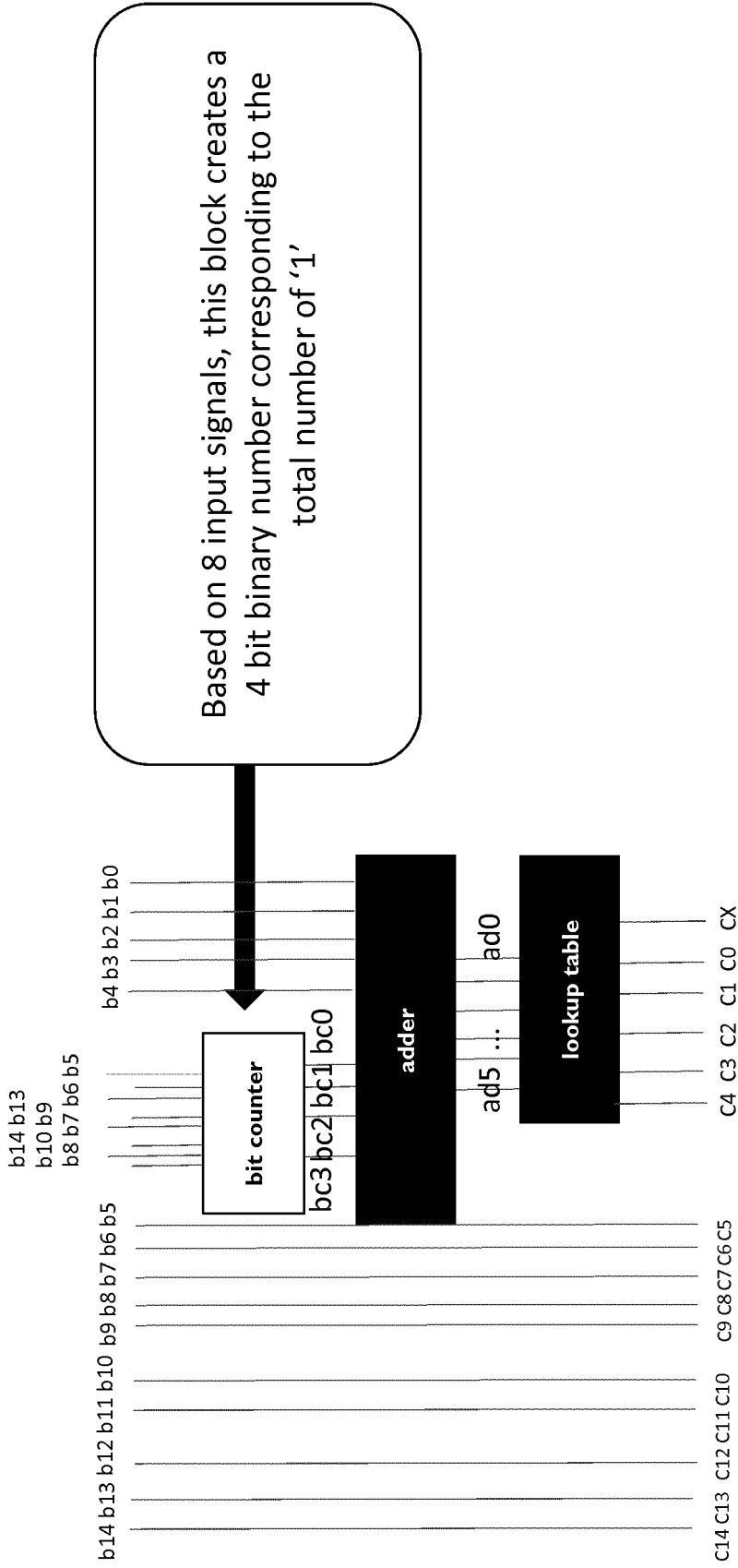


FIG. 20

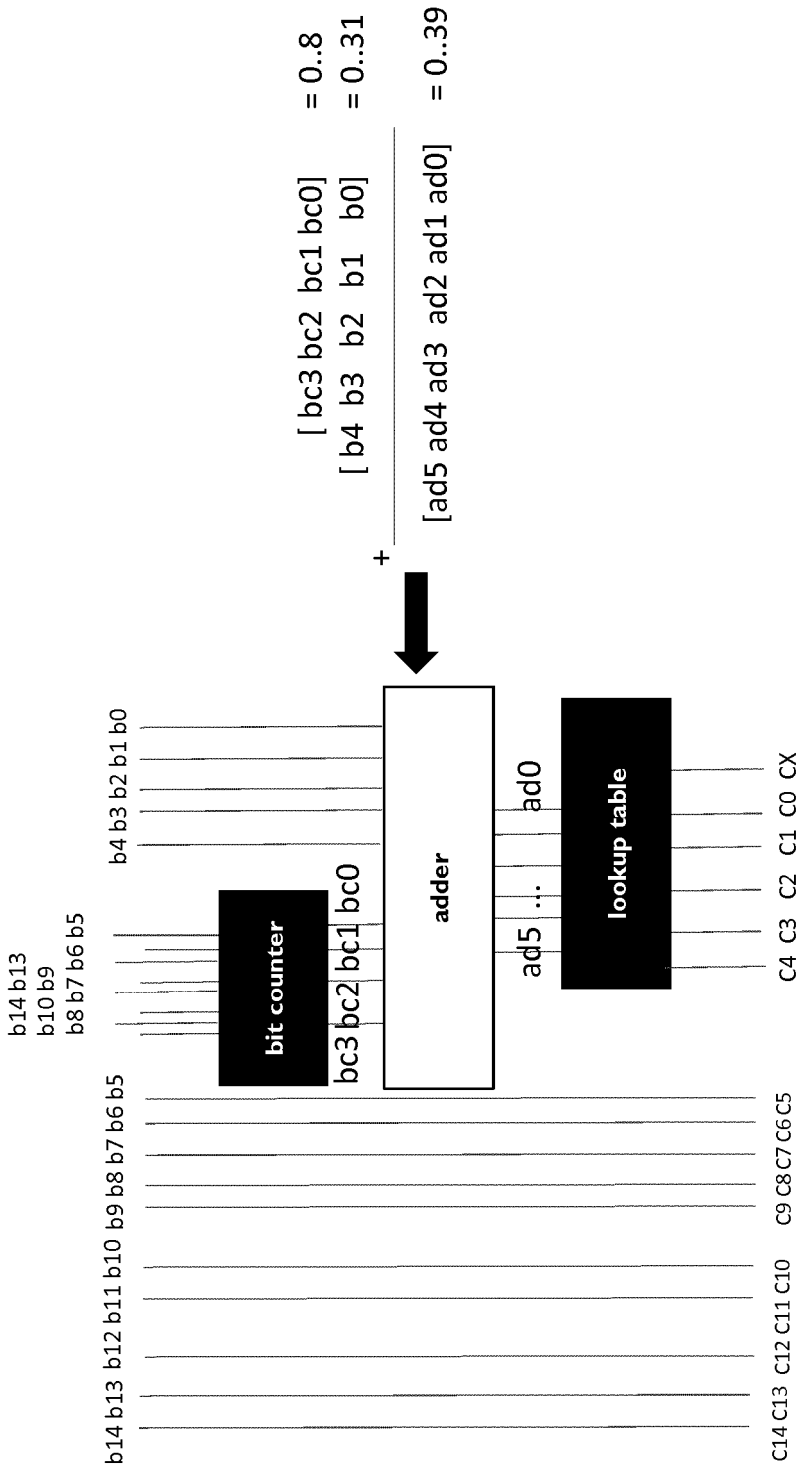


FIG. 21

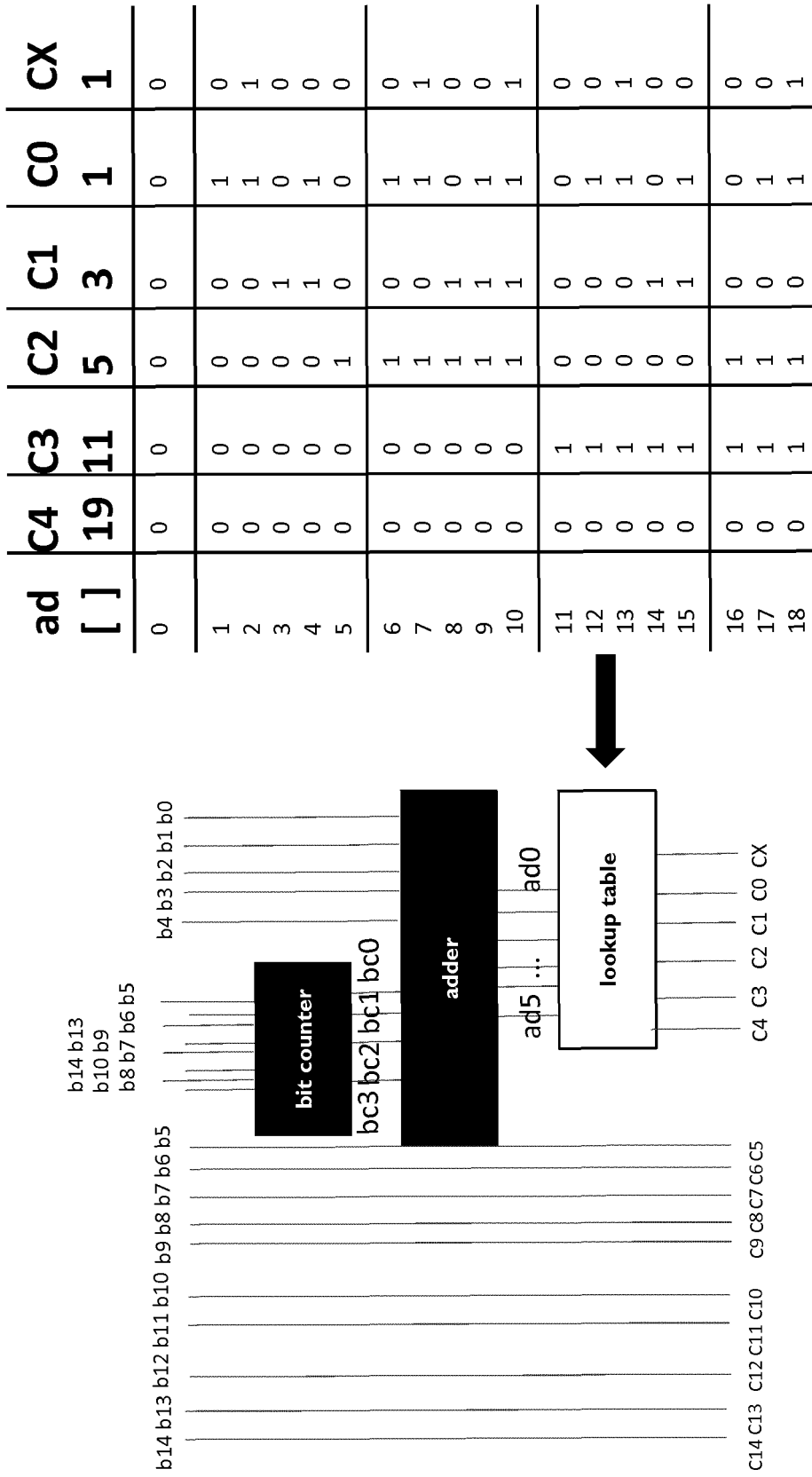


FIG. 22a

ad	C4	C3	C2	C1	C0	CX
[]	19	11	5	3	1	1
19	1	0	0	0	0	0
20	1	0	0	0	1	0
21	1	0	0	0	1	1
22	1	0	0	1	0	0
23	1	0	0	1	1	0
24	1	0	1	0	0	0
25	1	0	1	0	1	0
26	1	0	1	0	1	1
27	1	0	1	1	0	0
28	1	0	1	1	1	0
29	1	0	1	1	1	1
30	1	1	0	0	0	0
31	1	1	0	0	1	0
32	1	1	0	0	1	1
33	1	1	0	1	0	0
34	1	1	0	1	1	0
35	1	1	1	0	0	0
36	1	1	1	0	1	0
37	1	1	1	0	1	1
38	1	1	1	1	0	0
39	1	1	1	1	1	0

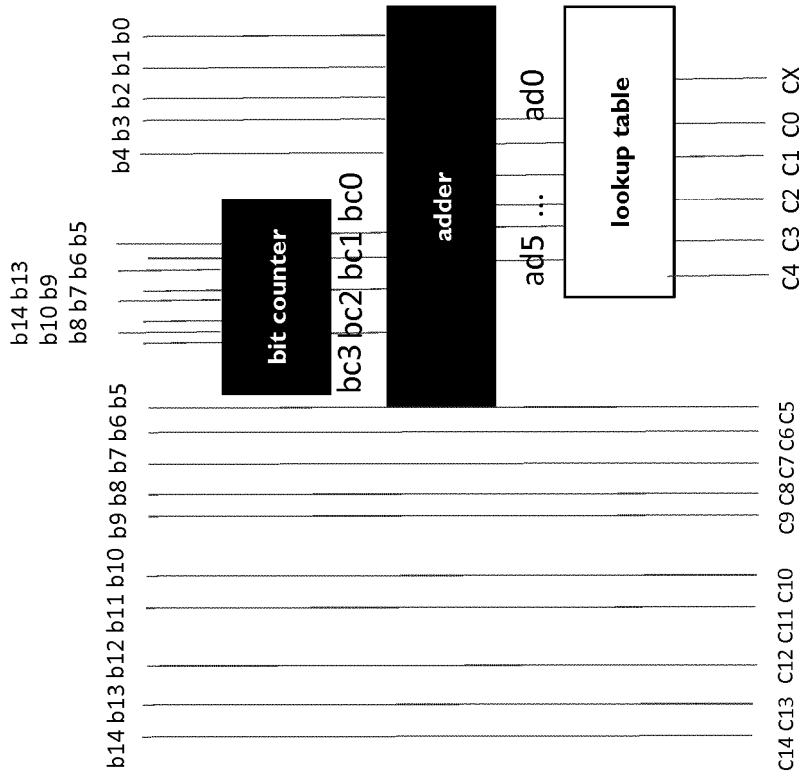


FIG. 22b

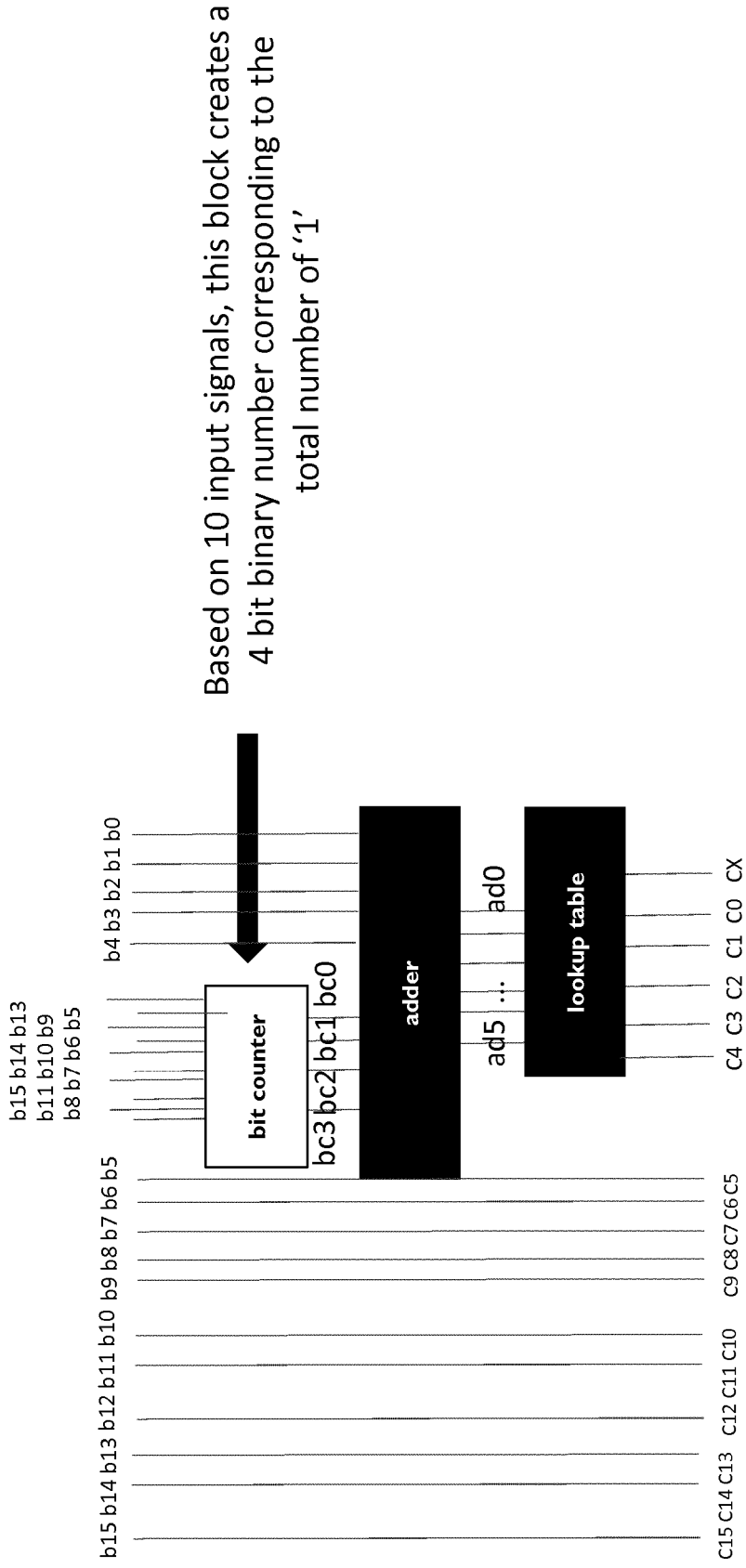


FIG. 23

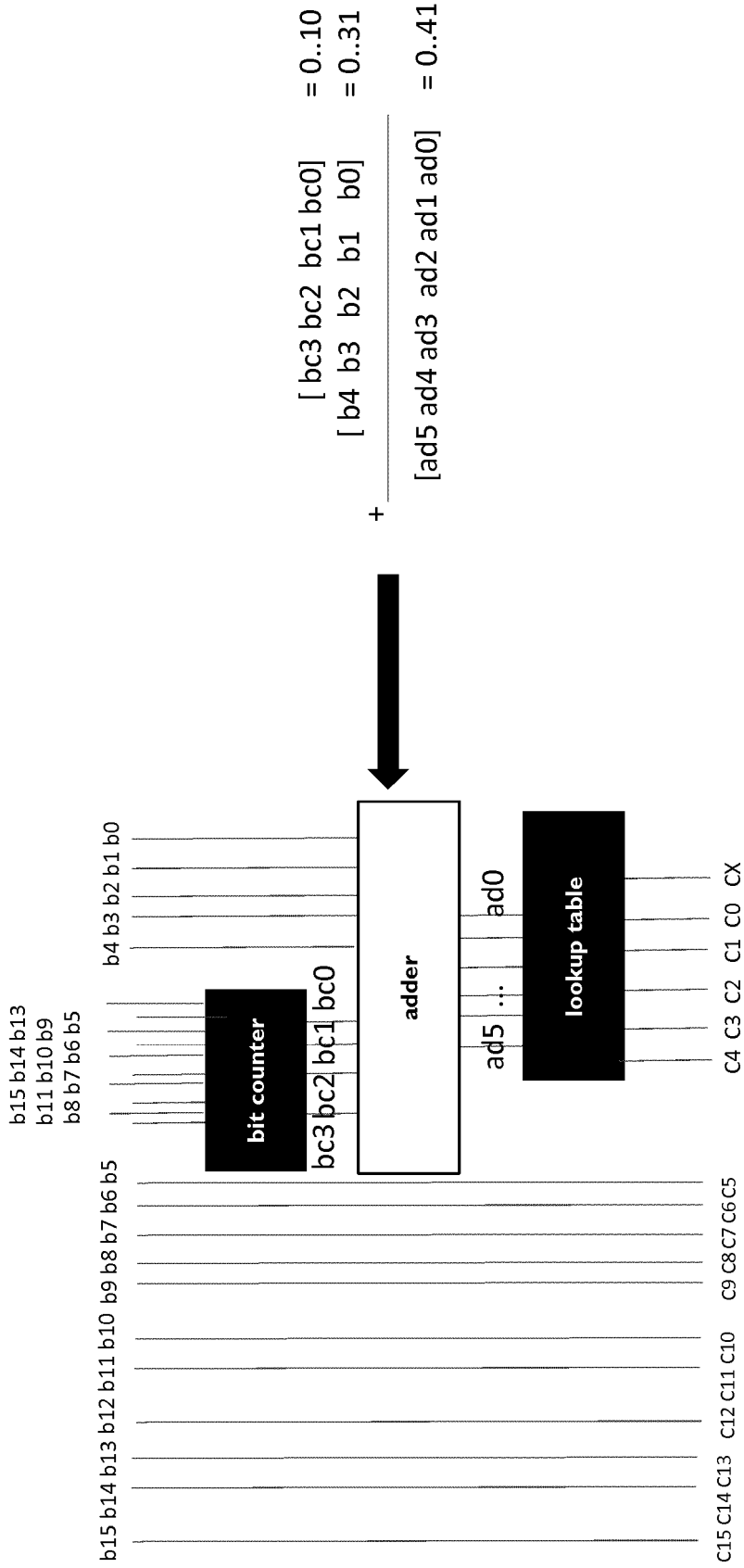


FIG. 24

ad	C4	C3	C2	C1	C0	CX
[]						
0	0	0	0	0	1	1
1	0	0	0	0	1	0
2	0	0	0	0	1	1
3	0	0	0	1	0	0
4	0	0	0	1	1	0
5	0	0	1	0	0	0
6	0	0	1	0	1	0
7	0	0	1	0	1	1
8	0	0	1	1	0	0
9	0	0	1	1	1	0
10	0	0	1	1	1	1
11	0	1	0	0	0	0
12	0	1	0	0	1	0
13	0	1	0	0	1	1
14	0	1	0	1	0	0
15	0	1	0	1	1	0
16	0	1	1	0	0	0
17	0	1	1	0	1	0
18	0	1	1	0	1	1
19	0	1	1	1	0	0
20	0	1	1	1	1	0

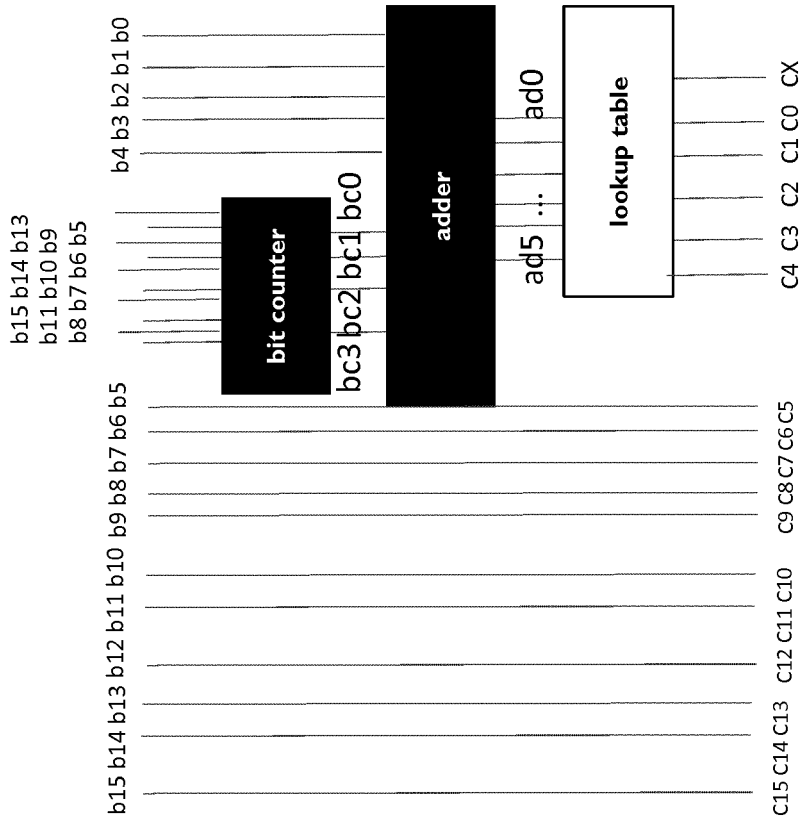


FIG. 25a

ad	C4	C3	C2	C1	C0	CX
[]	21	11	5	3	1	1
21	1	0	0	0	0	0
22	1	0	0	0	1	0
23	1	0	0	0	1	1
24	1	0	0	1	0	0
25	1	0	0	1	1	0
26	1	0	1	0	0	0
27	1	0	1	0	1	0
28	1	0	1	0	1	1
29	1	0	1	1	0	0
30	1	0	1	1	1	0
31	1	0	1	1	1	1
32	1	1	0	0	0	0
33	1	1	0	0	1	0
34	1	1	0	0	1	1
35	1	1	0	1	0	0
36	1	1	0	1	1	0
37	1	1	1	0	0	0
38	1	1	1	0	1	0
39	1	1	1	0	1	1
40	1	1	1	1	0	0
41	1	1	1	1	1	0

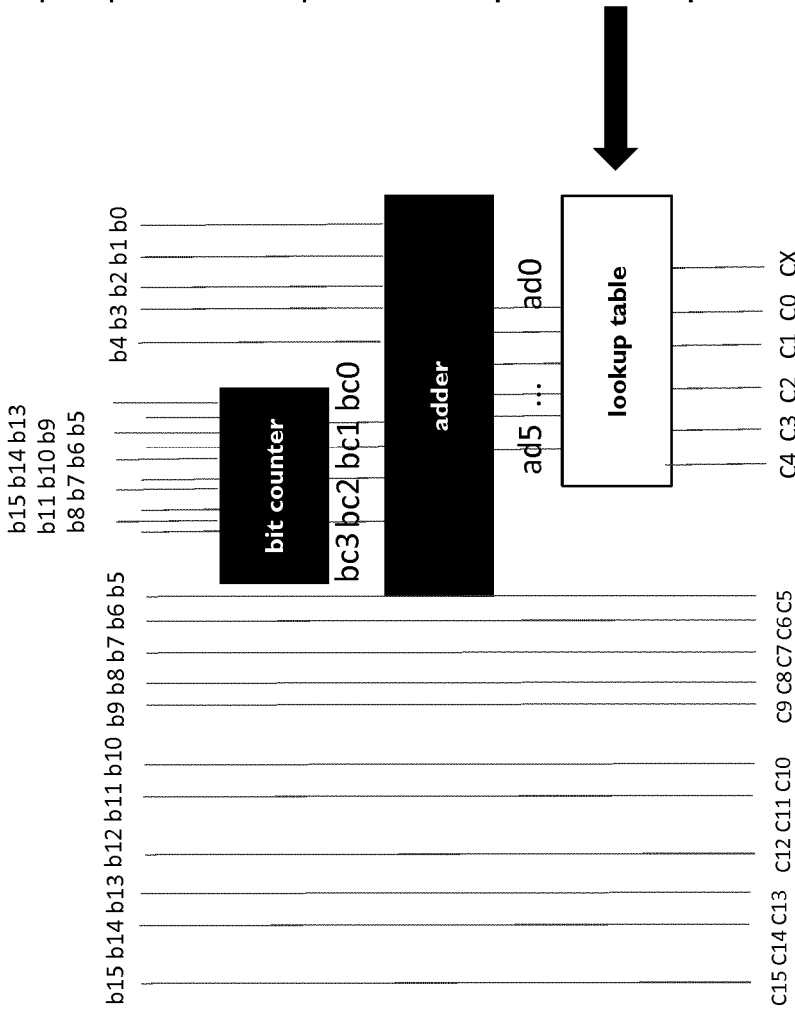


FIG. 25b

REFERENCES CITED IN THE DESCRIPTION

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Patent documents cited in the description

- WO 2014068017 A [0006] [0030] [0031] [0037]
[0038] [0041] [0108]
- US 2010188393 A [0007]
- US 2012320005 A [0007]