United States Patent

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[54] **DISPLAY SYSTEM UTILIZING LIGHT EMITTING DEVICES**

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[73] Assignee: **General Electric Company**

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[52] **U.S. Cl.**.....**340/324 R,** 250/213 A, 250/220 M

[51] **Int. Cl.**.....**H03k 19/14,** G02f 3/00

[58] **Field of Search**.....340/324 R, 334, 336; 250/220 M, 213 R, 213 A, 217 SS, 209; 315/134

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[57] **ABSTRACT**

Methods and apparatus for receiving, transferring, retaining and displaying information within a display system having inherent internal memory capabilities. Transfer and display elements including light-emitting and light-activated devices are employed in numerous configurations to provide display systems of high density with a minimum number of connections to external control circuitry with self-sustaining memory capabilities. Row-by-row, column-by-column and time sequential addressing of both rows and columns of display elements are disclosed.

14 Claims, 9 Drawing Figures

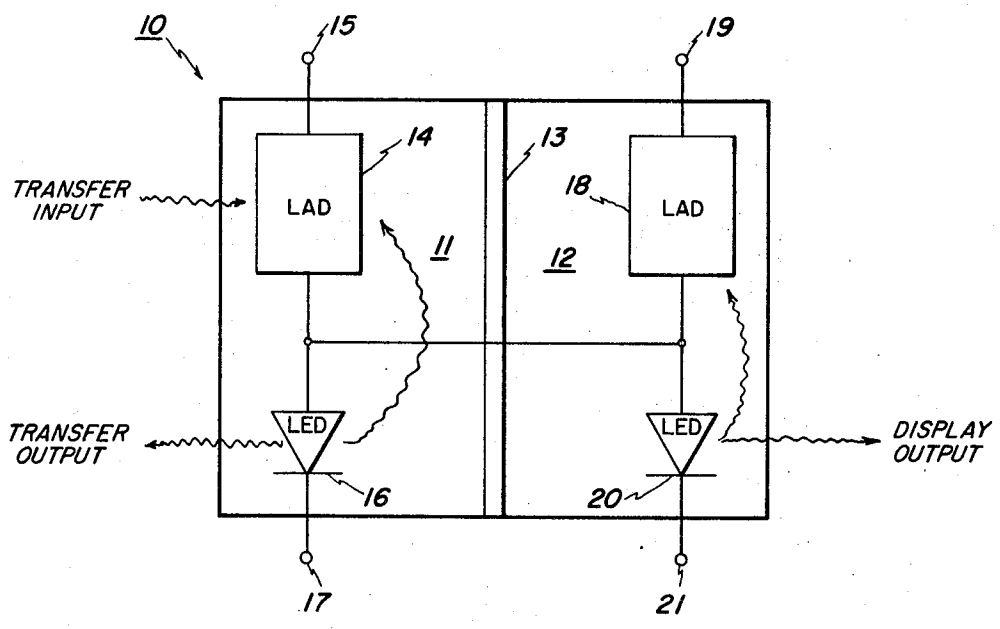


FIG. 1

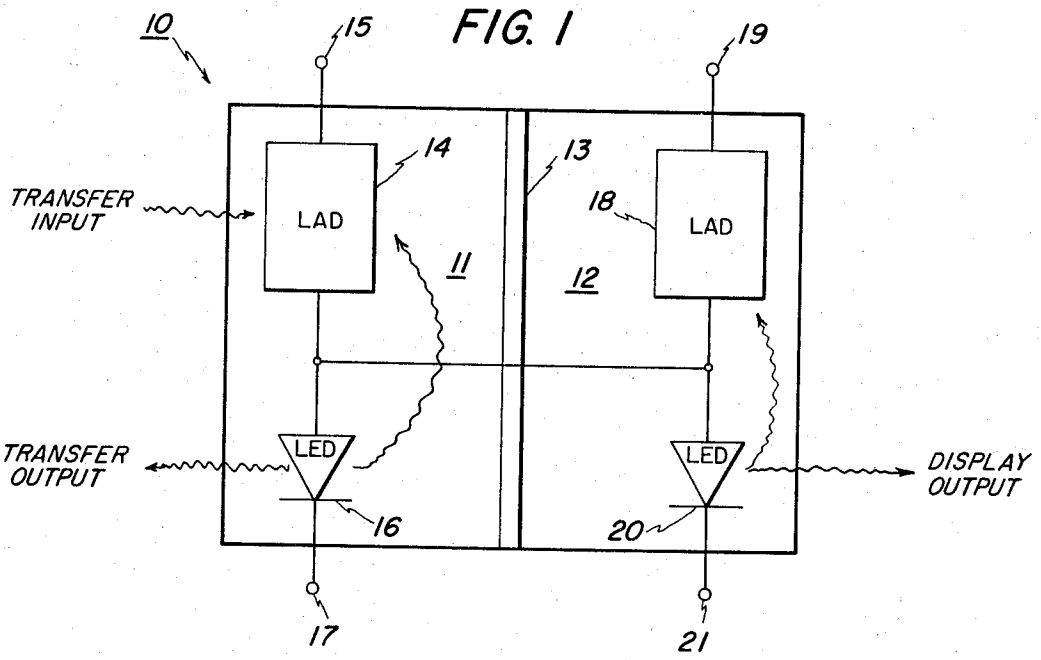
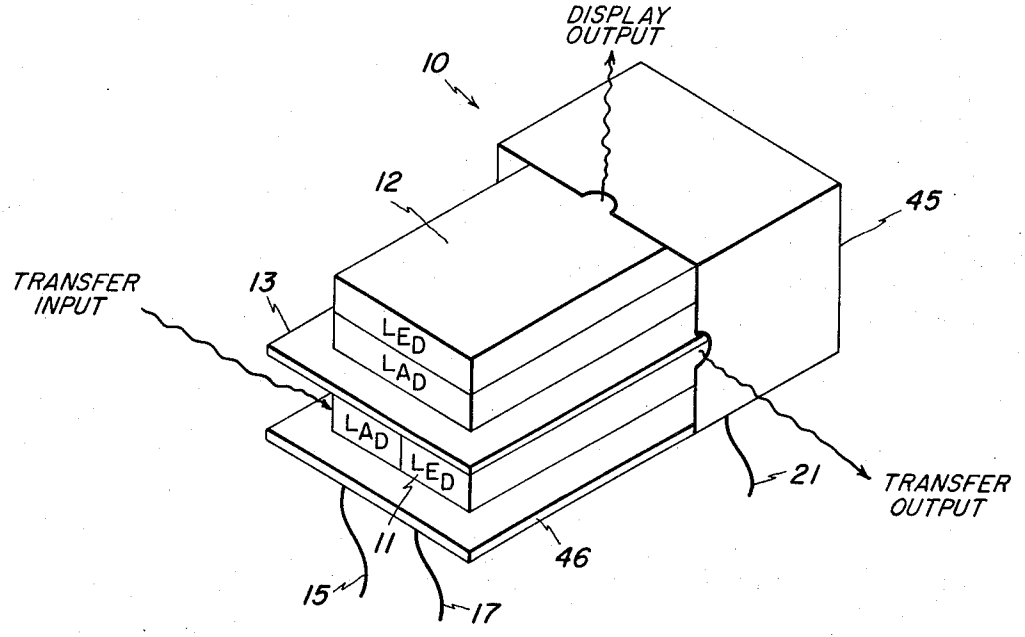


FIG. 3



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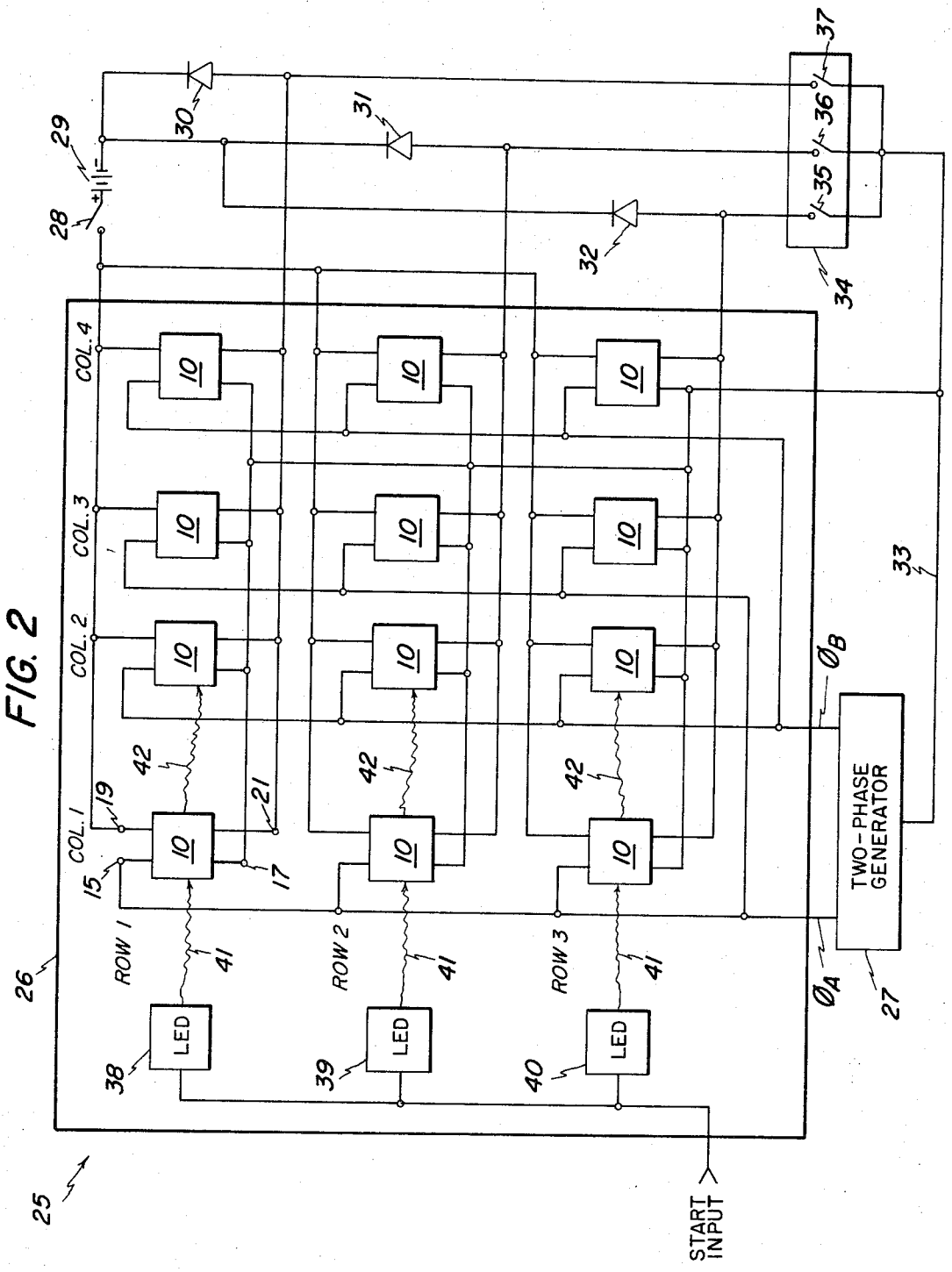

FIG. 2

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FIG. 4

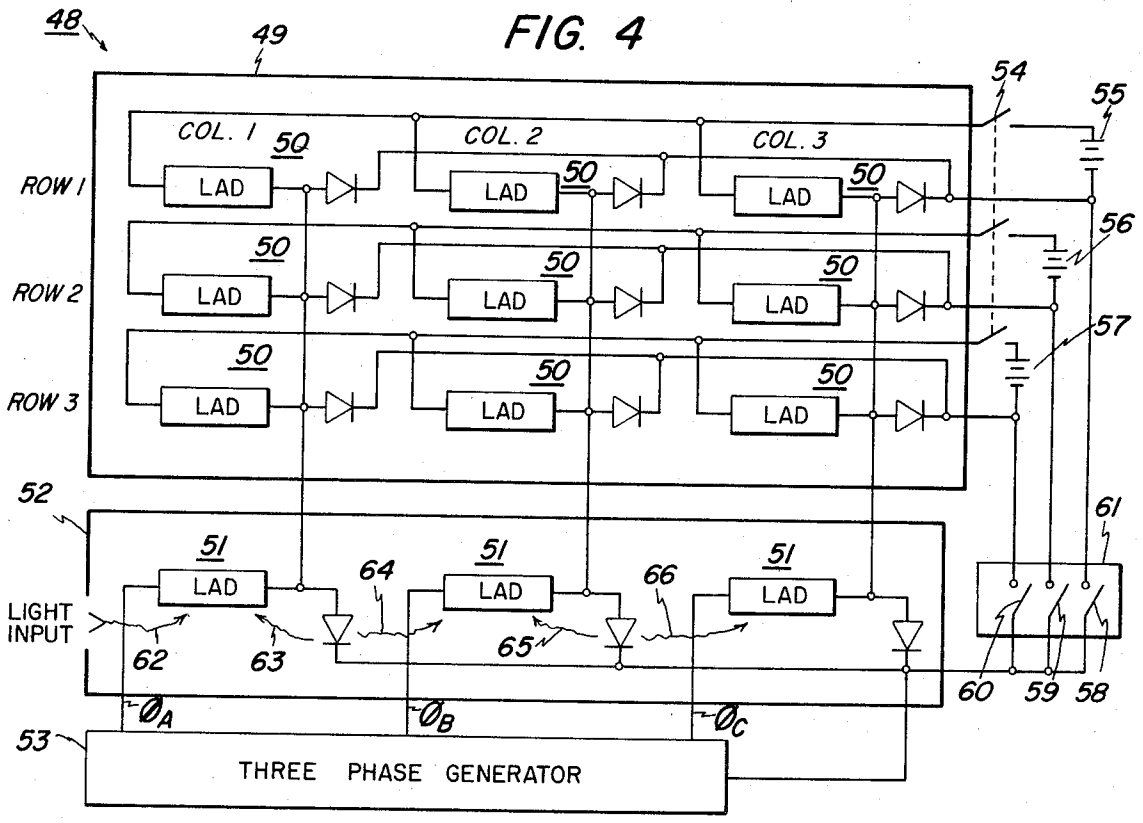

FIG. 5

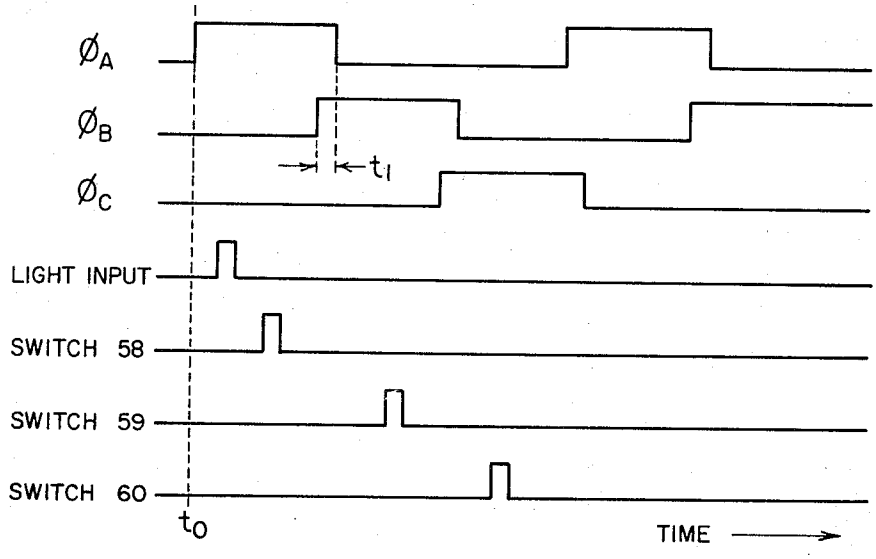

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FIG. 6

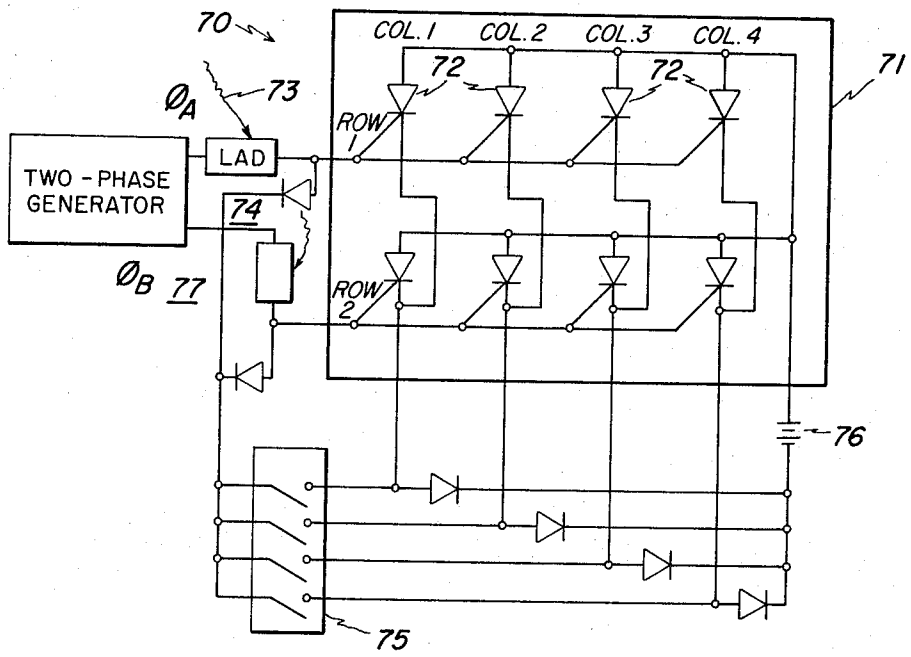
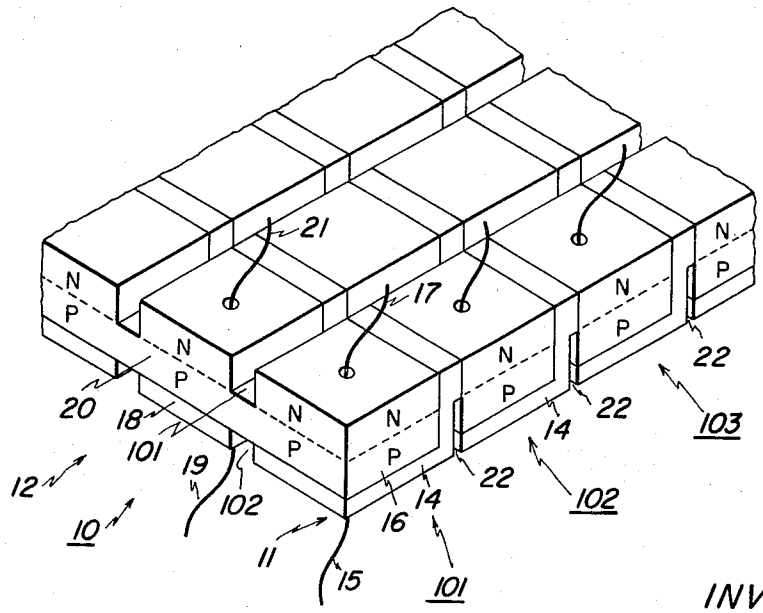


FIG. 8



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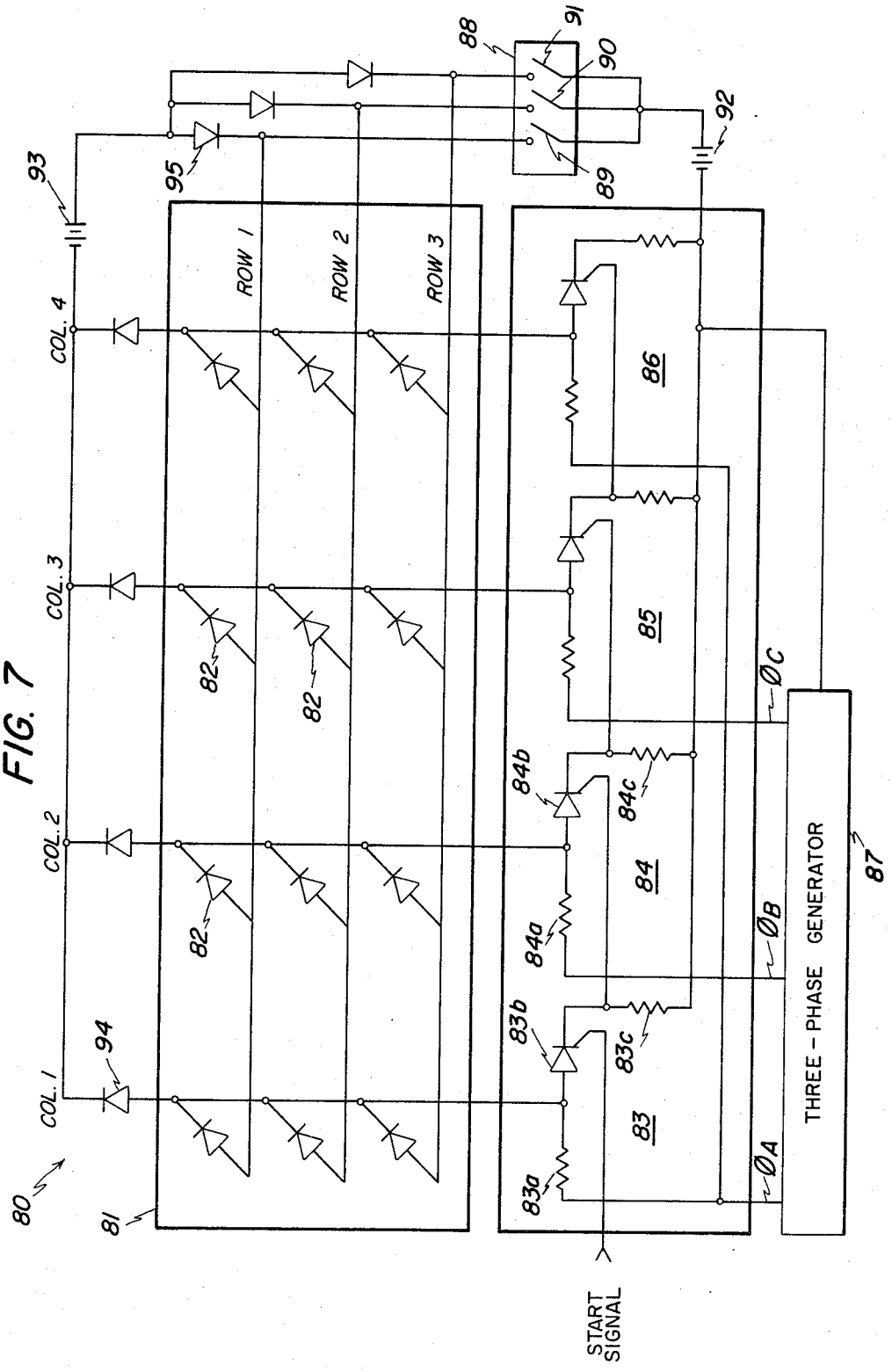

FIG. 7

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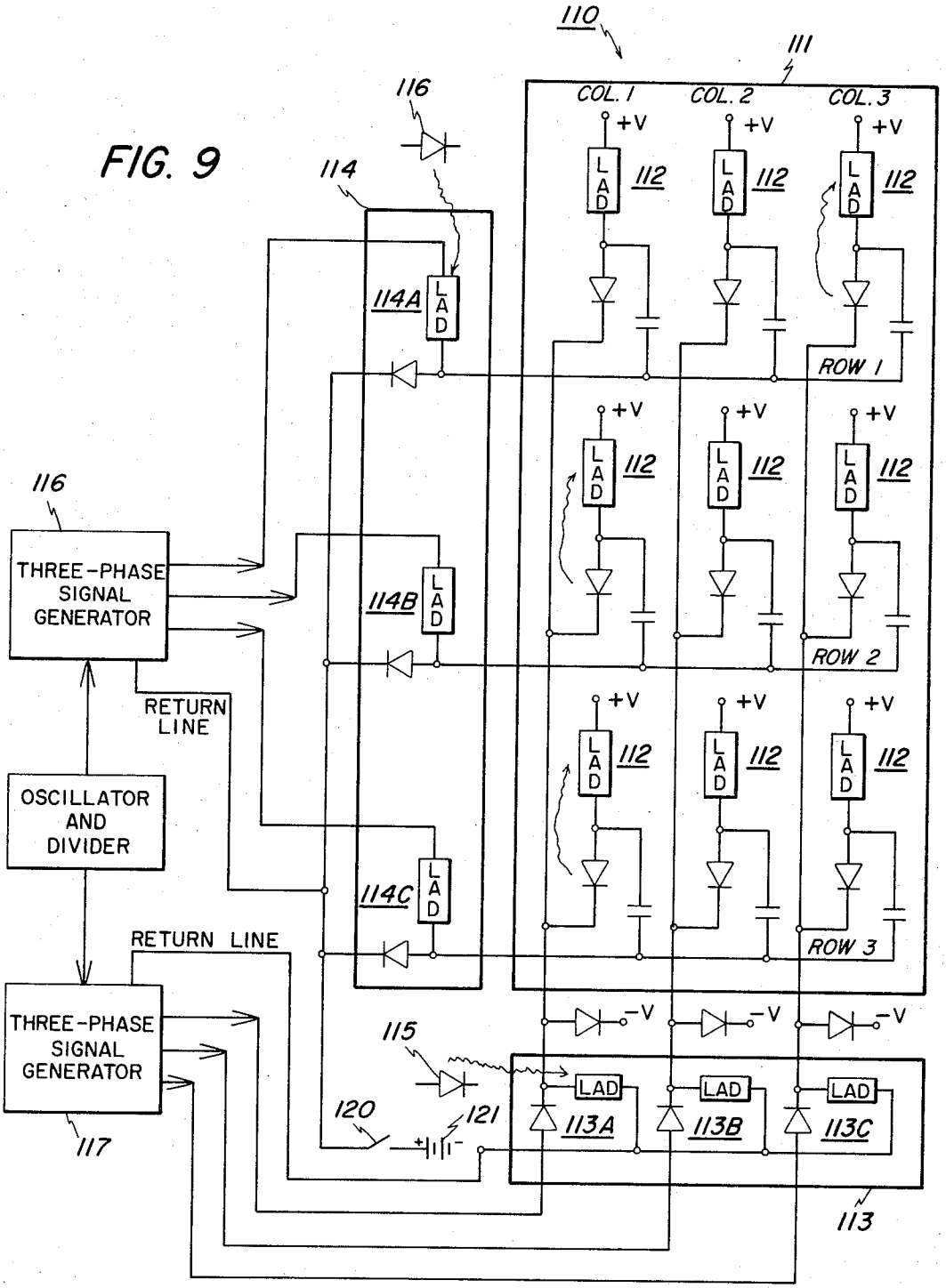
FIG. 9



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DISPLAY SYSTEM UTILIZING LIGHT EMITTING DEVICES

This invention relates to display systems and more particularly to novel addressing methods and apparatus for achieving translation of information within a display system as well as displaying and storing the information.

The rapid advances in data processing equipment have spurred the way for new optical display systems. Basically, there are two general types of display systems, either analog or digital display systems. Analog display systems include light valves, lasers and cathode ray tubes. Digital display systems include electroluminescent and injection luminescent devices such as light-emitting diodes. Within these two broad categories of display systems, numerous specific devices have been proposed and some are in use in conjunction with data processing systems. These display systems, however, lack the ability to provide an internal memory capability; i.e., the ability to store information within the display system itself and without the aid of external memory devices. Present-day display systems generally employ external memories which are used periodically to refresh or re-energize the display elements to produce a substantially flicker-free display. Not only are such display systems very costly and complex, but also are display size limited; i.e., since the display must be periodically refreshed, the size of the display is limited by the recycle time necessary to provide a flicker-free display. Additionally, the external circuitry necessary to generate the desired display increases very rapidly with the size and makes construction of such a display exceedingly costly and difficult.

It is therefore an object of this invention to provide a display system having internal memory characteristics.

It is a further object of this invention to provide novel transfer and display elements for a sequentially addressed display system.

It is a further object of this invention to provide a display system having a minimum number of external connections to external address and driving circuitry.

It is yet a further object of this invention to provide a sequentially addressed display system with inherent internal memory capability.

These and other objects of the instant invention are achieved in accord with one embodiment thereof by providing a novel transfer and display-memory element comprising a transfer circuit and a display-memory circuit. In one embodiment, each circuit includes a light-activated device (LAD) and a light-emitting device (LED). By arranging the transfer and display-memory elements in rows and columns, and by sequentially addressing either the rows or columns of elements, a display apparatus with inherent transfer and display-memory capabilities is provided. In another embodiment of the invention, a single transfer circuit is connected in common with each display circuit of a particular row or column so as to reduce substantially the number of transfer circuits in large memory display panels. In yet another embodiment of the invention, the transfer and display-memory elements are formed on a monolithic integrated circuit wafer for providing high density display panels.

In still another embodiment of the invention rows and columns of display-memory circuits are time sequentially scanned to provide a minimum number of control lines for a display system.

The novel features believed characteristic of the present invention are set forth in the appended claims. The invention itself, together with further objects and advantages thereof, may best be understood by reference to the following detailed description taken in connection with the appended drawing in which:

FIG. 1 is a schematic diagram of a transfer and display-memory element in accord with one embodiment of the invention;

FIG. 2 is a partial schematic and partial block diagram of a three by four matrix of transfer and display-memory elements arranged in accord with another embodiment of the instant invention;

FIG. 3 is a perspective view of a physical embodiment of the transfer and display-memory device of FIG. 1;

FIG. 4 is a schematic diagram of a display panel having inherent transfer and display-memory capabilities employing a common transfer circuit for each column of an array;

FIG. 5 is an amplitude versus time diagram illustrating the time relationship of signals in the embodiment of FIG. 4;

FIG. 6 is a schematic diagram of a display system employing p-n-p-n semiconductor devices;

FIG. 7 illustrates an alternative embodiment of the invention employing p-n-p-n devices without control electrodes as display-memory circuits;

FIG. 8 is a perspective view of a monolithic integrated semiconductor wafer including transfer and display-memory elements arranged in rows and columns to provide a solid state display panel;

FIG. 9 is an embodiment of the invention illustrating a time sequentially addressed display system.

By way of example, FIG. 1 illustrates one embodiment of a transfer and display-memory element **10** comprising a transfer circuit **11** and a display-memory circuit **12** separated by an optical barrier **13**. The transfer circuit **11** comprises a light-activated device (LAD) **14** such as a photoconductive or photovoltaic device which exhibits a bistable impedance characteristic. One lead of the LAD **14** is connected to a terminal **15** and the other lead of the LAD is connected to a light-emitting device (LED) **16** which may, for example, be a semiconductor light-emitting diode. The other lead of the LED **16** is connected to a terminal **17**.

The display-memory circuit **12** comprises a light-activated device (LAD) **18** having one lead connected to a terminal **19** and the other lead serially connected with a light-emitting device (LED) **20** with the other lead of the LED connected to a terminal **21**. The display-memory circuit **12** is connected to the transfer circuit **11** at the junctures of the LAD **14** and LED **16** and the junctures of LAD **18** and LED **20**. The transfer circuit **11** and the display-memory circuit **12** are not, however, optically interconnected in any way. In fact, the optical barrier **13** prevents any interaction between the two circuits.

In operation, a voltage pulse applied between terminals **15** and **17** coincidental with an incident light signal on LAD **14** causes radiation from the light-emitting device **16**. The coincidence of the voltage pulse and the incident light is necessary since the light-

activated device would otherwise be in a high impedance condition and would not permit the passage of sufficient current flow therethrough to cause the LED **16** to emit light. However, once LED **16** emits light, the regenerative feedback of the light from LED **16** to LAD **14** causes LAD **14** to remain in its low impedance state thereby permitting LED **16** to remain conductive so long as the voltage pulse between terminals **15** and **17** persists. The output of LED **16** is also available for transfer to the next or adjacent transfer and display-memory element in the event that they are coupled together, as will be described hereinafter. During the time that LED **16** is emitting light, it is possible to store and display this condition by applying a voltage pulse of appropriate magnitude and polarity between terminals **15** and **21** so that radiation is emitted from LED **20**. After establishing radiation form LED **20**, the radiation may be continued by connecting terminal **19** to an independent voltage supply so that current may be drawn from that voltage supply, through LAD **18** which is now in its low impedance state by virtue of the regenerative coupling from LED **20**.

In this way, incident radiation on LAD **14** produces an output from LED **16** each time a voltage pulse is applied between terminals **15** and **17**. A display and storage signal is provided each time a pulse is applied between terminals **15** and **21** during the time interval that LED **16** is conducting. LED **20** remains conducting so long as terminal **19** is connected to a source of voltage to maintain current flow through LED **20**.

The usefulness of the transfer and display-memory element **10** will become more apparent from the embodiment of the invention illustrated in FIG. **2**. In this figure, a transfer and display-memory system **15** comprising a display panel **26** including a 3×4 array of transfer and display-memory elements **10** interconnected to perform a transfer and display-memory function. As illustrated in the drawing, the display panel **26** is addressed on a column-by-column basis; i.e., information to be displayed and stored on the display panel is "shifted" into the display panel one column at a time. Although illustrated as column-by-column addressing, those skilled in the art can readily appreciate that row-by-row addressing could similarly be employed if desired. In the embodiment illustrated, however, a two-phase generator **27** which may, for example, include a continuously operating clock such as an oscillator, with means for providing two-phase related outputs, preferably of the same frequency and 180 electrical degrees out of phase with each other. These phase related signals are illustrated in the drawing as ϕ_A and ϕ_B. The exact nature of these signals will become more apparent from the detailed description of the operation of the embodiment illustrated. The ϕ_A output of the column address generator **27** is connected to columns **1** and **3** and the ϕ_B output is connected to columns **2** and **4** of the transfer and display-memory element **10**. As also illustrated in FIG. **2** terminal **19** of each element is connected together and to a switch **28** which provides both a reset and a memory erase function which will be more fully described hereinafter. The switch **28** is illustrated as being normally closed and is connected to the positive terminal of a voltage source **29** illustrated as a battery. The terminals **21** of the elements in row **1** are connected together and through a diode **30** to the negative terminal of the voltage source **29**. In a similar manner, terminals **21** of the elements in row **2** are connected together and through a diode **31** to the negative terminal of the voltage source **29** and terminals **21** of row **3** are connected together and through a diode **32** to the negative terminal of the voltage source **29**. Terminal **17** of all elements in the array are connected together and to a common return bus **33** which is also connected to one side of a character generator **34** illustrated as comprising three electrical switchs **35**, **36** and **37**. Switches **35**, **36** and **37** are respectively connected to the anodes of diodes **32**, **31** and **30**. Although the character generator **34** is illustrated as comprising simple mechanical switches, those skilled in the art can readily appreciate that other switching devices such as relays or semiconductor switches could similarly be employed and, in fact, as will be illustrated hereinafter, are actuated by information to be displayed on the panel **26**. The drawing also illustrates three start generators **38**, **39** and **40** which may typically comprise a light-emitting diode which upon receipt of a start input signal emits light. The start generators **38**, **39** and **40** have their optical outputs **41** arranged in such a manner as to be optically coupled to the column **1** transfer and display-memory elements **10**.

The operation of the transfer and display-memory system **25** can be understood by considering the sequence of events which occur, if, for example, it is desired to display the letter "O" on the panel **26**. To provide such a display, a start input signal is applied to each of the start generators **38**, **39** and **40**. Light emitted from these generators is coupled to the light activated devices in each of the elements in column **1**. If during a first time interval, the column and address generator **27** provides a ϕ_A output, which is coincidental with the radiation from the start generators, each element in column **1** will provide a radiation output **42** which is available for transfer to column **2**, In order that a transfer to column **2** may be accomplished, the ϕ_B signal from the column address generator **27** should occur before the signal appearing on the ϕ_A line terminates. During this period of coincidence, the radiation from the elements in column **1** reduce the impedance of the light-activated device in the column **2** elements and hence permit current flow through the light-emitting devices associated therewith so that the light-activated device continues to remain in a low impedance condition and hence effect the transfer of radiation from the column **1** element to the column **2** element.

Since it is desired to produce or display the letter "O," during the ϕ_A signal time, it is necessary to activate the necessary display circuits in column **1** so as to form the letter "O." This is achieved by momentarily, at least, closing switches **35**, **36** and **37** of the character generator during the time interval in which the ϕ_A signal is present. As a result of these momentary switch closures, current flows from terminal **15** to terminal **21** through the switches in the character generator and back to the column address generator **27** so that radiation is emitted from the light-emitting devices in column **1**. Once the radiation begins it is maintained by current flow from the voltage source **29** through terminal **19** and **21** back to the voltage source **29** through diodes **30**, **31** and **32**. In this way, once radiation com-

mences from a particular element, it continues until current flow to the device is interrupted. As illustrated in the figure, switch **28** provides such a means for interruption if desired.

To complete the formation and display of the alphanumeric letter "O" on the panel **26**, during the ϕ_B time interval, it is necessary to close switches **35** and **37** so that elements in column **2**, row **1** and row **3**, are activated. If these switches are closed during the ϕ_B time interval, the respective display elements will be illuminated. With the reoccurrence of the ϕ_A clock before the termination of the ϕ_B clock, radiation emitted from the transfer circuits of the elements in column **2** are transferred to the transfer circuits in the elements of column **3**. By closing switches **35** and **37** again during the ϕ_A time interval, the next portion of the letter "O" is formed. The final portion of the letter "O" is formed by the transfer of radiation from column **3** to column **4** and subsequently closing switches **35, 36** and **37** so that all elements in column **4** are activated. In this way, the letter "O" is formed by radiation from all the elements in columns **1** and **4** and only the elements in rows **1** and **3** of columns **2** and **3**. The display of the letter "O" will continue until current flow to the light-emitting devices in the display is interrupted. This continuous display represents the memory function of the transfer and display-memory system **25**. The memory may be completely "erased" by opening switch **28** or may be selectively erased by interrupting the current flow to any particular row, column or specific element if desired.

From the above description of an embodiment of the invention, those skilled in the art can readily appreciate the numerous attendant advantages of my invention. For example, whereas prior art display systems require recycling or refreshing of the display element to provide a flicker-free display, in accord with my invention, no such recycling is necessary. In addition, whereas prior art systems are limited in the number of elements which can be provided in a display by the recycle time, no such limitation is present in display systems constructed in accord with my invention. Additionally, by addressing a display panel in the manner described above, the number of external connections to be made to the display panel is substantially reduced.

FIG. **3** illustrates a transfer and display-memory element **10** constructed in the form of a module **45** having a base portion **46** with the transfer circuit **11** comprising an LAD and an LED supported thereon. Directly above the transfer circuit and optically isolated therefrom by the barrier **13** is the display-memory circuit **12** also comprising an LAD and an LED. The LAD and LED components may either be discrete devices or integrated circuit elements fabricated on a semiconductor wafer by suitable processing techniques. In this embodiment of the invention, it is preferable to arrange the components so that it is possible to interconnect a plurality of such modules to make a display panel, such as that described above with reference to FIG. **2**. As illustrated in FIG. **3**, a typical arrangement might include an input side of the module for receiving incident radiation and an output side of the module for providing an output radiation signal in response to incident radiation and an appropriate voltage signal. As further indicated in the figure, yet another side of the module provides the display and storage output. By this arrangement, optical coupling between adjacent modules can be readily provided.

The wave lengths of the radiation transmitted and received by the transfer circuit may be selected to be in the invisible range, for example, while the display and memory circuit may be selected to have a wavelength of radiation in the visible or infrared range if desired. Numerous combinations and variations in wavelength are available for varied applications. For example, the LAD's described herein may be photoconductive cells employing cadmium sulfide or cadmium selenide having on-to-off resistivity ratios of 10^5 or less and spectral responses in the visible and infrared regions. The LED's may, for example, be GaP light-emitting diodes having emissions in the red and green spectral regions or Ga(As,P) light-emitting diodes having emissions in the red and infrared regions. Accordingly, it is to be understood that the instant invention may be practised by employing various light-emitting and light-activated devices.

Although the embodiment of the invention illustrated in FIG. **2** employs two light-activated devices and two light-emitting devices, there are numerous applications in which certain simplifications can be employed. For example, whereas the embodiment illustrated in FIG. **2** employs a transfer circuit for each element in the array, it is possible by making only slight modifications to the electrical connections to employ a single transfer circuit for each column, in the case of column-by-column addressing. FIG. **4** illustrates a typical embodiment of such a display system with three rows and three columns.

In FIG. **4**, a display system **48** having inherent transfer and display-memory capabilities is described as including a display panel **49** comprising a 3×3 array of display-memory circuits **50** each including a light-activated device and a light-emitting device which may be similar to those described above with reference to FIGS. **1** and **2**. As illustrated, each display circuit **50** in a particular column is connected in parallel with a single transfer circuit **51**, which may also be similar to those described above with reference to FIGS. **1** and **2**. The three transfer circuits **51** comprise a column address generator **52**. The LAD of each transfer circuit **51** is connected to an output of a three-phrase generator **53** which in accord with this embodiment provides outputs labeled ϕ_A, ϕ_B and ϕ_C, respectively connected to the transfer circuits of column **1**, column **2** and column **3**. The three outputs from the three-phrase generator **53** are, for example, pulsed signals of the same frequency and spaced from the other signal by about 120 electrical degrees. The exact nature of these signals will be described hereinafter with respect to FIG. **5** of the drawing.

One terminal of the LAD's of each display circuit **50** and one side of a switch **54** are connected together to provide a function similar to that described above, i.e., to erase the information stored in the display circuits. The other side of the switch **54** is connected to the positive terminal of three voltage sources illustrated generally as batteries **55, 56** and **57** which, respectively, have their negative terminals connected to the LED's of row **1**, row **2** and row **3**. In addition to being connected to the LED's, the negative terminals of the

voltage sources 55, 56 and 57 are connected to switches 58, 59 and 60, respectively, of a character generator 61. Again, it should be understood that the character generator 61 is illustrated in one of its simplest forms, and it is to be understood that numerous other character generators are contemplated and accordingly, my invention is not intended to be limited solely to mechanical switches.

Each LED in the transfer circuits 51 has a terminal connected together and to a common terminal of the character generator 61 and the three-phase generator 53.

The operation of the display system 48 of FIG. 4 will now be described with reference to the signal diagram of FIG. 5 wherein there is illustrated the timing relationship between signals useful in practising the embodiment of the invention illustrated in FIG. 4. More particularly, FIG. 5 illustrates the timing relationship between the clock pulses ϕ_A, ϕ_B and ϕ_C. As illustrated, there is a short time period t_1 during which the ϕ_A and ϕ_B signals overlap or occur coincidentally in time, and a similar period between ϕ_B and ϕ_C, and between ϕ_C and ϕ_A. In addition to the output signals from the column address generator 52, a light input signal 62 is illustrated as the start signal for the transfer and display of information on the display system 48. The time relationship of the light input signal 62 with respect to the ϕ_A signal is illustrated in FIG. 5.

By way of illustration then, assume that it is desired to provide a transfer and display-memory function on the display system 48. Thus, for example, to provide display and storage at column 1-row 1, column 2-row 2 and column 3-row 3 locations, then in accord with the circuit configuration of FIG. 4, the light input signal 62 causes the LAD of transfer circuit 51 of column 1 to become a low impedance during this time. The occurrence of the ϕ_A clock signal during this time interval enables current flow through the LAD and LED and hence causes the emission of light from the LED. FIG. 4 illustrates the light emission as being divided in two parts. The first part, 63, provides regenerative feedback to the LAD to maintain its low impedance condition and hence permit the continued emission of light from the LED. The second part of the light emitted from the transfer circuit 51 of column 1, 64, provides an output signal to the adjacent LAD of transfer circuit 51 in column 2.

The display at column 1-row 1 is provided by closing switch 58 in the character generator 61 during the time interval that ϕ_A is being applied to the transfer circuit 51. When the switch closure occurs, additional current begins to flow through the LAD in the transfer circuit 51 of column 1 to the LED of the display circuit 50 of column 1-row 1 and back to the common return line. Once current flow is established through this LED, regenerative feed-back reduces the impedance of its associated LAD and current flow from the voltage source 55 through switch 54 is provided independent of the condition of the switch 58 in the character generator 61. In this way, continuous storage or memory of the information, as represented by a switch closure of the character generator is provided in the position column 1-row 1.

With the passage of time, the ϕ_B clock pulse is applied to the transfer circuit 51 of column 2. As illustrated in FIG. 5, however, there is a period of time t_1 in which the ϕ_A and ϕ_B pulses coincide. During this interval, the light 64 emitted from the transfer circuit 51 in column 1 is coupled to the adjacent transfer circuit 51 in column 2. Since ϕ_B is also present during this interval, the LED of the transfer circuit 51 of column 2 provides an output signal 65 which maintains this output condition even after the ϕ_A output goes to 0. When, during the pulse interval ϕ_B, character generator 61 provides a closure of switch 59, then as described above, the display circuit associated with column 2-row 2 emits light. Once light emission is initiated, it continues by virtue of the current provided from voltage source 56. In a similar manner, upon the occurrence of the ϕ_C clock pulse, there is a transfer from transfer circuit 51 of column 2 to transfer circuit 51 of column 3. This transfer is effected by the emission of light 66 and the coupling thereof to the transfer circuit 51 of column 3. With the closure of switch 60 in the character generator 61 during the ϕ_C time period, a light signal is emitted from the display circuit 50 of column 3-row 3. Light emission is sustained by the voltage source 57 in a manner described previously.

Display system 48 therefore provides a visual display at column 1-row 1, column 2-row 2 and column 3-row 3. This display continues without interruption and without the need for "refreshing" or "recycling" the display circuits. In fact, the display will continue until the current paths between voltage sources 55, 56, and 57 are interrupted by the opening of switch 54. After momentarily opening switch 54, all display circuits are placed in a reset condition and are ready for the next sequence of events to occur.

Those skilled in the art can readily appreciate that the display system illustrated in FIG. 4 not only has the attendant advantages described with reference to the embodiment illustrated in FIG. 2, but further is characterized by employing only a single transfer element for each column, in the case of column-by-column addressing. This feature is particularly significant since in large arrays of display circuits, the number of transfer circuits is equal to the number of columns or rows, depending upon the direction of transfer as opposed to the embodiment illustrated in FIG. 2 which requires the product of the number of rows and columns in transfer elements. The embodiment of the invention illustrated in FIG. 4 also describes an alternative means for providing voltage sources for sustaining the emission of light from selected display circuits. Whereas the embodiment illustrated in FIG. 2 employs only a single voltage source 29, the embodiment illustrated in FIG. 4 employs a number of voltage sources equal to the number of rows of display circuits. This increase in the number of voltage sources is due to the common connection between display circuits of a particular column. More specifically, a separate voltage source for each row eliminates the possibility of activating a display circuit in a row not selected by the character generator 61. Those skilled in the art can readily appreciate that other arrangements of voltage sources are possible and that the invention is not limited solely to the arrangement illustrated in FIGS. 2 and 4. These embodiments are by way of illustration of my invention and are not to be construed as limiting the scope thereof.

Another important feature of my invention is the versatility with which different control signals can be accommodated. For example, whereas the embodiment illustrated in FIG. 2 employs a two-phase clocking system, the embodiment illustrated in FIG. 4 employs a three-phrase clocking system. By merely changing the column (or row) interconnections, it is possible to accommodate most any type of clocking system. However, those skilled in the art can appreciate that the transfer circuit parameters in a two-phase system are more critical than in a three-phase system.

In the embodiments of my invention illustrated in FIGS. 1 through 4, I have illustrated the use of a light-emitting and light-activated device to perform the transfer and display-memory functions; however, as will be described hereinafter, my invention also includes other devices such as, for example, p-n-p-n semiconductor devices which preferably exhibit a negative resistance characteristic. In addition, as will also become apparent from a later discussion hereinafter, it is possible to employ the process technology of the semiconductor art and fabricate display systems of monolithic integrated circuit elements on semiconductor substrates. The manner in which other semiconductor devices, such as p-n-p-n devices, can be employed in display systems made in accord with the teachings of the instant invention, reference is made to FIG. 6.

In FIG. 6 a row-by-row sequentially addressed display system 70 is illustrated as comprising a 2 × 4 display panel 71 in which the display-memory circuits comprise single p-n-p-n devices 72 connected in the manner illustrated. By the use of a single p-n-p-n device, it is possible to replace the light-activated device and the light-emitting device in each display circuit. The p-n-p-n devices preferably exhibit a negative resistance characteristic which inherently provides regenerative feed-back so that one conduction is initiated by the passage of current between the anode and cathode electrodes, current continues to flow and hence light continues to be emitted therefrom until the current flow in interrupted. In other respects, the embodiment of the invention illustrated in FIG. 6 is substantially similar to those described with reference to FIGS. 2 and 4. The operation is initiated by the coincidence of a clock pulse ϕ_A and a light input signal 73 to the LAD of transfer circuit 74 so that a voltage pulse appears on the gate electrodes of the display devices 72. Upon closing one of the switches in the character generator 75, current flows through the display device associated with the particular switch and once current flow is initiated, it is sustained by the voltage source 76. Upon occurrence of the ϕ_B pulse, transfer is effected between transfer circuit 74 and transfer circuit 77. In a similar manner as just described, by closing one of the switches in the character generator 75, one or more of the light emitting devices 72 in row 2 is activated. Once activated, the emission of light is sustained by current flow from the source 76.

FIG. 7 illustrates yet another embodiment of my invention wherein negative resistance light-emitting devices without a gate electrode (in the case of a p-n-p-n structure) are employed. By the use of such devices, it is possible to reduce still further the number of electrical contacts which are to be made in the array. The embodiment of the invention illustrated in FIG. 7 also employs p-n-p-n semiconductor structures for the transfer circuits. Whereas the previous embodiments employed LED's and LAD's, with optical coupling between them to effect transfer, the embodiment illustrated in FIG. 7 employs direct electrical connections between adjacent transfer circuits and employs the negative resistance characteristic of each device to provide the regenerative feedback achieved by the optical feedback of the previous embodiments.

FIG. 7 illustrates a display system 80 comprising a display panel 81 including an array of p-n-p-n semiconductor light-emitting devices 82 arranged in a 3 × 4 matrix of rows and columns with the cathode terminals of each device in a column connected together and to a transfer circuit in a column address generator. More specifically, the cathodes of devices 82 in column 1 are connected to a transfer circuit 83 and those in columns 2, 3 and 4 are connected to transfer circuits 84, 85 and 86, respectively. The transfer circuits 83 through 86 each include two series connected resistors to produce the necessary voltage signals to effect the desired transfer. In particular, the transfer circuit 83 employs a first resistor 83*a* connected between the anode of solid state switch device 83*b* such as a silicon controlled rectifier or other p-n-p-n structure, and the ϕ_A output of a column address generator 87, similar to those described above. A second resistor 83*c* is connected between the cathode of the solid state switching device 83*b* and the common return line of a three-phase generator 87. The transfer circuits 84 through 86 are similarly connected with the first resistor in each case being connected to the three-phase generator and the second resistor being connected to the common return line.

The anodes of each display device 82 in a particular column are connected together and to a switch in a character generator 88. In particular, rows 1, 2 and 3 are respectively connected to switches 89, 90 and 91. The other terminals of these switches are connected together and to the positive terminal of a voltage source 92 which has its negative terminal returned to the common return line of the column address generator 87.

When a start signal is applied to the gate electrode of the solid state switching device 83*b* coincidentally with the ϕ_A clock pulse, current flows through the solid state switching device 83*b* and if any of the switches in the character generator 88 are closed, one or more of the display elements 82 in column 1 will emit light by virtue of current flow through the selected display element, the solid state switch 83 and the voltage source 92. The current flow, once initiated, is maintained by a voltage source 93. For example, if the display element 82 at column 1-row 1 is activated, with the closing of switch 89 during the ϕ_A pulse period, light emission from this display element is continued by current flow from the voltage source 93 through a diode 94, the display element 82 and a diode 95 back to the voltage source 93. Diodes 94 and 95 function to isolate the voltage source 93 from other display elements 82 which are not activated during a selected time interval.

The transfer from column 1 to column 2 is effected by the passage of current through the resistor 83*c* which produces a voltage drop thereacross sufficient to

enable the control gate electrode of the solid state switching device **84***b*. With the occurrence of the ϕ_B clock pulse coincidentally with the ϕ_A clock pulse the switching device **84***b* is permitted to conduct current and hence the transfer from column **1** to column **2** is effected. In a similar manner, transfer is effected through all other elements in the array and a desired pattern is displayed on the panel **81** in accord with the selected switch closures in the character generator **88**.

Although the embodiment of my invention illustrated in FIG. **7** employs discrete components, it is to be understood that integrated semiconductor circuit components could be employed. For example, the transfer circuits **83** through **86** could be formed in a semiconductor substrate by employing a plurality of closely spaced p-n-p-n devices with appropriate control voltages applied thereto to effect transfer from one column or row to another.

Those skilled in the art can readily appreciate that the embodiments of my invention illustrated and described above provide numerous advantages over prior art display systems which have no internal memory. Among these advantages are the reduction in the number of external connections necessary for the display panel, the reduction in the number of drive elements for the panel, the elimination of external circuitry necessary to refresh the display and much higher addressing rates for the display panel.

While the above described embodiments of my invention and variations thereof meet the needs of most applications, higher density arrays are more feasible when constructed on a semiconductor substrate in the form of integrated circuits. For example, by employing the process technology of the semiconductor art, it is possible to construct display panels of high density on semiconductor substrates such as GaAs, GaP, ZnS and other Class III–V and Class II–VI semiconductor materials. FIG. **8** is illustrative of one embodiment of the invention employing monolithic integrated circuit elements fabricated on a semiconductor substrate. More particularly, FIG. **8** illustrates a partial perspective isometric view of a row or column of transfer and display-memory elements useful in practicing the instant invention. So that the integrated circuit configuration of FIG. **8** may be compared with the discrete circuit arrangement of FIG. **1**, like reference numberals are employed where possible.

In FIG. **8** I have illustrated a transfer and display-memory element **10** comprising a transfer circuit **11** including a light-sensitive device **14** and a light-emitting device **16** including a p-n light-emitting junction. FIG. **8** also illustrates a display circuit **12** comprising a light-sensitive device **18** and a light-emitting device **20** including a p-n light-emitting junction. As illustrated, a common p-type region is provided for light-emitting devices **16** and **20**; a portion of this common p-type region provides a conduction path for current flow between the transfer circuit **11** and the display and memory circuit **12**. FIG. **8** also illustrates the terminals **15**, **17**, **19** and **21** connected to the integrated circuit elements corresponding to those illustrated in FIG. **1**. As illustrated in FIG. **8**, the light-emitting devices **16** and **20** are separated by a channel **101** formed in the n-type semiconductor material and the light-activated devices **14** and **18** are separated by a channel **102** which is substantially parallel to the channel **101** but on the opposite surface of the p-type region. Adjacent transfer and display-memory element **102** is separated from element **10** by an electric barrier **22**, which may, for example, be just a gap or an insulating material such as an oxide or nitride of silicon. The function of the electric barrier **22** is to separate the various light-activated regions **14**.

Although the embodiment of my invention illustrated in FIG. **8** employs separate transfer circuits for each row or column, it is to be understood that in accord with the other embodiments of my invention wherein I have illustrated that it is unnecessary in certain situation to employ transfer circuits for each row or column, it can be readily appreciated by those skilled in the art that in making a monolithic integrated circuit display system similar simplifications can also be made. Additionally, whereas FIG. **8** illustrates p-n light-emitting devices, as illustrated above, other light-emitting devices can also be employed if desired. Accordingly, my invention may assume various configurations and therefore is not limited solely to that disclosed in FIG. **8**.

In each of the embodiments of my invention that I have illustrated and described above, I have employed either column-by-column or row-by-row addressing. As is apparent to those skilled in the art, these techniques of addressing provide display systems with numerous advantages over prior art display systems. Yet a further improvement in display systems can be achieved in accord with another embodiment of my invention wherein I disclose addressing a display system in two dimension; i.e., both on a column-by-column and a row-by-row basis time sequentially. By employing both column-by-column and row-by-row addressing, hereinafter referred to merely as time sequential addressing, I am able to reduce still further the number of external connections necessary to operate a display system. In fact, as will become more apparent from the following description, it is possible to provide high density arrays with large numbers of array elements and to control both the transferring and the displaying of information thereon by approximately **10** external connections, no matter how large the number of display elements in the array.

In FIG. **9** I have illustrated a time sequentially addressed display system **110** comprising a display panel **111** having an array of display circuits **112** arranged in a 3 × 3 matrix of rows and columns. Each display circuit comprises an LED and an LAD, such as those described above and a capacitor connected between the junction of the LED and LAD and a common row line. The function of the capacitor will be described below. The display panel **111** is addressed by a column address generator **113** and a row address generator **114**. Each generator comprises a plurality of transfer circuits equal to the number of rows or columns to be addressed. For example, the column address generator **113** includes three transfer circuits each having an LED and an LAD for transferring information from one column to the next upon receipt of a start command signal from a signal source illustrated schematically as a light-emitting diode **115**. The row address generator **114** similarly includes a light-emitting and light-activated devices and also includes a start signal

generator **116**, also illustrated as a light-emitting device.

The operation of the time sequentially addressed display system may best be understood by considering the sequence of events which occur during a cycle of operation. For example, assume that the rate of transfer from column to column is much greater than that from row to row. A particular row, for example, row **1**, is selected by applying a voltage pulse to the row **1** transfer circuit **114A** from the three-phase signal generator **116**. Then, by stepping or scanning through all columns before the next row is selected, any or all display circuits in row **1** may be lighted simply by closing a character selection switch **120** at a time when the column scanning has reached the desired or selected display circuit. For example, to light the display circuit located at row **1**, column **3**, after having selected row **1** in the aforementioned manner, upon stepping or scanning through columns **1**, **2** and **3**, character selection switch **120** is closed during the interval of time during which column **3** is being scanned. The scanning of columns **1**, **2** and **3** is effected by the outputs from the three-phase signal generator **117** which controls the column scanning generator **113**. At the time when row **1** and column **3** are being scanned, and character switch **120** is closed, current flows from a voltage source **121**, illustrated generally as a battery, through the LAD in transfer circuit **113C** to the LED of row **1**, column **3** and through the capacitor associated therewith and the LAD of transfer circuit **114A** and through the three-phase generator **116** back to the voltage source **121**. Once lighted, the output is maintained by current flow from the voltage source associated with column **3**, illustrated in the drawing as +V. The current path in this case is from +V through the LAD, the LED and an isolation diode **118C** back to the negative terminal of the voltage source, illustrated in the drawing as −V. Those skilled in the art can appreciate that the capacitor provides direct current blocking while permitting alternating current to flow during the column scanning time period.

After addressing all display circuits in row **1**, column **2** is addressed by applying a signal to transfer circuit **114B** of the row address generator **114** from the three-phase signal generator **116**. During this period of time, all columns in the panel are sequentially addressed in a manner similar to that described above. In this way, each row and column is time sequentially addressed so that information as determined by the closures of the character switch **120**, are displayed and stored, if desired, on the display panel **111**.

From the above description of a time sequentially addressed display system, it is readily apparent that numerous benefits and advantages are derived. In particular, it can be readily appreciated that the size of the array may be increased to most any desired value without increasing the number of interconnecting lines between the display system and the environment. As illustrated, in general, a maximum of three lines from each of the two three-phase signal generators, two signal generator return lines and the sustaining voltage lines are employed regardless of the size of the array. Fewer lines can be employed if the generators are integral with the display. This feature is particularly attractive since it represents a solution to one of the most difficult problems encountered in providing large display systems which generally require at least one line for each row or column or both depending upon the particular method or means of addressing.

It is to be understood that although FIG. **9** illustrates the time sequentially addressed display system as comprising discrete semiconductor elements, those skilled in the art can readily appreciate that integrated circuit techniques similar to those described above can likewise be employed in making arrays. In fact, in view of the high density achievable by employing semiconductor techniques, and further in view of the limited number of external connections which need to be made to the display panel, the fabrication of integrated circuit display panels may, in fact, be preferable in many instances. Additionally, the transfer and display-memory circuits illustrated in several of the other embodiments of my invention may also be employed in the time sequentially addressed system of FIG. **9**. For example, the transfer circuits may employ p-n-p-n devices and the display circuits may similarly employ light-emitting p-n-p-n devices either with or without a control electrode. Accordingly, it is to be understood that the embodiment of my invention illustrated in FIG. **9** is merely by way of illustration of one embodiment thereof and is not to be construed in a limiting sense.

From the aforementioned description of several embodiments of my invention, it can be readily appreciated by those skilled in the art that I have discovered a new method and apparatus for achieving the translation of information within a display system as well as displaying and storing information without the need for any external memories or electronic circuitry to constantly refresh the display system. Further, apparatus constructed in accord with the instant invention permit higher addressing speeds than those attainable by prior art techniques and result in display systems which are not limited in size by recycle times or "flicker" problems of the prior art. In accord with yet another advantage of my invention, I have provided a two-dimensionally scanned array which employs time sequential addressing so as to permit the use of high density display panels with only a minimum number of external connections which are substantially independent of the number of array elements.

While the invention has been set forth herein with respect to certain specific embodiments and examples thereof, many modifications and changes will occur to those skilled in the art. Therefore, it is intended that the appended claims cover all such changes and modifications as fall within the true spirit and scope of my invention.

What I claim as new and desire to secure by Letters Patent of the United States is:

1. An electrical device comprising

a first electrical circuit including a first light-activated device and a first light-emitting device connected in series in the order named between a first terminal and a second terminal,

a second electrical circuit including a second light-activated device and a second light-emitting device connected in series in the order named between a third terminal and a fourth terminal,

said second light-activated device and said first light-emitting device connected in series in the order

named between said third terminal and said second terminal,

means providing an optical barrier between said first electric circuit and said second electrical circuit,

means providing optical coupling between said first light-emitting device and said first light-activated device,

means providing optical coupling between said second light emitting device and said second light-activated device,

whereby when operating potential is applied between said third and fourth terminals and a light signal is applied to said second light-activated device, the impedance of said second light-activated device is decreased to a small value and current flows through said second light-emitting device and causes light emission therefrom, said light emission being coupled to said second light-activated device maintains the impedance of said second light-emitting device at said low value independent of said light signal,

means establishing an electrical current flow through said second light-activated device and said first light-emitting device to cause light to be emitted by said first light-emitting device,

means for providing operating potential between said first and second terminals, whereby the impedance of said first light-activated device is decreased to a small value and current flows through said first light-emitting device and conduction is maintained therein independent of said light signal.

2. The combination of claim 1 in which said light-activated device is a photoconductive diode and in which said light-emitting device is a light emitting diode.

3. A display system comprising

a plurality of light emitting elements, each including a first terminal, a second terminal and a third terminal, said elements arranged in a plurality of rows and columns,

a plurality of row conductors, said row conductors arranged in sets including a first and a second conductor for each row, each of the first conductors connecting the first terminals of the elements of a respective row, each of the second conductors connecting the second terminals of the elements of a respective row,

a plurality of column conductors, each of the column conductors connecting the third terminals of the elements of a respective column,

means for applying operating potential between the first and second conductors of each of said rows,

transfer circuit means for sequentially energizing said column conductors to energize sequentially the third terminals of the elements connected thereto,

switching means for selectively and momentarily energizing said second conductors during each energization of a column conductor,

each of said elements having the characteristic that when an energizing potential is applied to said second terminal and another energizing potential is applied to said third terminal along with operating potential being applied between said first and second terminals, said element becomes energized and maintains energization until operating potential to said first and second terminals is interrupted,

whereby after a sequence of energization of the column conductors selective ones of said elements are energized and are maintained in energization until operating potential between said first and second terminals is interrupted.

4. The combination of claim 3 in which said light-emitting element is light-activated device and a light-emitting device connected in series in the order named between said first terminal and said second terminal, in which the common connection of said devices is said third terminal, and in which the output of said light-emitting diode is optically coupled to said light-activated device.

5. The combination of claim 3 in which said column conductors are arranged in two sets, one set including odd-numbered conductors and the other set including even-numbered conductors, said transfer circuit means providing energization alternately to said two sets of conductors.

6. The combination of claim 5 in which each of said light-emitting elements comprises

a first electrical circuit including a first light-activated device and a first light-emitting device connected in series in the order named between said first terminal and said second terminal,

a second electrical circuit including a second light-activated device and a second light-emitting device connected in series in the order named between said third terminal and a fourth terminal,

said second light-activated device and said first light-emitting device connected in series in the order named between said third terminal and said second terminal,

means providing an optical barrier between said first electric circuit and said second electrical circuit,

means providing optical coupling between said first light-emitting device and said first light-activated device,

means providing optical coupling between said second light-activated device,

whereby when operating potential is applied between said third and fourth terminals and a light signal is applied to said second light-activated device, the impedance of said second light-activated device is decreased to a small value and current flows through said second light-emitting device and causes light emission therefrom, said light emission being coupled to said second light-activated device maintains the impedance of said second light-emitting device at said low value independent of said light signal,

means establishing an electrical current flow through said second light-activated device and said first light-emitting device to cause light to be emitted by said first light-emitting device,

means for providing operating potential between said first and second terminals, whereby the impedance of said first light-activated device is decreased to a small value and current flows through said first light-emitting device and conduction is maintained therein independent of said light signal, and in which the second light-emitting device of each element in a row is optically coupled to the second

light-activated device of the succeeding element in the same row, in which the fourth terminals of said elements is connected to said transfer circuit means, in which the time of energizing of a column conductor overlaps the time of energization of the succeeding column conductor, and in which means for applying an optical signal is provided to activate the second light-activated devices of each of the elements in the first column of elements.

7. A display system comprising

a plurality of light-emitting elements, each including a first terminal, a second terminal, and a third terminal, said elements arranged in a plurality of rows and columns,

a plurality of row conductors, said row conductors arranged in sets including a first and a second conductor for each row, each of the first conductors connecting the first terminals of the elements of a respective row, each of the second conductors connecting the third terminals of the elements of a respective row,

a plurality of column conductors, each of the column conductors connecting the second terminals of a respective column,

means for applying operating potential between said first conductors and said column conductors,

transfer circuit means for sequentially energizing the second conductors of said rows to energize the third terminals of the elements connected thereto,

switching means for selectively and momentarily energizing said column conductors during each energization of a second conductor of a row,

each of said elements having the characteristic that when an energizing potential is applied to said second terminal and another energizing potential is applied to said third terminal along with operating potential being applied between said first and second terminals, said element becomes energized and maintains energization until operating potential to said first and second terminals is interrupted,

whereby after a sequence of energization of the column conductors selective ones of said elements are energized and maintained in energization until operating potential between said first and second terminals is interrupted.

8. The combination of claim 7 in which said light-emitting elements are p-n-p-n negative resistance devices having main current-carrying terminals corresponding to said first and second terminals and a gate electrode corresponding to said third terminal.

9. A display system comprising

a plurality of light-emitting elements each including a first terminal and a second terminal,

said elements arranged in a plurality of rows and columns,

a plurality of row conductors, each of said row conductors connecting the first terminals of said elements of a respective row,

a plurality of column conductors, each of said column conductors connecting the second terminals of said elements of a respective column,

means for applying operating potential between said column conductors and said row conductors,

each of said elements having the characteristic that when a sufficiently large potential is applied across said first and second terminals, said device becomes energized and only a small potential is required to sustain energization thereof, said operating potential means providing potential high enough to sustain energizing but not high enough to initiate energization therein,

circuit transfer means for sequentially energizing the conductors of said columns to energize the second terminals of the elements connected thereto,

means for selectively and momentarily energizing the conductors of said row during each energization of a column conductor, the simultaneous application of energization by said row conductor energizing means and said column conductor energizing means being sufficient to initiate energization of said element,

whereby after a sequence of energization of the column conductors, selective ones of said elements are energized and maintained energized until the circuits between said first and second terminals are interrupted.

10. The combination of claim 9 in which said light-emitting elements are p-n-p-n light-emitting devices.

11. The combination of claim 9 in which an isolation diode is provided in circuit between each of said row and column conductors and a terminal of a source of operating potential.

12. A display system comprising

a plurality of light-emitting elements, each including a first terminal, a second terminal and a third terminal, said elements arranged in a plurality of rows and columns,

a plurality of row conductors arranged in sets including a first and a second conductor for each row, each of the first conductors connecting the first terminals of said elements in a respective row, each of the said second conductors connecting the third terminals of said elements in a respective row,

a plurality of column conductors, each conductor connecting the second terminal of a respective column,

means for applying operating potential between said first conductors and said column conductors,

each of said elements having the characteristic that when an energizing potential is applied to said second terminal and another energizing potential is applied to said third terminal along with operating potential being applied between said first and second terminals, said element becomes energized and maintains energization until operating potential to said first and second terminals is interrupted.

first circuit transfer means for sequentially energizing the second conductors of said rows to energize the third terminals of the elements connected thereto,

second circuit transfer means for sequentially energizing the conductors of said columns to energize the second terminals of the elements connected thereto,

switching means for selectively and momentarily applying additional energization between each of

said column conductors and said second conductors of said rows during each energization of a column conductor, each of said second conductors taken in sequence for energization with said column conductors,

whereby after a sequence of energization of the second conductors of the rows and in conjunction therewith a plurality of sequences of energization of the column conductors for each energization of a second conductor of a row, selective ones of said elements are energized and maintained in energization until the application of operating potential between said first and second terminals is interrupted.

13 The combination of claim 12 in which the rate of sequential energizing of said second circuit transfer means is a multiple of the rate of sequential energizing of said first circuit transfer means, said multiple numerically equal to the number of said elements in a row.

14. The combination of claim 12 in which said light-emitting element is a light-activated device and a light-emitting device connected in series between said first and second terminals, in which the common connection of said devices is said third terminal, and in which the output of said light-emitting diode is optically coupled to said light-activating device.

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