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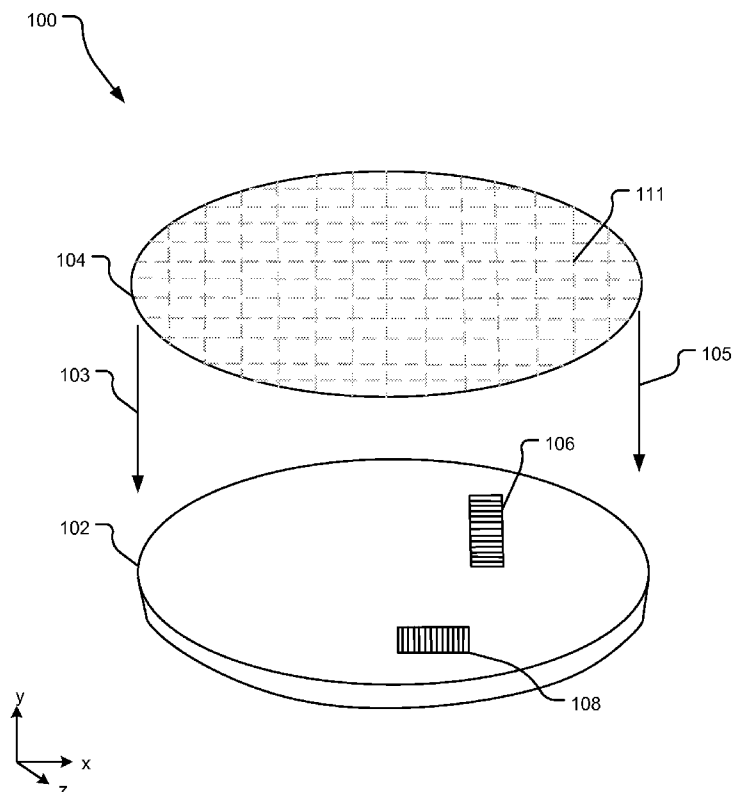
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(54) Title: ALIGNMENT MARK RECOVERY WITH REDUCED TOPOGRAPHY



(57) Abstract: When opaque films are deposited on semi-conductor wafers, underlying alignment marks 106, 108 may be concealed. The re-exposure of such alignment marks 106, 108 is one source of resulting surface topography. In accordance with one implementation, alignment marks 106, 108 embedded in a wafer 102 may be exposed by removing material from one or more layers and by replacing such material with a transparent material. In accordance with another implementation, the amount of material removed in an alignment mark recovery process may be mitigated by selectively ashing or etching above a stop layer.

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ALIGNMENT MARK RECOVERY WITH REDUCED TOPOGRAPHY

Cross-reference to Related Applications

The present application claims benefit of priority to U.S. Non-Provisional Patent Application No. 13/753,792, entitled "Alignment Mark Recovery with Reduced Topography" and filed on January 30, 2013, which is specifically incorporated by reference herein for all that it discloses or teaches.

Technical Field

The invention relates generally to lithographic processes involving semi-conductors and more particularly to technology for aligning a semi-conductor wafer with a mask or other hardware, such as during a lithographic printing process.

Summary

Implementations described and claimed herein provide for semi-conductor wafer alignment mark recovery processes that yield reduced surface topography. In accordance with one implementation, an alignment mark recovery process includes creating a cavity by removing opaque material oriented over an alignment mark embedded in a wafer to expose the alignment mark and thereafter filling the cavity with a transparent material to a depth substantially equal to the depth of the cavity.

This Summary is provided to introduce an election of concepts in a simplified form that are further described below in the Detailed Description. This Summary is not intended to identify key features or essential features of the claimed subject matter, nor is it intended to be used to limit the scope of the claimed subject matter. Other features, details, utilities, and advantages of the claimed subject matter will be apparent from the following more particular written Detailed Description of various implementations and implementations as further illustrated in the accompanying drawings and defined in the appended claims.

Brief Descriptions of the Drawings

FIG. 1 illustrates an alignment of a patterned template with a semi-conductor wafer using alignment marks.

FIG. 2 illustrates a cross-sectional view of a semi-conductor wafer having a number of layers and embedded alignment marks.

FIG. 3 illustrates another cross-sectional view of a semi-conductor wafer having a number of layers including a patterned photoresist layer on top of an undercut soluble polymer layer.

FIG. 4 illustrates another cross-sectional view of a semi-conductor wafer with a cavity etched therein to expose embedded alignment marks through a transparent layer.

FIG. 5 illustrates yet another cross-sectional view of a semi-conductor wafer with a filler layer deposited across the wafer to fill a cavity that tunnels through a number of opaque layers.

FIG. 6 illustrates yet another cross-sectional view of a semi-conductor wafer with alignment marks visible through transparent layers overlying the alignment marks.

FIG. 7 illustrates a cross-sectional portion of a semi-conductor wafer taken along the x-y plane of FIG. 1.

FIG. 8 illustrates a first alignment mark recovery process step wherein a portion of an upper opaque layer on a semi-conductor wafer is removed by a milling or etching operation.

FIG. 9 illustrates another alignment mark recovery process step wherein a portion of a lower opaque layer on a semi-conductor wafer is removed by a selective removal process to expose alignment marks.

FIG. 10 illustrates a flow-chart of example operations for an alignment mark recovery process according to one implementation.

FIG. 11 illustrates another flow-chart of example operations for an alignment mark recovery process according to another implementation.

Detailed Description

NanoImprint lithography (NIL) offers advanced pattern fidelity similar to ebeam lithography, but is significantly faster and offers throughput similar to optical lithography. Unlike optical lithography patterning, NIL requires direct contact between a wafer and a template mask that is pressed against the wafer. This direct contact permits capillary forces to draw droplets of liquid photoresist on the wafer into patterned grooves on the template mask. However, when significant topography is present on the wafer prior to NIL imprinting, such capillary forces may be insufficient to draw the liquid photoresist into the cavities. In such cases, NIL imprinting can be problematic.

As used herein, the term “significant surface topography” refers to features created on the surface of a wafer that are large enough to prevent the NIL template from making direct and substantially uniform contact with a photoresist on the wafer during NIL patterning.

Typically, this type of direct contact between the wafer and the NIL template is prevented when one hundred or more nanometers of topography are present on the surface of the wafer. Alignment mark recovery processes are one source of surface topography on semi-conductor and thin film head wafers

Alignment marks are visible marks made on or embedded in a semi-conductor wafer that can be used to align the wafer with a template mask (in the case of NIL patterning) or a photo mask (in the case of optical lithography patterning). However, the alignment marks may be concealed when one or more opaque film layers are deposited on the wafer.

Therefore, some semi-conductor processes include steps to remove the opaque films in the region over the alignment marks after they are concealed. For example, the opaque layers may be milled or etched away in some areas to recover (i.e., expose or make visible) the alignment marks. However, these milling or etching processes typically create significant surface topography.

Although polishing processes can remove some surface topography, polishing is time consuming and can create wafer uniformity problems. Additionally, polishing is not always time or cost efficient. Implementations of the methods disclosed herein significantly reduce surface topography created by alignment mark recovery processes. Consequently, the amount of polishing required after performing such a process is reduced or eliminated.

FIG. 1 illustrates an alignment 100 of a patterned template mask 104 with a wafer 102 using alignment marks 106 and 108. In one implementation, this alignment is performed as part of a NIL patterning step. The template mask 104 is a rigid, transparent plate with a grooved pattern on a wafer-facing side (e.g., the grooved pattern on the underside of the template mask 104 exemplified by dotted lines 111). In another implementation, the template 104 is of square or rectangular shape and sized such that it can “stamp” several different non-overlapping areas within the wafer 102 (i.e., a “step-and-repeat” process)

The wafer 102 is a substrate with a variety of layers formed thereon to perform a variety of different functions. Each of the layers on the wafer 102 may be independently formed, such as through a spin-coating, deposition, or a plating process. To create structures or patterns in one or more layers on the wafer 102, a template mask (such as the template mask 104) can be used to create a patterned photoresist (not shown) on the wafer 102 that

will “mask” and thus protect certain portions of the wafer 102 during one or more layer application processes.

In one implementation, the template mask 104 is a transparent template suitable for NIL imprinting on the wafer 102. A patterned photoresist is created on the wafer 102 by applying a template-facing side of the wafer with droplets of a liquid photoresist (not shown) and by bringing the template mask 104 into contact with the wafer 102 so that the droplets of photoresist on the wafer are pulled into the grooved patterns 111 on the template mask 104 by capillary forces. However, before the template mask 104 and the wafer 102 are brought into contact with one another, the template mask 104 and the wafer 102 are aligned using one or more alignment marks 106, 108 on the wafer (as illustrated by arrows 103 and 105 in FIG. 1). After contact is made between the aligned wafer 102 and template mask 104, the liquid photoresist is hardened by an exposure to a high intensity light directed through the transparent template mask 104.

In another implementation, the template 104 is a photo mask suitable for use in an optical lithography patterning process. Here, a patterned photoresist may be formed on the wafer 102 by directing high intensity light through transparent portions of the photo mask and, subsequently, through a lens (not shown) to project an image or pattern onto a liquid layer of photoresist deposited on the wafer 102. However, before the liquid photoresist is exposed to the high intensity light, the template 104 and the wafer 102 are aligned using one or more alignment marks 106 and 108 on the wafer 102. In one implementation, the photo mask 104 is rectangular and corresponds to an exposure field on the wafer 102 that is considerably smaller than the surface of the wafer 102. Here, a patterned resist is formed by utilizing what is known as a “step-and-repeat” process, wherein the alignment and exposure processes are repeated for several positions of the photo mask until the photoresist is patterned across substantially the entire surface of the wafer 102.

In both of the above implementations, the alignment marks 106 and 108 are used to precisely align the template 104 with the wafer 102 prior to the NIL or optical lithography patterning process. In addition to optical lithography and NIL, alignment marks are commonly used in a variety of semi-conductor fields to which the herein disclosed implementations may also apply.

Multiple techniques may be employed to align the wafer 102 with the template mask 104. During one such alignment process, a wafer stage (not shown) supporting the wafer 102 is moved relative to a stationary laser beam (not shown). The passage of the alignment marks

under the laser beam produces diffracted and scattered light, which is photo-electrically detected as an alignment signal.

In another alignment process, the alignment 106 and 108 marks are illuminated with a monochromatic light that is reflected and recorded by a CCD camera. The recorded signal
5 can then be used to measure a photoelectric intensity or surface reflectivity as a function of position across the alignment mark. This signal can be correlated with a reference signal to give an amount of misalignment of the wafer 102 with a desired position.

However, these and other alignment processes may not be performed if the alignment marks are not visible. Thus, if one or more opaque thin film layers are deposited on the wafer
10 above the alignment marks 106 and 108, then the alignment marks 106 and 108 may have to be recovered (i.e., re-exposed) prior to the alignment process. One way to do this is by etching or milling away at the opaque layers. However, etching or milling away at the opaque thin film layers over the alignment marks 106 and 108 can, in some cases, create surface topography unsuitable for subsequent NIL imprinting. Therefore, one solution is to replace
15 opaque material removed from the wafer 102 with a transparent film. Another solution is to mitigate the amount of topography created by using a selective etching or ashing process. Such methods yield reduced surface topography as compared to traditional alignment mark recovery processes.

As used herein, the terms “transparent film” or “transparent material” may also refer
20 to translucent films or materials.

In at least one implementation, the alignment marks 106 and 108 illustrated in FIG. 1 have been recovered according to a method disclosed herein that results in surface topography suitable for a subsequent NIL imprinting process. FIGs. 2-6 illustrate different steps that relate to the same or alternate implementations of an alignment mark recovery
25 process that yields reduced surfaced topography as compared to existing methods.

FIG. 2 illustrates a cross-sectional view of a wafer 200 with a number of layers and alignment marks (e.g., alignment marks 236 and 238) embedded therein. Although the wafer 200 may be any semi-conductor wafer, the wafer illustrated is to be diced into thin film heads for use in hard drive disc assemblies. The wafer 200 includes a substrate layer 214 that is a
30 hard, thermally stable material such as aluminum titanium carbide (AlTiC). A non-magnetic, nonconductive layer of basecoat 216 is formed on top of the substrate 214, which may be, for example, a layer of alumina. A thin resistive layer 218, which may be tantalum nitride (TaN), is formed on top of the basecoat 216, and a second layer of alumina 220 is formed on top of the thin resistive layer 218. In one example implementation, the substrate 214 is 1200μm

thick (y-direction); the basecoat 216 is approximately five microns thick; the resistive layer 218 is approximately six nanometers thick; and the second layer of alumina is approximately five microns thick.

Alignment marks 236 and 238 are formed in a metal layer 222 embedded in the wafer. In one implementation, this metal layer is NiFe. The metal layer 222 has a substantially even thickness across the wafer 200 and descends into a number of grooves formed in the wafer 200. The grooves in the wafer 200 splice through the underlying layers 218 and 220 and into the basecoat layer 216. Thus, the metal layer 222 also has a number of grooves formed therein that splice through the underlying layers 218 and 220 and into the basecoat layer 216. The grooves in the metal layer 222 are of a width (x-direction) that is substantially equal to the separation between the grooves. In various implementations, the width of each of the grooves may range between approximately 400 nanometers and four microns. The height (y-direction) of each of the grooves may range between approximately 800 nanometers and 20 microns. Widths and heights outside of these ranges are also contemplated herein.

The x-y cross-section of FIG. 2 shows each of the alignment marks 236 and 238 as a separate, single groove in the metal layer 222. However, an alignment mark typically includes a grouping of several grooves. In one implementation, an alignment mark includes between seven and seventeen grooves. In another implementation, the alignment mark includes as many as 90 grooves. Therefore, the alignment marks 226 and 238 may represent groupings of any number grooves.

A transparent layer 224 is on top of and in contact with the alignment mark layer 222. In one implementation, the transparent layer 224 is alumina. In another implementation, the transparent layer 224 is silicon dioxide (SiO_2). In yet another implementation, the transparent layer 224 is a layer of opaque material that is applied so thin as to allow for some light to be transmitted through the transparent layer 224. For example, the transparent layer 224 may be of a generally opaque material having thickness less than 50 nanometers.

A number of opaque film layers 240, 242, and 244 are formed on top of the transparent layer 224, concealing the underlying alignment marks 236 and 238. Here, the first opaque film layer 240 is a bottom shield layer that protects several more layers collectively forming a read/write stack (i.e., the second opaque film layer 242) from electromagnetic interference. The third opaque film layer 244 includes one or more hard mask layers to protect the read/write stack 242.

Prior to NIL or optical lithography printing, material from the opaque film layers 240, 242, and 244 may have to be removed in order to recover the underlying alignment marks 236 and 238.

FIG. 3 illustrates another cross-sectional view of a wafer 300 having a number of layers including a patterned photoresist layer 350 on top of an undercut soluble polymer layer 348. The wafer 300 also has embedded alignment marks 336 and 338 underlying a transparent layer 324. The alignment marks 336 and 338 are grooves formed in a metal layer 322. Opaque layers 340, 342, and 344 are formed on top of the transparent layer 324, concealing the alignment marks 336 and 336.

The soluble polymer layer 348 and the overlying patterned layer 350 are formed on the wafer 300 during a preliminary step in an alignment mark recovery process. The soluble polymer layer 338 is applied to the wafer 300. In one implementation, the polymer layer 338 is applied via a spin-coating process. Thereafter, the wafer 300 is baked to drive off solvent. A layer of liquid photoresist 350 is then deposited, such as through a spin-coating or other deposition process, on top of the soluble polymer layer 348. The liquid photoresist 350 is patterned so as to leave exposed a portion of the wafer surface above the alignment marks 336 and 338 (as illustrated in FIG. 3). In one implementation, this patterning is done by an optical lithography process wherein portions of the liquid photoresist are exposed to high intensity light, thus changing the solubility of either the exposed or unexposed portions (depending upon the type of photoresist). The unchanged portions are removed by a developer solution, leaving behind the patterned photoresist layer 350.

The soluble polymer layer 348 is soluble in the developer solution used to remove the developable portions of the patterned photoresist layer 350. Thus, the soluble polymer layer 348 is isotropically dissolved beneath developed portions of the patterned photoresist. This effect causes the soluble polymer layer 348 to slightly undercut the patterned photoresist layer 350, as illustrated in FIG. 3. In one implementation, the soluble polymer is polymethylglutarimide (PMGI).

Because there may be some uncertainty as to the exact locations of the underlying alignment marks 336 and 338, the patterned photoresist layer 350 may be patterned to expose a substantial margin around the alignment marks 336 and 338. In one implementation, this margin is substantially between one and two microns on each side of the alignment marks 336 and 338. The patterned photoresist layer 350 functions to protect portions of the wafer 300 during a subsequent etching process (such as that described with respect to FIG. 4, below). After the etching process, the soluble polymer layer 348 and the patterned

photoresist layer 350 can be removed. In one implementation, the soluble polymer layer 348 and the patterned photoresist 350 are removed by using standard photoresist solvents.

FIG. 4 illustrates another cross-sectional view of a semi-conductor wafer 400 with a cavity 452 etched therein to expose embedded alignment marks 436 and 438 through a transparent layer 424. The cavity 452 has been milled or etched to remove material from a number of opaque layers 440, 442, and 444 in order to expose the embedded alignment marks 436 and 438 below. Thus, the cavity 425 has a base with a perimeter that substantially surrounds the underlying alignment marks 436 and 438.

A soluble polymer layer 438 and overlying patterned photoresist 450 were formed on top of the opaque layers 440, 442, and 444 to protect the now un-etched portions of the wafer 400 during the milling or etching process.

In one implementation, the milling or etching process expands the cavity 452 into the underlying transparent layer 424 (i.e., in the y-direction) in order to ensure that the opaque films have been completely cleared from the transparent surface.

FIG. 5 illustrates yet another cross-sectional view of a semi-conductor wafer 500 with a filler layer 556 deposited across the wafer 500 to fill a cavity 552 that tunnels through a number of opaque layers 540, 542, and 544. The cavity 552 was created in order to expose embedded alignment marks 536, 538 through another transparent layer 524, below. However, the formation of the cavity incidentally created unwanted surface topography. To solve this problem, the filler layer 556 was deposited.

The filler layer 556 is a transparent thin film that has a thickness (y-direction) approximately equal to the depth of the cavity 554. In one implementation, the filler layer 556 is blanket alumina that is approximately 30-150 nanometers thick (y-direction). In another implementation, the thickness of the filler layer 556 is greater than one micron. Prior to filling the cavity 552 with the filler layer 556, a soluble polymer layer 548 and overlying patterned photoresist layer 550 were formed on top of the opaque layers 540, 542, and 544. The patterned photoresist layer 550 and soluble polymer layer 548 are formed such that an area on the surface of the wafer is exposed having a perimeter that substantially encompasses the underlying alignment marks 536 and 538.

The patterned photoresist 550 and soluble polymer layer 548 prevent underlying portions of the underlying wafer 500 from contacting the transparent film layer 556 during the deposition process. After deposition of the filler layer 556, the soluble polymer layer 548 and overlying patterned photoresist 550 can be removed, such as by a standard photoresist solvent. This process, which may also be referred to herein as a "liftoff process", also

removes portions of the filler layer 556 that are deposited on top of the patterned photoresist layer 550.

FIG. 6 illustrates yet another cross-sectional view of a semi-conductor wafer 600 with alignment marks 636 and 638 visible through transparent layers 624 and 656 overlying the alignment marks 636 and 638. The transparent layer 656 was deposited in order to reduce surface topography created by etching or milling away the opaque layers 640, 642, 646. Subsequently, a patterned photoresist (not shown) and an underlying soluble polymer layer (not shown), such as those illustrated and discussed with respect to FIG. 5, were removed.

The semi-conductor wafer 600 has a substantially planar surface with the alignment marks 636 and 638 visible through the transparent layers 624 and 656. In one implementation, the steps described above with respect to FIGs. 2-6 are utilized in a single process, and the amount of topography remaining on the wafer after removal of the photoresist after can be polished without creating substantial variations in thickness across the wafer.

FIGs. 7-9 illustrate structures relating to implementations of another alignment mark recovery process. FIG. 7 illustrates a cross-sectional portion of a semi-conductor wafer 700 taken along the x-y plane of FIG. 1. The semi-conductor wafer 700 has a base portion (not shown), which may include, for example, a bottom substrate, a basecoat, and a variety of layers performing a variety of functions. Alignment marks 704 are formed on the base portion of the wafer as grooves in a metal layer (not shown). The grooves in the metal layer nest within grooves in an overlying transparent film layer 708. The transparent film layer 708 underlies first and second opaque layers 710 and 712. In one implementation, the opaque layers 710 and 712 are hardmask layers. In another implementation, the first opaque layer 710 is tantalum nitride (TaN) and the second opaque layer 712 is amorphous carbon (aC).

One or more removal steps can be undertaken to remove the opaque layers 710 and 712 from an area above the alignment marks 704, so as to expose the alignment marks through the transparent film layer 708. To avoid creating excess surface topography, one or more of the opaque material layers 710 and 712 is to be selectively removed.

FIG. 8 illustrates a first alignment mark recovery process step wherein a portion of an upper opaque layer 810 on a semi-conductor wafer 800 is removed by a milling or etching operation. The upper opaque layer 810 is above and in contact with a lower opaque layer 812, which is above and in contact with a transparent film layer 808. In one implementation, the

upper opaque layer 810 is a hard mask material such as tantalum nitride (TaN). Alignment marks 804 are embedded in the wafer 800 just below the transparent film layer 808.

Prior to this milling or etching operation, the wafer is coated with a layer of liquid photoresist, which may be performed by a spin-coating process. The liquid photoresist is masked and exposed to a high intensity light to modify the solubility of portions of the photoresist. Thereafter, the more soluble portions are removed by a developer solution so that the other hardened portions (i.e., the patterned photoresist) remain on the wafer, leaving behind a patterned photoresist that protects the portions of wafer that will not be subsequently etched or milled.

In one implementation, material from the upper opaque layer 810 is removed from an area above the alignment marks 804 by a short milling or etching process. In another implementation, such material is removed by a wet or dry etching process. In the same or an alternate implementation, the milling or etching operation that removes the upper opaque layer 810 also removes material from one or more other opaque and/or transparent layers on top of the transparent layer 808.

In any or all of the above implementations, some of the lower opaque layer 812 may be left behind on the wafer 800 to be subsequently removed by a selective etching or ashing process (such as that described with respect to FIG. 9, below).

FIG. 9 illustrates another alignment mark recovery process step wherein a portion of a lower opaque layer 912 on a semi-conductor wafer 900 is removed by a selective removal process to expose alignment marks 904 embedded in the wafer 900. The lower opaque layer 912 is above and in contact with the transparent film layer 908, which is selected to be a “stop” layer for the selective removal process.

Prior to removing material from the lower opaque layer 912, a patterned photoresist is created on the wafer to protect portions of the lower opaque layer 912 that will not be removed in the selective removal process. In one implementation, this patterned photoresist is formed before material is removed from one or more upper opaque layers (such as the opaque layer 910). Therefore, this same protective photoresist (not shown) may be left in place while material is removed from the lower opaque layer 912 as well.

At the alignment mark recovery process step illustrated by FIG. 9, a selective ashing or etching process is used to selectively remove opaque material from above the stop layer 908 without removing material from the stop layer 908 itself. In one example implementation, the stop layer 908 is transparent alumina, the lower opaque layer 912 is amorphous carbon (aC), and an ashing process is used to remove material from the lower

opaque layer 912 above the alignment marks 904. In another implementation, the stop layer 908 is silicon dioxide, the lower opaque layer 912 is amorphous carbon, and a selective etch process is used to remove the material in the lower opaque layer 912 above the alignment marks 904. In another implementation, the stop layer is SiO₂ and a chlorine-based etch is used.

By selectively ashing or etching through the lower opaque film layer 912 as described above, no material from the transparent film layer 908 is removed. Therefore, the resulting topography on the surface of the wafer 900 is reduced as compared to some existing processes that overetch or overmill into the transparent layer 904 to remove the one or more overlying opaque layers.

FIG. 10 illustrates a flow-chart of example operations for an alignment mark recovery process according to one implementation. A first deposition operation 1005 first deposits a soluble polymer on a semi-conductor wafer surface. The soluble polymer is preferably soluble in a developer solution used to develop away a photoresist. The deposition operation 1005 deposits the soluble polymer layer in a substantially even manner, such as by spin-coating the wafer. In one implementation, the soluble polymer is PMGI.

A second deposition operation 1010 deposits a layer of liquid photoresist on top of the soluble polymer layer, such that the liquid photoresist is in contact with the soluble polymer and deposited substantially evenly across the wafer. Like the first deposition operation 1005, the second deposition operation 1010 may also be performed by spin-coating the wafer.

A pattern and development operation 1015 patterns the photoresist to expose a portion of the wafer surface above one or more alignment marks embedded in the wafer. In one implementation, the pattern is created in the photoresist by an optical lithography patterning process. For example, a high intensity light can be directed through a patterned photo mask and subsequently through a lens that projects the pattern of the patterned photo mask onto the wafer surface. Depending on the type of photoresist utilized, this light exposure will modify the solubility of either the exposed or unexposed portions of the photoresist. The more soluble portions can be removed, such as by a developer solution.

The developed portions of the resist are located physically above one or more of the alignment marks embedded in the wafer. In removing these portions of the photoresist, the developer solution also isotropically dissolves portions of the soluble polymer layer underlying the developed portions of the photoresist, thus exposing an area on the wafer surface (hereinafter “the exposed area”) that substantially encompasses one or more underlying alignment marks.

A removal operation 1020 removes material from one or more layers in the developed area in order to recover or expose the alignment marks underlying the developed area. In one implementation, material is removed from one or more opaque thin film layers. In another implementation, material is removed from both opaque thin film and transparent thin film
5 layers. The removal operation 1020 may be either a milling or an etching operation that mills or etches a cavity into the exposed area of the wafer. After the removal or etching operation, the alignment marks are visible in the developed area. One or more transparent layers may separate the alignment marks from the surface of the wafer.

A filling operation 1020 fills the cavity etched or milled in the removal
10 operation 1015 with a transparent film. In one implementation, this transparent film is deposited substantially evenly across the entire wafer. Thus, the transparent film coats the wafer surface and also the developed area (i.e., the base of the cavity etched or milled) above the alignment marks. The amount of film deposited on the wafer is substantially equal to the amount of material removed from the cavity. Therefore, the cavity etched or milled by the
15 removal operation 1020 is “filled” to its original level with the transparent film.

After the filling operation 1020, the patterned photoresist is removed by a standard photoresist solvent, such as a resist-strip that chemically alters the patterned photoresist so that it no longer adheres to the substrate. The soluble polymer layer underlying the substrate is also removed by this solvent.

20 After the patterned photoresist is removed, the surface of the wafer is substantially coplanar with an original surface of the wafer (i.e., the surface existing prior to application of the soluble polymer layer).

FIG. 11 illustrates another flow-chart of example operations for an alignment mark recovery process according to another implementation. A deposition operation 1105 deposits
25 a layer of liquid photoresist on a semi-conductor wafer surface. The liquid photoresist is deposited in a substantially even manner across the wafer surface.

A pattern and development operation 1110 patterns the photoresist to expose a portion of the wafer surface above one or more alignment marks embedded in the wafer. In one implementation, the pattern is created in the photoresist by an optical lithography patterning
30 process. For example, a high intensity light can be directed through a patterned photomask and subsequently through a lens that projects the pattern of the patterned photomask onto the wafer surface. Depending on the type of photoresist utilized, this light exposure will modify the solubility of either the exposed or unexposed portions of the photoresist. The more soluble portions are removed, such as by a developer solution, to expose an area (the

“exposed area”) that substantially encompasses one or more alignment marks embedded below the wafer surface.

A removal operation 1115 is either a milling or an etching operation that mills or creates a cavity in the exposed area of the wafer, removing material from at least one layer.

5 The material removed may be either transparent or opaque. However, the removal operation 1115 leaves some opaque material remaining in the exposed area, so that the embedded alignment marks are not visible. One or more transparent layers may separate the alignment marks from the opaque material in the exposed area.

10 A selective removal operation 1120 selectively ashes or etches to remove the remaining opaque material overlying the alignment marks in the exposed area without removing any material from a stop layer below the opaque material. In one implementation, the stop layer is a transparent thin film layer. In the same or an alternate implementation, the opaque material is aC and the selective removal operation is an ashing process that ashes away the aC but does not remove any of the transparent thin film.

15 After the selective removal operation 1120, a photoresist removal operation 1125 removes the patterned photoresist by a standard photoresist solvent. After the photoresist removal operation 1125, the remaining surface topography on the wafer is not significant relative to the requirements of NIL.

20 The specific steps discussed with respect to each of the implementations disclosed herein are a matter of choice and may depend on the materials utilized and/or the topography-related requirements of a given system. The steps discussed may be performed in any order, adding and omitting as desired, unless explicitly claimed otherwise of a specific order is inherently necessitated by the claim language.

25 The above specification, examples, and data provide a complete description of the structure and use of exemplary implementations of the invention. Since many implementations of the invention can be made without departing from the spirit and scope of the invention, the invention resides in the claims hereinafter appended.

Claims

WHAT IS CLAIMED IS:

1. A method comprising:
 - 5 creating a cavity by removing opaque material oriented over an alignment mark embedded in a wafer to expose the alignment mark; and
 - filling the cavity with a transparent material to a depth substantially equal to a depth of the cavity.
- 10 2. The method of claim 1, further comprising:
 - forming a patterned photoresist above an opaque surface layer that leaves exposed an area of the opaque surface layer above the alignment mark.
- 15 3. The method of claim 2, further comprising:
 - removing the patterned photoresist from the wafer.
- 20 4. The method of claim 1, wherein filling the cavity with the transparent material further comprises filling the cavity with the transparent material to a height substantially coplanar with an edge of an opaque surface layer that is most distal to a base of the cavity.
- 25 5. The method of claim 1, wherein creating the cavity further comprises removing material by etching or milling the wafer.
- 30 6. The method of claim 1, wherein filling the cavity with the transparent material further comprises depositing a transparent thin film across a surface of the wafer.
7. The method of claim 1, wherein the alignment mark is separated from a base of the cavity by another transparent layer.
8. The method of claim 1, wherein the cavity has a perimeter that substantially surrounds the underlying alignment mark.
9. A semi-conductor wafer comprising:

a cavity in an opaque surface layer that substantially overlies an alignment mark embedded in the wafer; and

a layer of transparent material deposited in the cavity to a depth substantially equal to a depth of the cavity.

5

10. The semi-conductor wafer of claim 9, wherein the alignment mark is visible through the layer of transparent material.

11. The semi-conductor wafer of claim 9, wherein the layer of transparent material has an edge substantially coplanar with an edge of the opaque surface layer that is most distal to a base of the cavity.

10

12. The semi-conductor wafer of claim 9, wherein the alignment mark is separated from a base of the cavity by another transparent layer.

15

13. The semi-conductor wafer of claim 9, further comprising a patterned photoresist above the opaque surface layer that leaves exposed an area of the opaque surface layer substantially overlying the alignment mark.

20

14. The semi-conductor wafer of claim 13, further comprising a soluble polymer layer on the opaque surface layer in contact with the patterned photoresist.

15. A system comprising:

25

a wafer having a cavity in an opaque surface layer that substantially overlies an alignment mark embedded in the wafer, wherein a layer of transparent material is deposited in the cavity to a depth substantially equal to a depth of the cavity; and
a mask template to be aligned with the wafer using the alignment mark.

30

16. The system of claim 15, wherein the alignment mark is visible through the layer of transparent material.

17. The system of claim 15, wherein the layer of transparent material has an edge substantially coplanar with an edge of the opaque surface layer that is most distal to a base of the cavity.

18.The system of claim 15, wherein the alignment mark is separated from a base of the cavity by another transparent layer.

5 19.The system of claim 15, further comprising a patterned photoresist above the opaque surface layer that leaves exposed an area of the opaque surface layer substantially overlying the alignment mark.

10 20.The system of claim 19, further comprising a soluble polymer layer on the opaque surface layer in contact with the patterned photoresist.

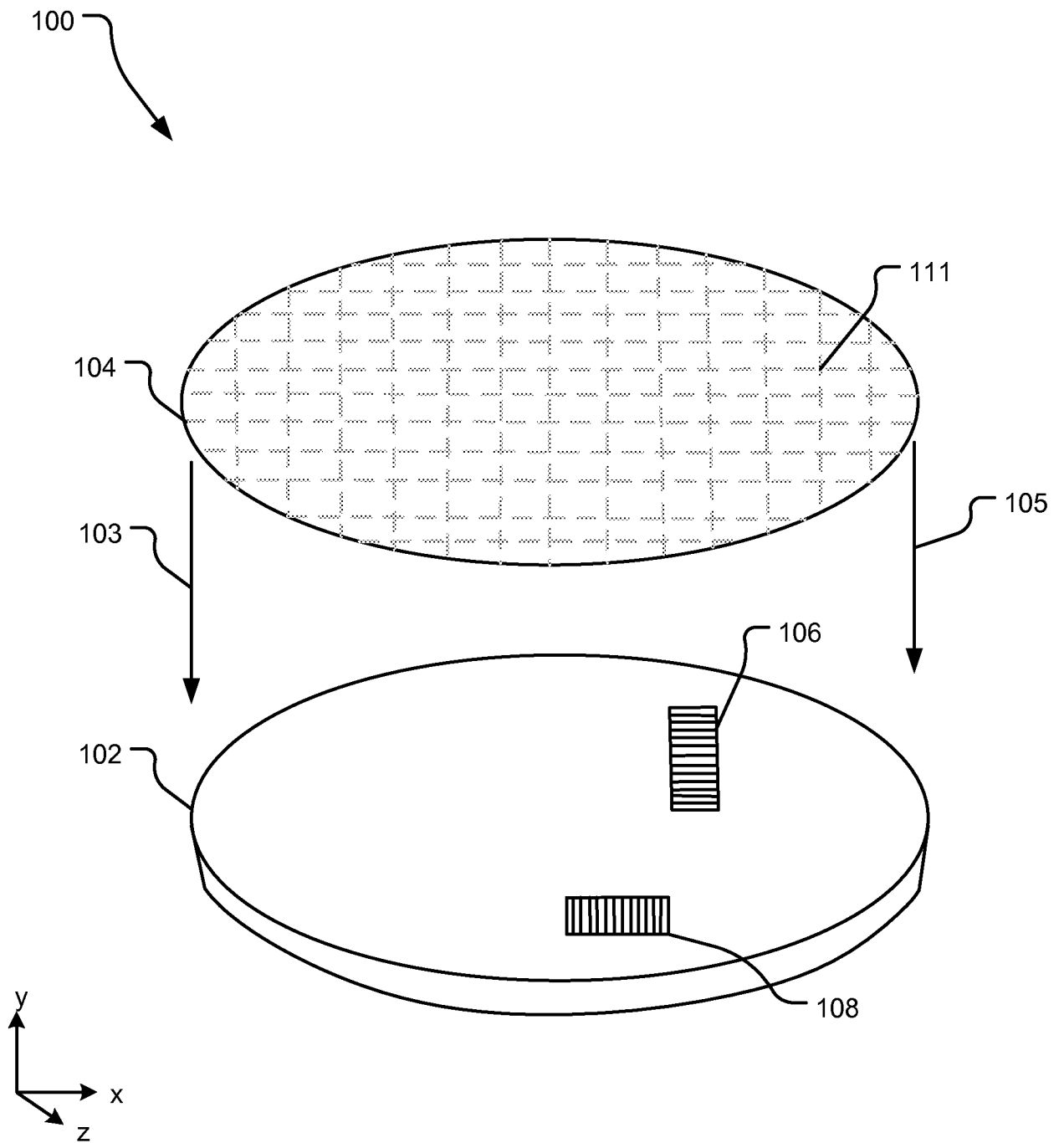


FIG. 1

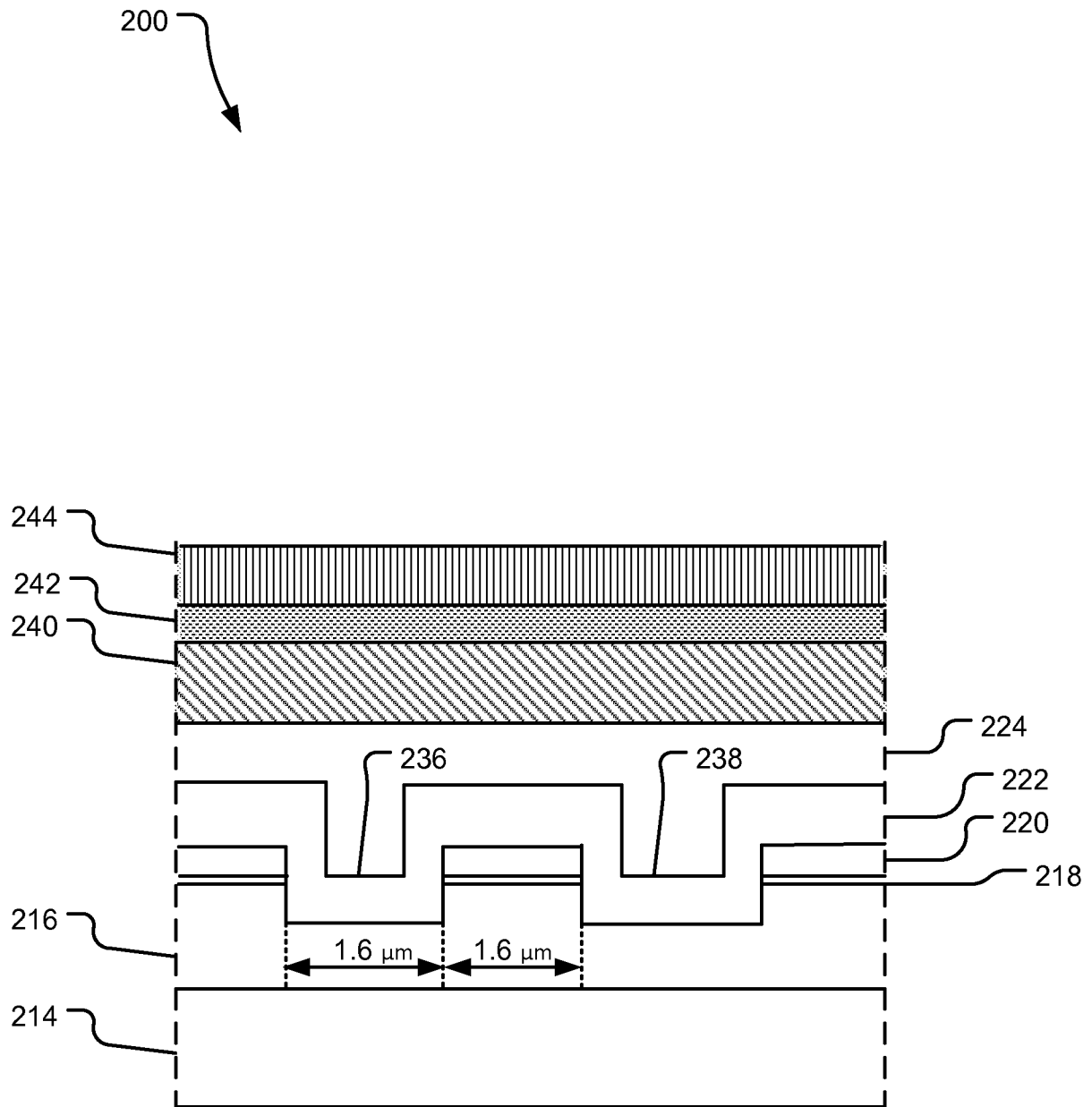
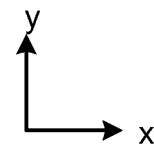


FIG. 2



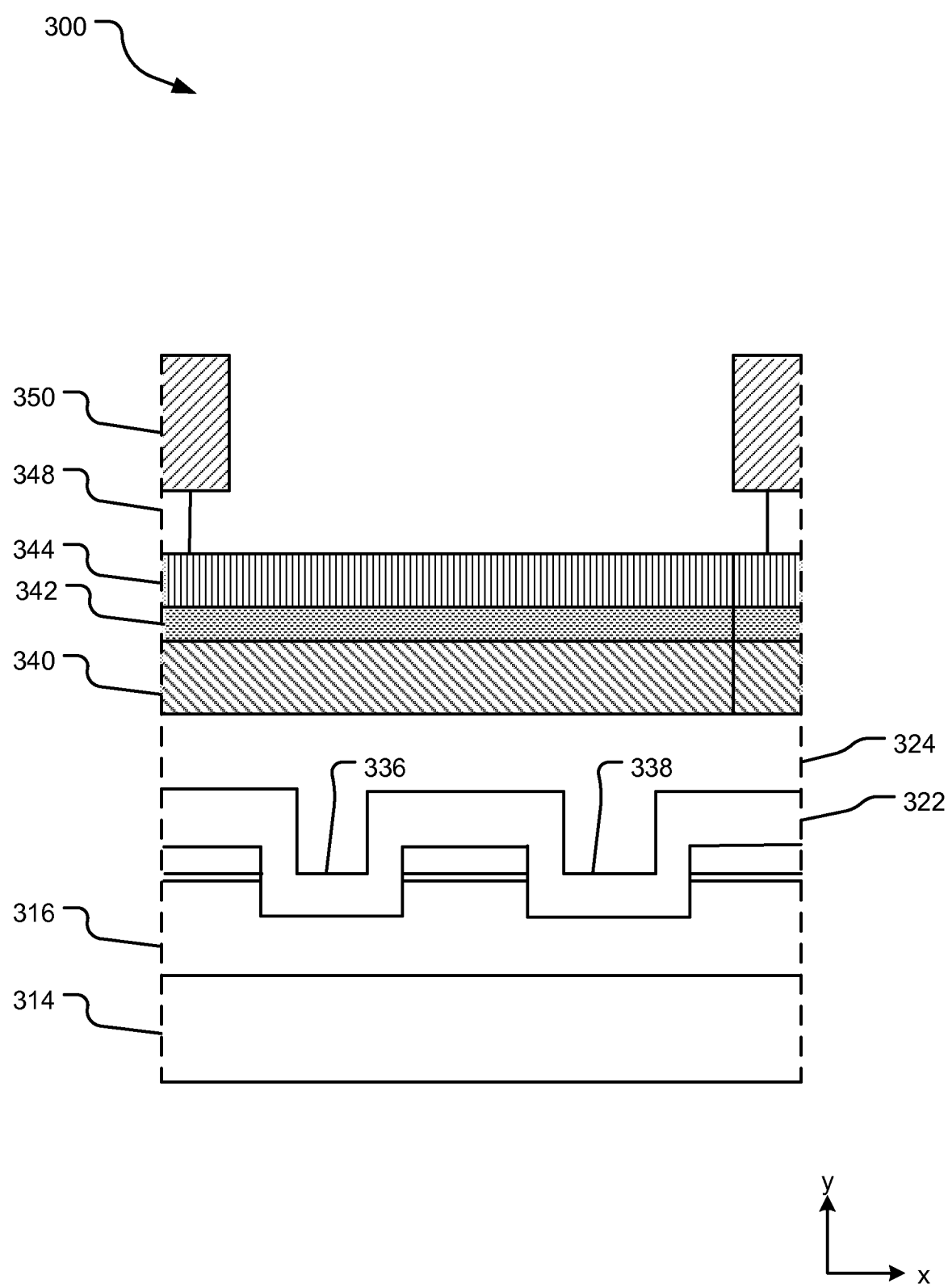


FIG. 3

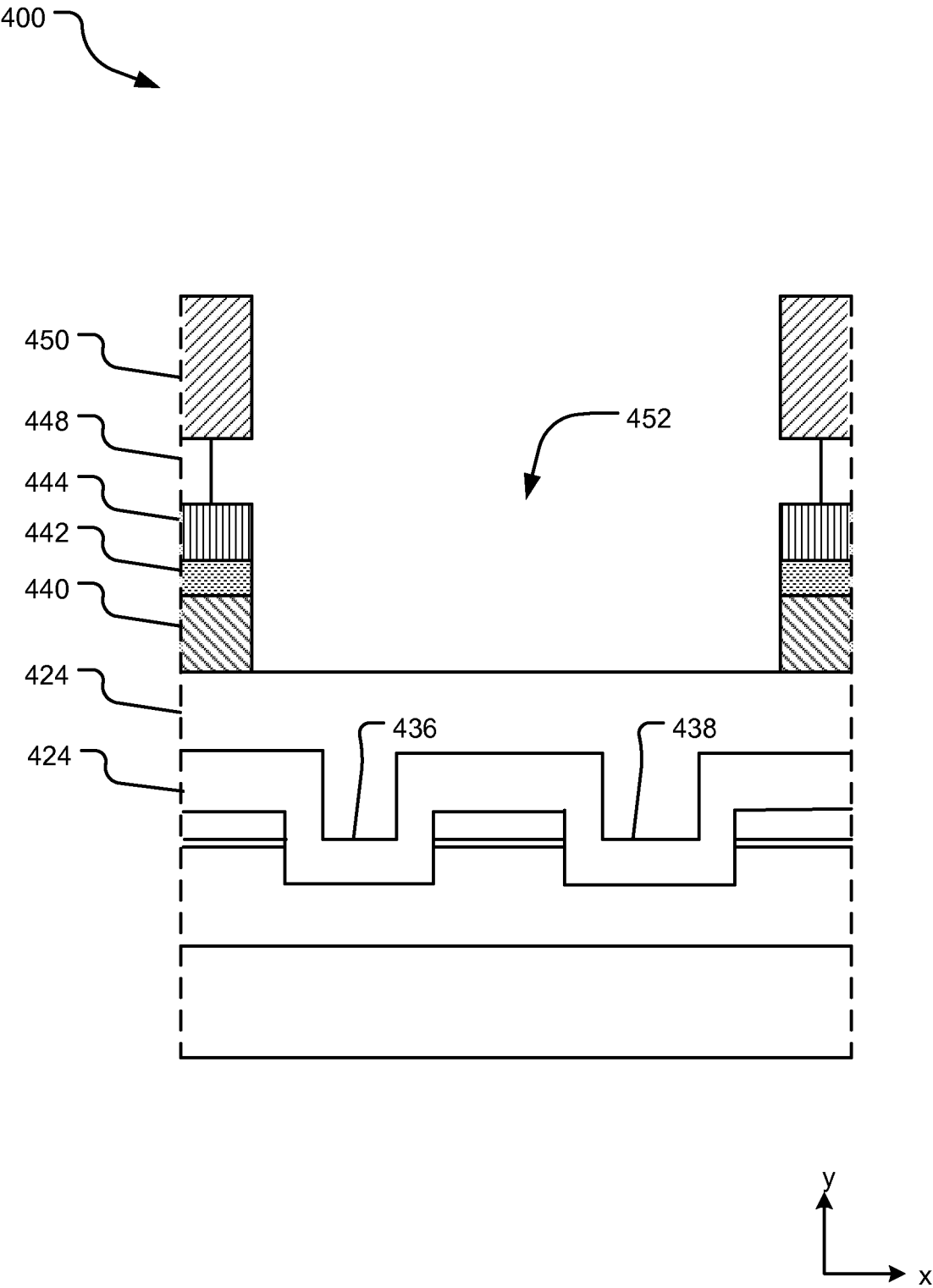


FIG. 4

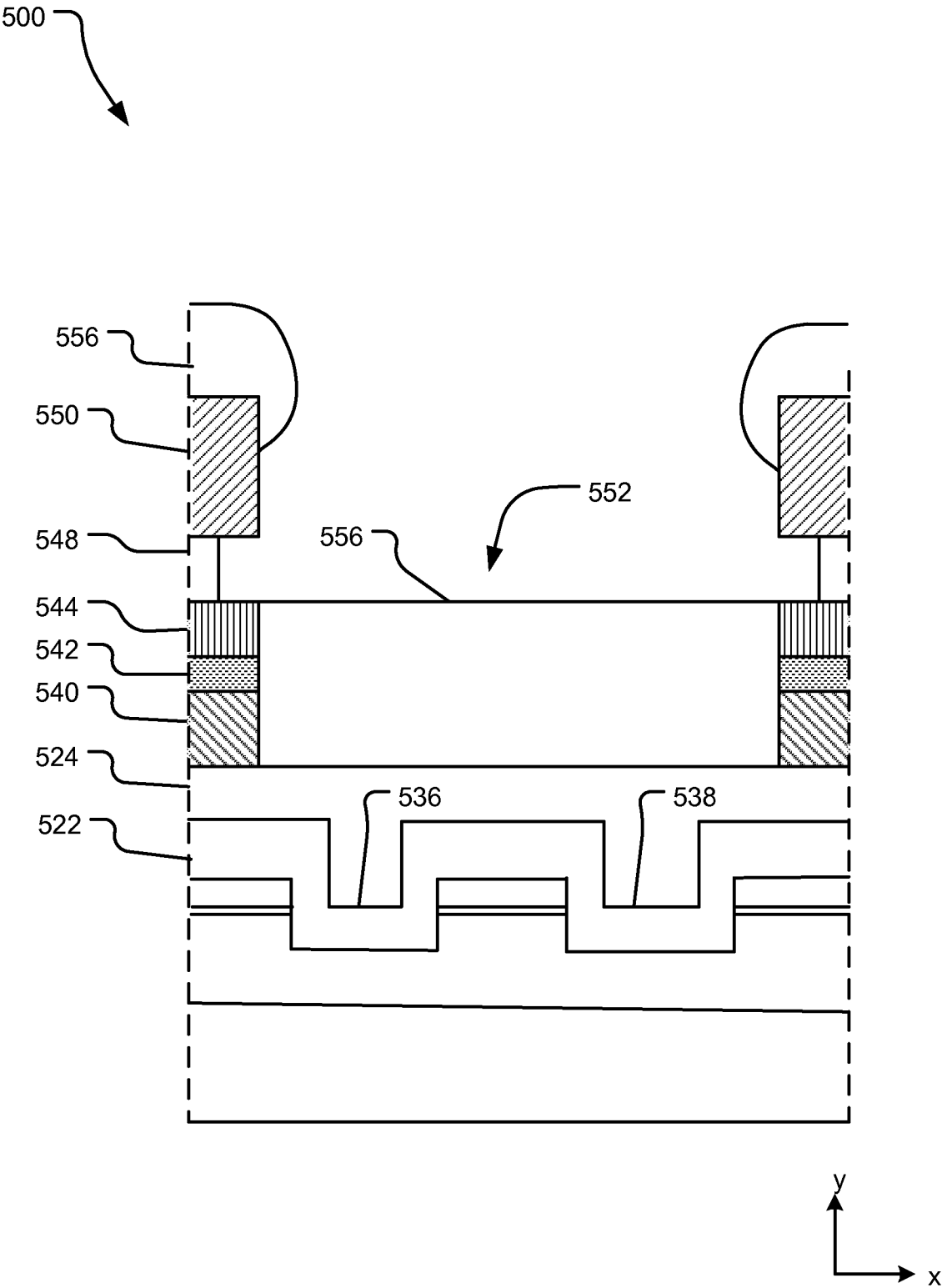


FIG. 5

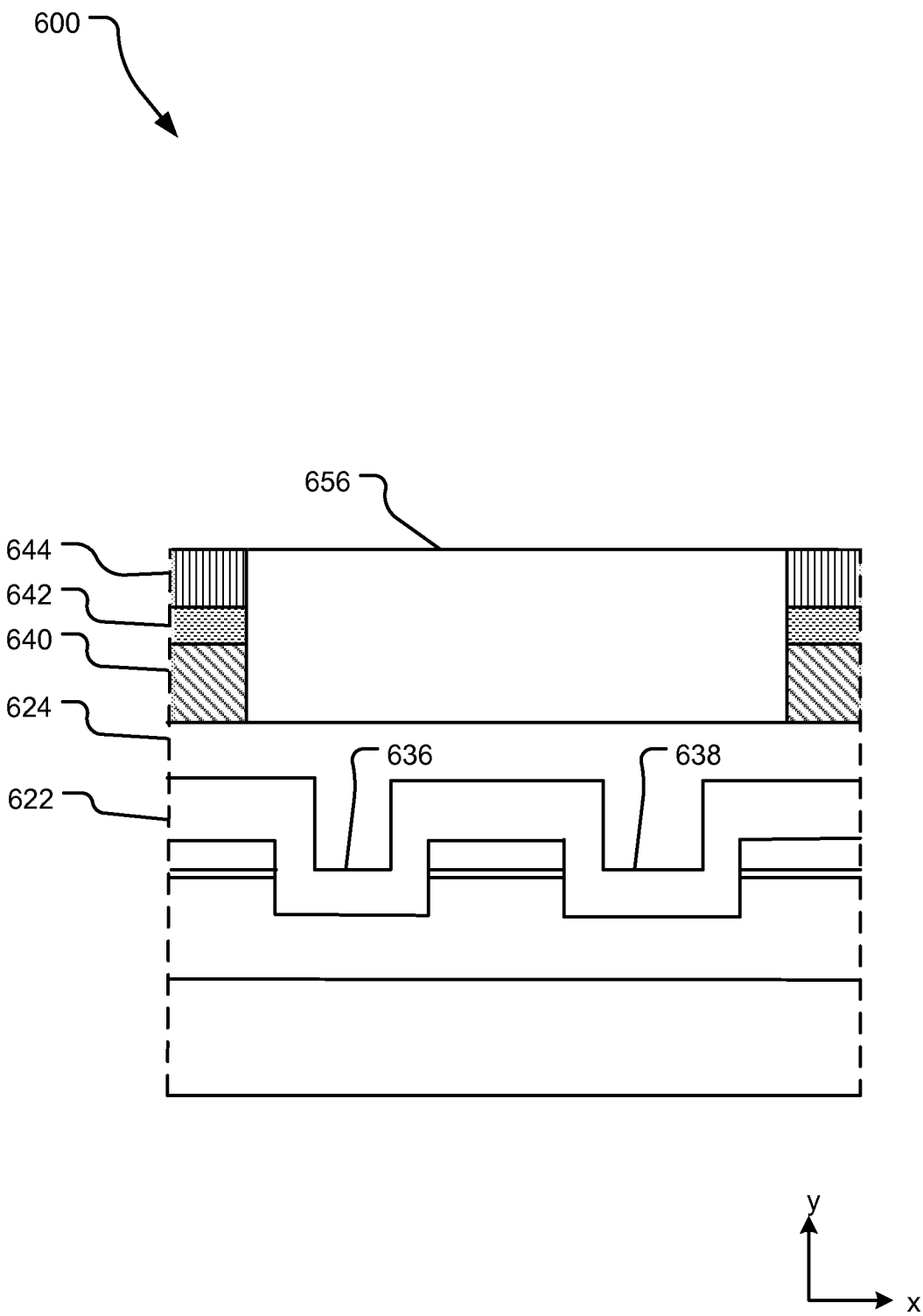


FIG. 6

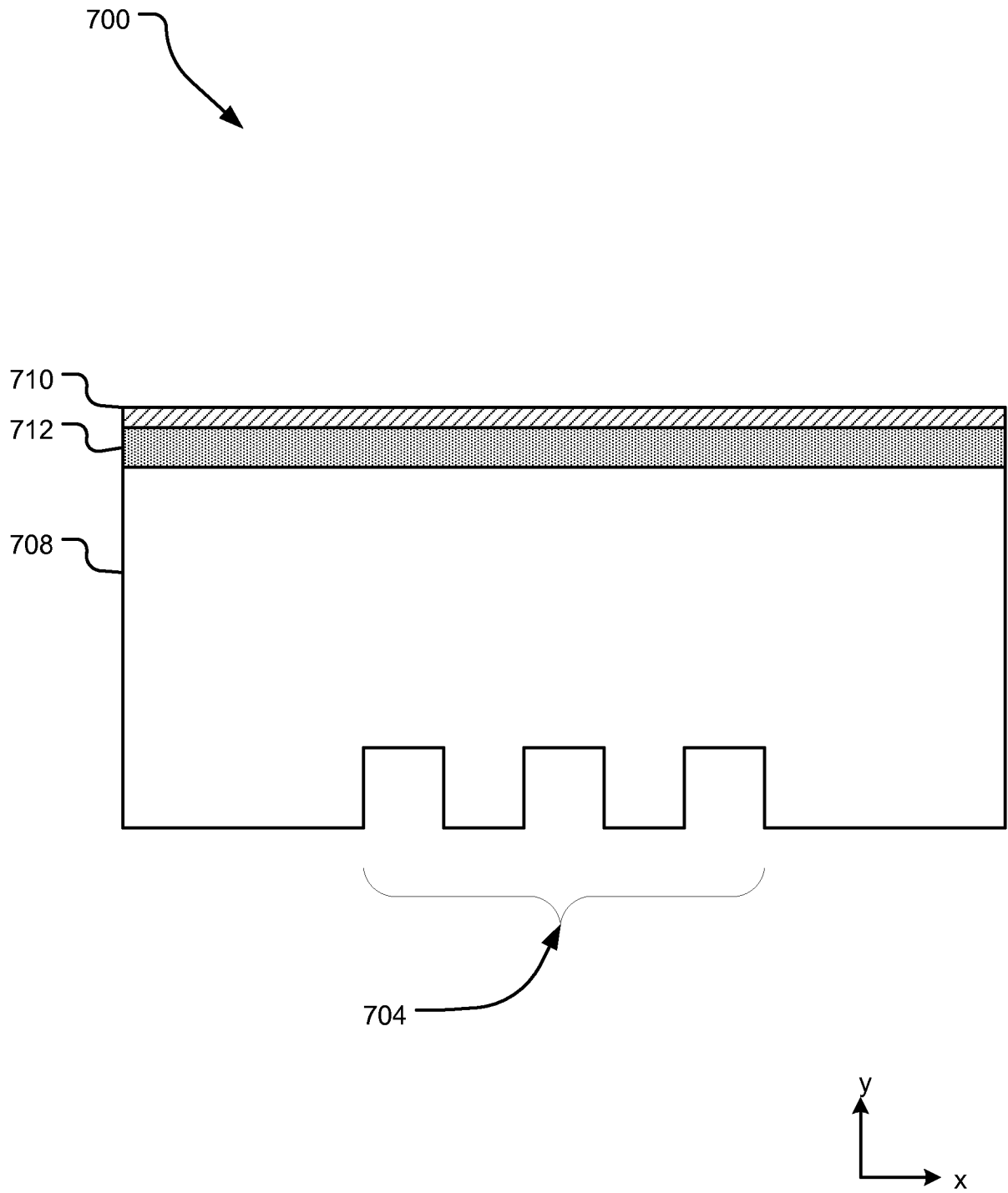


FIG. 7

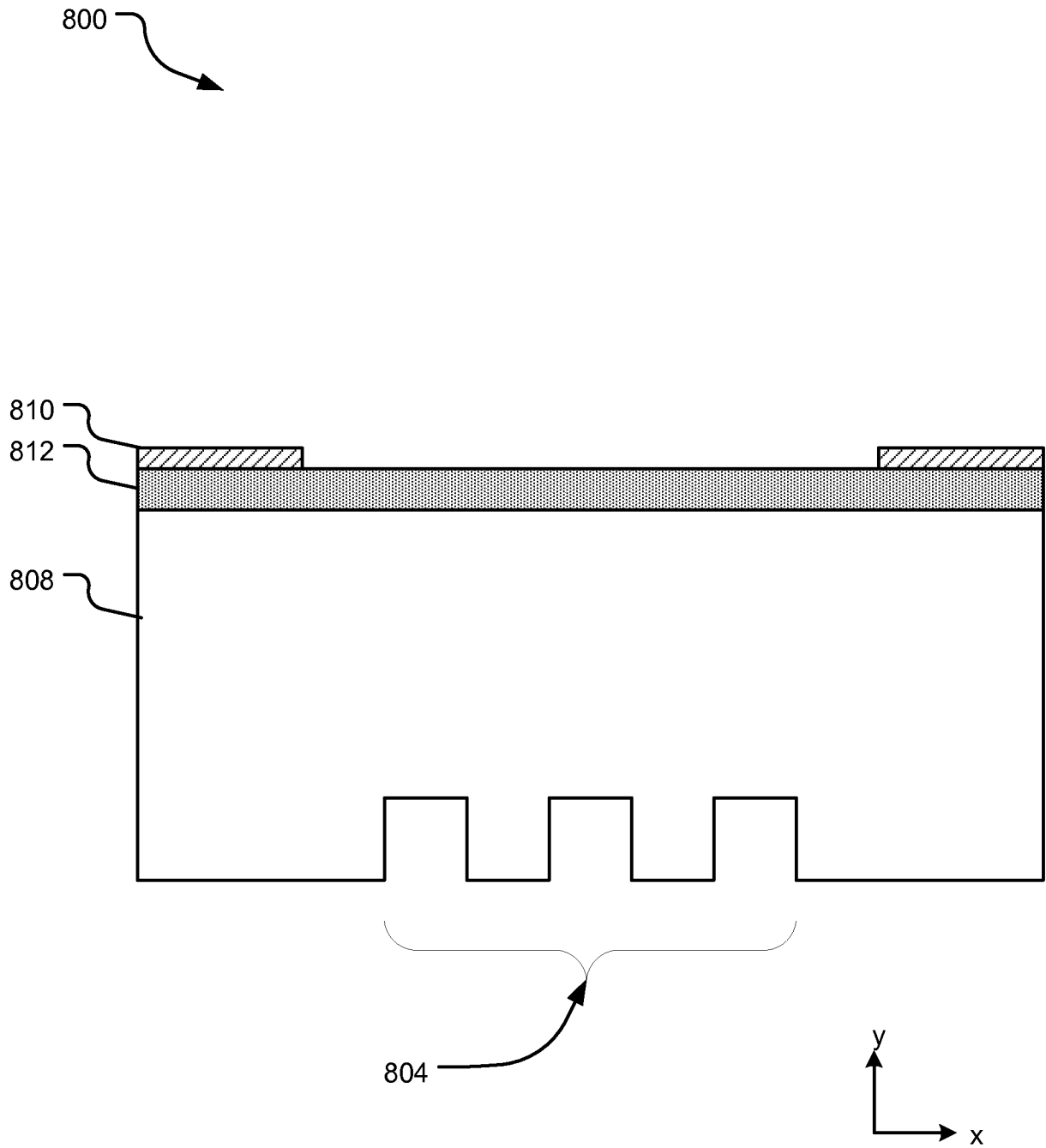


FIG. 8

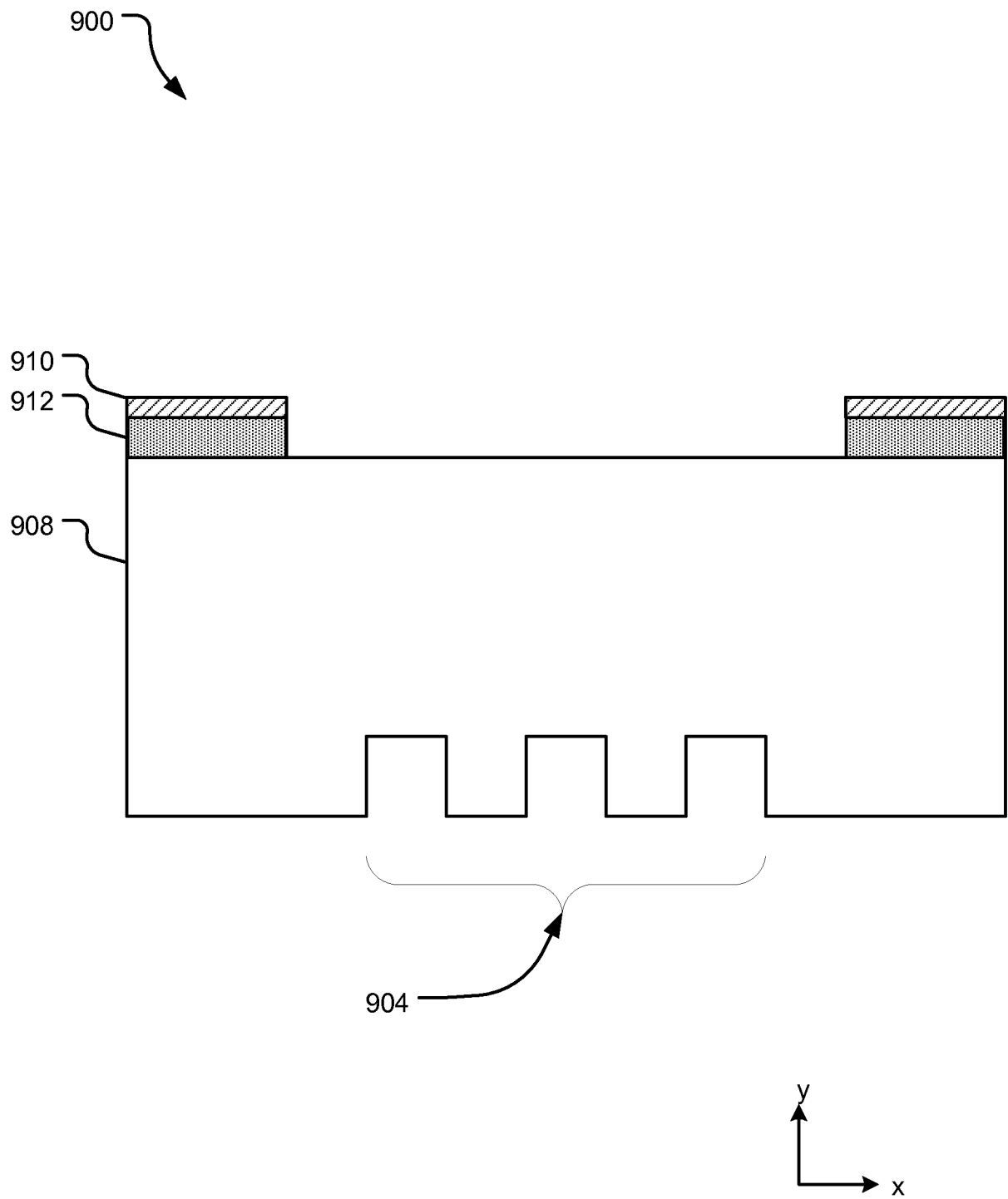


FIG. 9

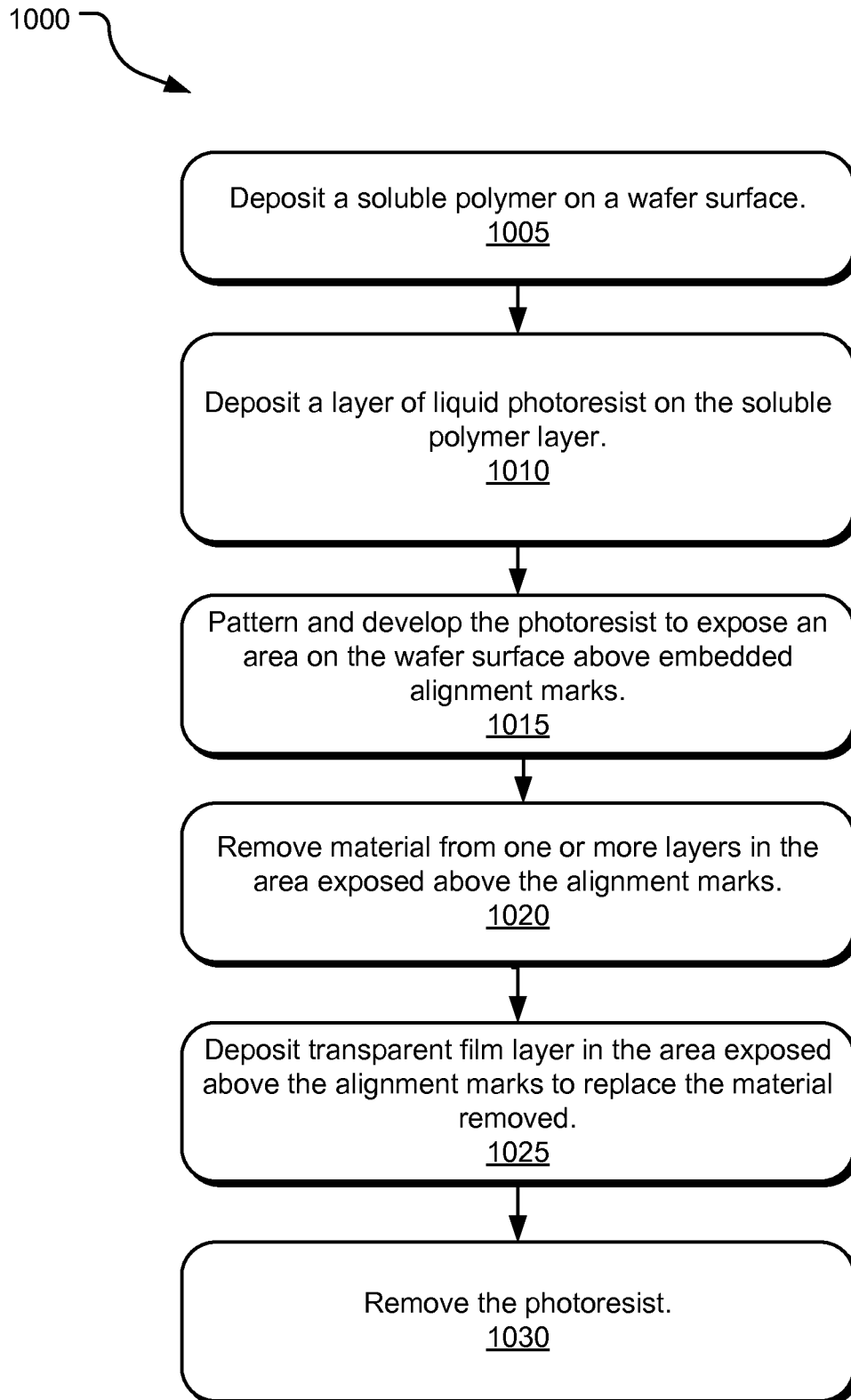


FIG. 10

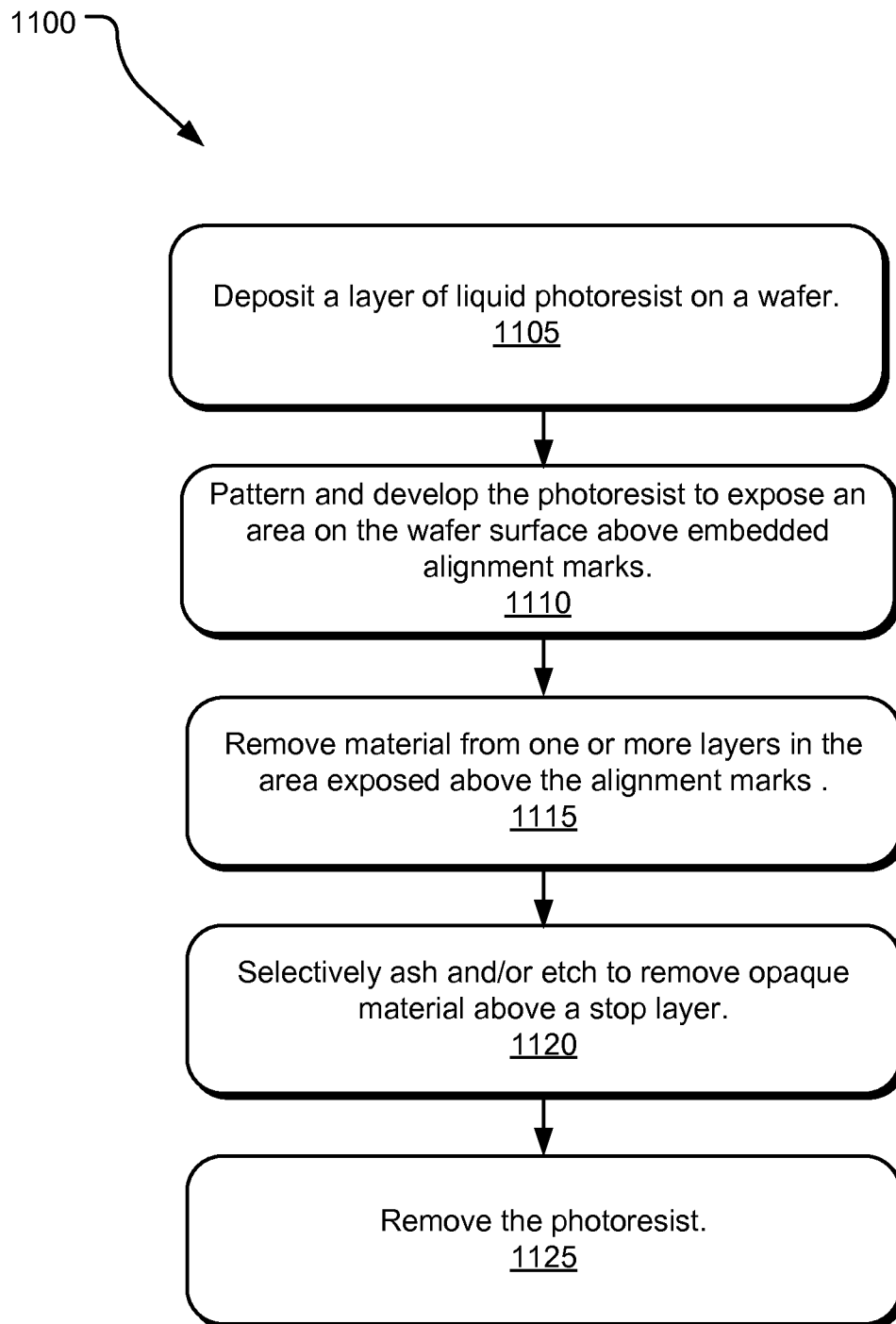


FIG. 11

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2014/013801**A. CLASSIFICATION OF SUBJECT MATTER****H01L 23/544(2006.01)i**

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H01L 23/544; H01L 29/00; H01L 21/71; G03B 27/52; G02B 1/11; H05K 3/30; H01L 21/02; H01L 23/02; G03F 9/00; H05K 7/06

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Korean utility models and applications for utility models

Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

eKOMPASS(KIPO internal) & keywords: wafer, cavity, alignment mark, opaque surface, transparent material, photoresist

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2011-0006400 A1 (JEAN-CHARLES SOURIAU et al.) 13 January 2011 See paragraphs [0006], [0042]-[0074], claim 1 and figures 4A-7B.	1,4-6,9-11,15-17
Y		2-3,13,19
A		7-8,12,14,18,20
Y	US 2002-0096359 A1 (LOUIS L. HSU et al.) 25 July 2002 See abstract, paragraphs [0036]-[0038] and figures 15-17.	2-3,13,19
A	US 2009-0017580 A1 (LARRY SMITH) 15 January 2009 See abstract, paragraphs [0015]-[0026] and figures 1-8.	1-20
A	US 2004-0257552 A1 (SVEN HANSEN) 23 December 2004 See abstract; paragraphs [0016]-[0028] and figures 2-4.	1-20
A	JP 2004-286892 A (RICOH CO., LTD.) 14 October 2004 See abstract, paragraphs [0028]-[0055] and figures 1-7.	1-20



Further documents are listed in the continuation of Box C.



See patent family annex.

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"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search

20 May 2014 (20.05.2014)

Date of mailing of the international search report

20 May 2014 (20.05.2014)

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INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/US2014/013801

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 2011-0006400 A1	13/01/2011	EP 2273548 A2 FR 2947948 A1 FR 2947948 B1 JP 2011-018907 A US 8288841 B2	12/01/2011 14/01/2011 09/03/2012 27/01/2011 16/10/2012
US 2002-0096359 A1	25/07/2002	US 6617702 B2	09/09/2003
US 2009-0017580 A1	15/01/2009	US 8338267 B2	25/12/2012
US 2004-0257552 A1	23/12/2004	AT 1342004 A AT 413305 B AT A1342004 A DE 10303902 A1 DE 10303902 B4 US 2006-0199085 A1 US 7057707 B2	15/06/2005 15/01/2006 15/06/2005 19/08/2004 09/12/2004 07/09/2006 06/06/2006
JP 2004-286892 A	14/10/2004	None	